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# Étude de faisabilité d'un récepteur homodyne à 20 GHz basé sur les jonctions à six ports

**Contrat de recherche nº 67CRC-5-3109/001/ST**

**Rapport final**

*Présenté à*

Monsieur Mario Caron
Centre de recherches en communication

*Préparé par*

Naïm Batani et François Gagnon
École de technologie supérieure

Le 29 mars 1996

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--
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# Étude de faisabilité d'un récepteur homodyne à 20 GHz basé sur les jonctions à six ports

# Rapport final


## *Executive Summary*

*The purpose of this feasibility study was to determine the performance and complexity of a homodyne receiver based on a six port junction. Analysis of the RF section of this receiver has been established and its demonstration can be found in a number of publications. Therefore, this study was mainly concerned about the feasibility of a demodulator capable of recovering the in-phase (I) and quadrature (Q) components when a Quadrature Phase Shift Keying (QPSK) modulated signal is received.*

*The main topics of this research were: • theoretical analysis of the signal processing functions needed to achieve coherent demodulation; • modeling and simulation of these signal processing functions; • preliminary evaluation of the hardware design complexity of the devised demodulator in order to determine the technology to be considered for its implementation. The theoretical analysis of the signal processing functions has demonstrated that the performance of the receiver under consideration is equivalent to an optimum receiver subject to identical conditions. The receiver was modeled and simulated in the presence of wideband Gaussian noise and an adjacent channel interferer. Simulation results confirmed the previous results for the receiver performance. A novel architecture, for the signal processing functions, was generated in the form of a block diagram. This architecture was further modeled and simulated and its performance evaluated as a function of the number of quantization bits. These results will allow the system designer to determine the trade-offs between the performance requirements and the sampling speed and number of quantization bits to be used. A case studied herein demonstrates the possibility of using readily available microelectronics technology to recover the I and Q components of a QPSK signal sampled at 116 Msamples/s. The resulting quantization noise is 20 dB below the recovered signals. The major modules in this case are four A/D converters, four filters and a maximum of two Field Programmable Gate Array (FPGA) chips.*

*The proposed implementation is of average complexity and can be achieved at a competitive cost for this application.*

## Sommaire

L'étude de faisabilité visait à établir les performances et la complexité d'un récepteur homodyne basé sur une jonction à six ports. L'analyse de la section fréquence radio, RF, de ce récepteur était déjà établie et des publications démontrent sa faisabilité. Cette étude était principalement concentrée sur la section du démodulateur. La recherche fut basée sur l'analyse du traitement du signal pour démoduler de façon cohérente, sur la simulation numérique sous diverses conditions et sur la conception préliminaire d'un tel récepteur pour déterminer la technologie nécessaire à sa réalisation. L'analyse a démontré qu'un tel récepteur permet d'obtenir les mêmes performances qu'un récepteur optimal sous des conditions équivalentes. Ces résultats ont été confirmés par des simulations en présence de bruit sur une large bande et d'un signal interférent du canal adjacent. L'analyse a aussi permis de trouver une nouvelle architecture de traitement du signal simplifiée pour la reconstitution des signaux en phase et en quadrature. Cette architecture a été partitionnée et simulée avec un nombre de bits de quantification variable. À partir des spécifications du système, il sera alors possible de connaître la quantification et le rythme de traitement nécessaire à la réception cohérente du signal. Par exemple, pour une reconstitution des signaux en phase et en quadrature au rythme de 116 Méchantillons/s et avec une puissance du bruit de quantification de plus de 20 dB inférieure au signal, la technologie micro-électronique nécessaire à la réception utilisant la jonction six ports est disponible ainsi que de coût et de complexité très raisonnables. Dans ce cas la complexité suivante pourrait être nécessaire à la reconstitution des signaux: quatre convertisseurs A/N à huit bits, quatre filtres analogiques et un ou deux circuits de logique programmable.

## 1.0 Introduction

Ce rapport final met un terme aux travaux faisant partie du contrat de recherche, numéro 67CRC-5-3109/001/ST, entre l'ÉTS et le CRC sur l'étude de faisabilité d'un récepteur homodyne à 20 GHz basé sur les jonctions à six ports. Ce projet a permis de démontrer la faisabilité d'un tel récepteur en utilisant des technologies présentement disponibles. Le rapport présente l'ensemble des analyses et des résultats de simulation permettant de soutenir cette démonstration. Ces résultats permettront, entre autres, de quantifier la complexité et les performances associées à un tel récepteur.

Ce rapport est présenté comme suit. La seconde section porte sur le contexte de cette étude de faisabilité, on y résume la problématique et les objectifs de ce projet. À la section trois, les résultats fonctionnels d'analyse et de simulation sont présentés, ces résultats démontrent que, sans tenir compte de la complexité, le récepteur fonctionne de la même façon qu'un récepteur idéal. Les résultats d'analyse de complexité sont présentés à la quatrième section, on y analyse l'effet de la

quantification et de l'architecture de l'unité de traitement numérique des signaux. Ce rapport se termine par une conclusion et nos recommandations quant à l'utilisation de la jonction six ports pour la réception homodyne. Les modèles de simulation sont présentés à l'annexe A, l'ensemble des résultats de simulations à l'annexe B, l'analyse théorique est présentée à l'annexe C, l'analyse de complexité à l'annexe D et l'analyse de la jonction six ports se trouve à l'annexe E, nous nous référerons aux diverses sections de ces annexes tout au long de ce rapport.

## 2.0 Contexte de l'étude de faisabilité

### 2.1 Problématique

La réception de signaux de fréquence élevée, ici 20 GHz, nécessite généralement plusieurs étages de conversion du signal à des fréquences intermédiaires. Le coût de réalisation matérielle de ces conversions est relativement élevé. Récemment, monsieur Renato Bosisio et son équipe à l'École Polytechnique de Montréal, ont proposé une architecture de réception basée sur la jonction six ports. Le signal reçu est amplifié et alimente cette jonction, les puissances de quatre sorties (ports) sont détectées, filtrées puis échantillonnées. Ainsi la jonction est utilisée pour accomplir une conversion directe du signal en des signaux en bande de base. Ces signaux doivent toutefois être traités numériquement puisque les puissances échantillonnées ne sont pas directement proportionnelles aux signaux désirés. Une analyse plus détaillée du fonctionnement de la jonction six ports se trouve à l'annexe E. Dans le cas spécifique de ce contrat, le signal reçu porte une modulation numérique QPSK de 116 Mbits/s mise en forme avec un filtre de cosinus élevé ($\alpha = 0.4$). L'échantillonnage des puissances doit donc se faire à des taux d'au moins 58 MHz, sinon 116 MHz ou plus, à de telles vitesses, un traitement du signal trop complexe serait difficilement envisageable. De plus, puisqu'un signal d'une largeur de bande de 500 MHz est introduit à l'entrée de la jonction, quelle sera l'influence des canaux adjacents et du bruit sur cette bande ?

### 2.2 Objectifs

L'étude de faisabilité tente de répondre aux questions fondamentales posées par l'introduction d'un tel changement technologique dans la réception des signaux. De façon spécifique, on désire analyser les points suivants :

- les performances d'un tel système en présence de bruit et d'interférence sur une large bande, en fonction de la fréquence d'échantillonnage ;

- la complexité du module de traitement numérique du signal et la quantification nécessaire pour soutenir la démodulation cohérente du signal.

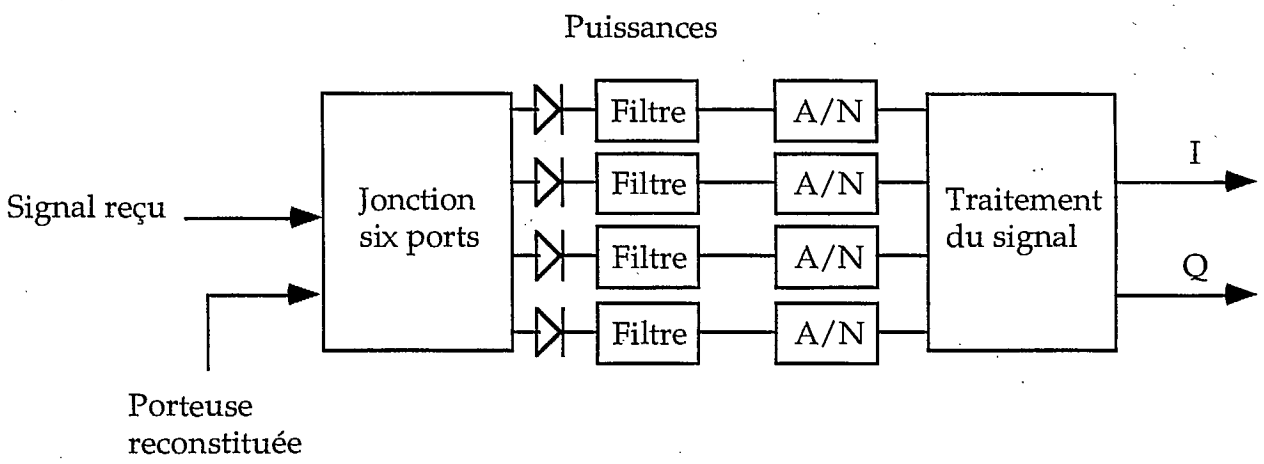
## 3.0 Résultats fonctionnels

Afin de démontrer la faisabilité d'un récepteur à jonction six ports, les performances en présence de bruit de ce récepteur ont été simulées et déterminées analytiquement. Ces résultats ont pu être obtenus en trois étapes typiques d'une démarche scientifique : observation des performances, démonstration théorique et validation des résultats.

### 3.1 Observation des performances

La première étape de cette étude consistait à observer les résultats de simulations du récepteur utilisant la jonction six ports sous diverses conditions. Ainsi, la jonction a été utilisée pour la réception d'un signal sinusoïdal non modulé (voir les détails à l'annexe B.2.1), la démodulation QPSK avec et sans jonction six ports (B.2.2 et B.2.3) ainsi que quelques essais préliminaires en variant le nombre de bits de quantification lors de l'échantillonnage des quatre ports permettant de dériver les signaux I et Q transmis. L'ensemble des résultats de simulation indique que la démodulation résultante permet d'obtenir les mêmes performances qu'une démodulation cohérente.

Rappelons que la réception consiste à utiliser la jonction pour obtenir quatre combinaisons linéaires du signal reçu et d'une porteuse localement reconstituée. Les puissances de ces combinaisons sont détectées à l'aide de diodes, ces puissances sont filtrées et puis échantillonnées. Un module de traitement du signal reconstitue les signaux en phase (I) et en quadrature (Q) à partir de ces échantillons. La figure ci-dessous illustre ce récepteur.




Les résultats de ces observations indiquent que l'ordre dans lequel les opérations de filtrage et de reconstitution sont accomplies ne déterminait pas significativement les performances. Ainsi, que le filtrage soit fait analogiquement avant la conversion

numérique et la reconstitution des signaux I et Q, ou qu'il soit accomplit numériquement après la reconstitution importe peu. Ceci fut agréablement surprenant. Tout indiquait que l'opération de reconstitution des signaux I et Q était essentiellement linéaire.

### 3.2 Démonstration de la linéarité de la démodulation

La seconde étape a permis de démontrer que le récepteur était à toutes fins pratiques l'équivalent d'un démodulateur cohérent. Ainsi le signal, qu'il soit additionné d'une interférence ou de bruit, est traité de telle sorte que l'on obtienne les mêmes signaux I et Q que pour une démodulation cohérente.

La détection de puissance introduit des éléments non linéaires au signal filtré puis détecté. Mais puisque les proportions de ces éléments non linéaires sont connues pour les quatre sorties, on utilise une combinaison linéaire de ces sorties pour éliminer les termes non linéaires. Une autre combinaison linéaire des valeurs résultantes est ensuite accomplie pour déterminer les valeurs de I et de Q. Le traitement analytique complet est présenté à l'annexe C.

Ce traitement est possible si les combinaisons linéaires accomplies dans la jonction à six ports sont connues. Ainsi, lors de la calibration de cette jonction, ces combinaisons sont déterminées et on peut alors fixer les constantes nécessaires à la détermination de I et de Q.

Notons que la démonstration présentée à l'annexe C utilise un traitement du signal différent de ce que les chercheurs de l'École Polytechnique nous ont soumis. Ce nouveau traitement est beaucoup plus simple puisqu'il évite l'utilisation de produits ou de divisions de signaux. Ce nouveau traitement du signal a été simulé avec succès et les résultats sont présentés à l'annexe B.3.1.

### 3.3 Validation du fonctionnement

Cette troisième étape consistait essentiellement à vérifier les résultats de performances en présence d'un signal interférent de puissance égale sur un canal adjacent (B.2.5). De plus, des simulations avec un autre modèle de jonction à six port ont été accomplies (B.2.6). Ces résultats ont confirmé la validité de ce type de démodulateur.

## 4.0 Résultats de complexité

L'analyse de la complexité concerne essentiellement le module de traitement numérique du signal. Un aspect déterminant concerne le taux d'échantillonnage

nécessaire à la sortie de ce module. Si l'on désire des valeurs de I et de Q suréchantillonnées au double du taux de transmission des symboles (116 Méchantillons/s = 2 x 58 Msymboles/s), l'échantillonnage A/N et le traitement nécessaire pour reconstituer I et Q devra s'accomplir à ce rythme. Sans considérer la rapidité de l'acquisition de la porteuse et de l'horloge, un rythme de 58 MHz peut suffire pour démoduler le signal. Notons que si les stratégies d'acquisition nécessitent des signaux I et Q à un rythme de 116 MHz, la technologie nécessaire pour l'acquisition à ce rythme pourra être utilisée pour la reconstitution des signaux I et Q. De plus, puisque le traitement du signal est sans mémoire, il peut être parallèlisé à souhait grâce à l'utilisation de multiplexeur et de démultiplexeur. Une petite latence sera alors introduite.

Ainsi on peut premièrement évaluer la complexité du problème en soi, et ensuite discuter des technologies disponibles pour réaliser le module de reconstitution à divers taux d'échantillonnage. L'algorithme présenté à l'annexe D, suggère une simplification de l'architecture par partitionnement du problème. En effet, de façon globale il y a un port dont la valeur de tension ne dépend que de l'amplitude de la porteuse. Cette valeur ne variant pas, elle n'est lue que lors de la calibration de l'appareil. Le circuit combinatoire résultant a donc trois entrées quantifiées sur n bits et deux sorties d'au plus huit bits. De façon immédiate, si les entrées peuvent être quantifiées sur huit bits, il suffirait d'un circuit de mémoire de $2^{(3x8)}$ = 16 Madresses par 16 bits pour accomplir cette reconstitution (de tels circuits existent à des taux d'accès excédant les 100 MHz). En analysant le circuit existant on peut même partitionner le problème en trois circuits de mémoire de 64 Kadresses (voir les détails à l'annexe D).

La dernière question demeurant en suspend concerne donc le nombre de bits de quantification nécessaires à la reconstitution des signaux I et Q et ce, pour les signaux échantillonnés et les signaux utilisés pour le traitement interne dans le problème partitionné. Afin de mesurer l'effet de cette quantification, nous avons procédé à la simulation de ce processus de quantification. Le signal I a été remplacé par une rampe afin de mesurer le rapport signal à bruit de quantification introduit par le module de reconstitution. Les détails de ces simulations sont présentés à l'annexe B section 3.2. On y découvre que pour une quantification globale à 8 bits, le rapport signal à bruit de quantification est d'environ 34 dB. Ainsi, avec une telle quantification le bruit introduit par les arrondissements de la reconstitution est nettement plus faible que le bruit gaussien nominal présent sur le canal.

Si les spécifications de système le permettent, on pourrait diminuer la quantification globale à six bits, pour un rapport signal à bruit de quantification de l'ordre de 23 dB. De plus, les sorties devraient pouvoir être quantifiée à seulement quatre bits. Le circuit combinatoire résultant, correspondrait alors, dans le pire des cas, à l'utilisation d'une mémoire de $2^{(3x6)}$adresses avec un contenu de huit bits, ce qui correspond à un circuit de 256 Koctets.

Les technologies de logique programmable peuvent aussi être utilisée, le plus petit circuit (EPM7032) de la compagnie ALTERA fonctionne à 125 MHz et comporte 36 entrées-sorties possibles. La technologie programmable nécessaire à la réalisation d'une quantification à six ou huit bits est donc disponible. Si le volume de production le permet, on peut même utiliser des techniques VLSI dédiées (« Full Custom ») ou de matrice de portes (« Gate Arrays ») pour réaliser le circuit de reconstitution.

## 5.0 Conclusions

Pour conclure, cette étude permet d'affirmer que la démodulation homodyne en utilisant la jonction à six ports est réalisable et que la technologie pouvant réaliser le démodulateur existe. Un certain nombre de spécifications seraient toutefois nécessaires pour donner une évaluation précise du coût du module de reconstitution. Il faudrait pour ce faire connaître le volume de production ainsi que le rythme et la quantification nécessaires aux signaux I et Q. Nous pouvons toutefois affirmer que le système est **réalisable et de complexité raisonnable**. Ainsi, lorsque les spécifications seront connues, nous recommandons la réalisation d'un prototype « preuve de concept » afin de démontrer la faisabilité mais surtout la complexité raisonnable du résultat.

# Annexe A

# Paramètres et modules du simulateur

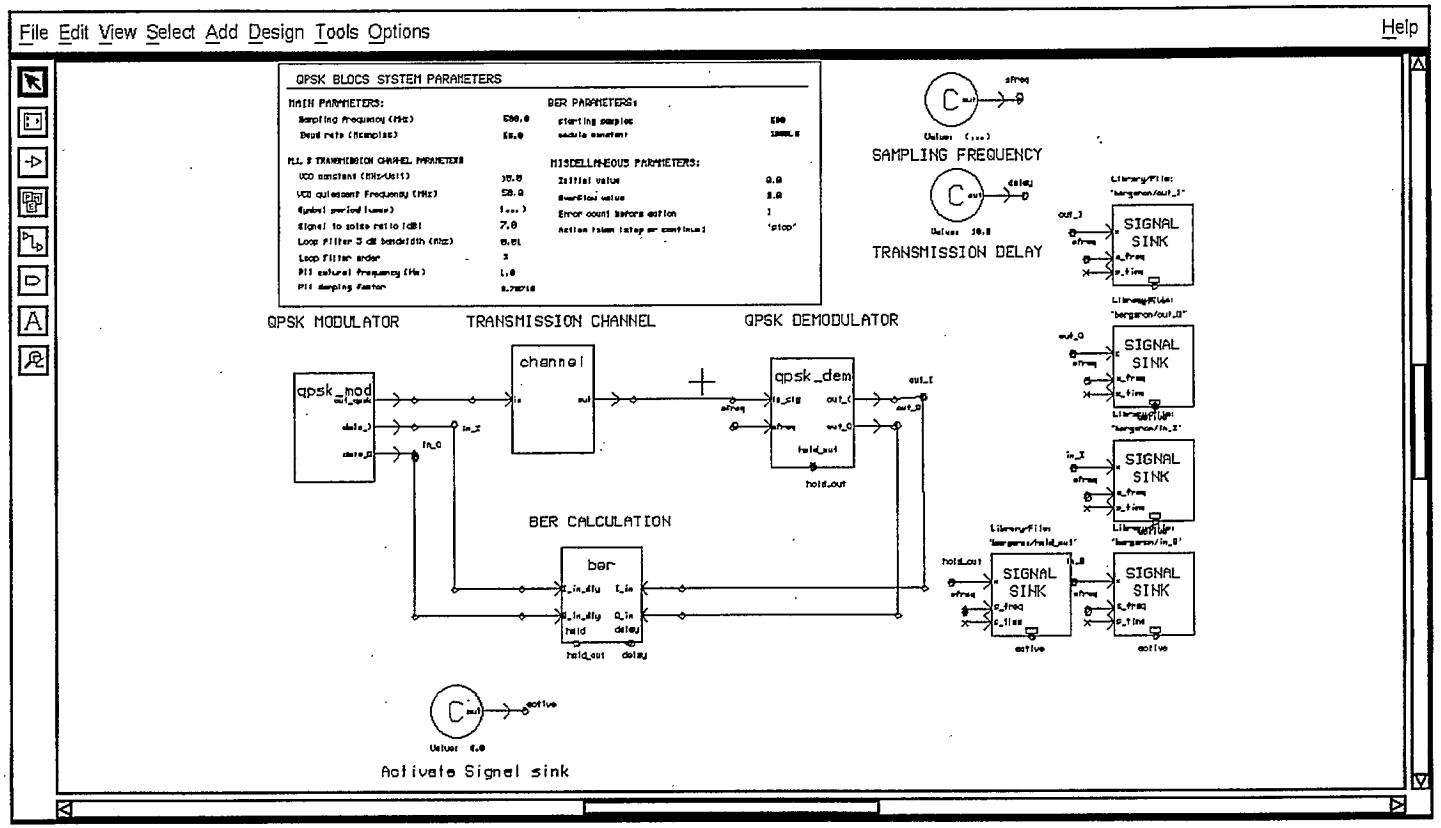
**Marc Bergeron ÉTS/LACIME**
**Le 1 avril 1996**

# Table des matières

A1. Paramètres du démodulateur QPSK classique en bande de base
A2. Paramètres du démodulateur utilisant le six ports
A3. Nouveaux paramètres du six ports
A4. Paramètres du système avec ajout d'interférence
A5. Paramètres du six ports modélisé analogiquement
A6. Paramètres du six ports modélisé et numérisé

# Section A1

## Paramètres du démodulateur QPSK classique en bande de base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QPSK BLOCS SYSTEM PARAMETERS
MAIN PARAMETERS:
BER PARAMETERS:
MISCELLANEOUS PARAMETERS:
SAMPLING FREQUENCY
TRANSMISSION DELAY
QPSK MODULATOR
TRANSMISSION CHANNEL
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qpsk_dem
BER CALCULATION
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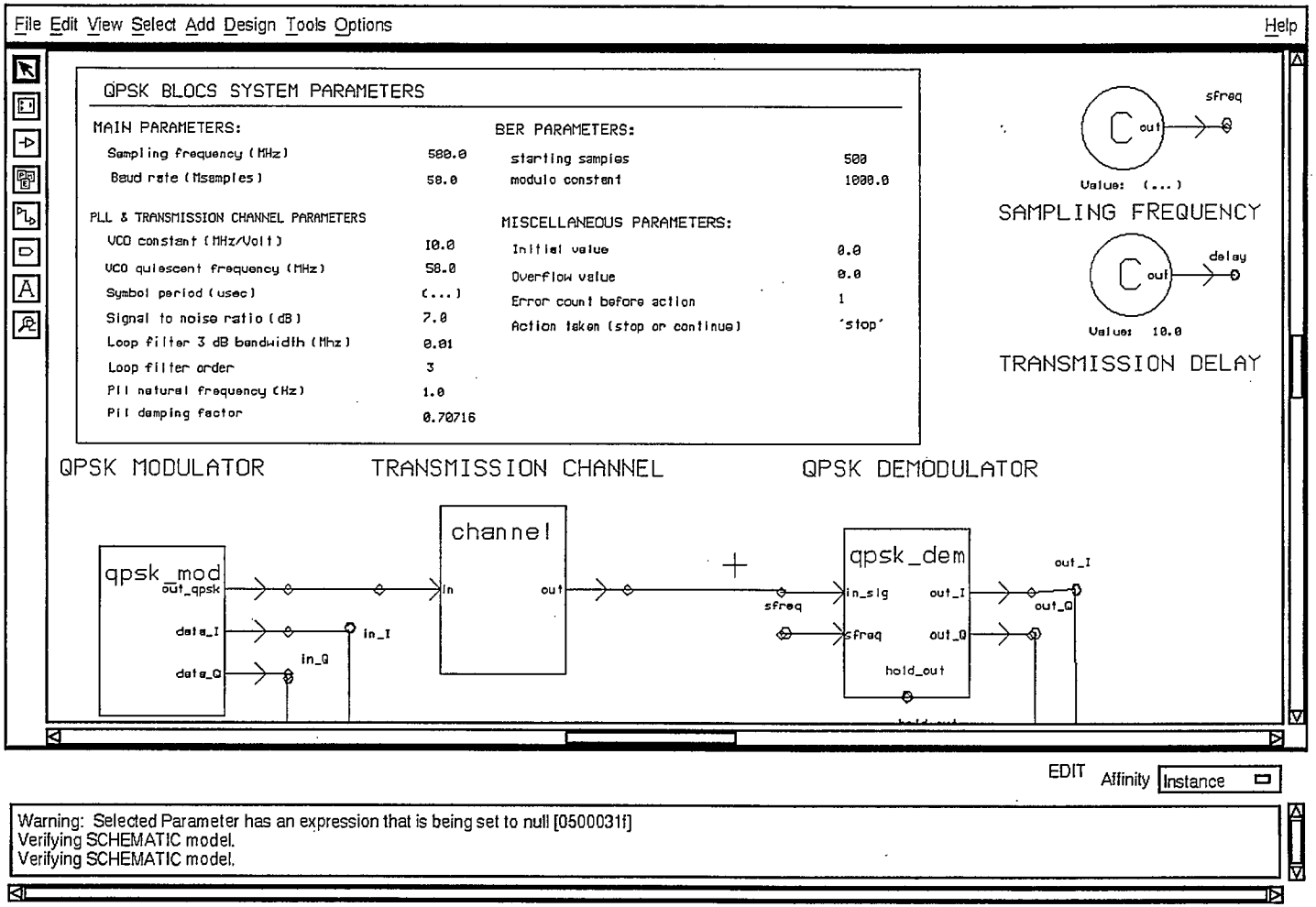
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MAIN PARAMETERS:
Sampling frequency (MHz) 500.0
Baud rate (Msamples) 50.0
PLL & TRANSMISSION CHANNEL PARAMETERS
VCO constant (MHz/Volt) 10.0
VCO quiescent frequency (MHz) 50.0
Symbol period (usec) (...)
Signal to noise ratio (dB) 7.0
Loop filter 3 dB bandwidth (Mhz) 0.01
Loop filter order 3
PII natural frequency (Hz) 1.0
PII damping factor 0.70716
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starting samples 500
modulo constant 1000.0
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Overflow value 0.0
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out
Value: (...)
SAMPLING FREQUENCY
delay
out
Value: 10.0
TRANSMISSION DELAY
QPSK MODULATOR
TRANSMISSION CHANNEL
QPSK DEMODULATOR
qpsk_mod
out_qpsk
data_I
data_Q
in_I
in_Q
channel
in
out
sfreq
qpsk_dem
in_sig
sfreq
out_I
out_Q
hold_out
out_I
out_Q
EDIT
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Warning: Selected Parameter has an expression that is being set to null [0500031f]
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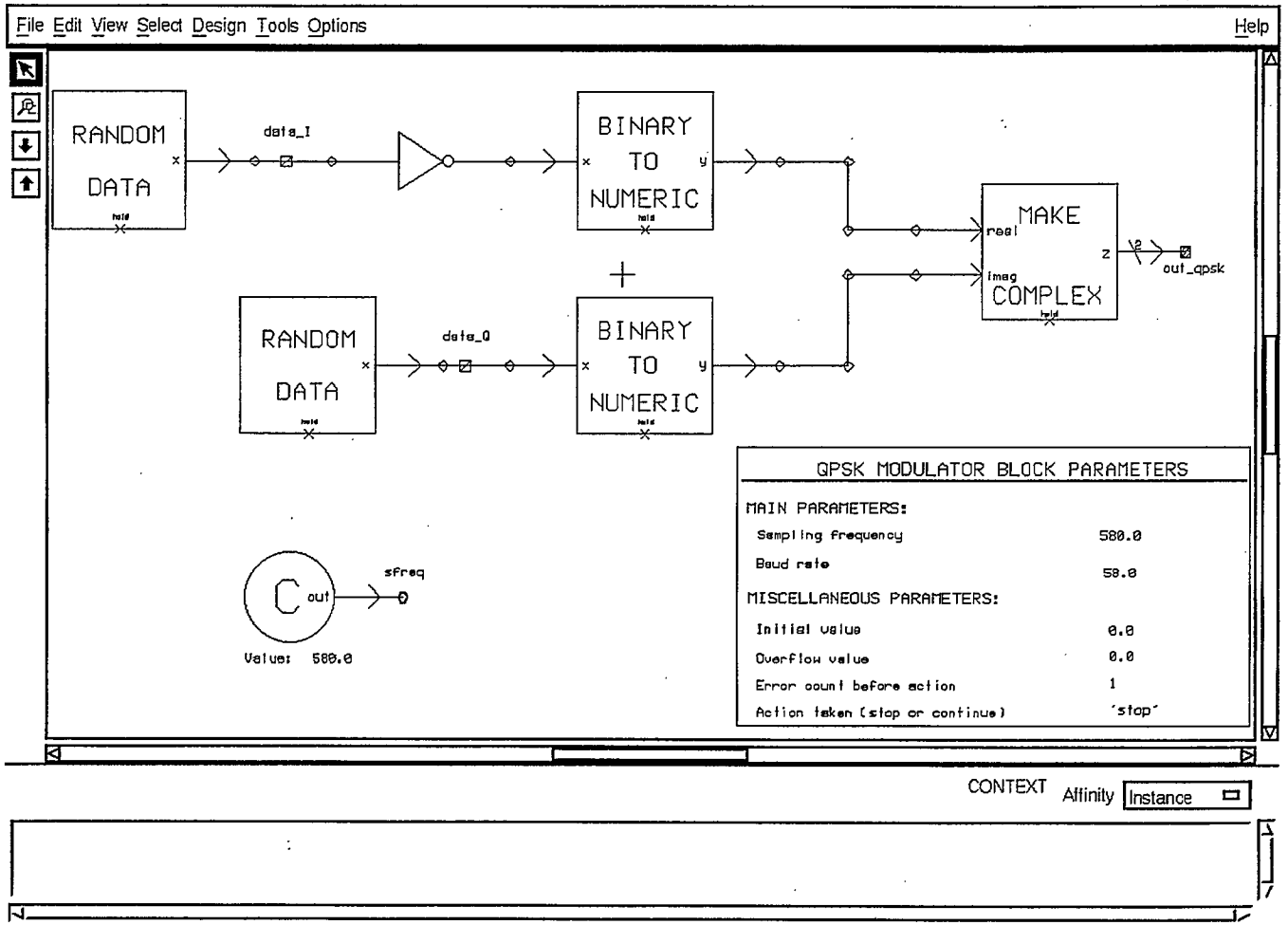
Verifying SCHEMATIC model.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RANDOM DATA
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real
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out_qpsk
RANDOM DATA
data_Q
BINARY TO NUMERIC
C out
sfreq
Value: 580.0
QPSK MODULATOR BLOCK PARAMETERS
MAIN PARAMETERS:
Sampling frequency 580.0
Baud rate 58.0
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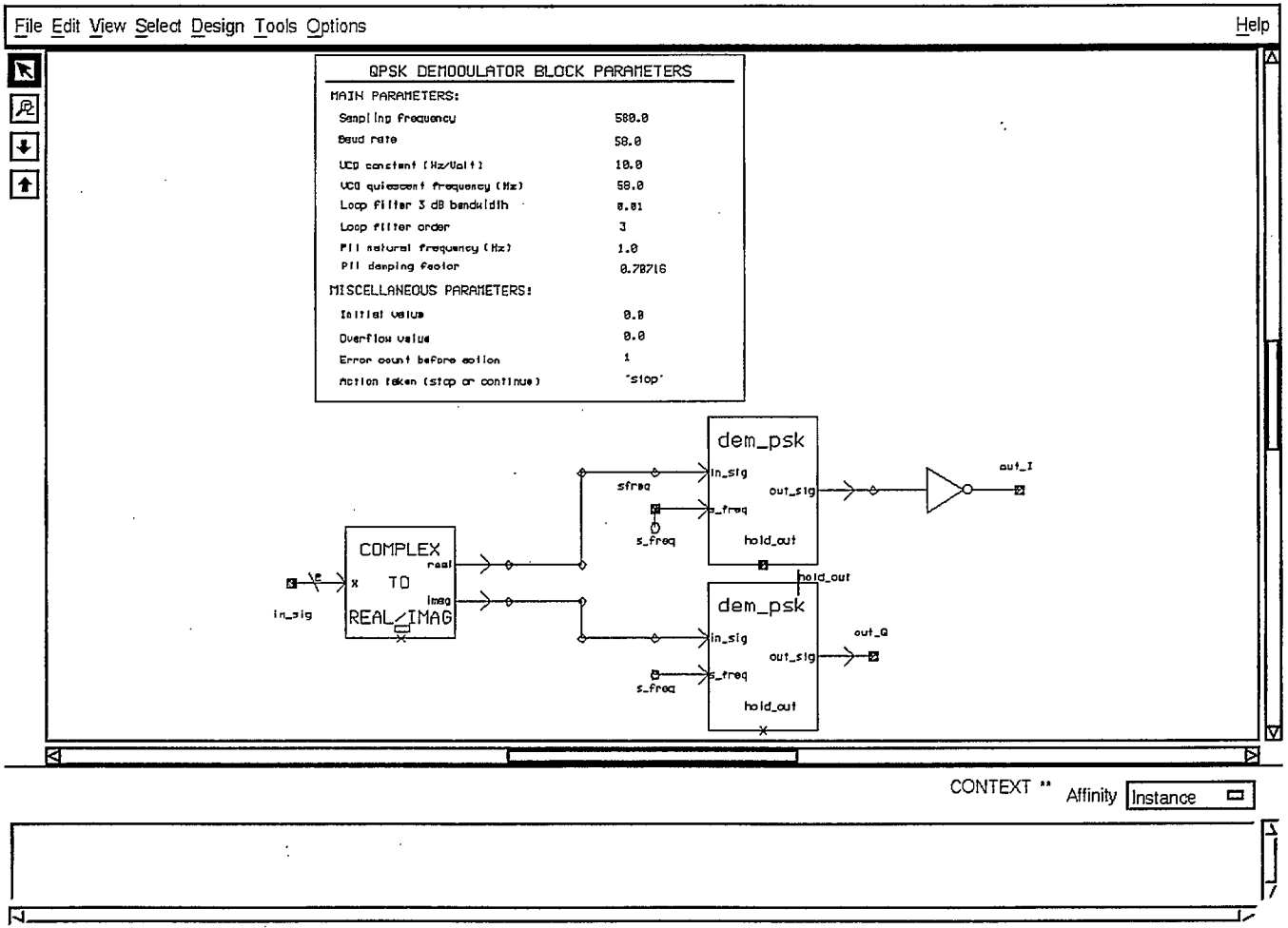
CONTEXT Affinity Instance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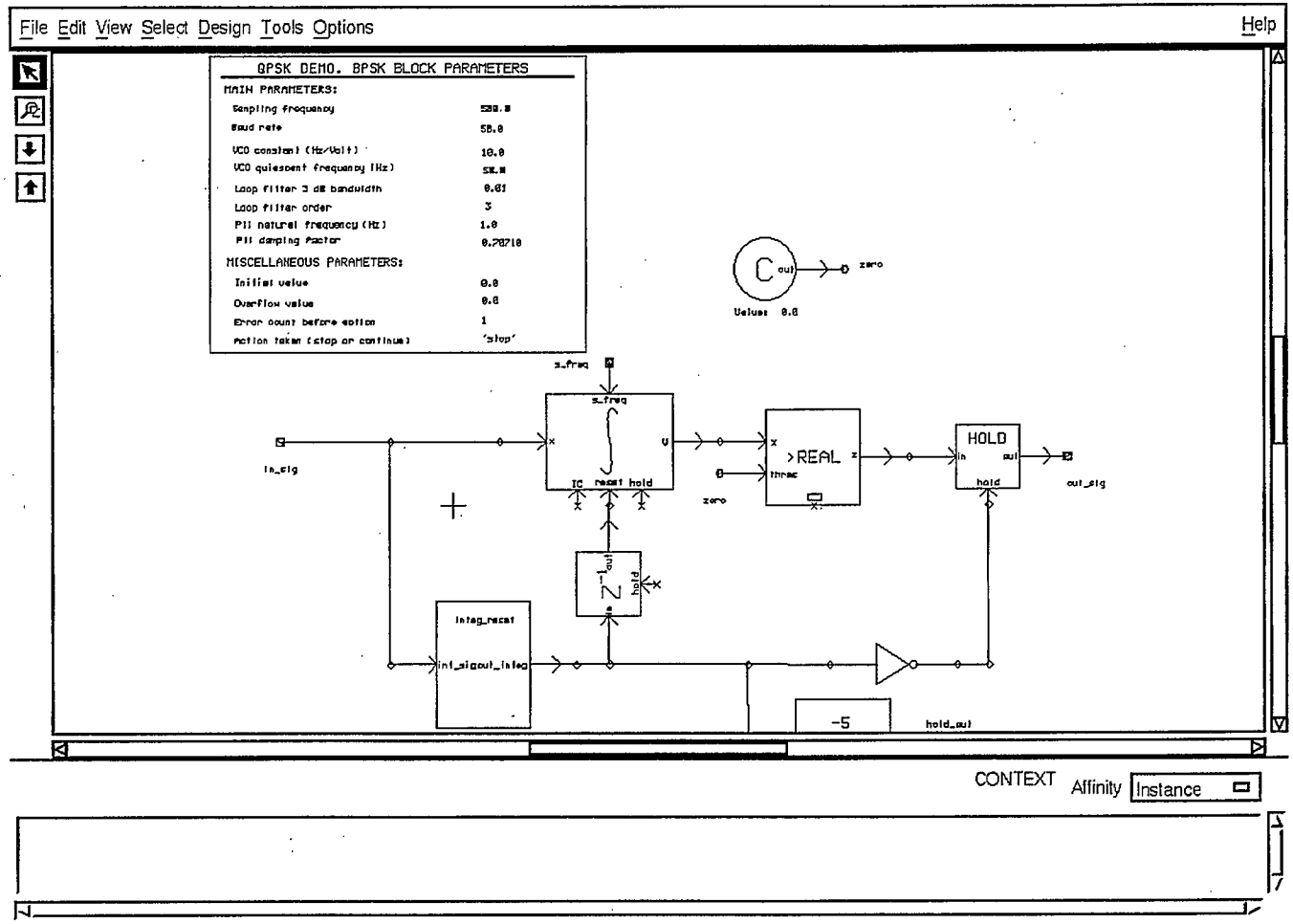
Baud rate 58.0
VCO constant (Hz/Volt) 10.0
VCO quiescent frequency (Hz) 58.0
Loop filter 3 dB bandwidth 0.01
Loop filter order 3
PLL natural frequency (Hz) 1.0
PLL damping factor 0.70716
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) "stop"
dem_psk
in_sig
out_sig
s_freq
hold_out
sfreq
out_I
COMPLEX
TO
REAL/IMAG
real
imag
in_sig
out_Q
CONTEXT **
Affinity
Instance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QPSK DEMO. BPSK BLOCK PARAMETERS
MAIN PARAMETERS:
Sampling frequency
Baud rate 58.0
VCO constant (Hz/Volt) 10.0
VCO quiescent frequency (Hz)
Loop filter 3 dB bandwidth 0.01
Loop filter order 3
PII natural frequency (Hz) 1.0
PII damping factor 0.70710
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
C
out
zero
Value: 0.0
s_freq
in_sig
IC
reset
hold
>REAL
thres
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in
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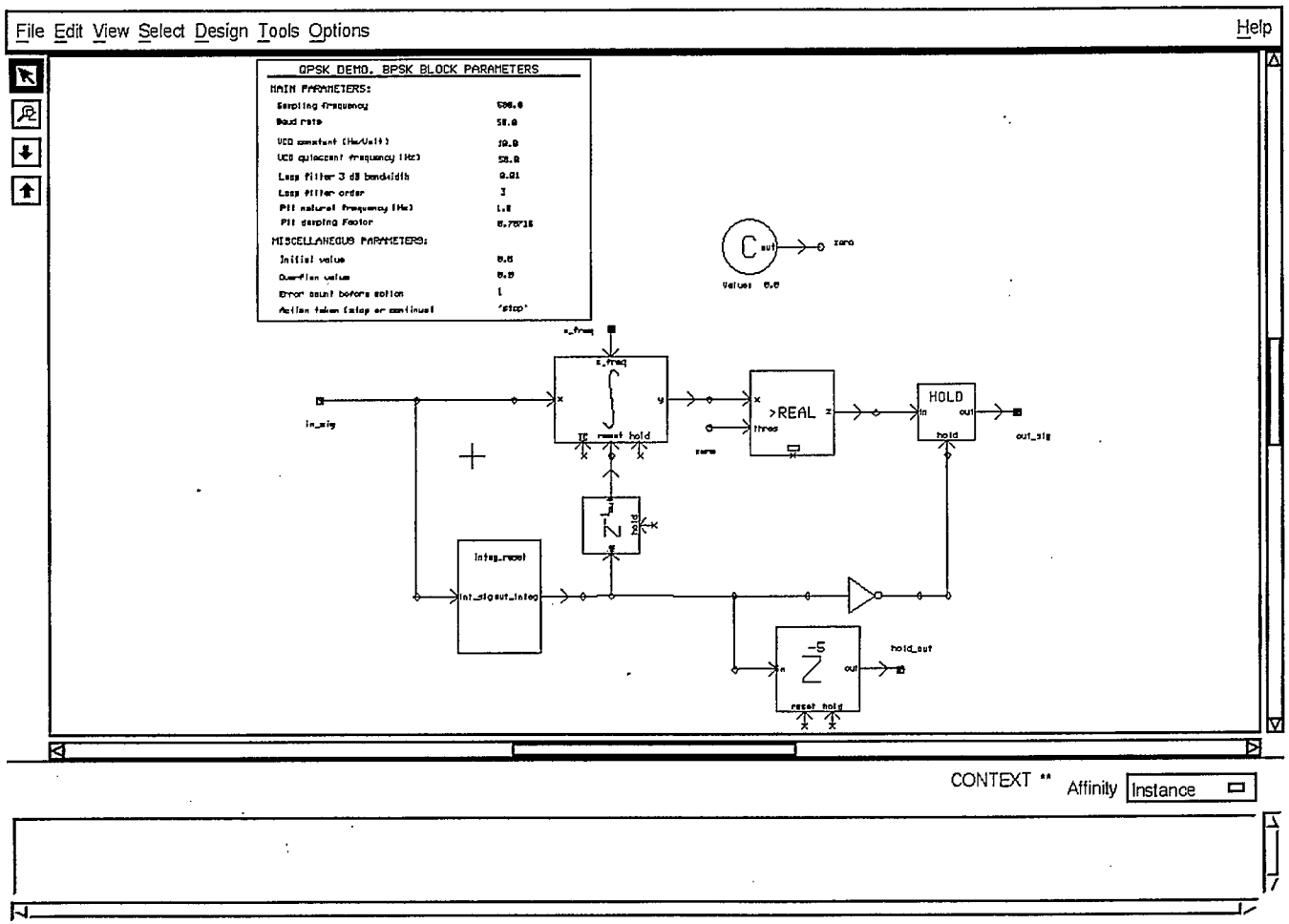
out_sig
integ_reset
int_sig
out_integ
-5
hold_out
CONTEXT
Affinity
Instance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QPSK DEMO. BPSK BLOCK PARAMETERS
MAIN PARAMETERS:
Sampling frequency
Baud rate
VCO constant (Hz/Volt)
VCO quiescent frequency (Hz)
Loop filter 3 dB bandwidth
Loop filter order
Pll natural frequency (Hz)
Pll damping Factor
MISCELLANEOUS PARAMETERS:
Initial value
Overflow value
Error count before action
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Value: 0.0
x_freq
in_sig
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int_sig
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-5
out
reset
hold
hold_out
CONTEXT **
Affinity
Instance

File Edit View Select Design Tools Options Help

## QPSK RESET INTEGRATOR BLOCK PARAMETERS

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| VCO constant (Hz/Volt) | 10.0 |
| VCO quiescent frequency (Hz) | 58.0 |
| Loop filter 3 dB bandwidth | 0.01 |
| Loop filter order | 3 |

MISCELLANEOUS PARAMETERS:

| | |
|---|---|
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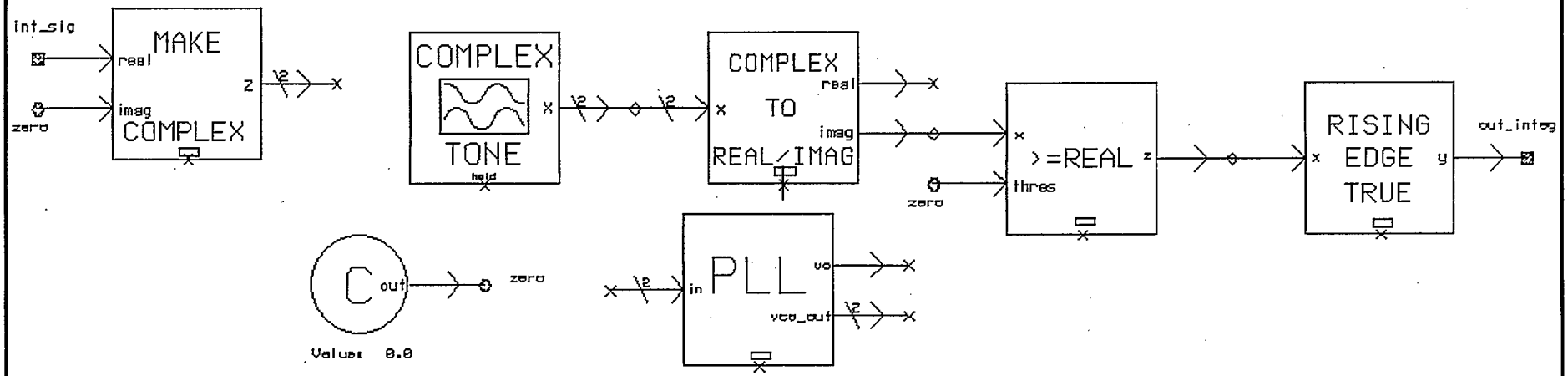
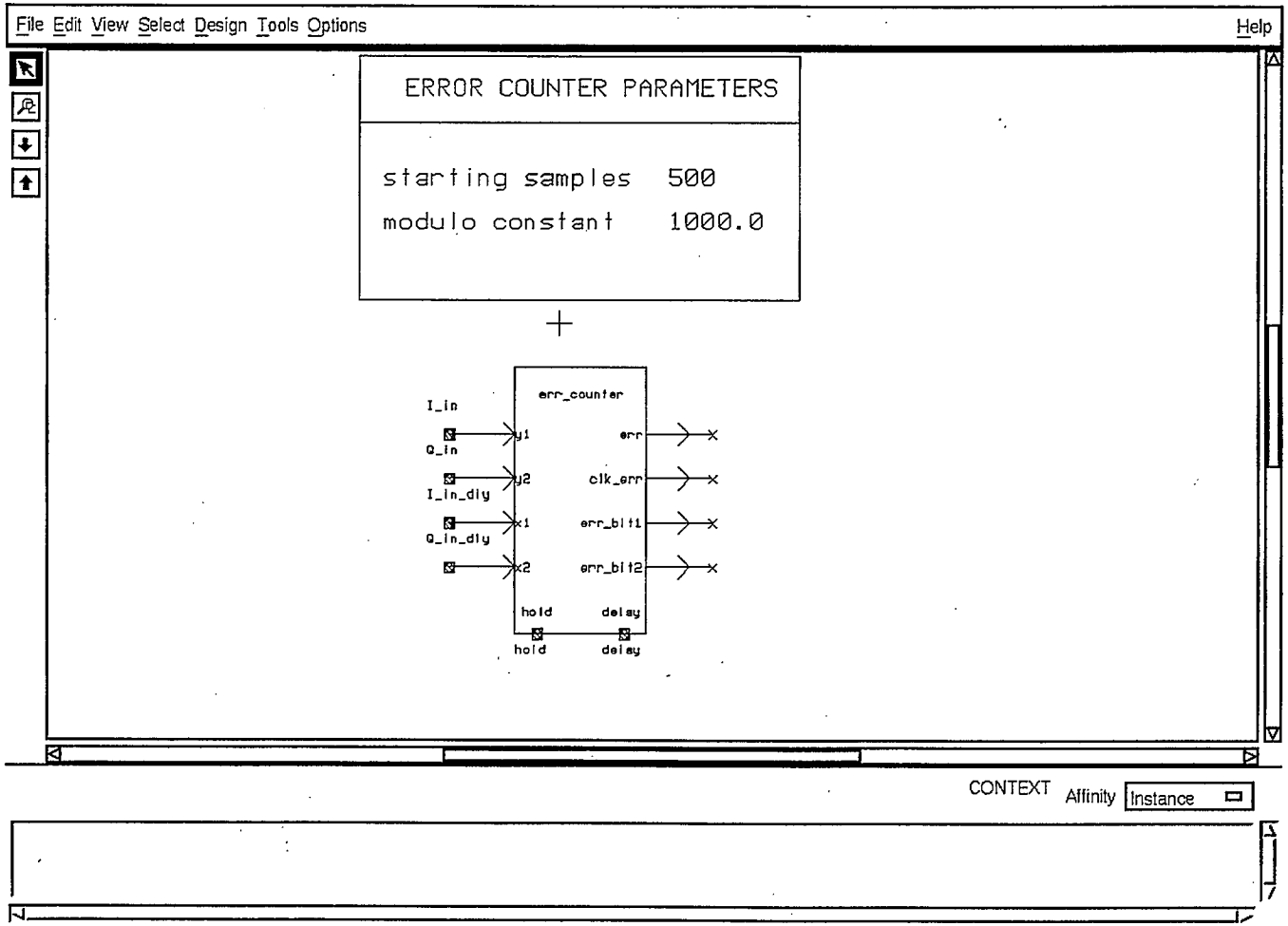
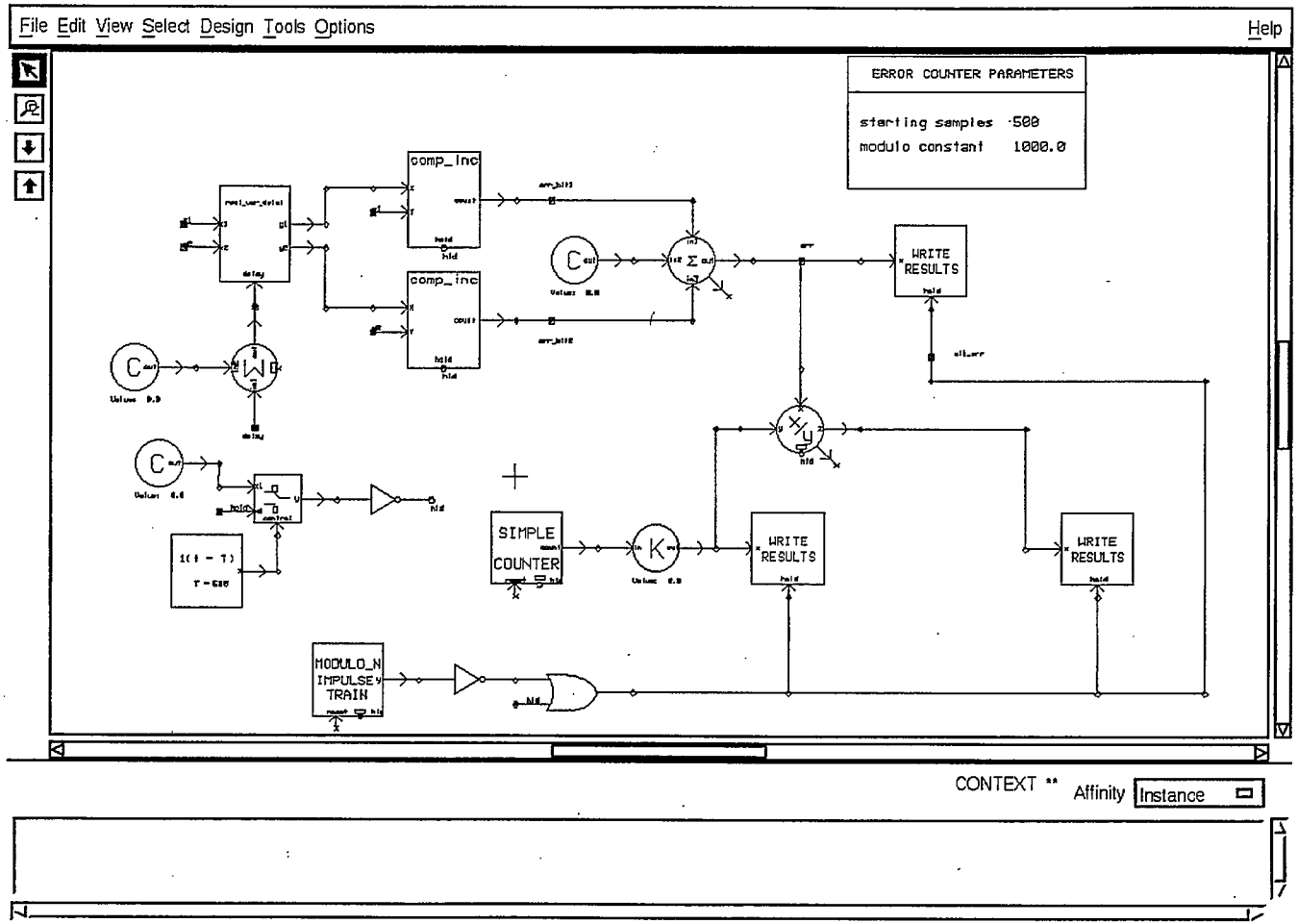
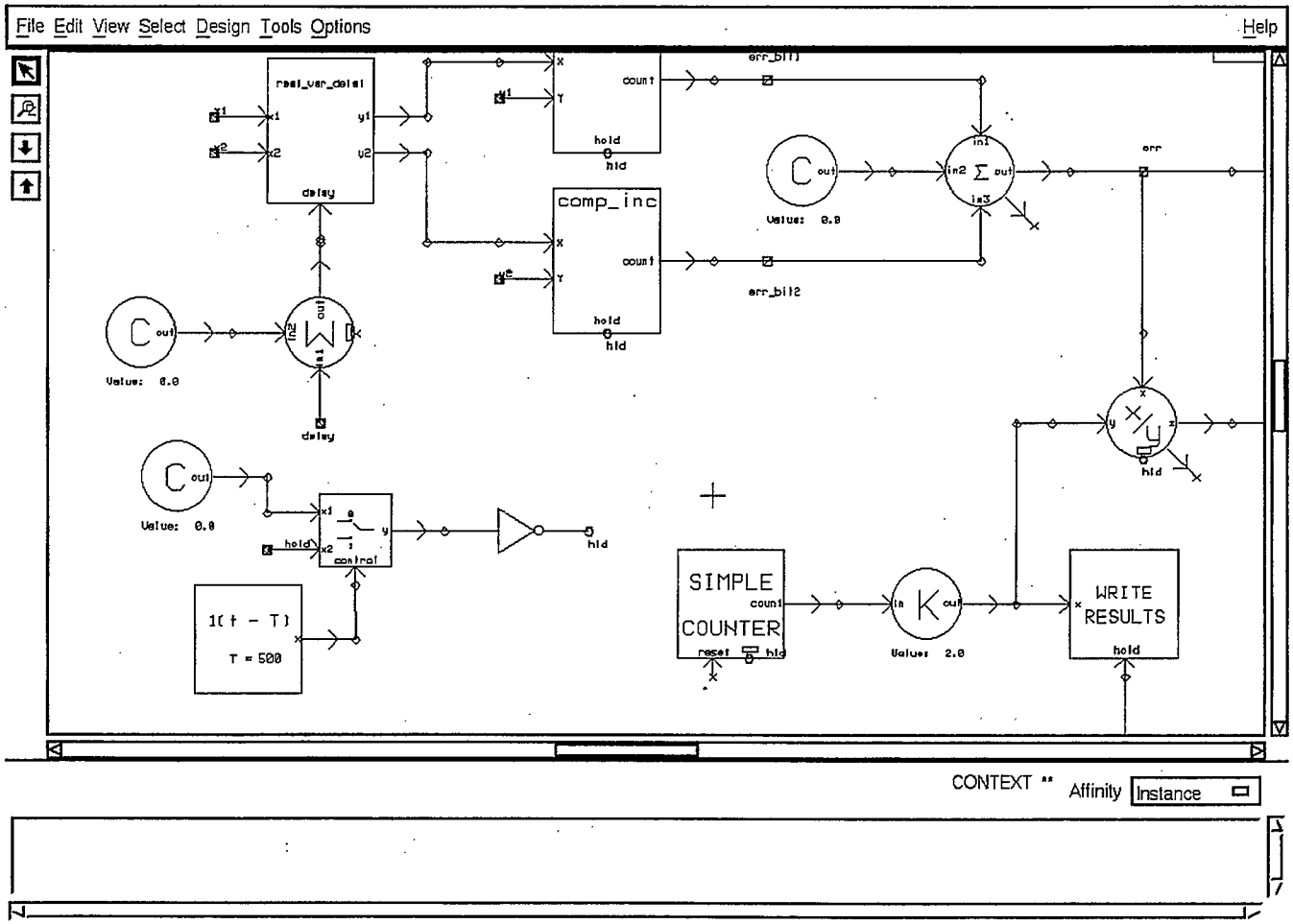
| Overflow value | 0.0 |
| Error count before action | 1 |
| Action taken (stop or continue) | 'stop' |



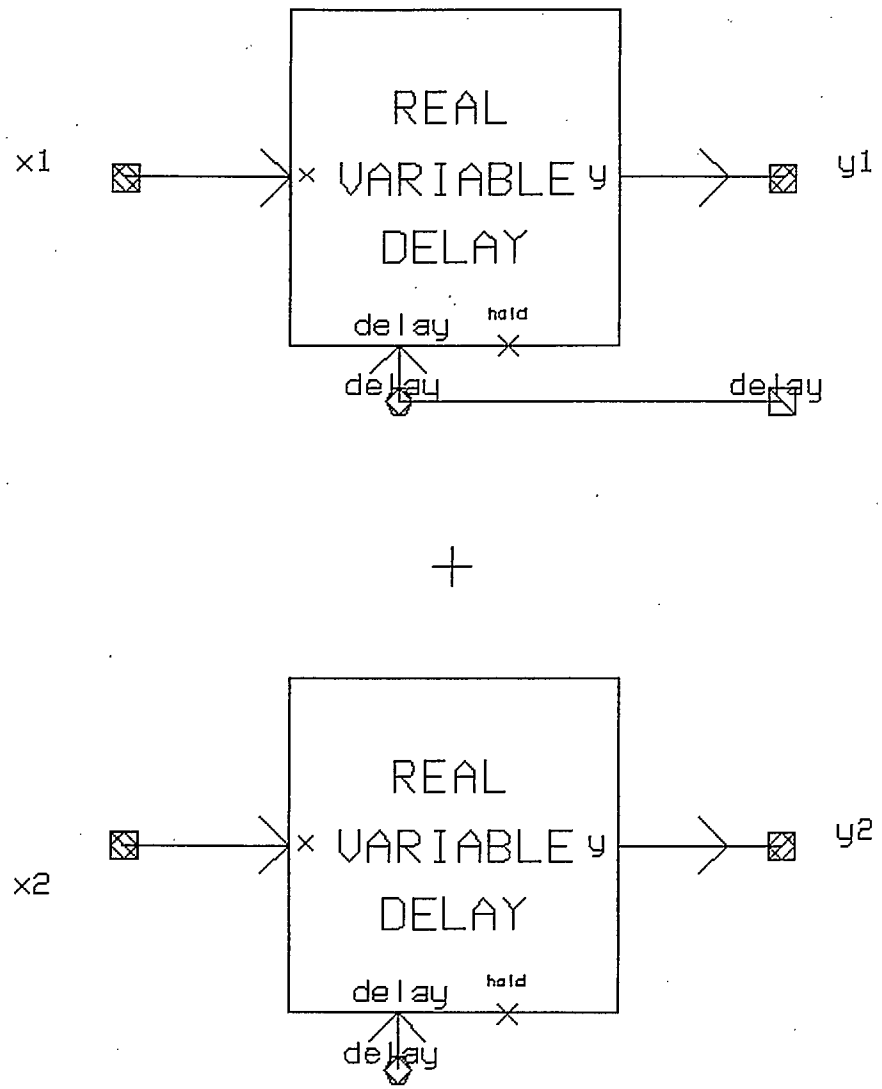

CONTEXT ** Affinity Instance


File Edit View Select Design Tools Options
Help
ERROR COUNTER PARAMETERS
starting samples 500
modulo constant 1000.0
err_counter
I_in
Q_in
I_in_dly
Q_in_dly
y1
y2
x1
x2
err
clk_err
err_bit1
err_bit2
hold
delay
hold
delay
CONTEXT
Affinity
Instance

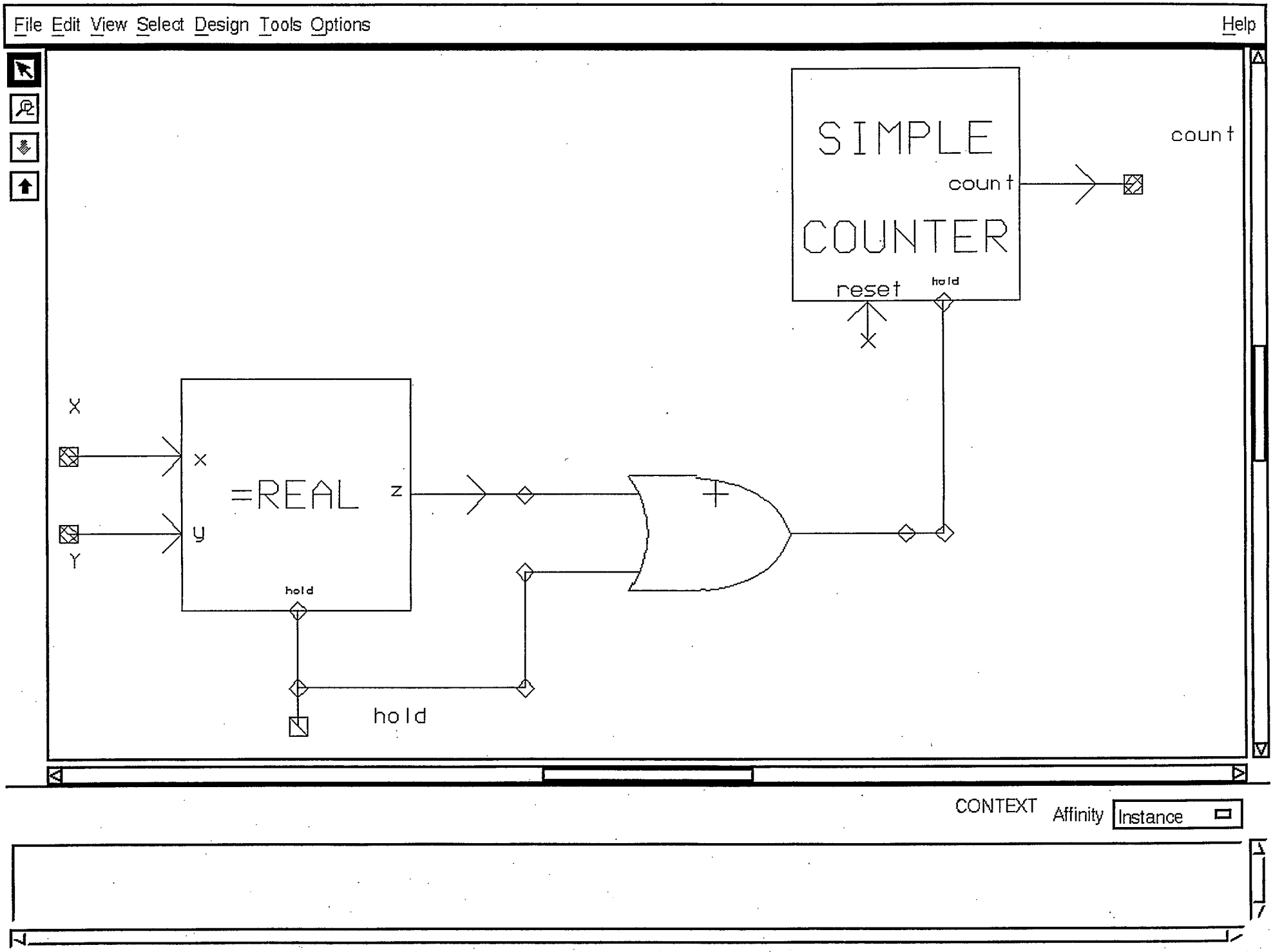

File Edit View Select Design Tools Options
Help
ERROR COUNTER PARAMETERS
starting samples 500
modulo constant 1000.0
comp_inc
comp_inc
WRITE RESULTS
SIMPLE COUNTER
WRITE RESULTS
WRITE RESULTS
MODULO_N IMPULSE TRAIN
CONTEXT **
Affinity
Instance


File Edit View Select Design Tools Options
Help
real_var_delay
delay
count
hold
hld
comp_inc
err_bit1
err_bit2
err
Value: 0.0
Value: 0.0
Value: 0.0
Value: 2.0
hold
control
1( t - T )
T = 500
SIMPLE
COUNTER
reset
WRITE
RESULTS
CONTEXT **
Affinity
Instance

File Edit View Select Design Tools Options Help

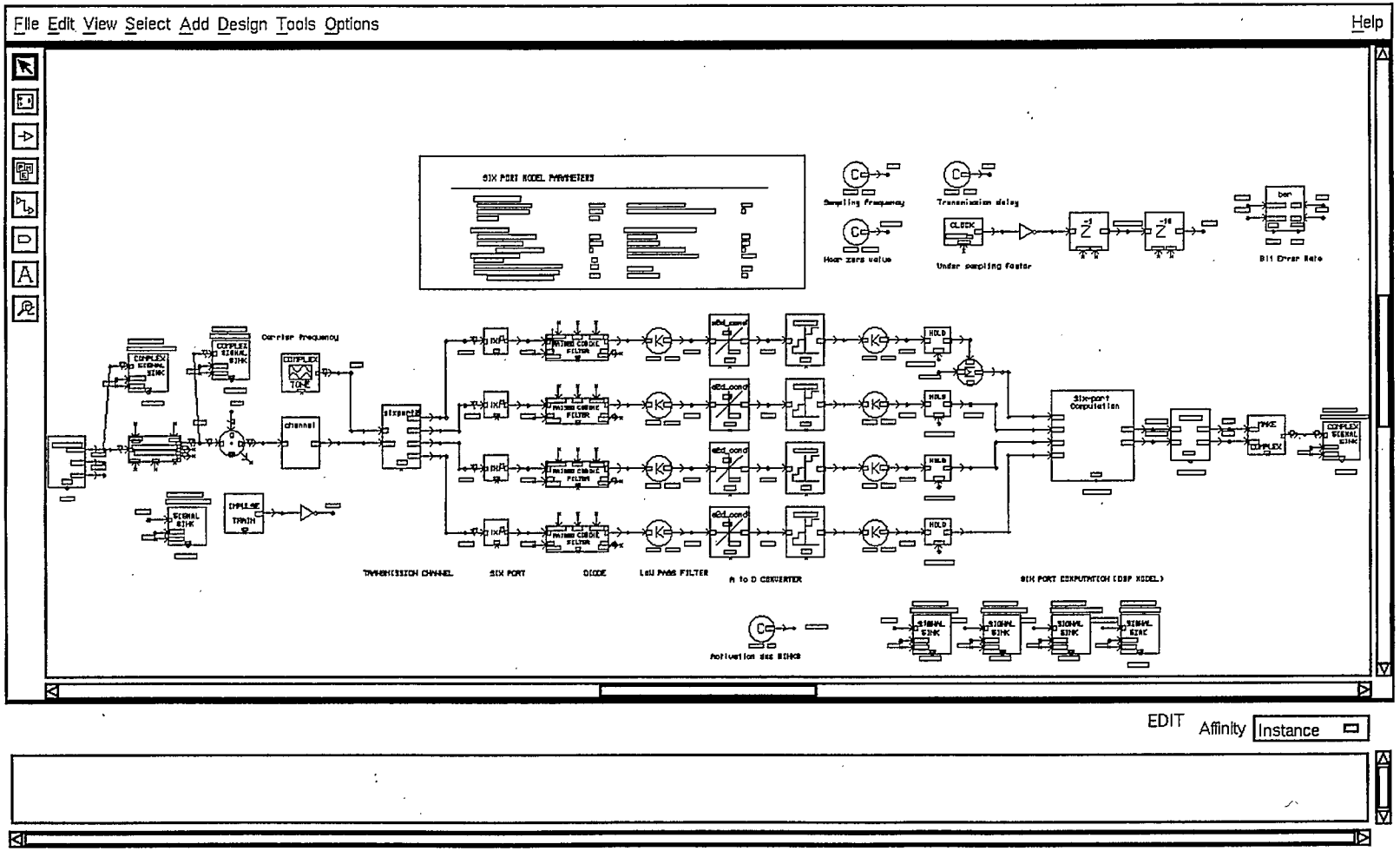


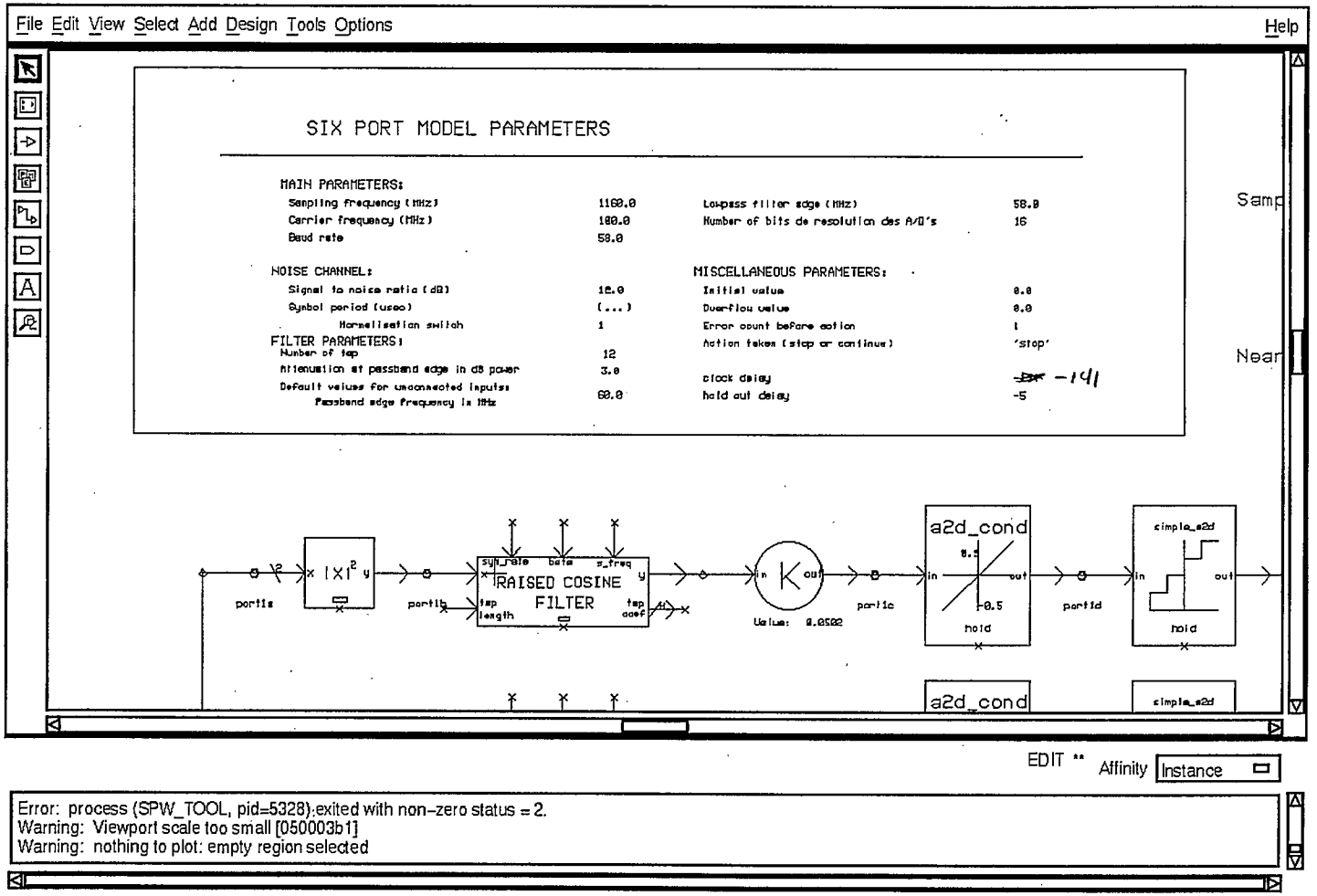

CONTEXT ** Affinity Instance

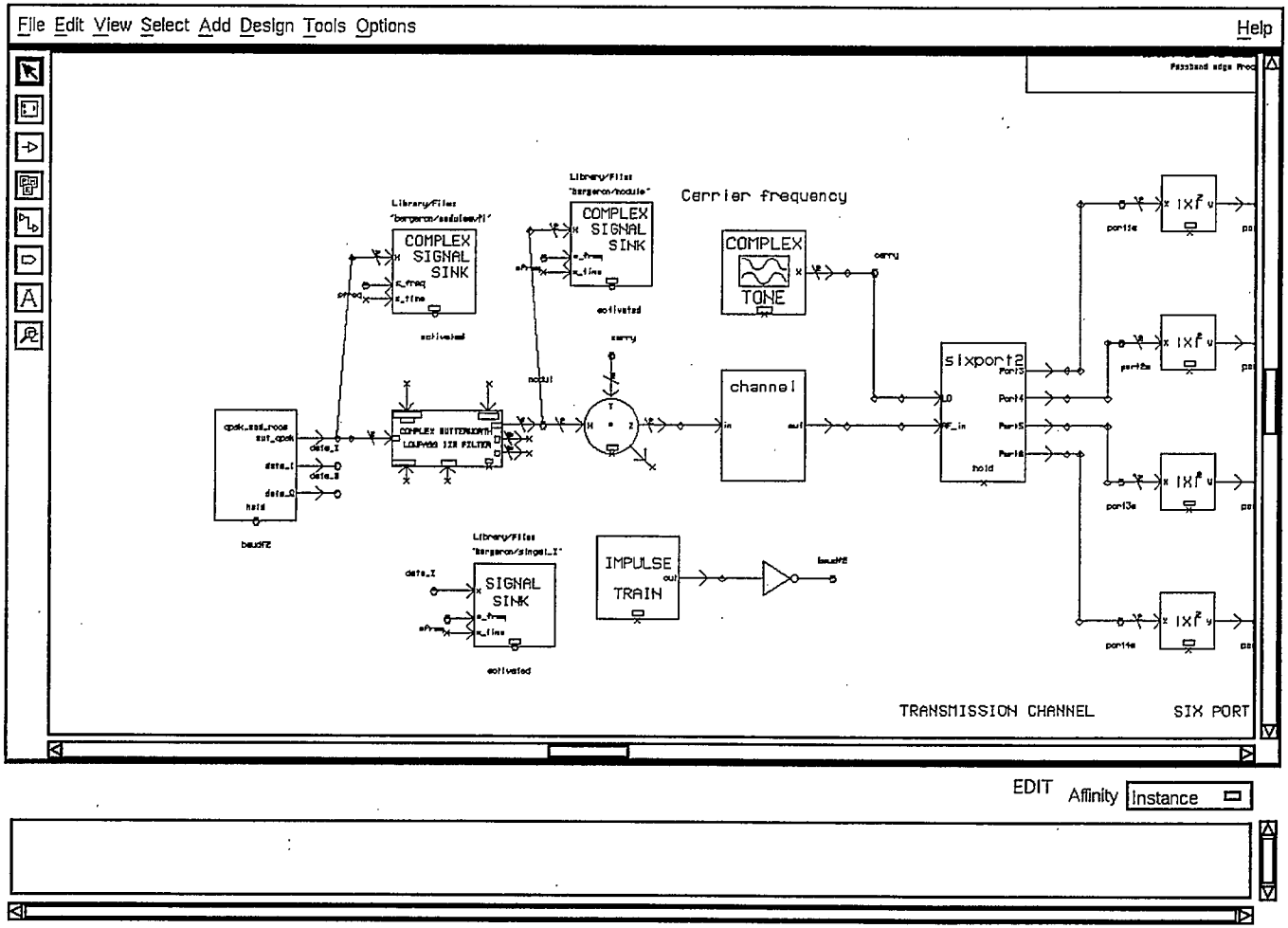

File Edit View Select Design Tools Options
Help
SIMPLE
COUNTER
count
reset
hold
count
X
Y
x
y
=REAL
z
hold
hold
CONTEXT
Affinity
Instance

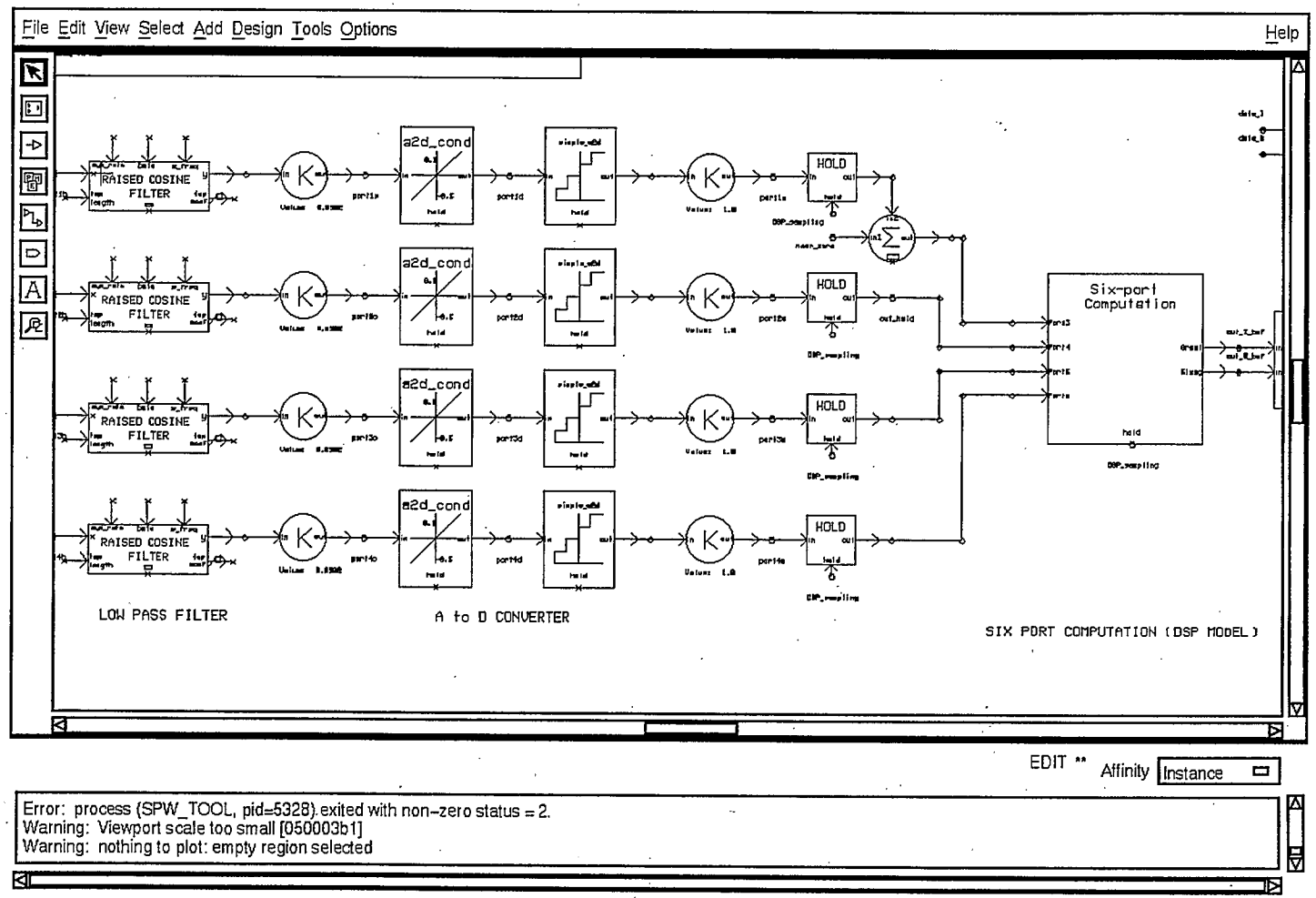
# Section A2

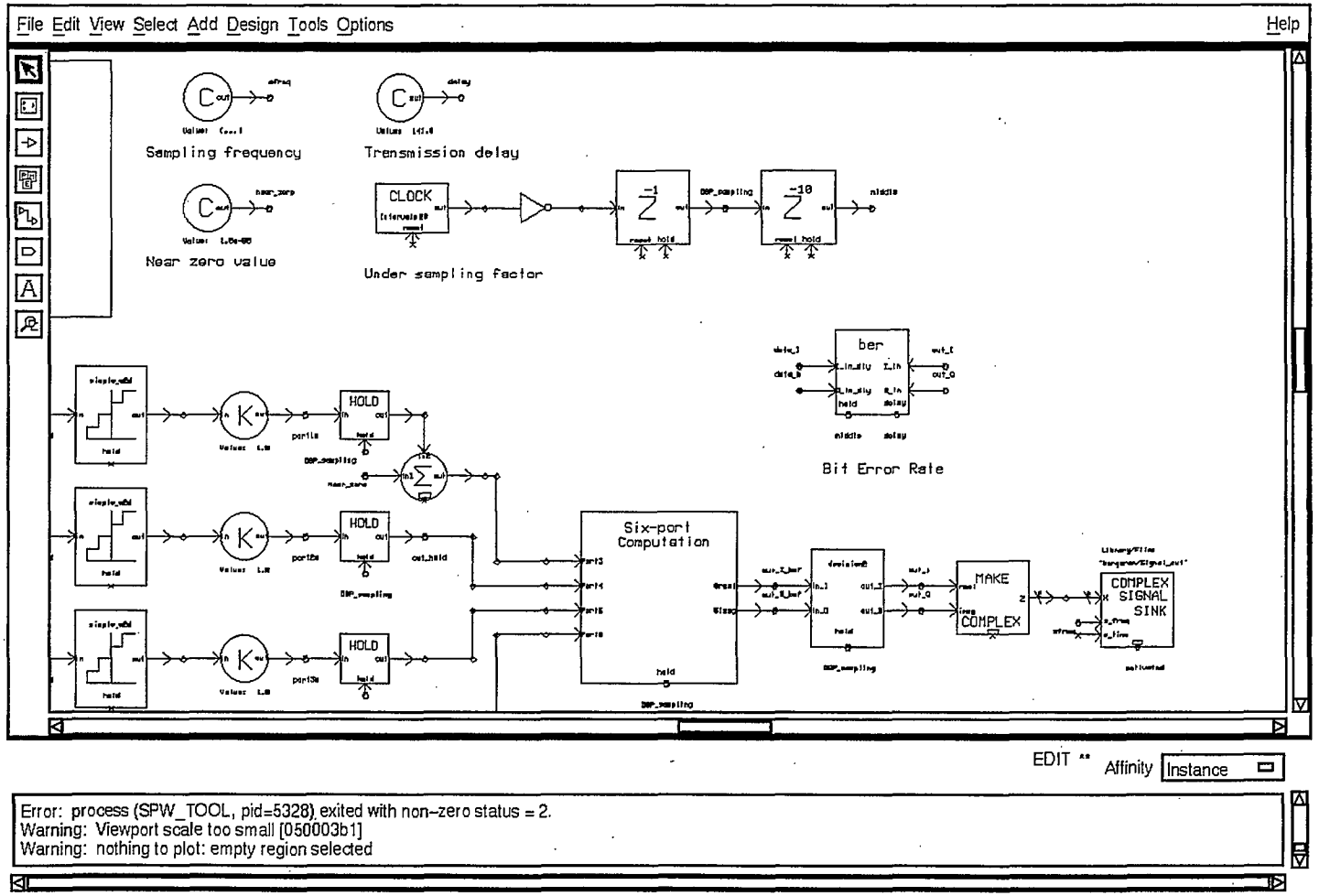
## Paramètres du démodulateur utilisant le six ports

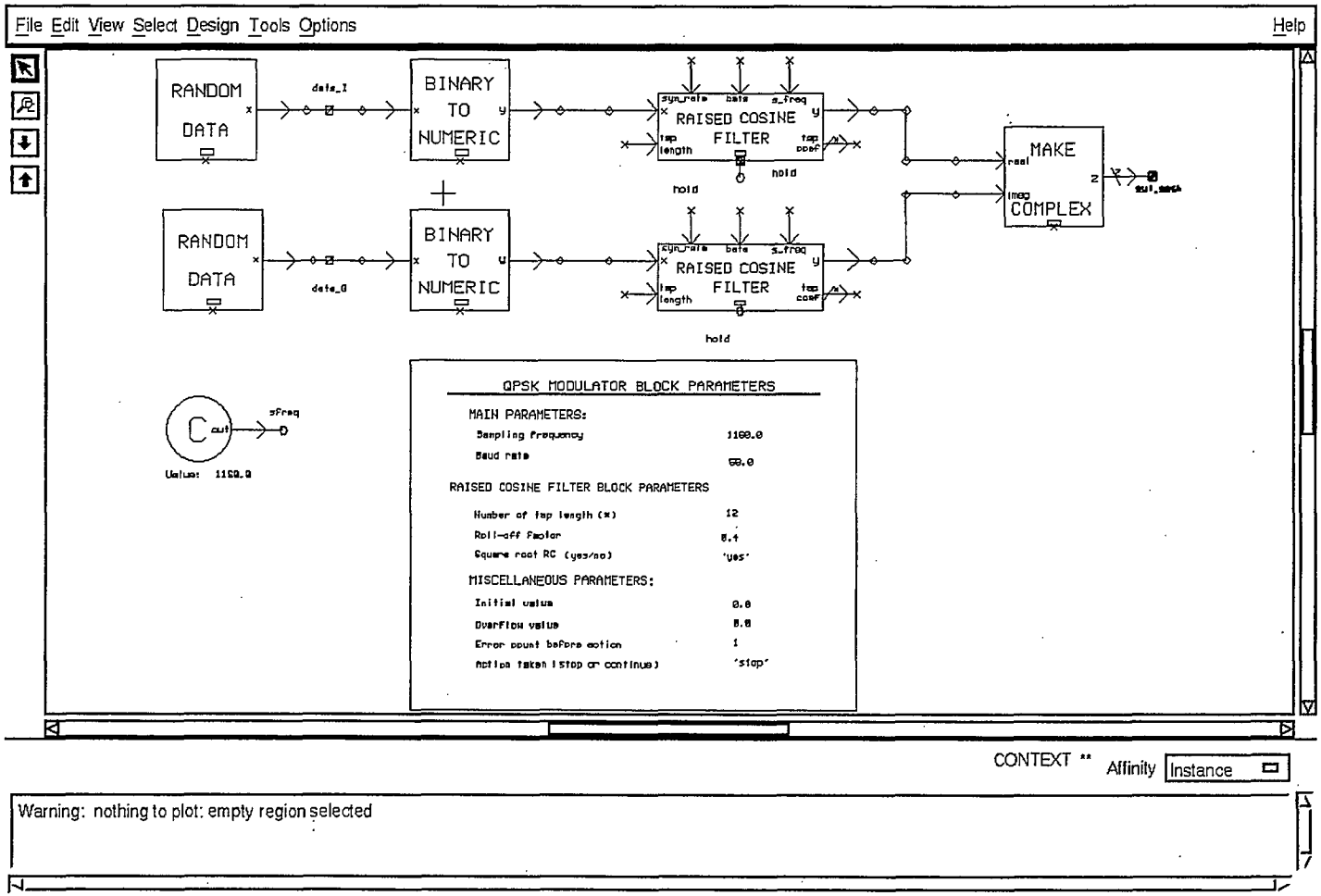

File Edit View Select Add Design Tools Options
Help
SIX PORT MODEL PARAMETERS
Sampling Frequency
Transmission delay
Hear zero value
Under sampling factor
Bit Error Rate
Carrier Frequency
channel
TRANSMISSION CHANNEL
SIX PORT
DIODE
Low Pass FILTER
A to D CONVERTER
Six-port Computation
SIX PORT COMPUTATION (DSP MODEL)
EDIT
Affinity
Instance

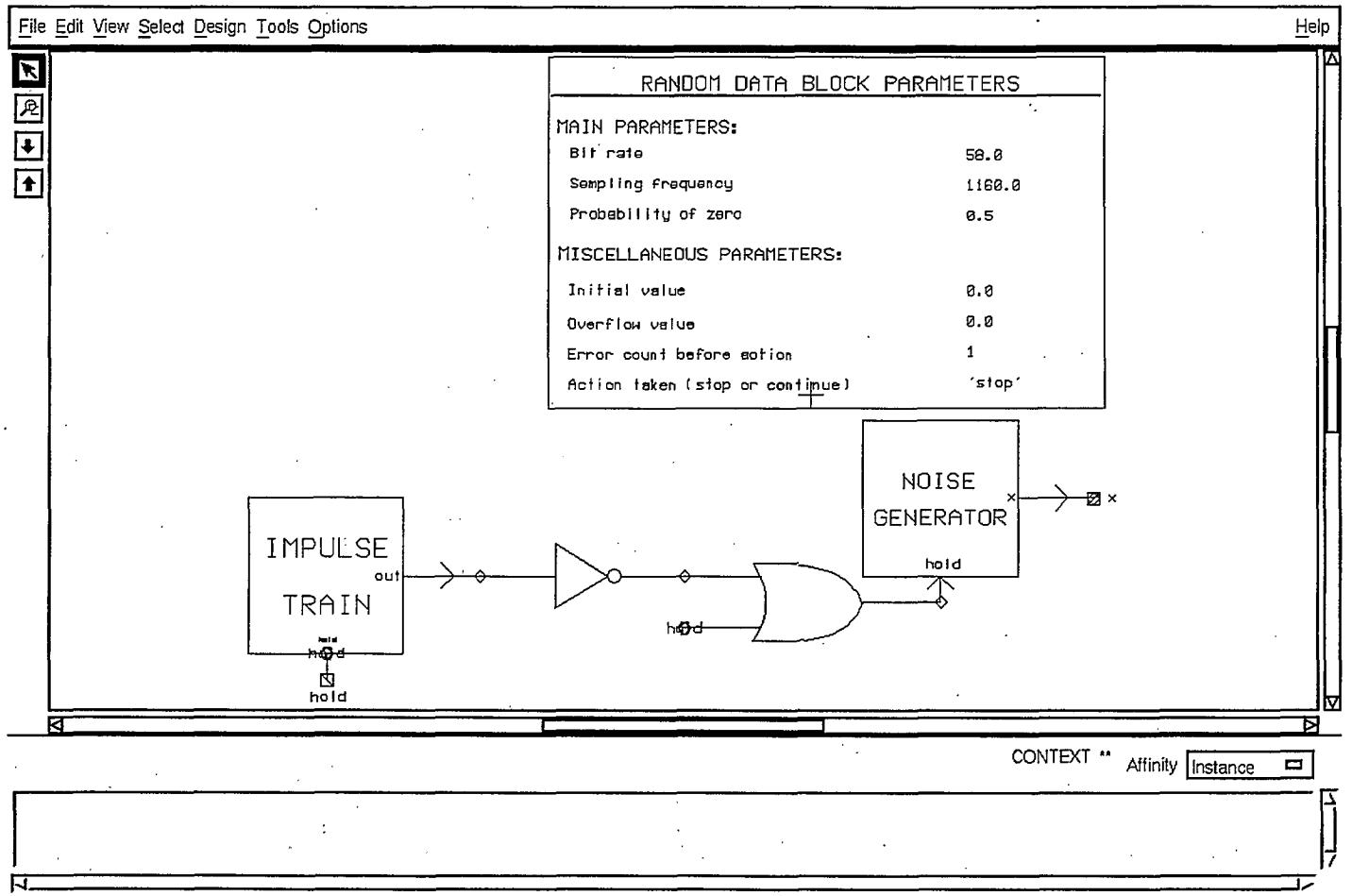

File Edit View Select Add Design Tools Options
Help
SIX PORT MODEL PARAMETERS
MAIN PARAMETERS:
Sampling frequency (MHz) 1160.0
Carrier frequency (MHz) 180.0
Baud rate 58.0
Lowpass filter edge (MHz) 58.0
Number of bits de resolution des A/D's 16
NOISE CHANNEL:
Signal to noise ratio (dB) 16.0
Symbol period (usec) (...)
Normalisation switch 1
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
FILTER PARAMETERS:
Number of tap 12
Attenuation at passband edge in dB power 3.0
Default values for unconnected inputs:
Passband edge frequency in MHz 60.0
clock delay
hold out delay -5
-141
Samp
Near
RAISED COSINE FILTER
a2d_cond
simple_a2d
hold
EDIT **
Affinity
Instance
Error: process (SPW_TOOL, pid=5328):exited with non-zero status = 2.
Warning: Viewport scale too small [050003b1]
Warning: nothing to plot: empty region selected

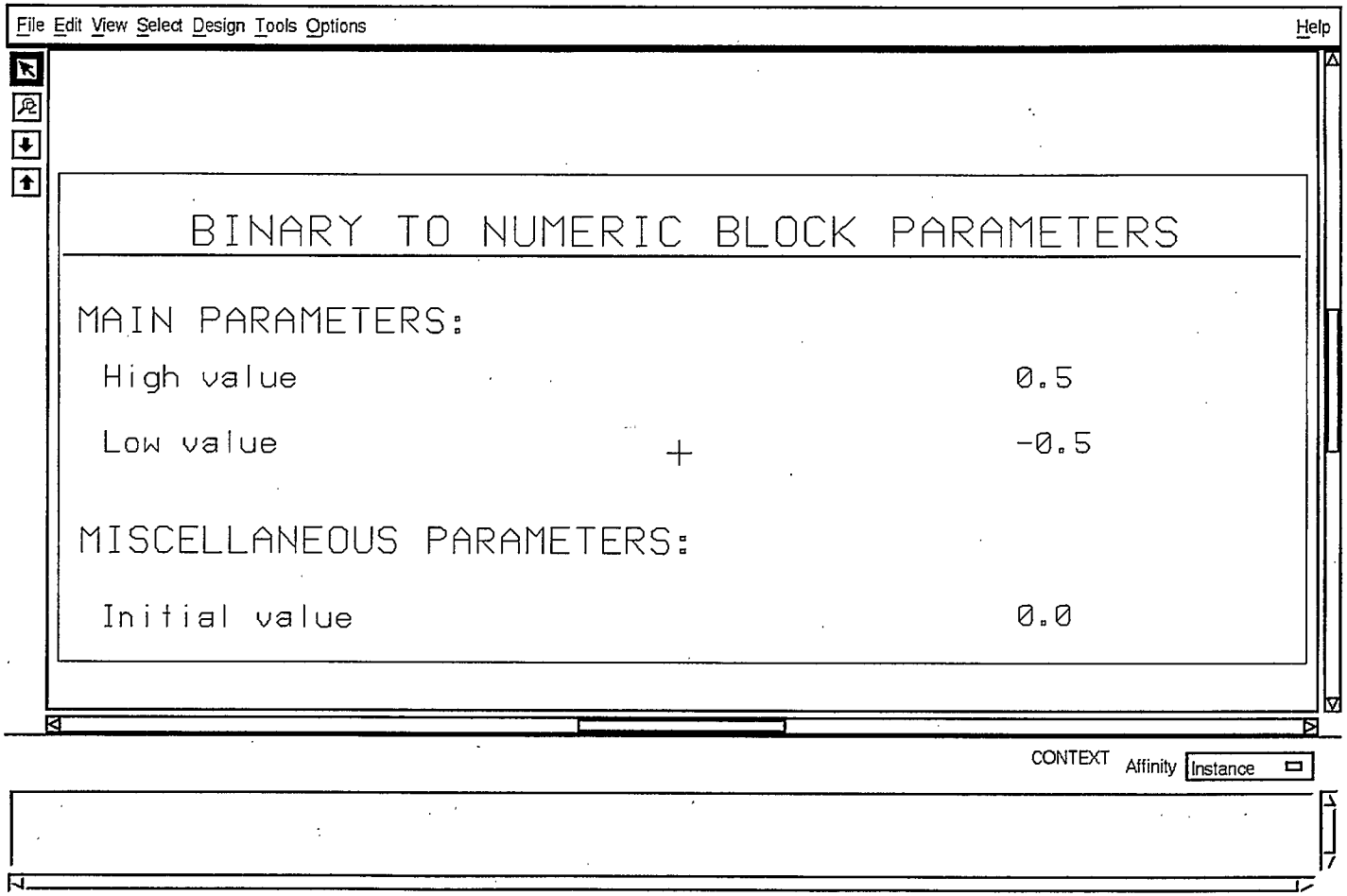

File Edit View Select Add Design Tools Options
Help
Carrier frequency
COMPLEX SIGNAL SINK
COMPLEX SIGNAL SINK
COMPLEX TONE
channel
sixport2
IMPULSE TRAIN
SIGNAL SINK
TRANSMISSION CHANNEL
SIX PORT
EDIT
Affinity
Instance

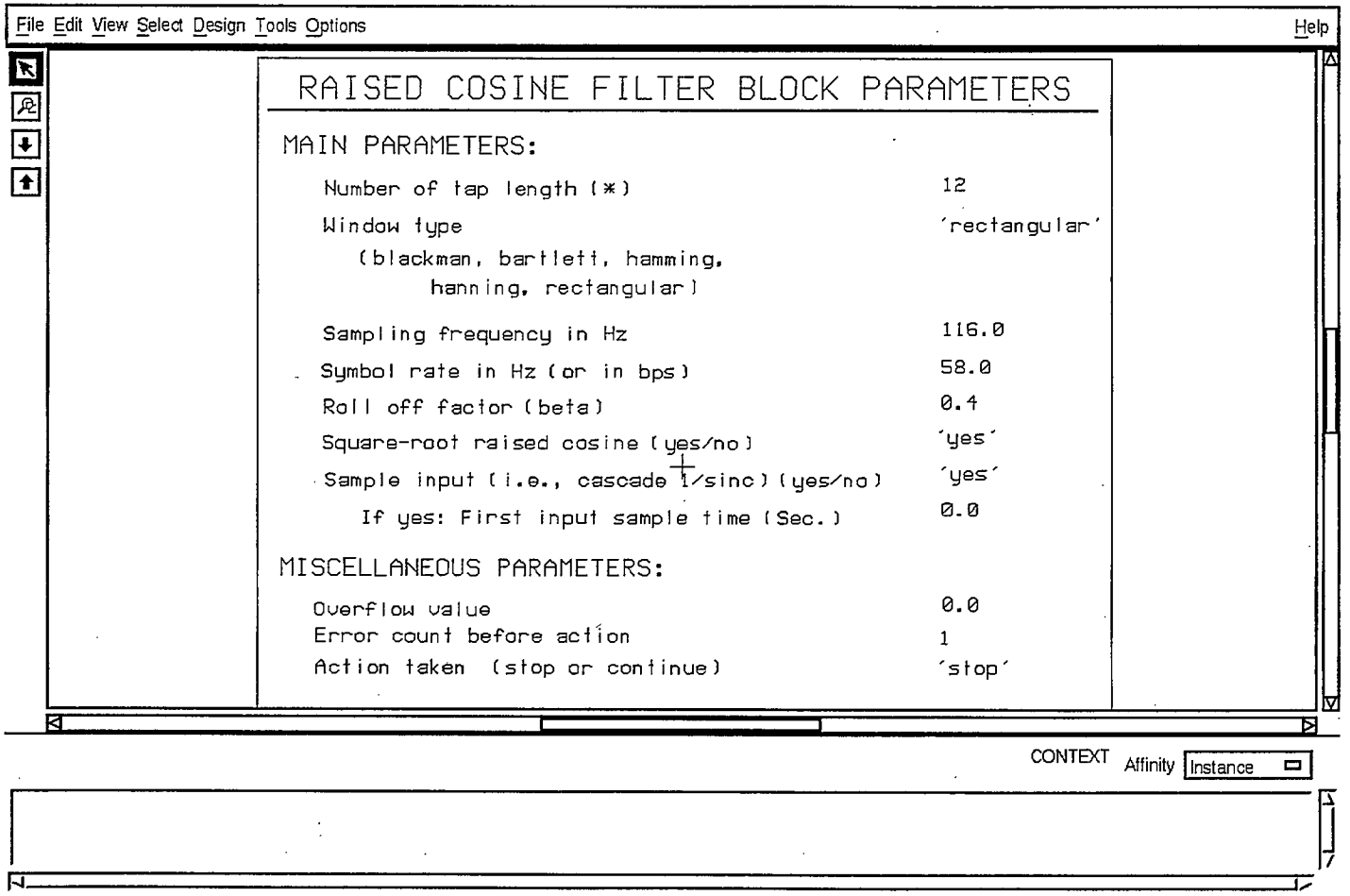

File Edit View Select Add Design Tools Options
Help
RAISED COSINE FILTER
a2d_cond
HOLD
Six-port Computation
LOW PASS FILTER
A to D CONVERTER
SIX PORT COMPUTATION (DSP MODEL)
EDIT **
Affinity
Instance
Error: process (SPW_TOOL, pid=5328) exited with non-zero status = 2.
Warning: Viewport scale too small [050003b1]
Warning: nothing to plot: empty region selected

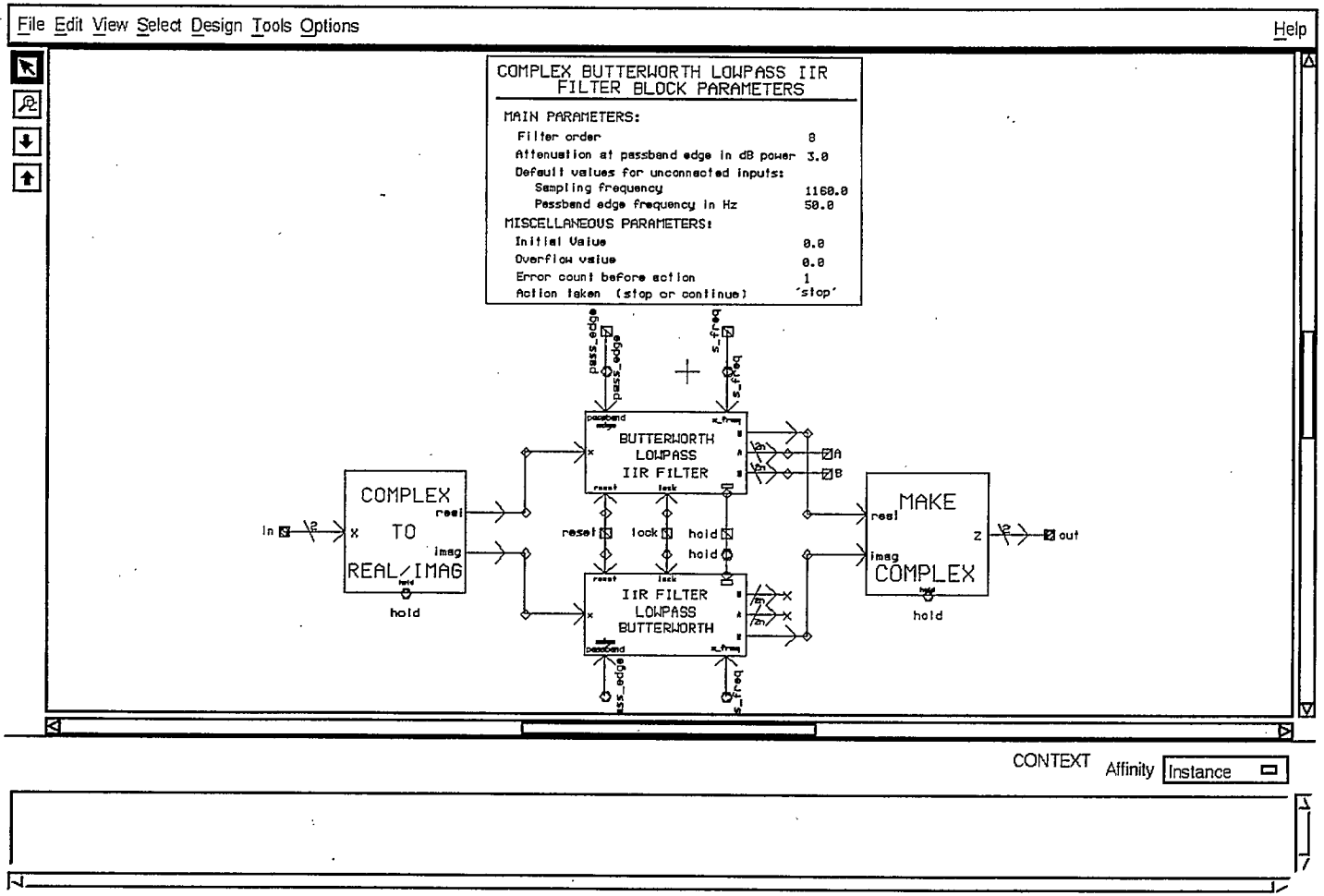

File Edit View Select Add Design Tools Options
Help
Sampling frequency
Transmission delay
Near zero value
CLOCK
Under sampling factor
ber
Bit Error Rate
HOLD
Six-port
Computation
MAKE
COMPLEX
COMPLEX
SIGNAL
SINK
EDIT
Affinity
Instance
Error: process (SPW_TOOL, pid=5328) exited with non-zero status = 2.
Warning: Viewport scale too small [050003b1]
Warning: nothing to plot: empty region selected

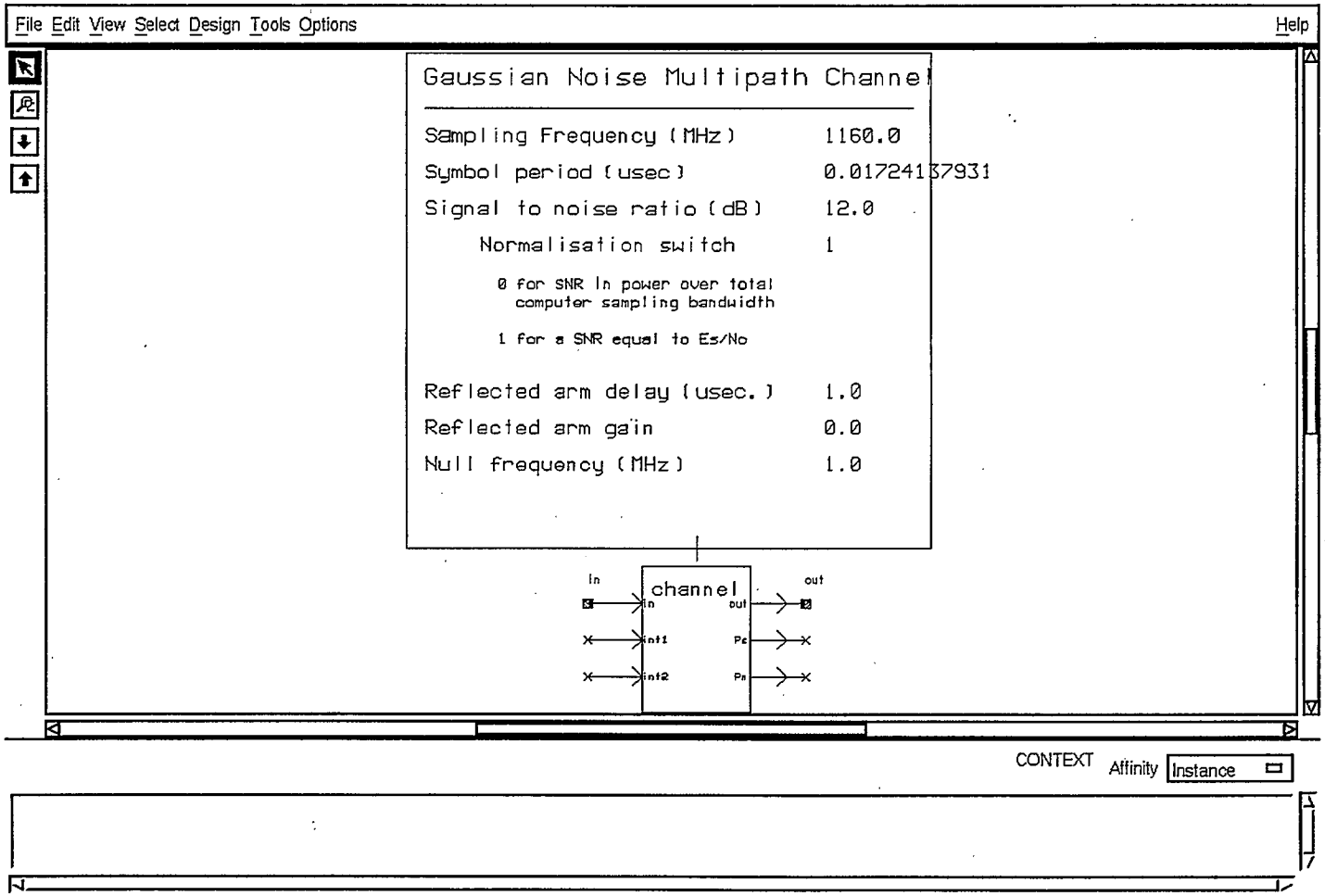

File Edit View Select Design Tools Options
Help
RANDOM DATA
data_I
BINARY TO NUMERIC
sym_rate
beta
s_freq
RAISED COSINE FILTER
tap length
tap coef
hold
MAKE COMPLEX
real
imag
RANDOM DATA
data_Q
BINARY TO NUMERIC
RAISED COSINE FILTER
sFreq
Value: 1160.0
QPSK MODULATOR BLOCK PARAMETERS
MAIN PARAMETERS:
Sampling frequency 1160.0
Baud rate 58.0
RAISED COSINE FILTER BLOCK PARAMETERS
Number of tap length (*) 12
Roll-off Factor 0.4
Square root RC (yes/no) 'yes'
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 8.0
Error count before action 1
Action taken (stop or continue) 'stop'
CONTEXT **
Affinity
Instance
Warning: nothing to plot: empty region selected

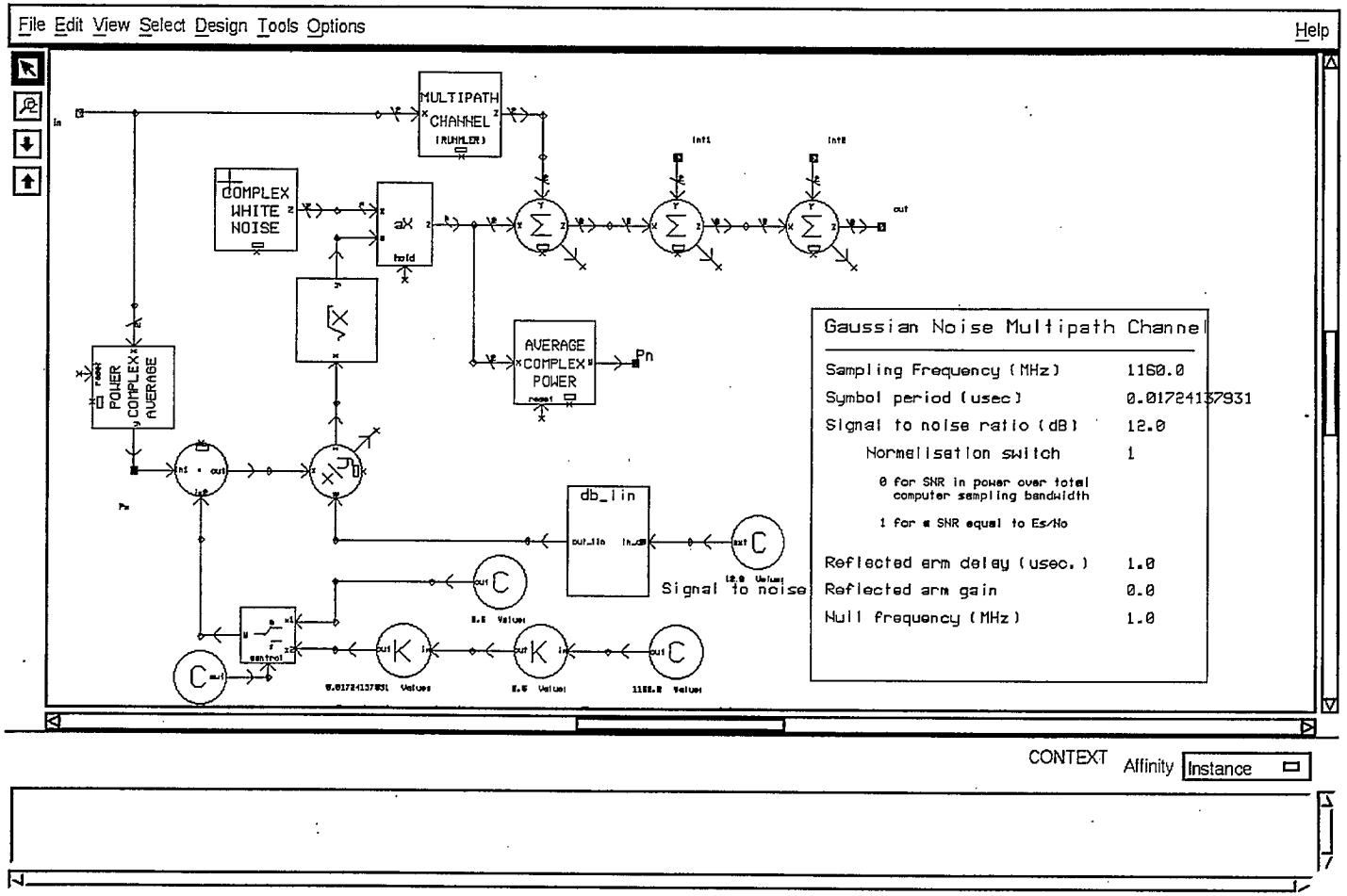

File Edit View Select Design Tools Options
Help
RANDOM DATA BLOCK PARAMETERS
MAIN PARAMETERS:
Bit rate
50.0
Sampling frequency
1160.0
Probability of zero
0.5
MISCELLANEOUS PARAMETERS:
Initial value
0.0
Overflow value
0.0
Error count before action
1
Action taken (stop or continue)
'stop'
NOISE
GENERATOR
hold
IMPULSE
TRAIN
out
hold
hold
CONTEXT **
Affinity
Instance

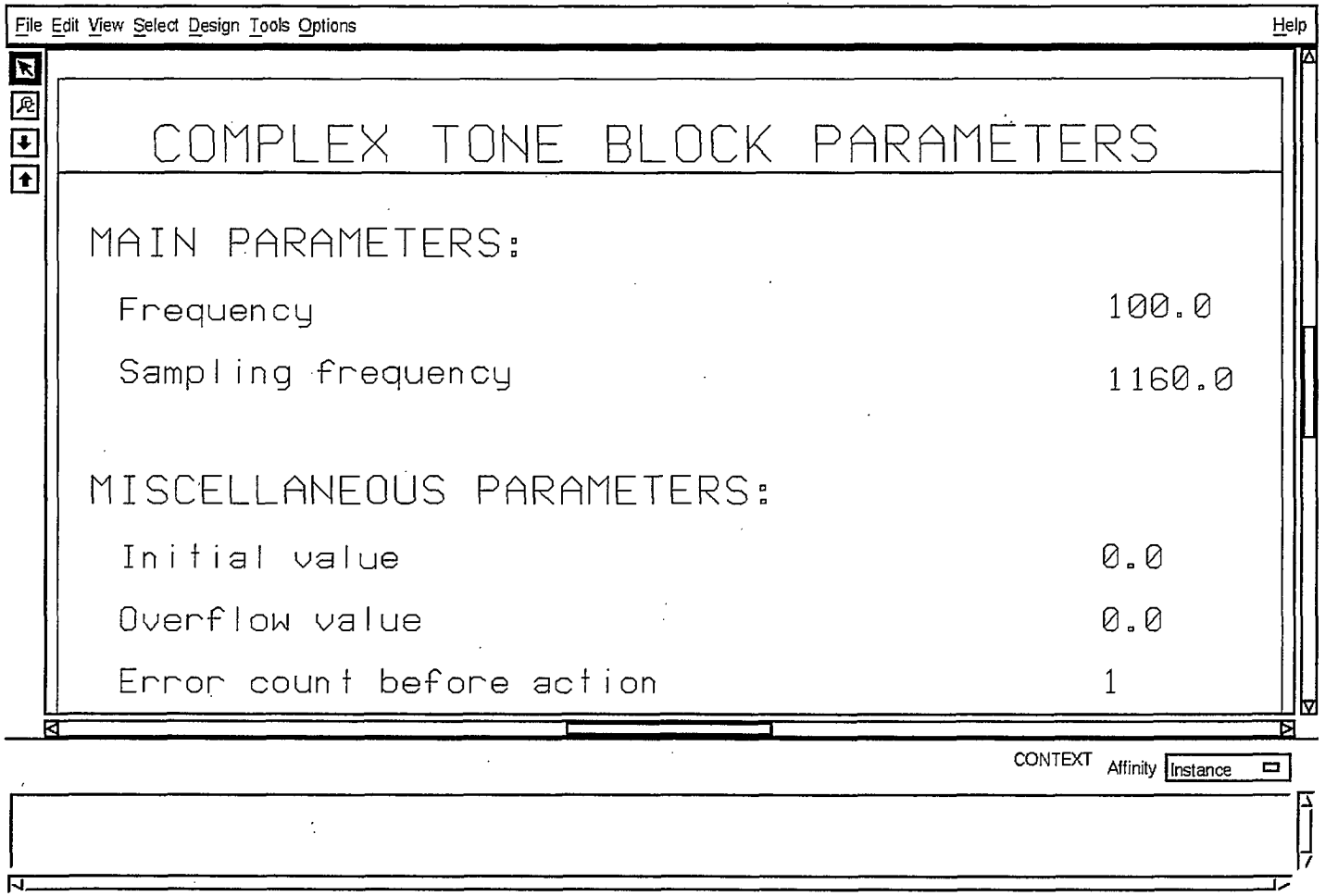

File Edit View Select Design Tools Options
Help
BINARY TO NUMERIC BLOCK PARAMETERS
MAIN PARAMETERS:
High value
0.5
Low value
-0.5
MISCELLANEOUS PARAMETERS:
Initial value
0.0
CONTEXT
Affinity
Instance

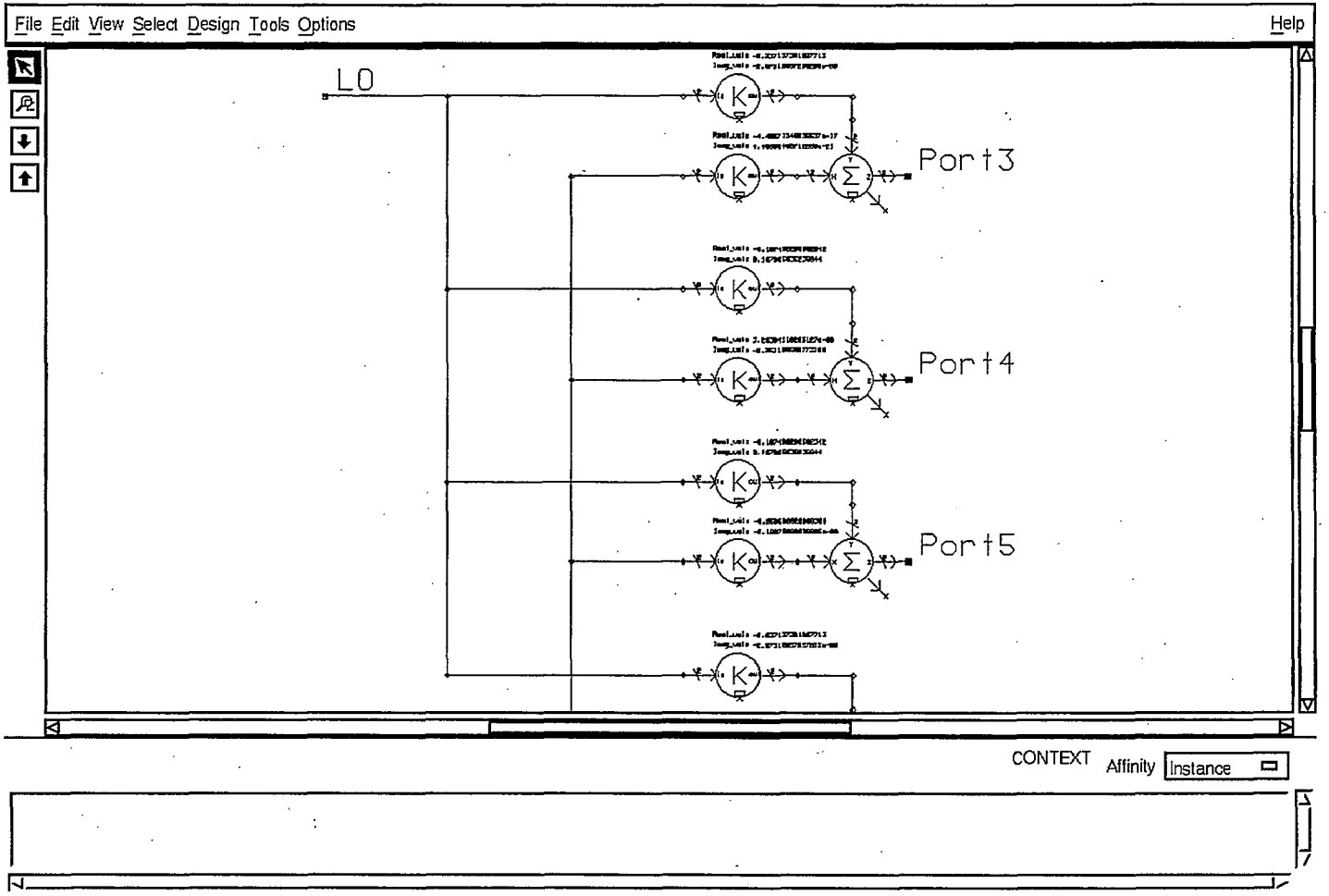

File Edit View Select Design Tools Options
Help
RAISED COSINE FILTER BLOCK PARAMETERS
MAIN PARAMETERS:
Number of tap length (*) 12
Window type 'rectangular'
(blackman, bartlett, hamming,
hanning, rectangular)
Sampling frequency in Hz 116.0
Symbol rate in Hz (or in bps) 58.0
Roll off factor (beta) 0.4
Square-root raised cosine (yes/no) 'yes'
Sample input (i.e., cascade 1/sinc) (yes/no) 'yes'
If yes: First input sample time (Sec.) 0.0
MISCELLANEOUS PARAMETERS:
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
CONTEXT
Affinity
Instance

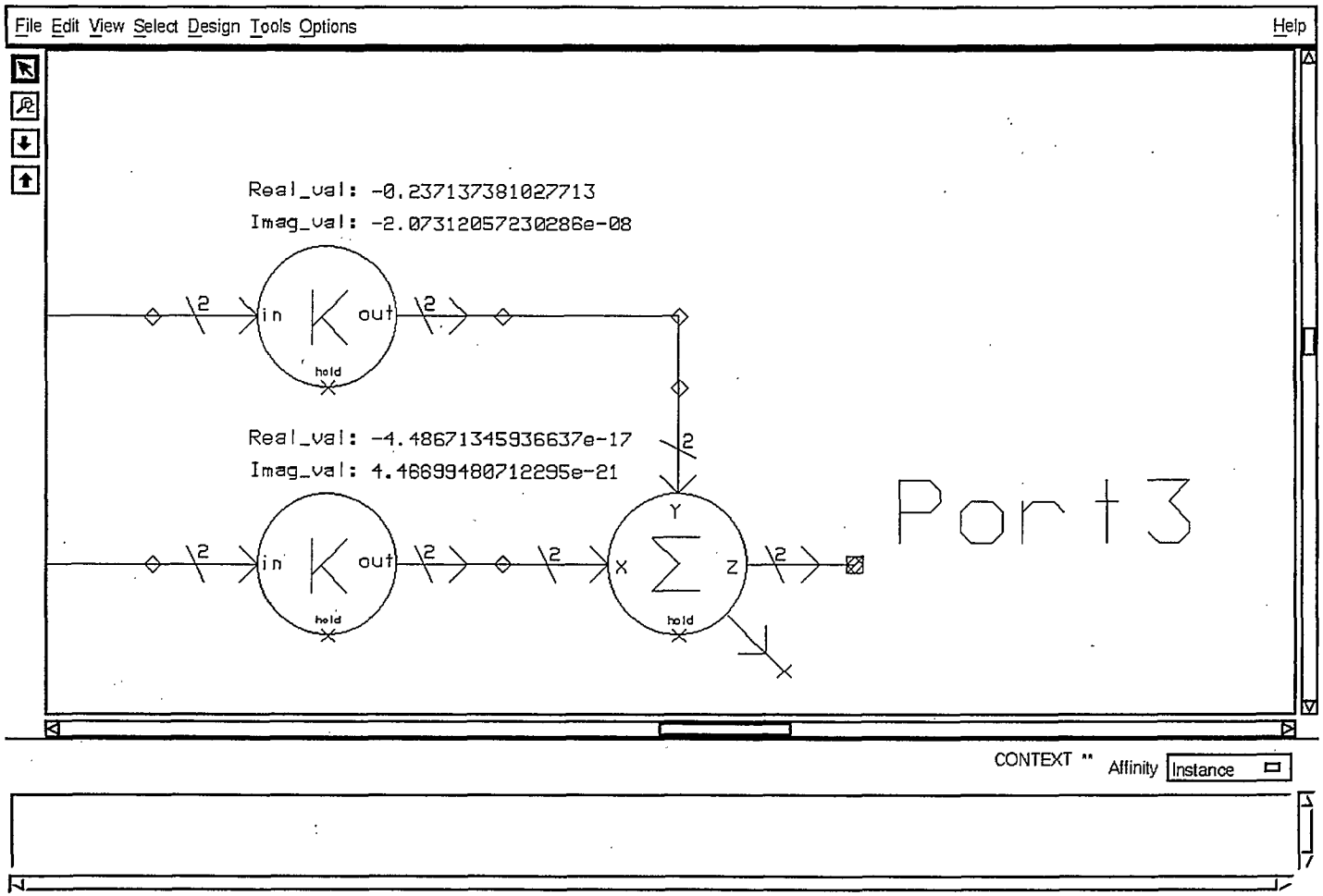

File Edit View Select Design Tools Options
Help
COMPLEX BUTTERWORTH LOWPASS IIR FILTER BLOCK PARAMETERS
MAIN PARAMETERS:
Filter order 8
Attenuation at passband edge in dB power 3.0
Default values for unconnected inputs:
Sampling frequency 1160.0
Passband edge frequency in Hz 50.0
MISCELLANEOUS PARAMETERS:
Initial Value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
pass_edge
s_freq
BUTTERWORTH LOWPASS IIR FILTER
IIR FILTER LOWPASS BUTTERWORTH
COMPLEX TO REAL/IMAG
MAKE COMPLEX
in
out
reset
lock
hold
CONTEXT
Affinity
Instance

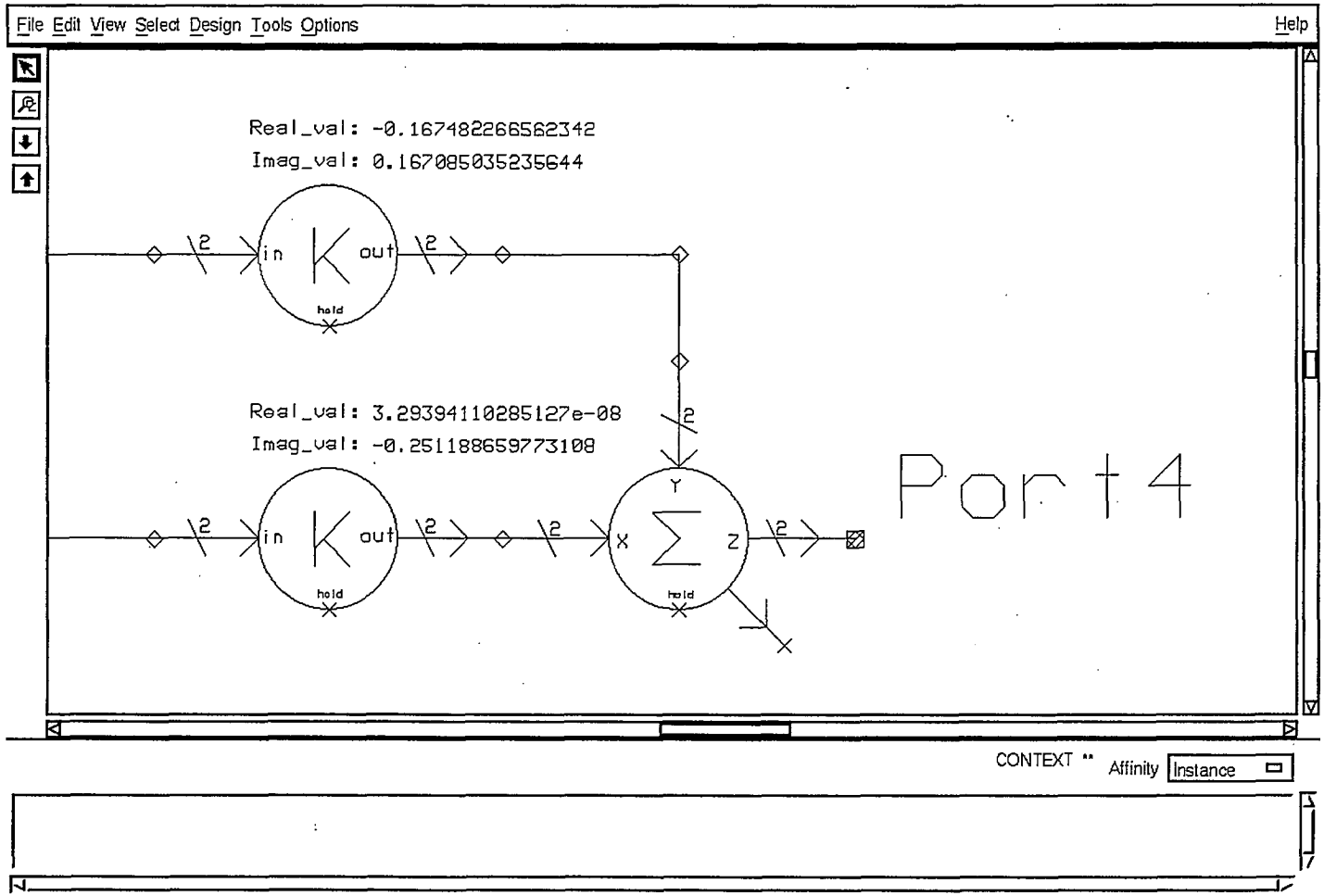

File Edit View Select Design Tools Options
Help
Gaussian Noise Multipath Channel
Sampling Frequency (MHz) 1160.0
Symbol period (usec) 0.017241379311
Signal to noise ratio (dB) 12.0
Normalisation switch 1
0 for SNR in power over total computer sampling bandwidth
1 for a SNR equal to Es/No
Reflected arm delay (usec.) 1.0
Reflected arm gain 0.0
Null frequency (MHz) 1.0
In
channel
out
in
out
int1
Pc
int2
Pa
CONTEXT
Affinity
Instance

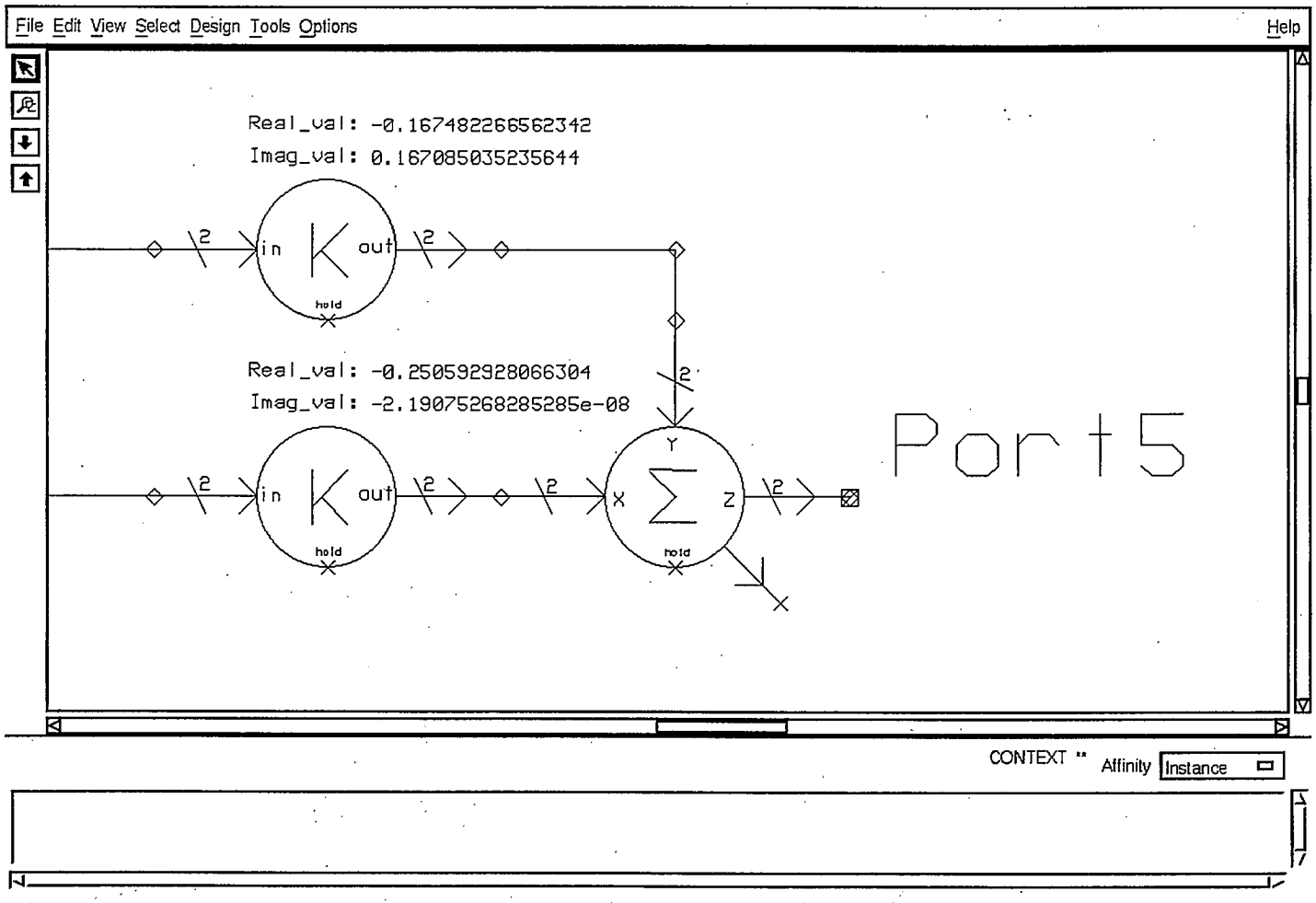

File Edit View Select Design Tools Options
Help
MULTIPATH CHANNEL
(RUMMLER)
COMPLEX WHITE NOISE
hold
AVERAGE COMPLEX POWER
Pn
POWER COMPLEX AVERAGE
db_lin
Signal to noise
Gaussian Noise Multipath Channel
Sampling Frequency (MHz) 1160.0
Symbol period (usec) 0.017241157931
Signal to noise ratio (dB) 12.0
Normalisation switch 1
0 for SNR in power over total computer sampling bandwidth
1 for e SNR equal to Es/No
Reflected arm delay (usec.) 1.0
Reflected arm gain 0.0
Null frequency (MHz) 1.0
CONTEXT
Affinity
Instance

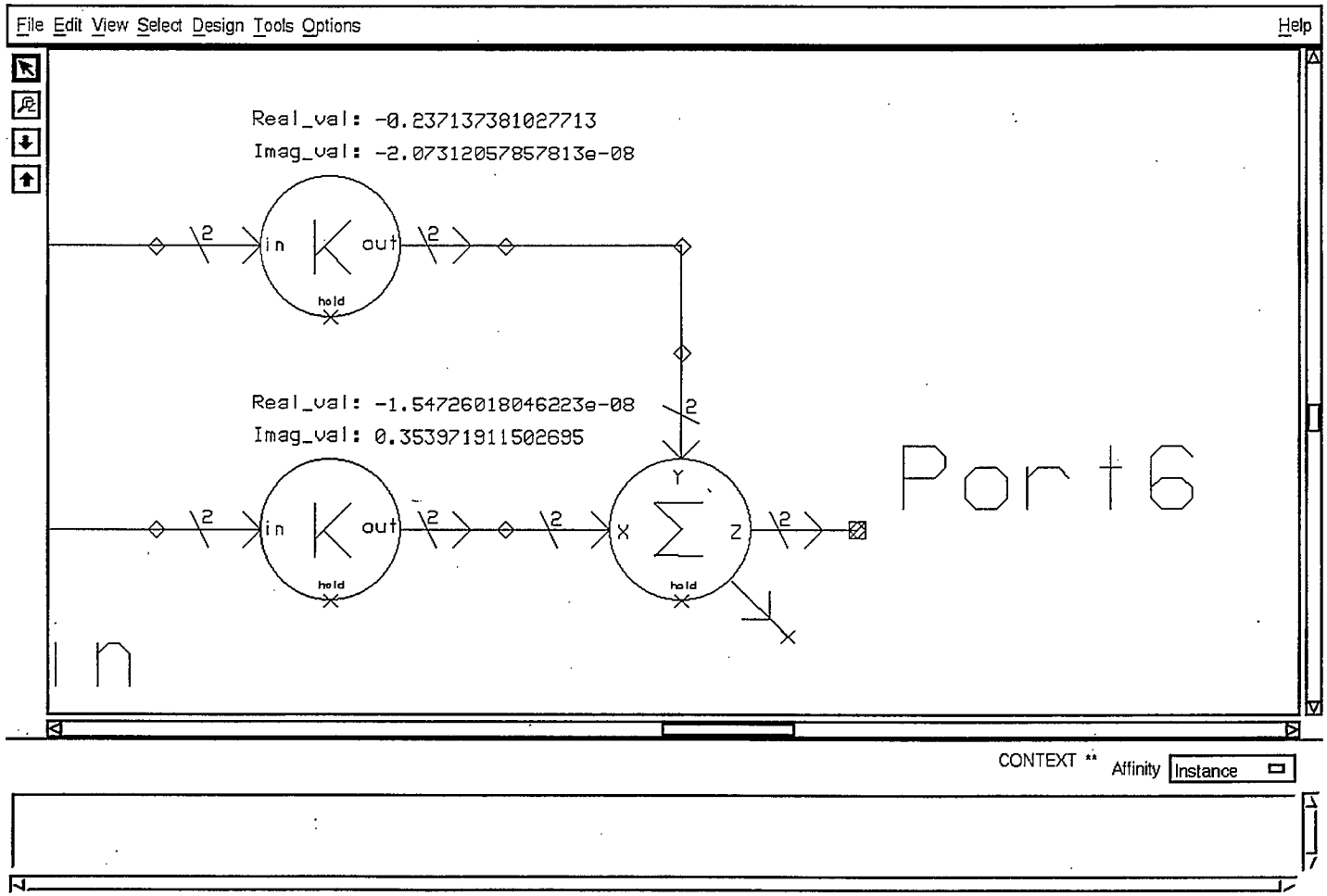

File Edit View Select Design Tools Options
Help
COMPLEX TONE BLOCK PARAMETERS
MAIN PARAMETERS:
Frequency
100.0
Sampling frequency
1160.0
MISCELLANEOUS PARAMETERS:
Initial value
0.0
Overflow value
0.0
Error count before action
1
CONTEXT
Affinity
Instance

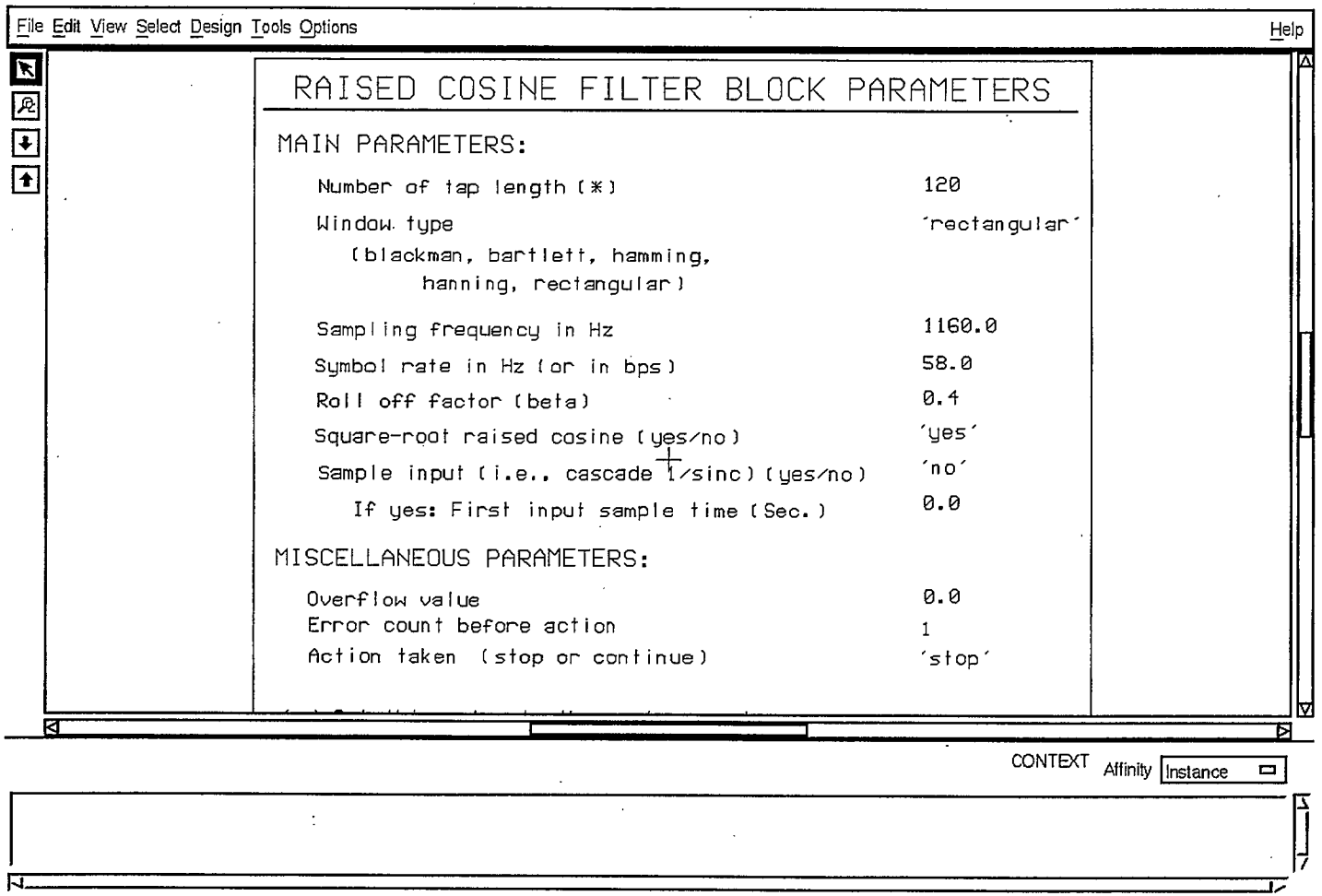

File Edit View Select Design Tools Options
Help
LO
Port3
Port4
Port5
CONTEXT
Affinity
Instance

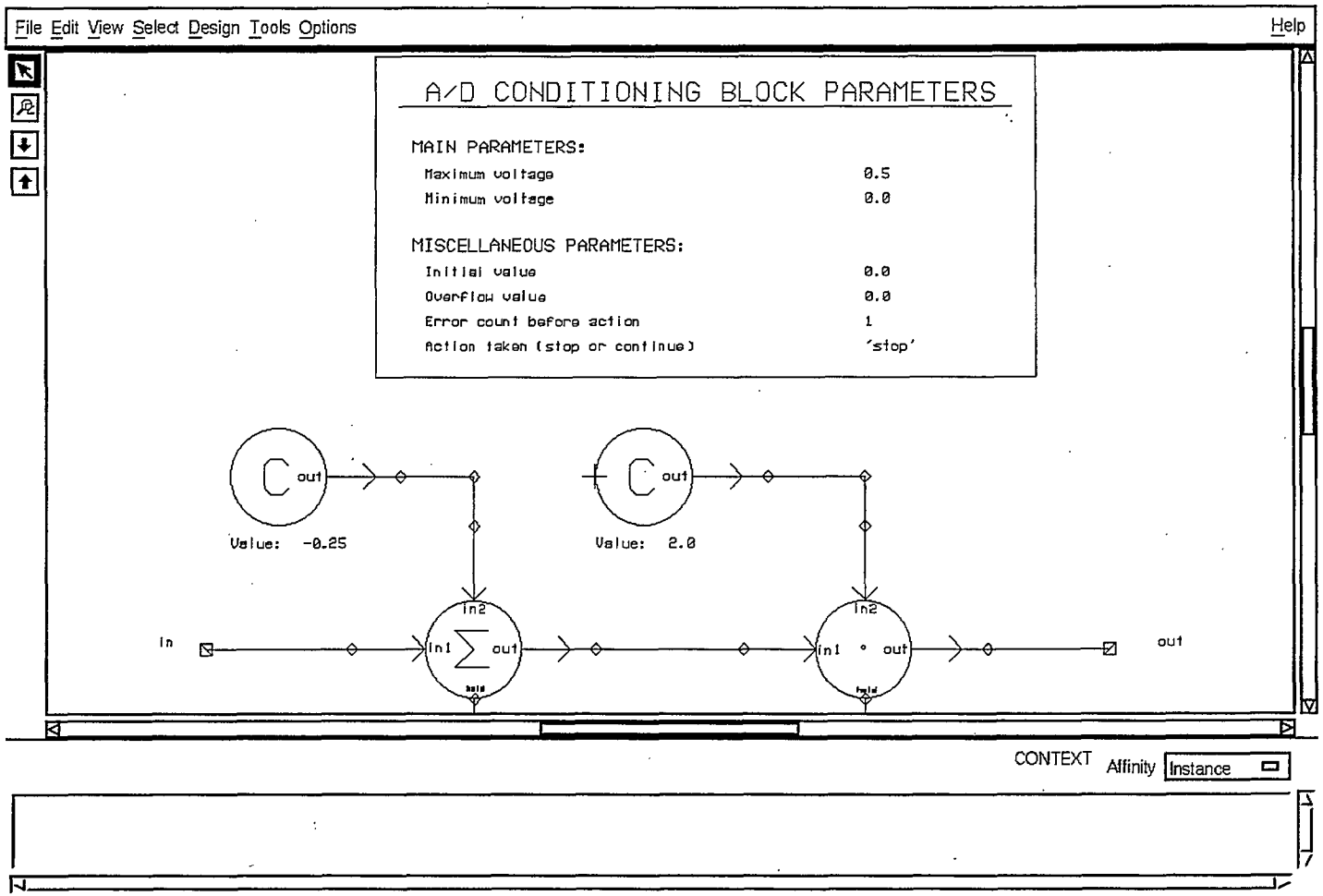

File Edit View Select Design Tools Options
Help
Real_val: -0.237137381027713
Imag_val: -2.07312057230288e-08
in
out
hold
Real_val: -4.48671345936637e-17
Imag_val: 4.46699480712295e-21
Port3
X
Y
Z
CONTEXT **
Affinity
Instance

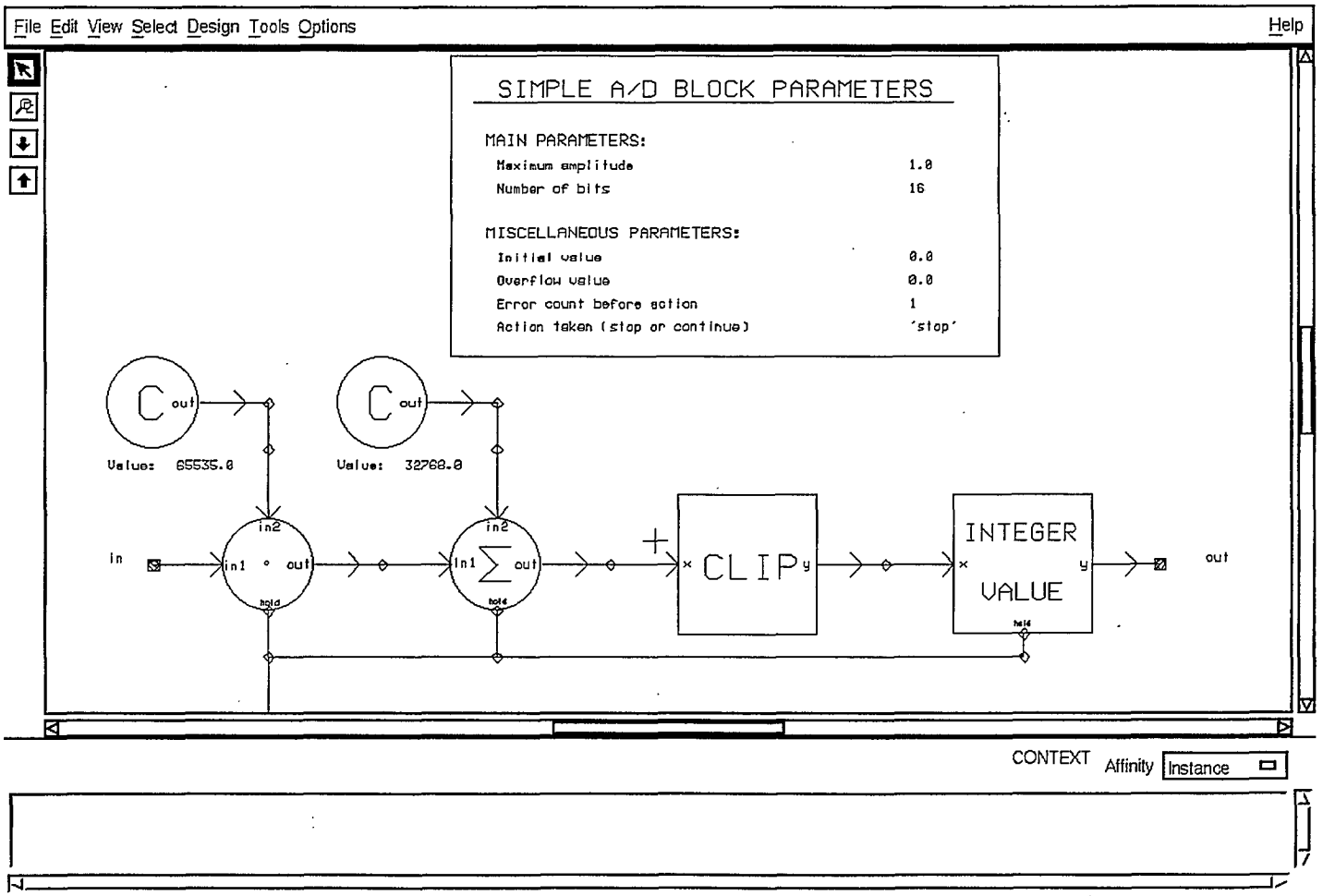

File Edit View Select Design Tools Options
Help
Real_val: -0.167482266562342
Imag_val: 0.167085035235644
in
out
hold
Real_val: 3.29394110285127e-08
Imag_val: -0.251188659773108
X
Y
Z
Port4
CONTEXT **
Affinity
Instance

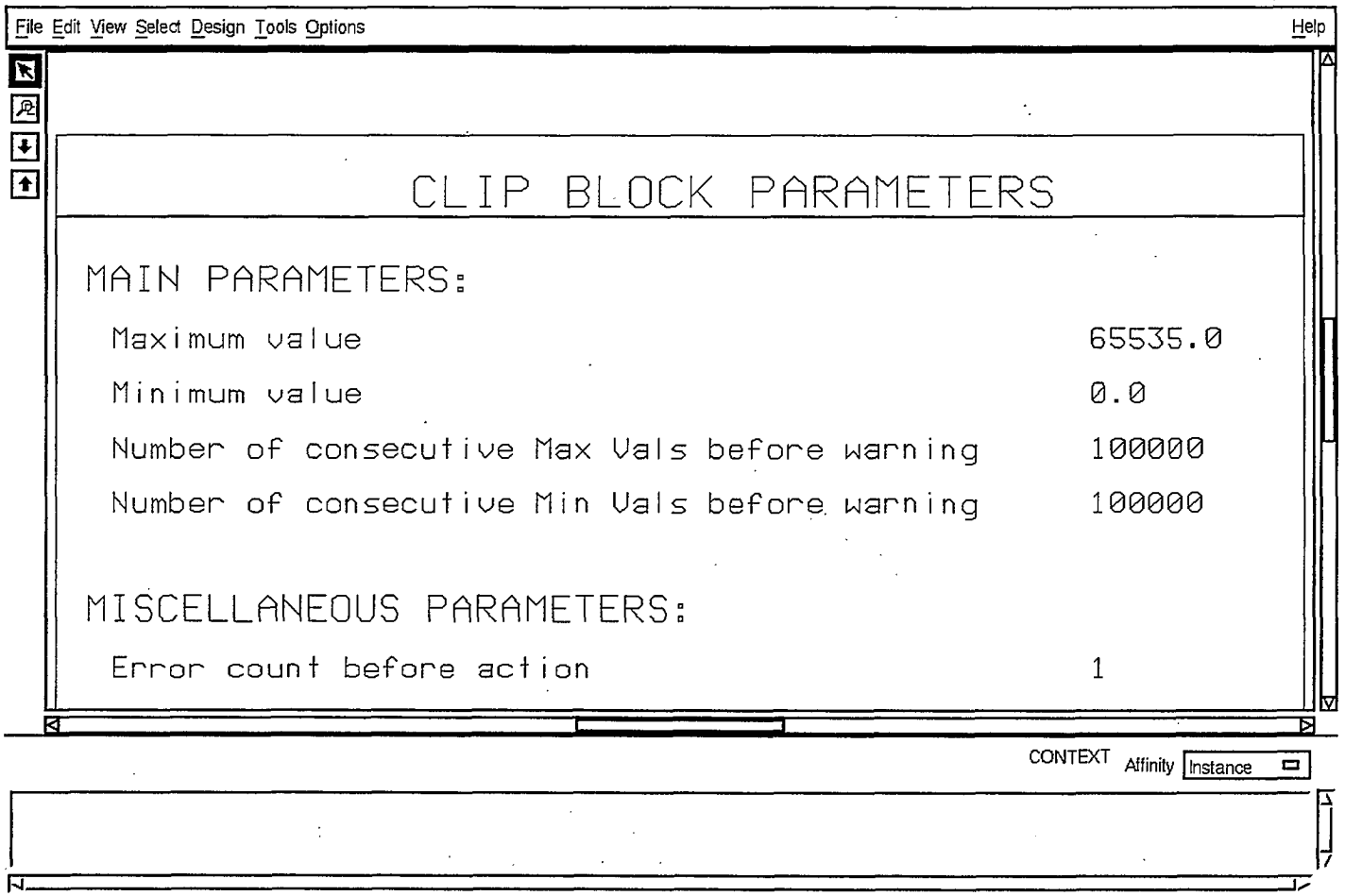

File Edit View Select Design Tools Options
Help
Real_val: -0.167482266562342
Imag_val: 0.167085035235644
2
in
out
2
hold
Real_val: -0.250592928066304
Imag_val: -2.19075268285285e-08
2
2
in
out
2
2
X
Y
Z
2
hold
Port5
CONTEXT **
Affinity
Instance

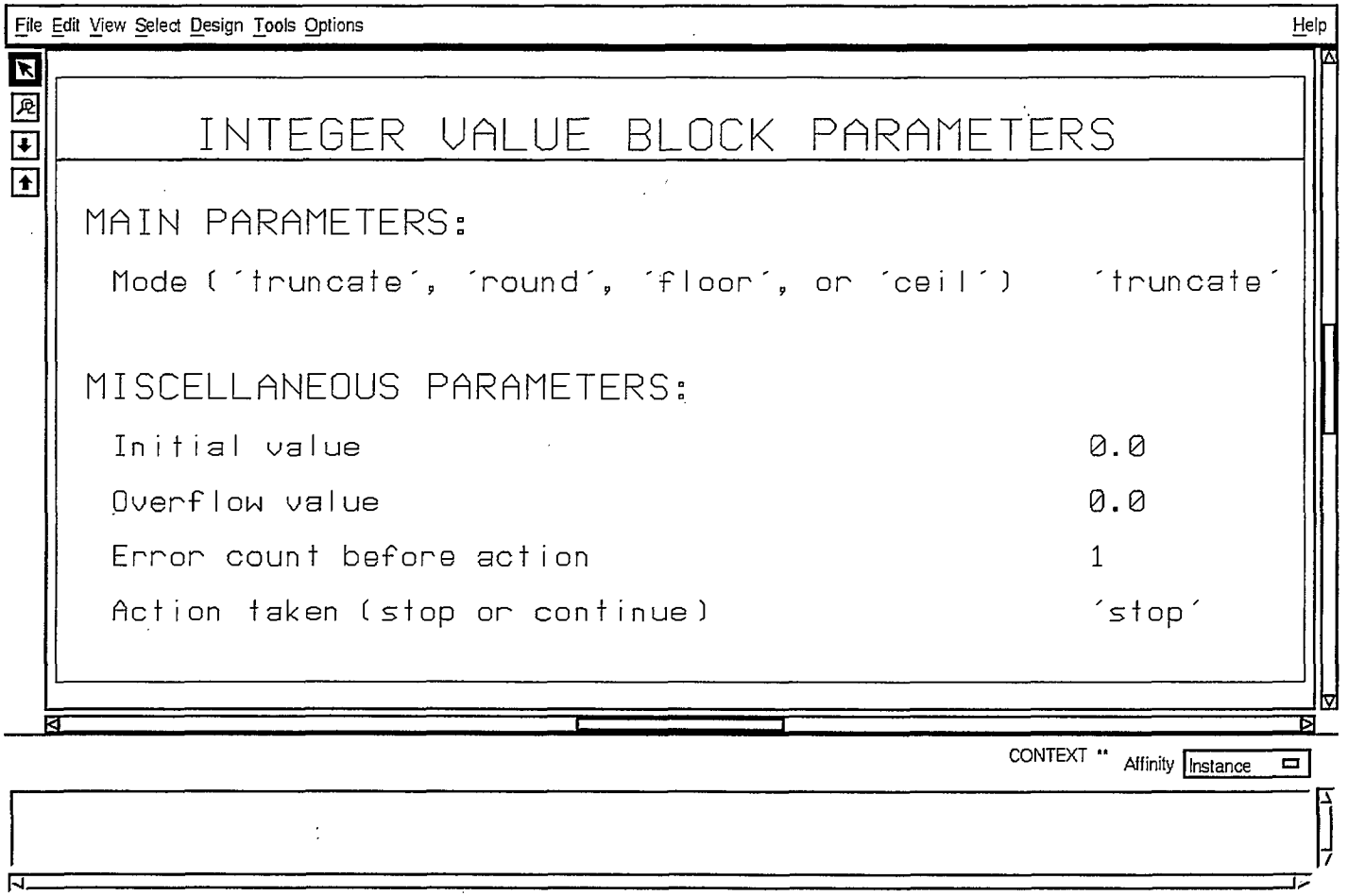

File Edit View Select Design Tools Options
Help
Real_val: -0.237137381027713
Imag_val: -2.07312057857813e-08
2
in
out
2
hold
Real_val: -1.54726018046223e-08
Imag_val: 0.353971911502695
2
2
in
out
2
2
X
Y
Z
2
hold
hold
Port6
In
CONTEXT **
Affinity
Instance

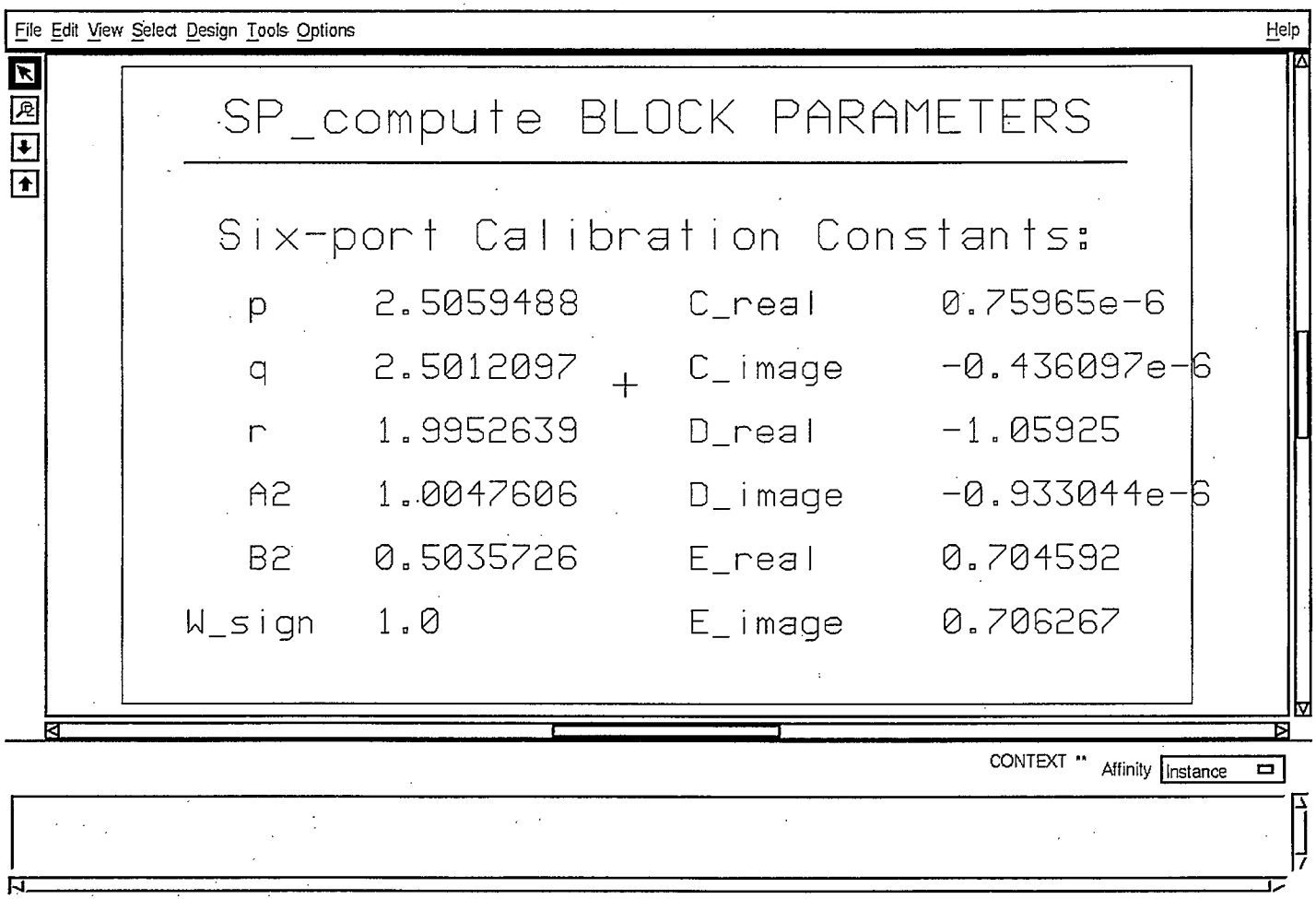

File Edit View Select Design Tools Options
Help
RAISED COSINE FILTER BLOCK PARAMETERS
MAIN PARAMETERS:
Number of tap length (*) 120
Window type 'rectangular'
(blackman, bartlett, hamming,
hanning, rectangular)
Sampling frequency in Hz 1160.0
Symbol rate in Hz (or in bps) 58.0
Roll off factor (beta) 0.4
Square-root raised cosine (yes/no) 'yes'
Sample input (i.e., cascade 1/sinc) (yes/no) 'no'
If yes: First input sample time (Sec.) 0.0
MISCELLANEOUS PARAMETERS:
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
CONTEXT
Affinity
Instance

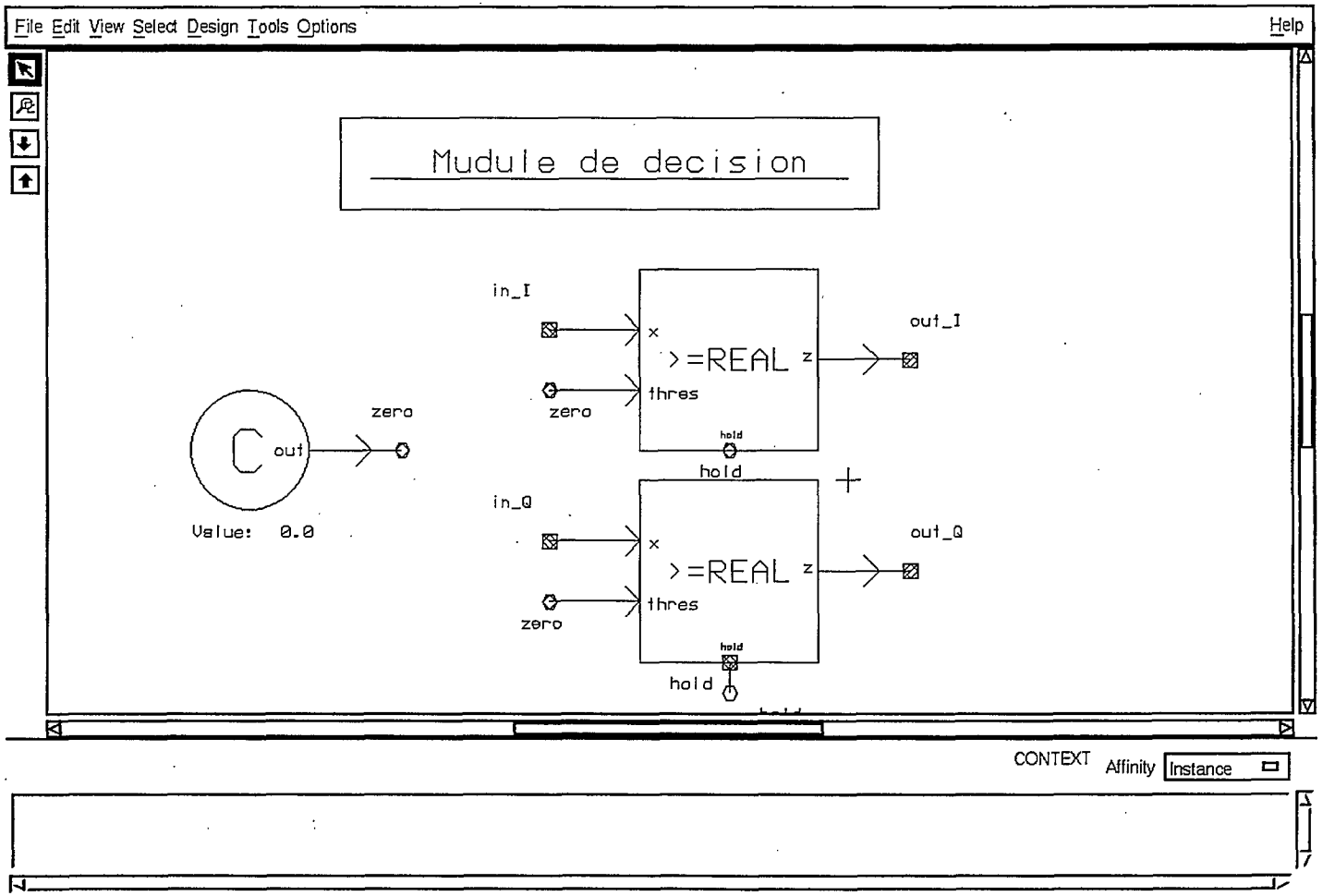

File Edit View Select Design Tools Options
Help
A/D CONDITIONING BLOCK PARAMETERS
MAIN PARAMETERS:
Maximum voltage 0.5
Minimum voltage 0.0
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
C out
Value: -0.25
C out
Value: 2.0
In
In2
In1
out
In2
In1
out
out
CONTEXT
Affinity
Instance

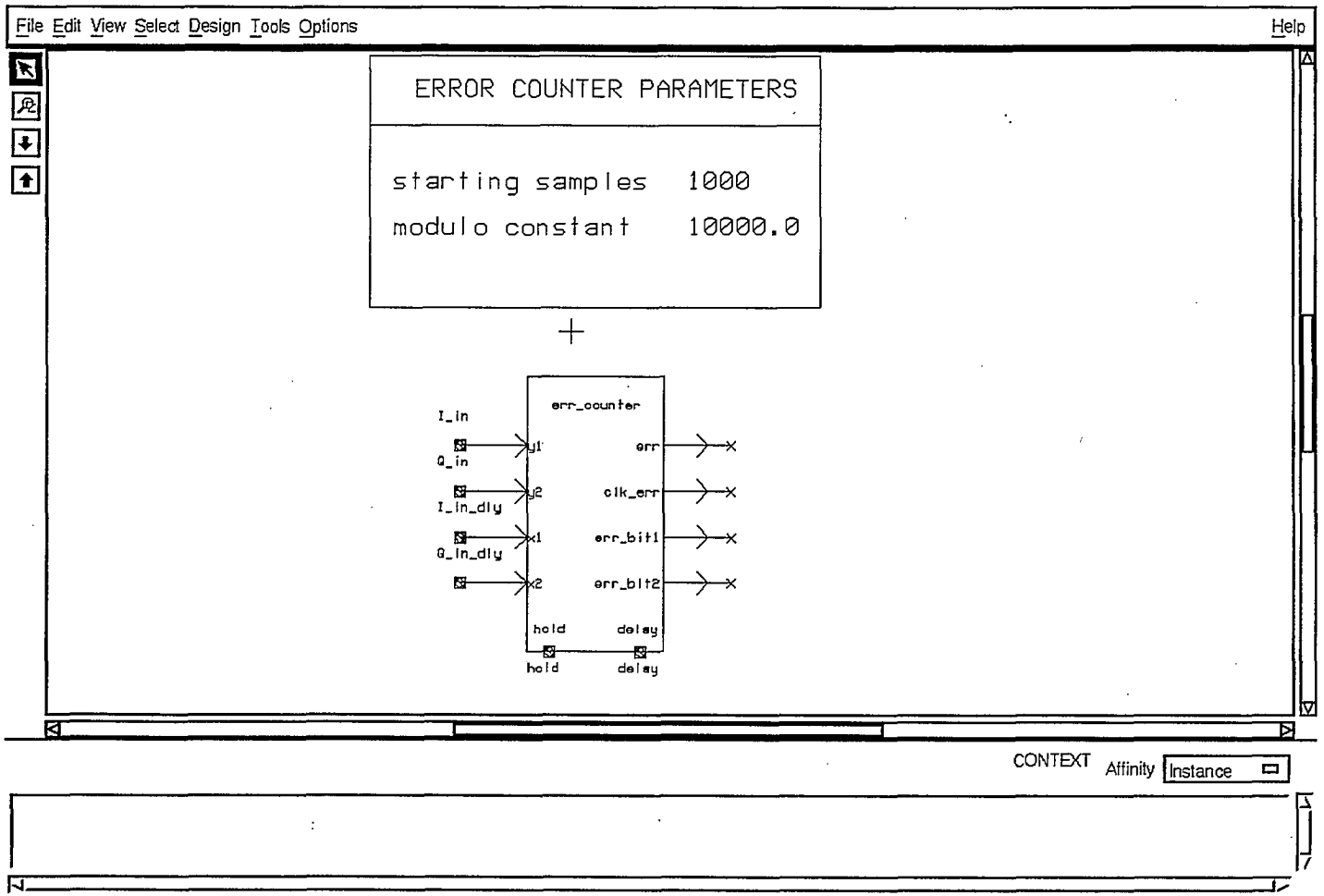

File Edit View Select Design Tools Options
Help
SIMPLE A/D BLOCK PARAMETERS
MAIN PARAMETERS:
Maximum amplitude 1.0
Number of bits 16
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
C out
Value: 65535.0
C out
Value: 32768.0
in
in2
in1
out
hold
CLIP
INTEGER
VALUE
out
CONTEXT
Affinity
Instance

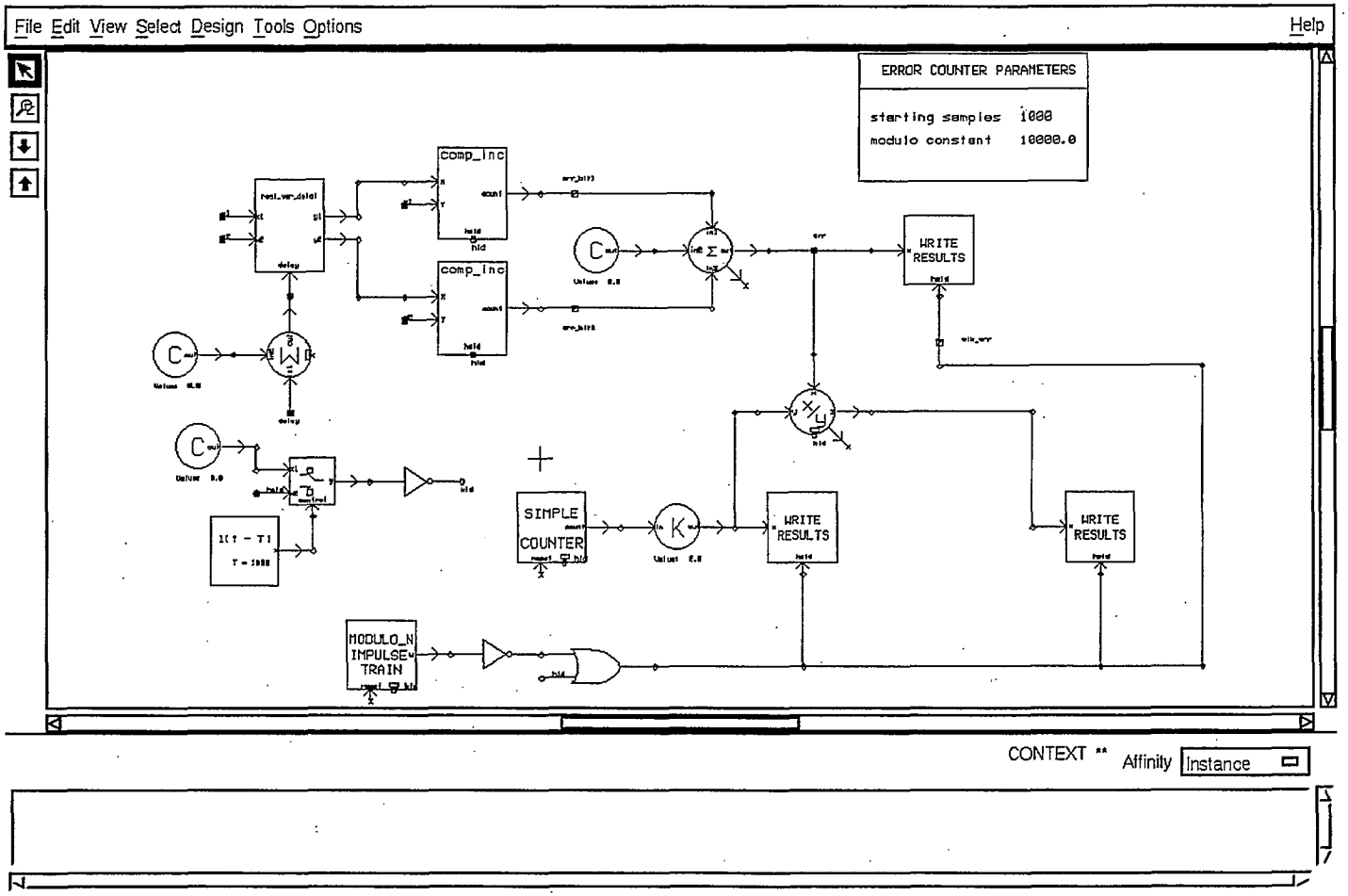

File Edit View Select Design Tools Options
Help
CLIP BLOCK PARAMETERS
MAIN PARAMETERS:
Maximum value 65535.0
Minimum value 0.0
Number of consecutive Max Vals before warning 100000
Number of consecutive Min Vals before warning 100000
MISCELLANEOUS PARAMETERS:
Error count before action 1
CONTEXT Affinity Instance

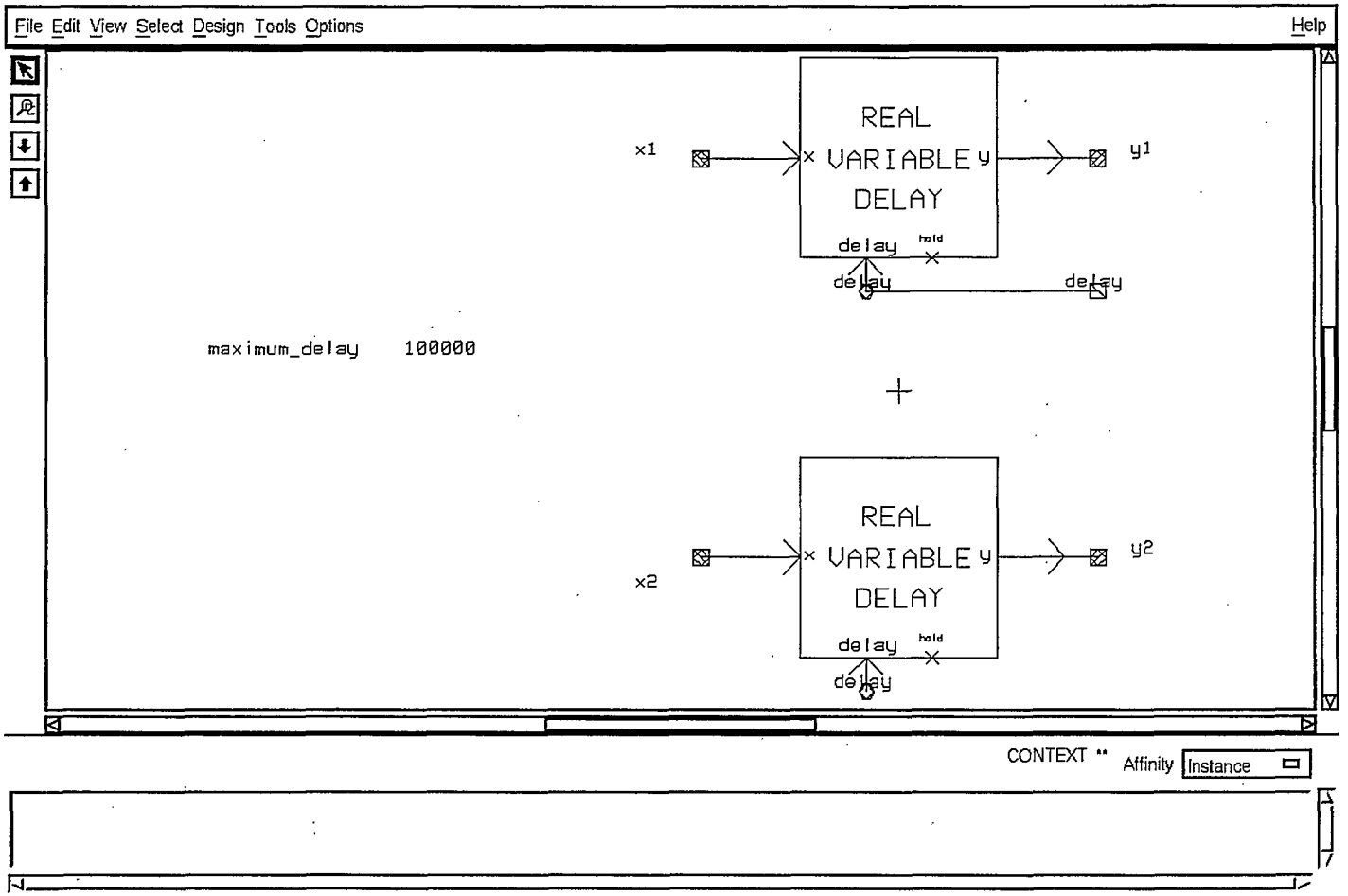

File Edit View Select Design Tools Options
Help
INTEGER VALUE BLOCK PARAMETERS
MAIN PARAMETERS:
Mode ('truncate', 'round', 'floor', or 'ceil') 'truncate'
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
CONTEXT ''
Affinity
Instance

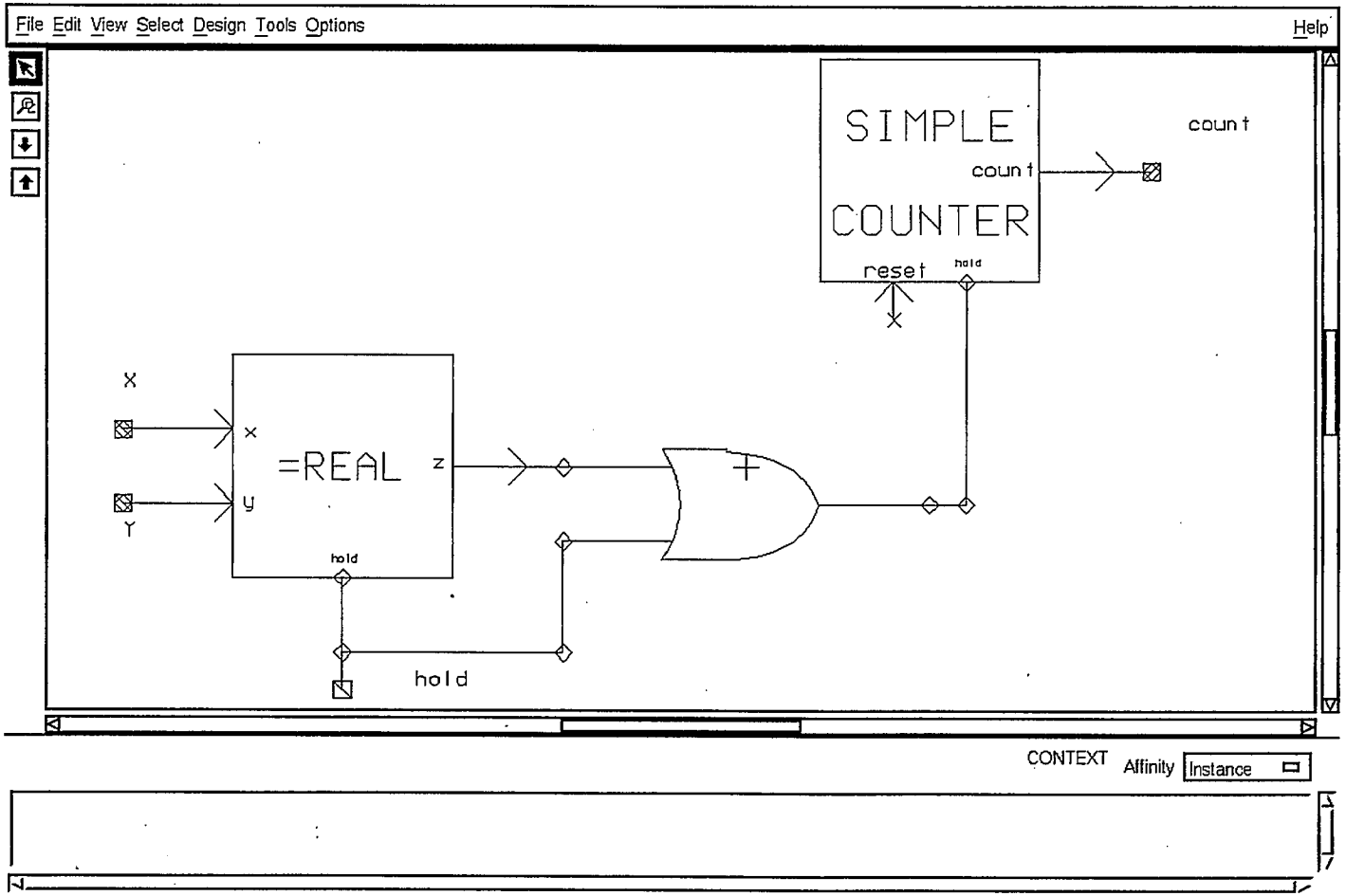

File Edit View Select Design Tools Options
Help
SP_compute BLOCK PARAMETERS
Six-port Calibration Constants:
p 2.5059488
q 2.5012097
r 1.9952639
A2 1.0047606
B2 0.5035726
W_sign 1.0
C_real 0.75965e-6
C_image -0.436097e-6
D_real -1.05925
D_image -0.933044e-6
E_real 0.704592
E_image 0.706267
CONTEXT **
Affinity
Instance


File Edit View Select Design Tools Options
Help
Mudule de decision
in_I
out_I
>=REAL
x
z
thres
zero
hold
out
zero
Value: 0.0
in_Q
out_Q
>=REAL
x
z
thres
zero
hold
hold
CONTEXT
Affinity
Instance


File Edit View Select Design Tools Options
Help
ERROR COUNTER PARAMETERS
starting samples 1000
modulo constant 10000.0
err_counter
I_in
Q_in
I_in_dly
Q_in_dly
y1
y2
x1
x2
err
clk_err
err_bit1
err_bit2
hold
delay
hold
delay
CONTEXT
Affinity
Instance

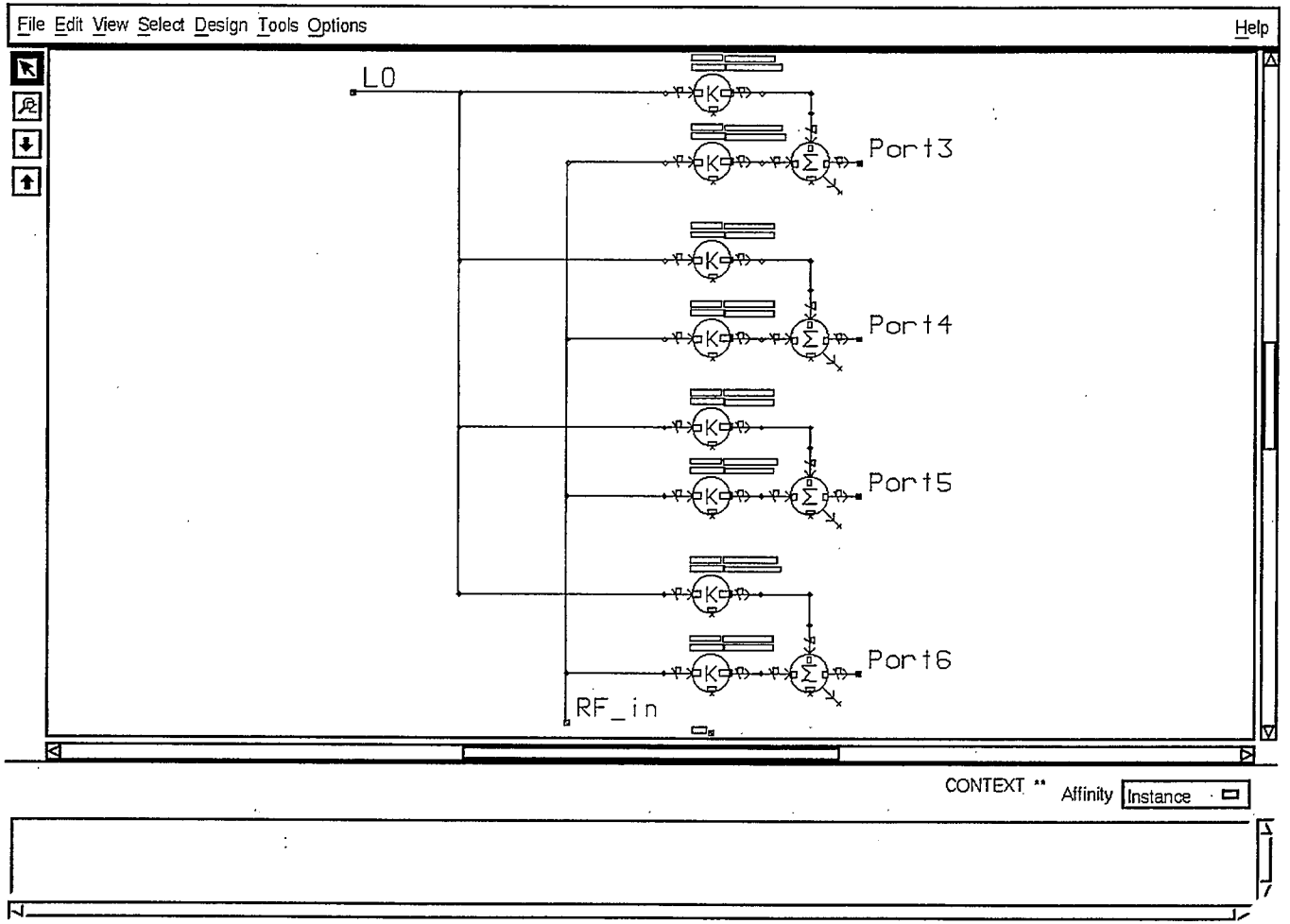

File Edit View Select Design Tools Options
Help
ERROR COUNTER PARAMETERS
starting samples 1000
modulo constant 10000.0
comp_inc
comp_inc
WRITE RESULTS
WRITE RESULTS
WRITE RESULTS
SIMPLE COUNTER
MODULO_N IMPULSE TRAIN
CONTEXT ** Affinity Instance

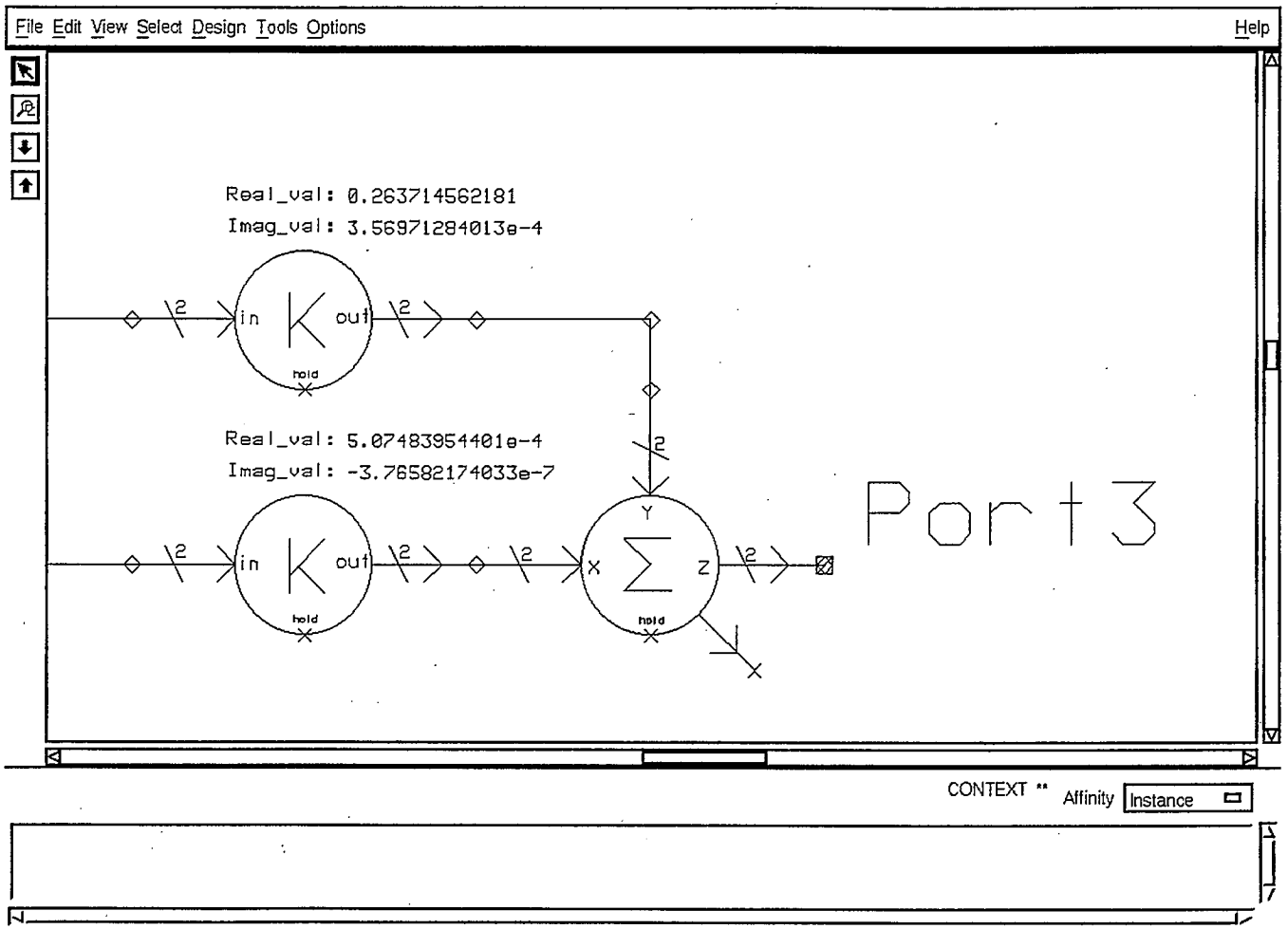

File Edit View Select Design Tools Options
Help
x1
REAL
VARIABLE
DELAY
x
y
y1
delay
hold
delay
delay
maximum_delay 100000
x2
REAL
VARIABLE
DELAY
x
y
y2
delay
hold
delay
CONTEXT **
Affinity
Instance

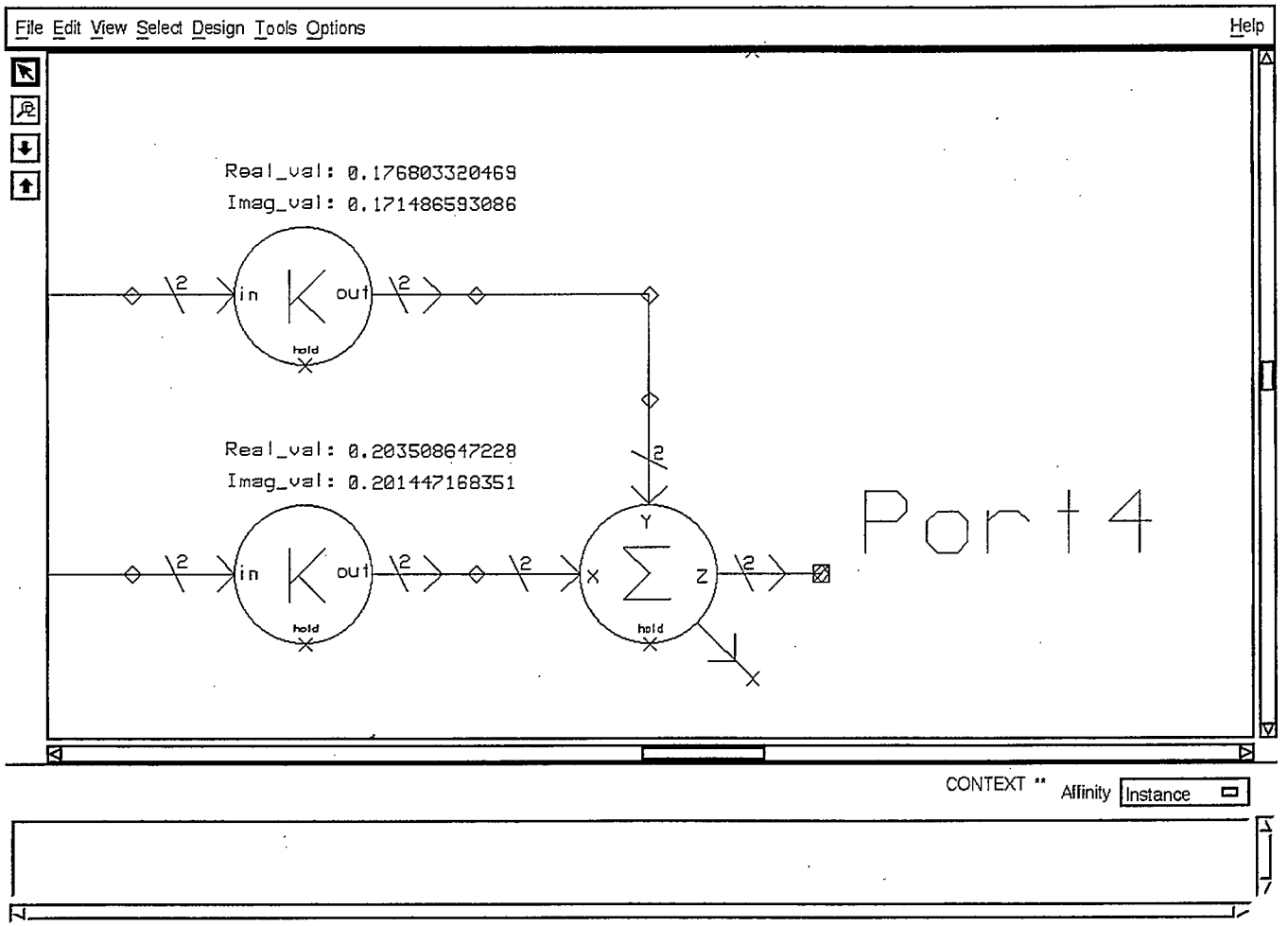

File Edit View Select Design Tools Options
Help
SIMPLE
COUNTER
count
count
reset
hold
X
=REAL
x
y
z
hold
hold
CONTEXT
Affinity
Instance

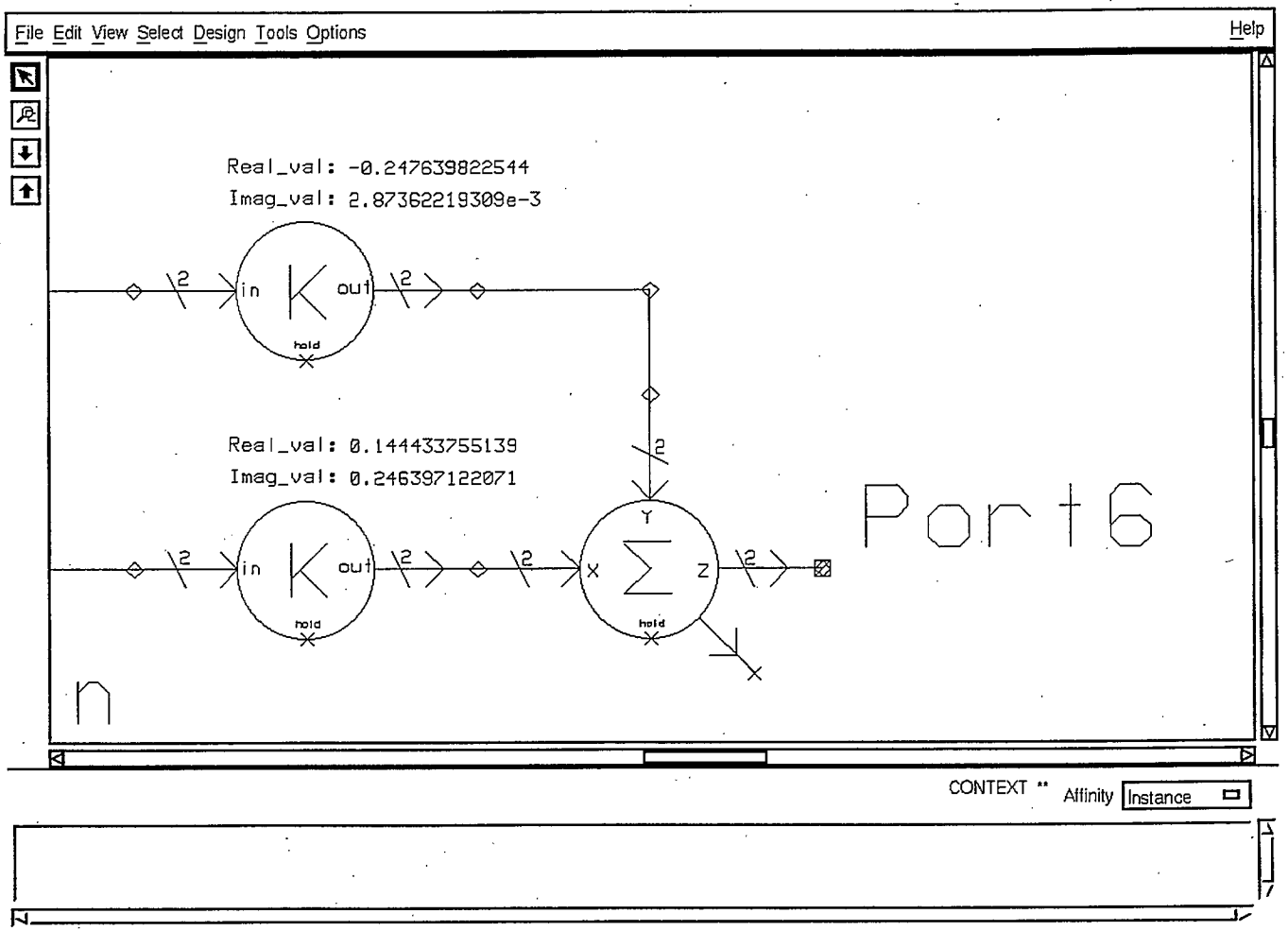
# Section A3

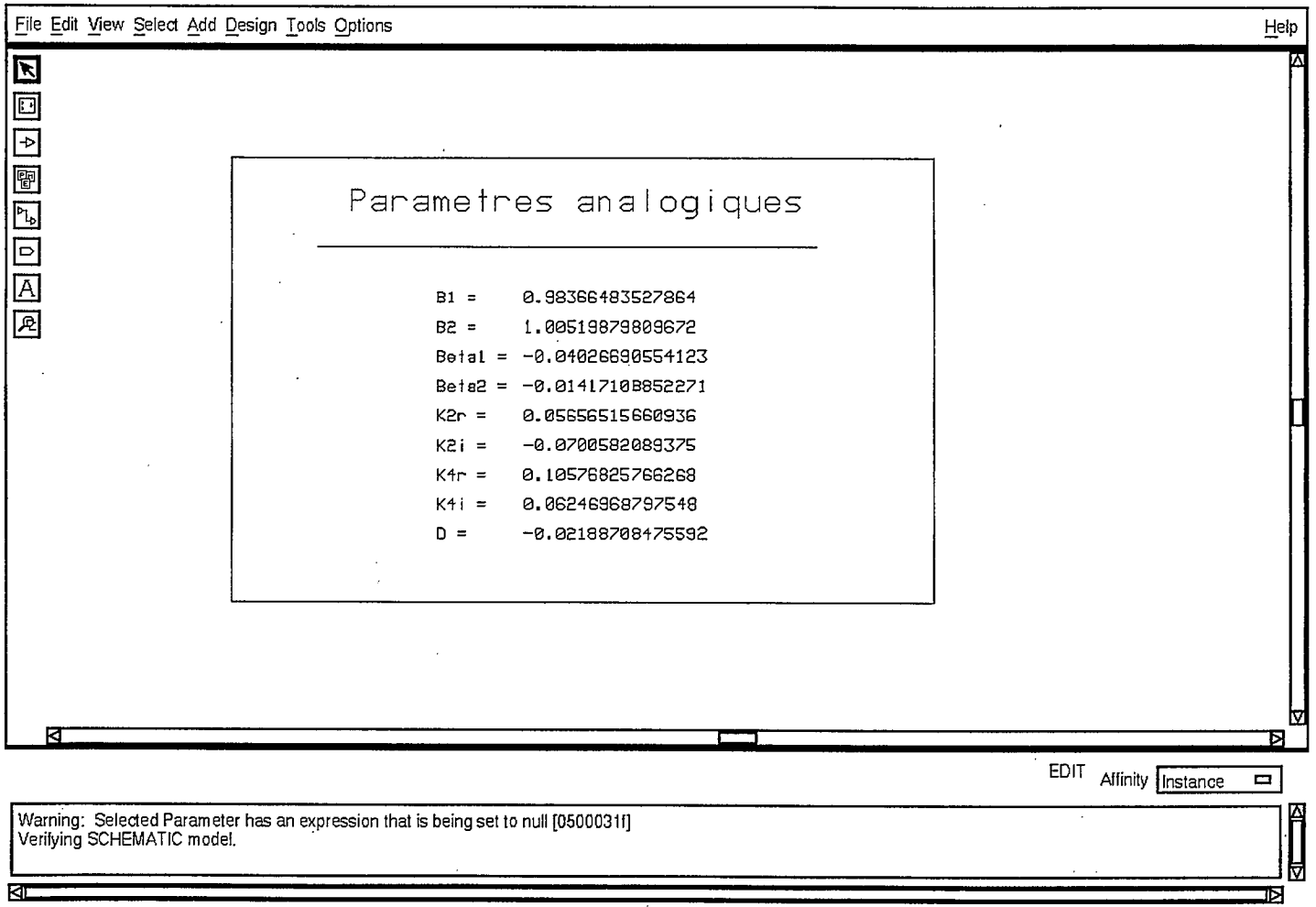
## Nouveaux paramètres du six ports


File Edit View Select Design Tools Options
Help
LO
Port3
Port4
Port5
Port6
RF_in
CONTEXT **
Affinity
Instance


File Edit View Select Design Tools Options
Help
Real_val: 0.263714562181
Imag_val: 3.56971284013e-4
Real_val: 5.07483954401e-4
Imag_val: -3.76582174033e-7
in
out
hold
X
Y
Z
Port3
CONTEXT **
Affinity
Instance

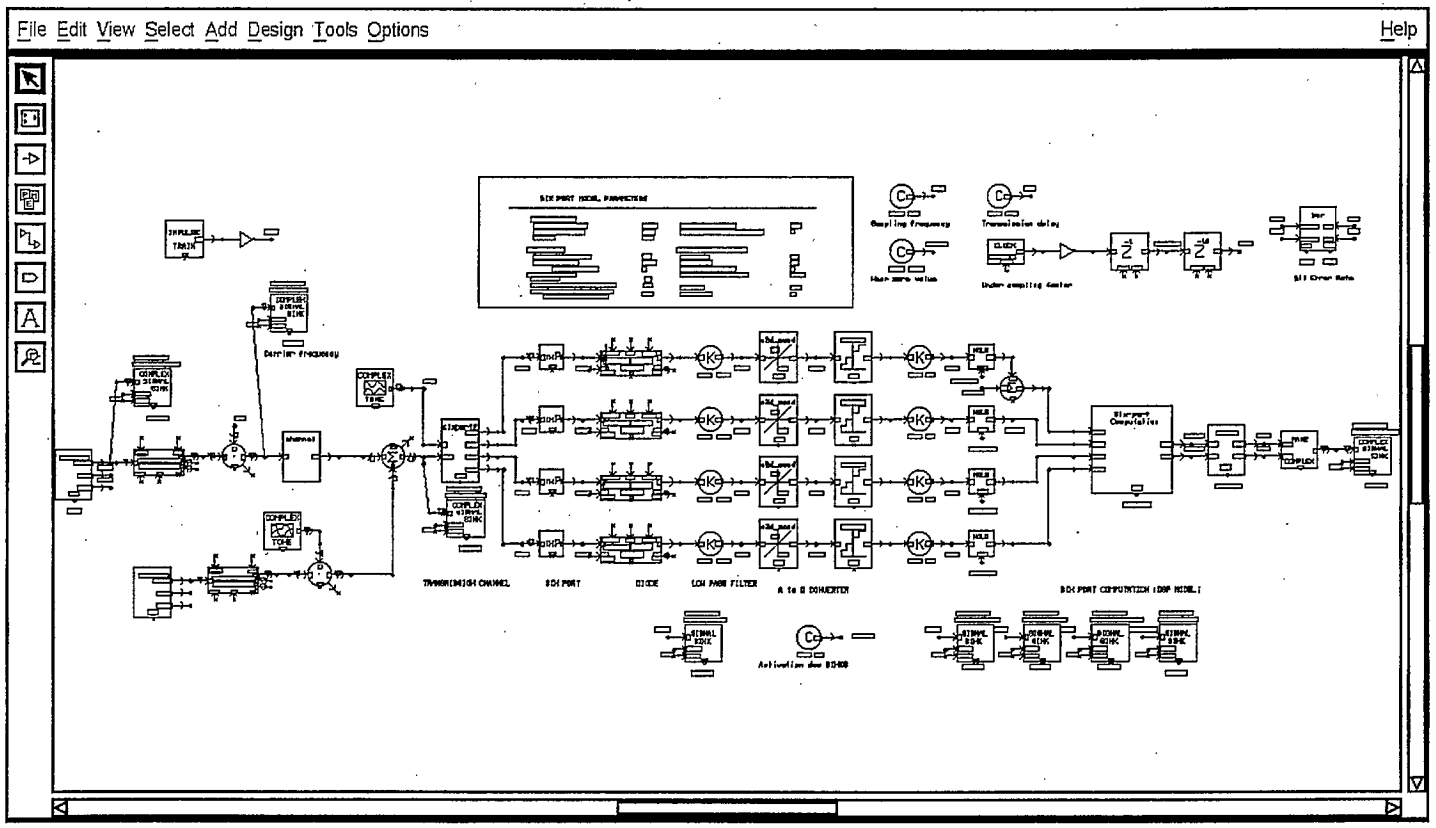

File Edit View Select Design Tools Options
Help
Real_val: 0.176803320469
Imag_val: 0.171486593086
2
in
out
2
hold
Real_val: 0.203508647228
Imag_val: 0.201447168351
2
2
in
out
2
2
Y
X
Z
2
hold
Port4
CONTEXT **
Affinity
Instance

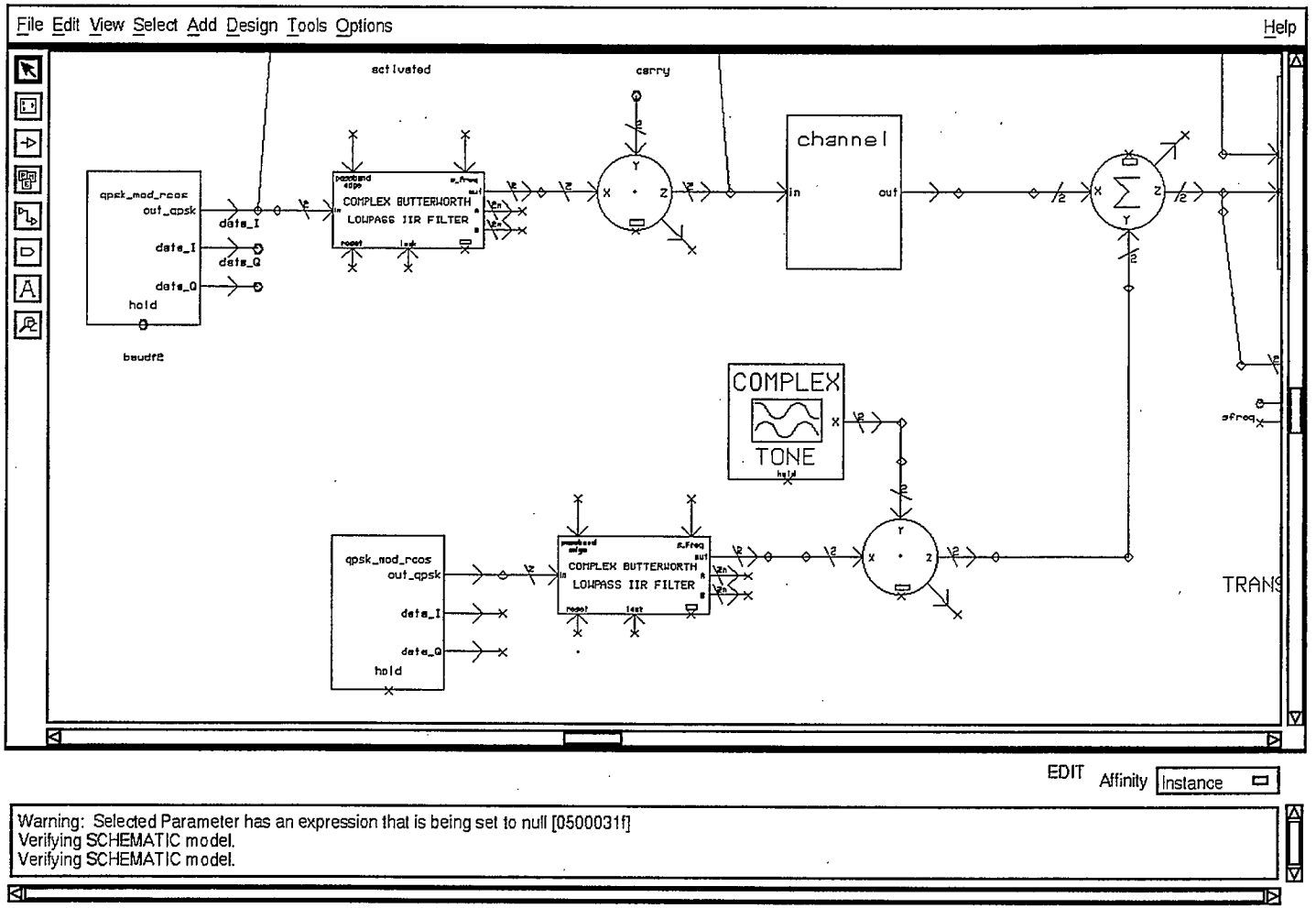

File Edit View Select Design Tools Options
Help
Real_val: -0.247639822544
Imag_val: 2.87362219309e-3
2
in
out
2
hold
Real_val: 0.144433755139
Imag_val: 0.246397122071
2
2
in
out
2
2
X
Y
Z
2
hold
hold
Port6
n
CONTEXT **
Affinity
Instance

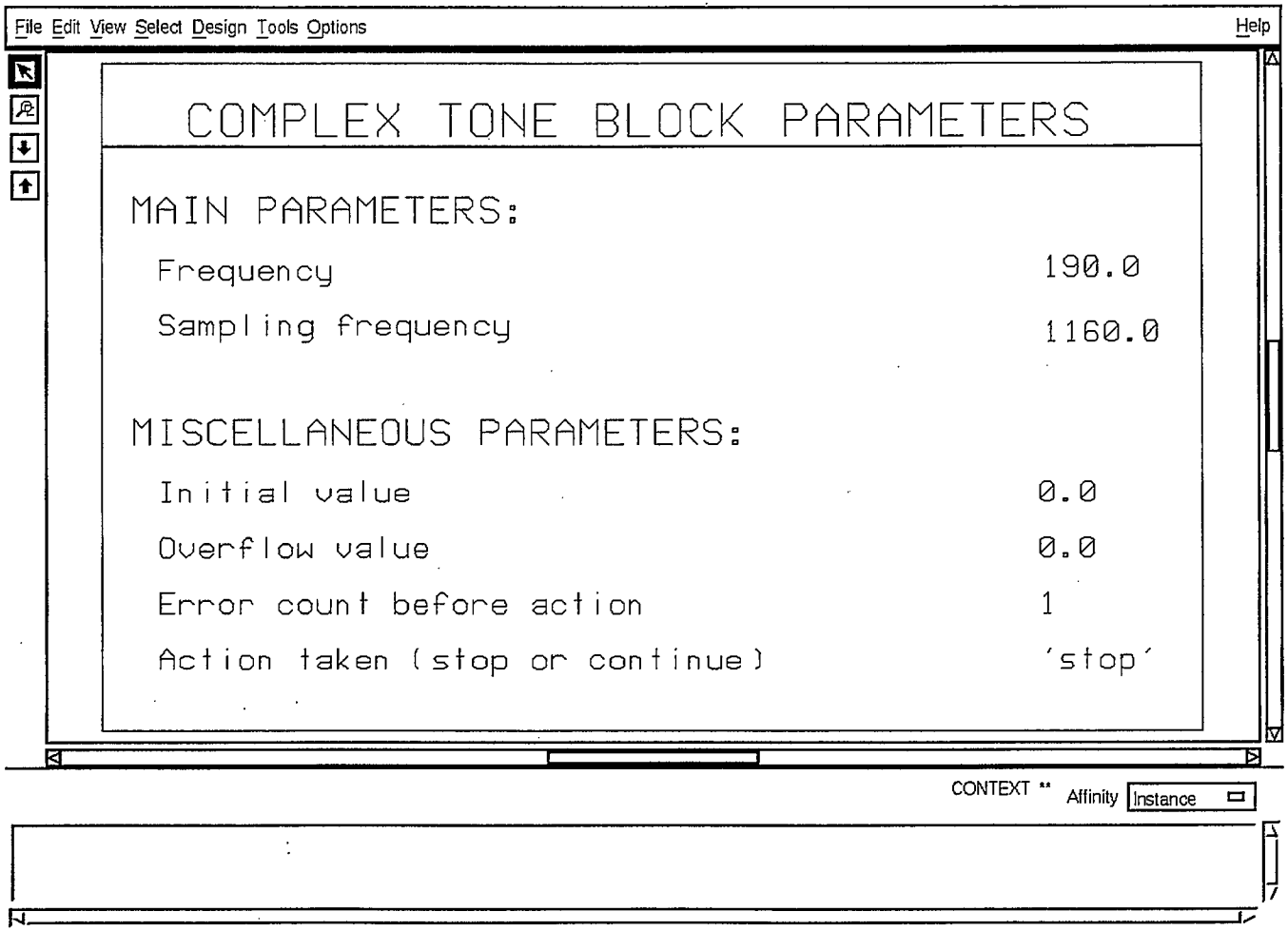

File Edit View Select Add Design Tools Options
Help
Parametres analogiques
B1 = 0.98366483527864
B2 = 1.00519879809672
Beta1 = -0.04026690554123
Beta2 = -0.01417108852271
K2r = 0.05656515660936
K2i = -0.0700582089375
K4r = 0.10576825766268
K4i = 0.06246968797548
D = -0.02188708475592
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.

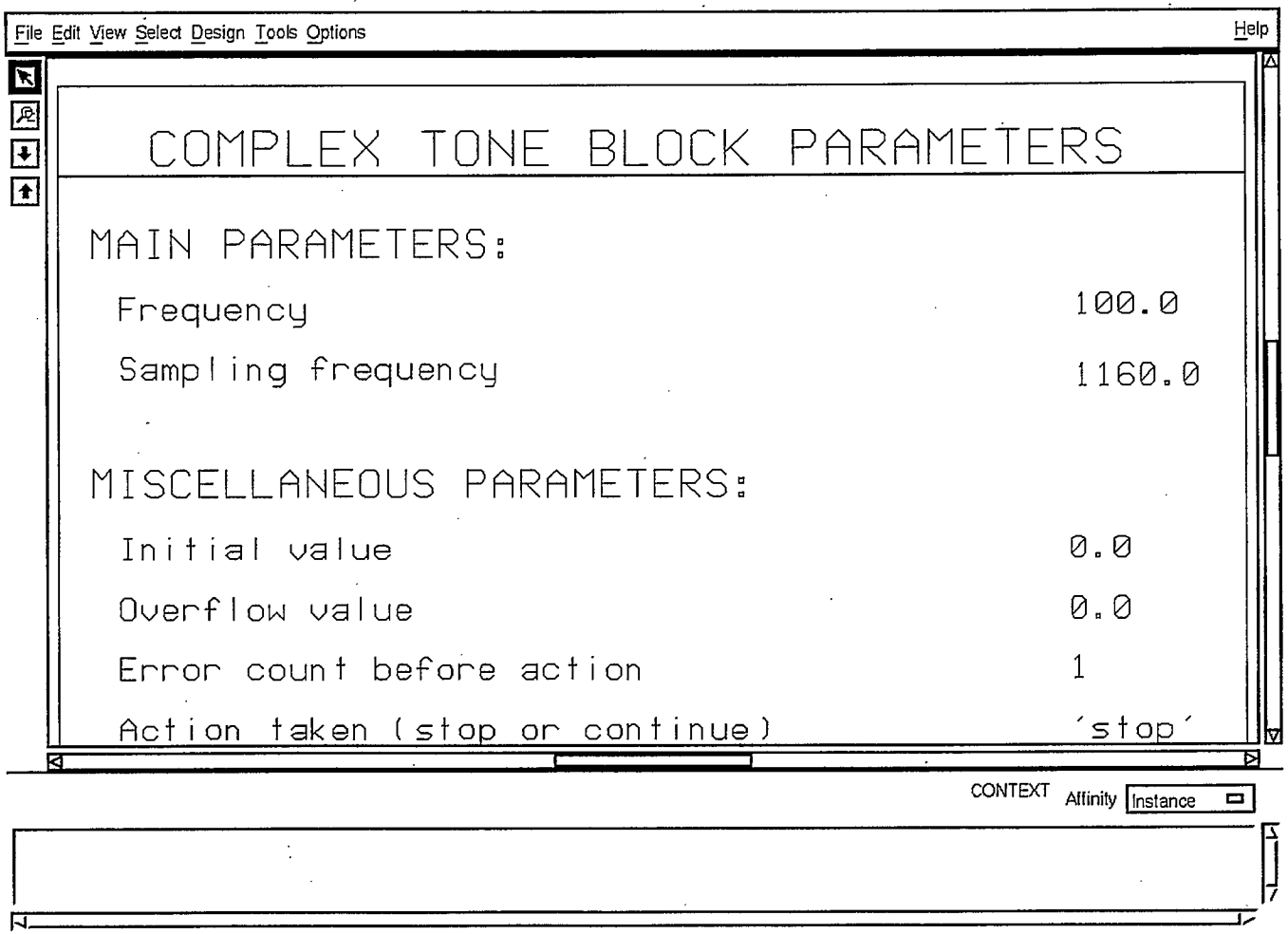
# Section A4

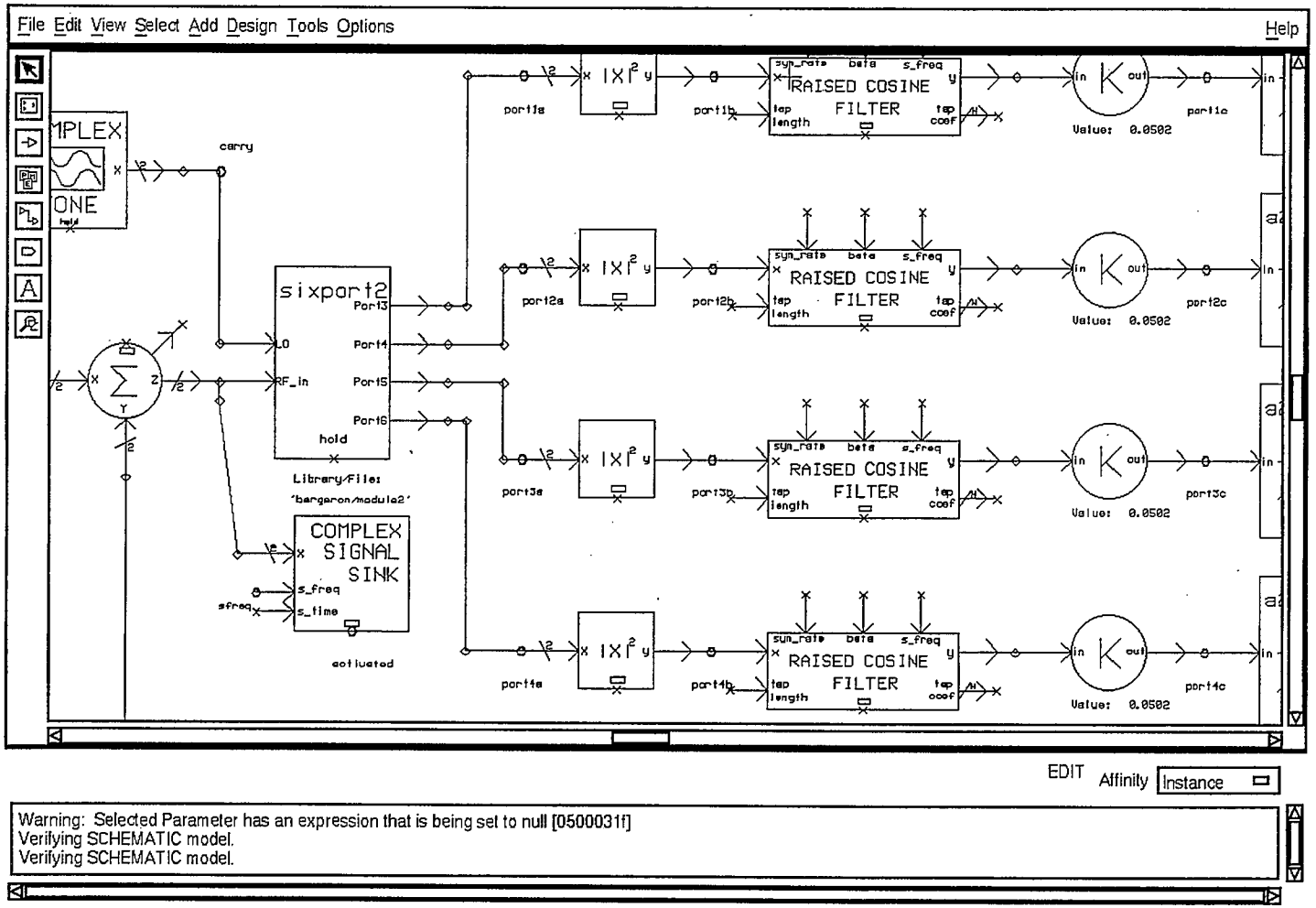
## Paramètres du système avec ajout d'interférences

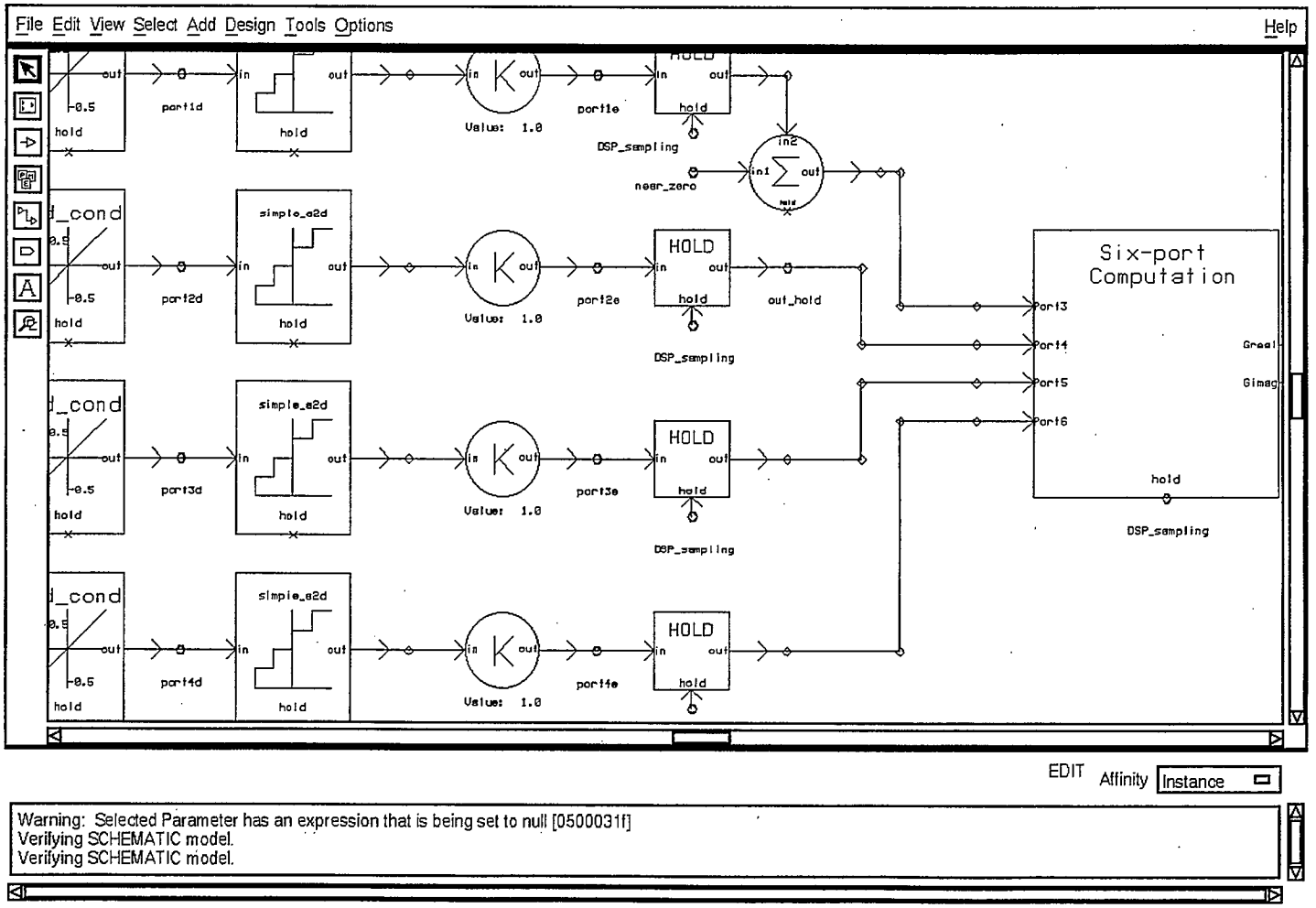

File Edit View Select Add Design Tools Options
Help
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.
Verifying SCHEMATIC model.

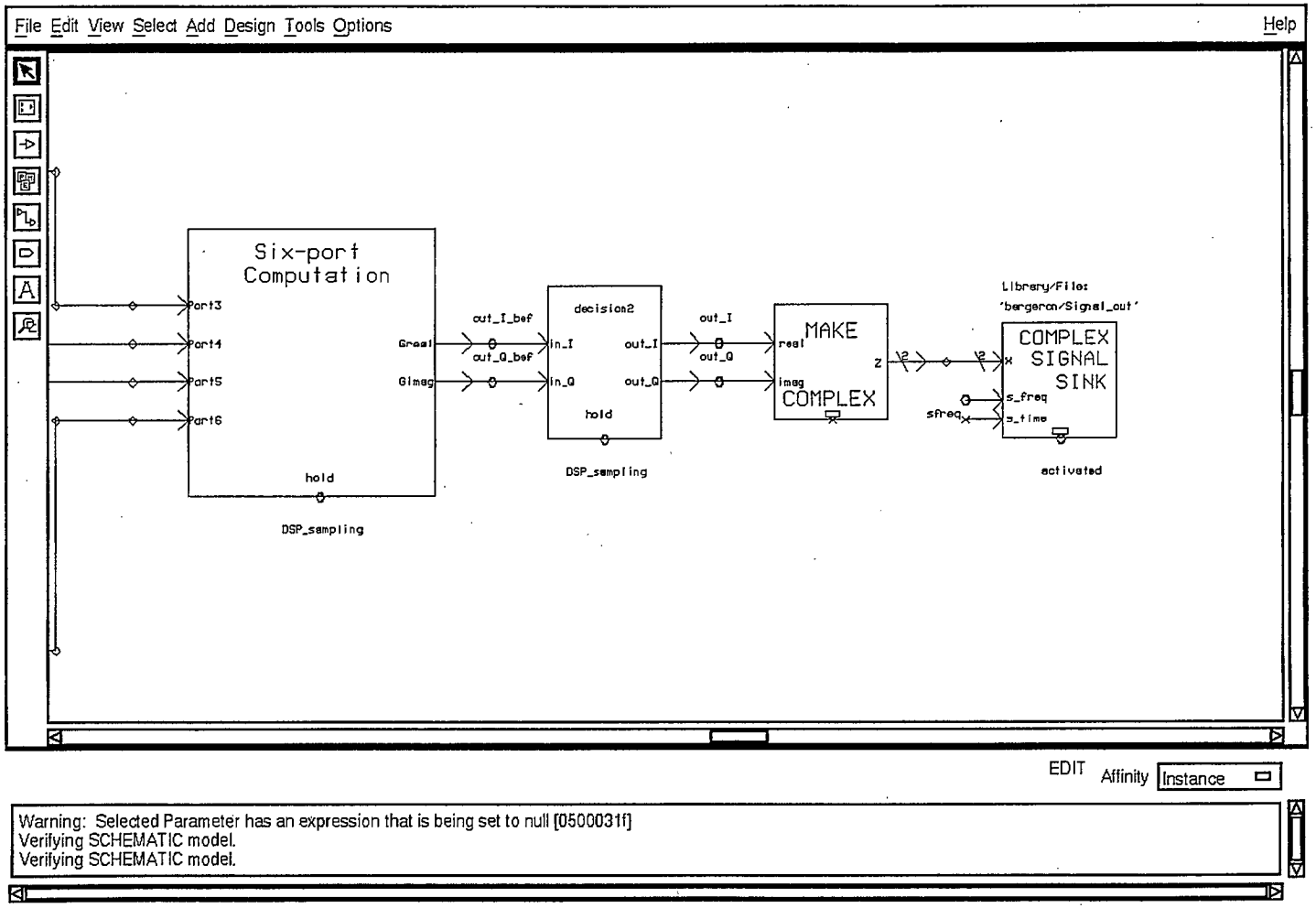

File Edit View Select Add Design Tools Options
Help
activated
carry
channel
in
out
qpsk_mod_rcos
out_qpsk
data_I
data_Q
hold
baudf2
COMPLEX BUTTERWORTH
LOWPASS IIR FILTER
COMPLEX
TONE
TRANS
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.
Verifying SCHEMATIC model.

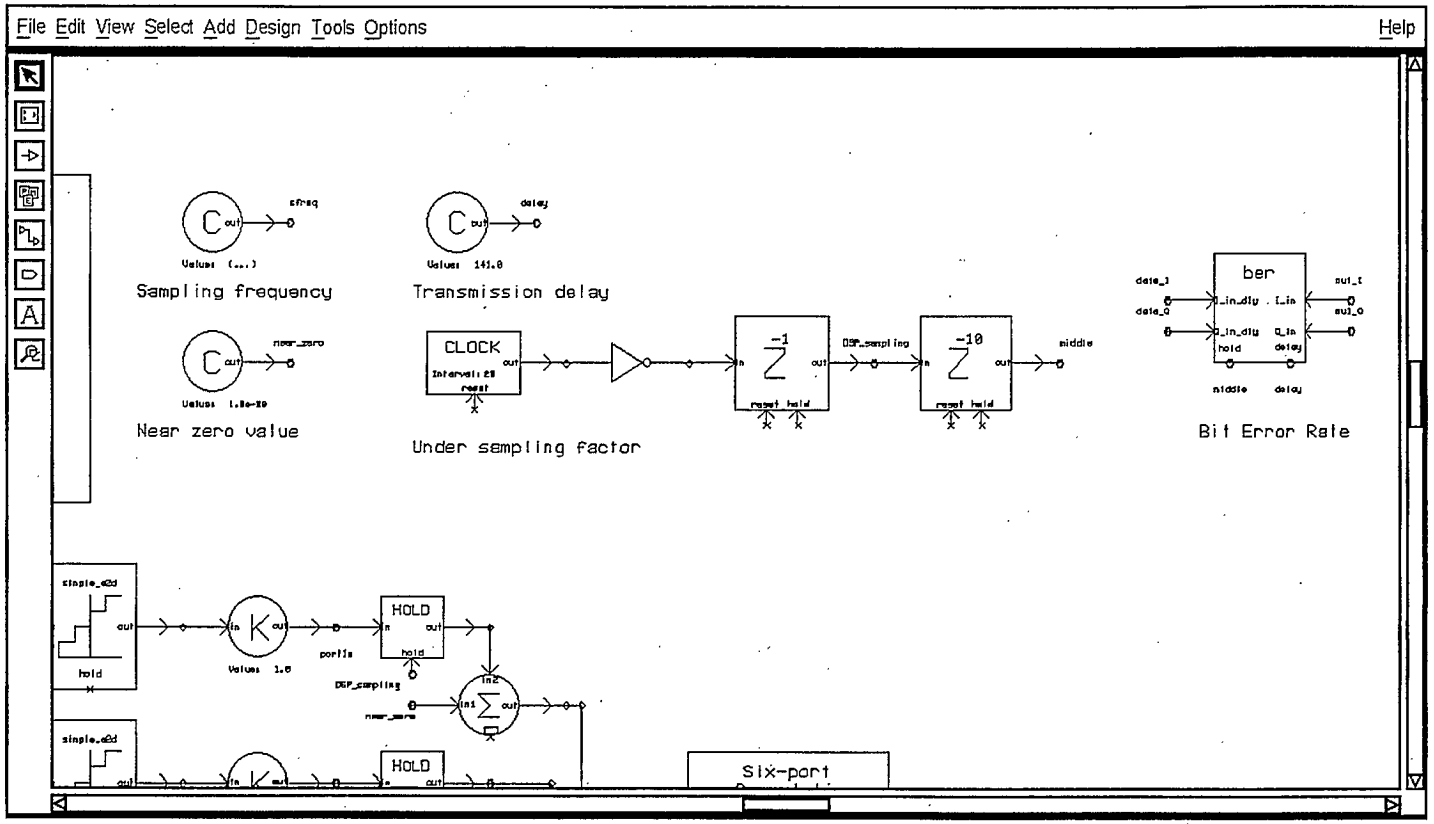

File Edit View Select Design Tools Options
Help
COMPLEX TONE BLOCK PARAMETERS
MAIN PARAMETERS:
Frequency 190.0
Sampling frequency 1160.0
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
CONTEXT ** Affinity Instance


File Edit View Select Design Tools Options
Help
COMPLEX TONE BLOCK PARAMETERS
MAIN PARAMETERS:
Frequency 100.0
Sampling frequency 1160.0
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
CONTEXT Affinity Instance


File Edit View Select Add Design Tools Options
Help
MPLEX
ONE
carry
sixport2
Port3
Port4
Port5
Port6
RF_in
hold
Library/File:
'bergeron/module2'
COMPLEX
SIGNAL
SINK
s_freq
s_time
activated
RAISED COSINE
FILTER
syn_rate
beta
s_freq
tap length
tap coef
Value: 0.0502
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.
Verifying SCHEMATIC model.

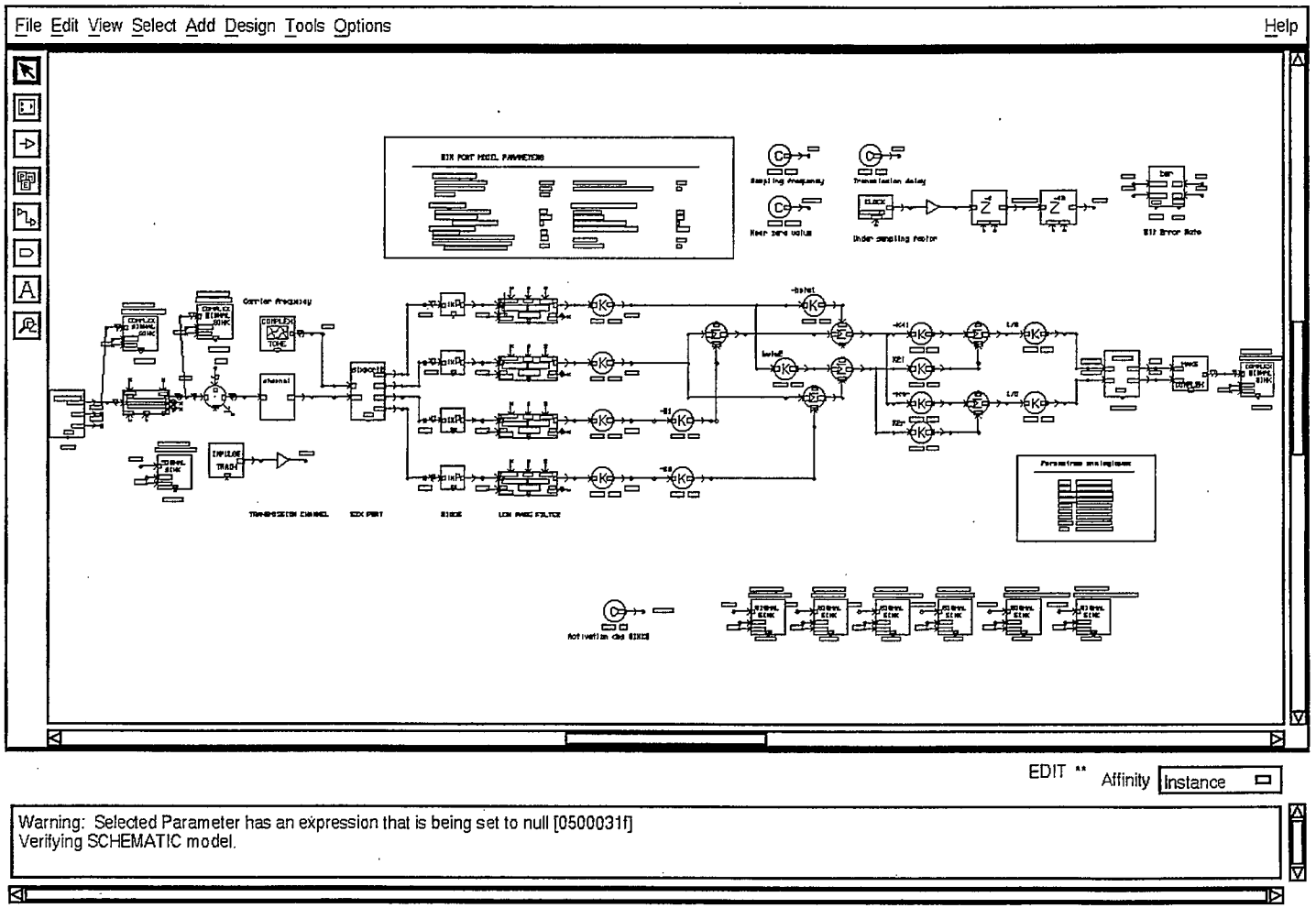

File Edit View Select Add Design Tools Options
Help
Six-port
Computation
HOLD
simple_s2d
Value: 1.0
DSP_sampling
near_zero
out_hold
Greal
Gimag
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.
Verifying SCHEMATIC model.

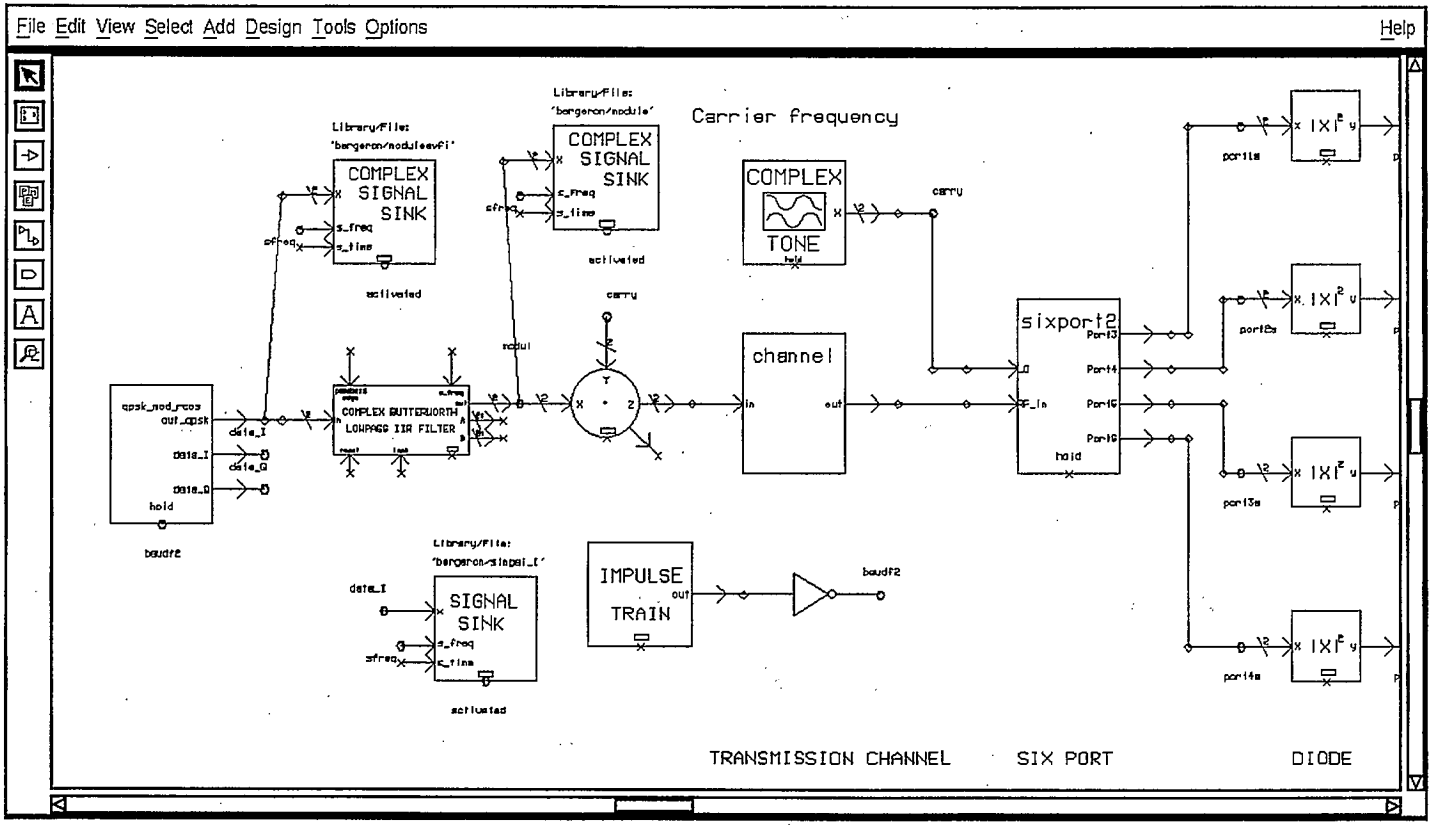

File Edit View Select Add Design Tools Options
Help
Six-port
Computation
Port3
Port4
Port5
Port6
Greal
Gimag
hold
DSP_sampling
out_I_bef
out_Q_bef
decision2
in_I
in_Q
out_I
out_Q
hold
DSP_sampling
out_I
out_Q
MAKE
real
imag
COMPLEX
z
2
2
Library/File:
'bergeron/Signal_out'
COMPLEX
SIGNAL
SINK
s_freq
s_time
sfreq
activated
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.
Verifying SCHEMATIC model.


File Edit View Select Add Design Tools Options
Help
Sampling frequency
Transmission delay
Near zero value
Under sampling factor
CLOCK
-1
-10
DSP_sampling
middle
ber
Bit Error Rate
HOLD
Six-port
EDIT
Affinity
Instance
Warning: Selected.Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.
Verifying SCHEMATIC model.

# Section A5

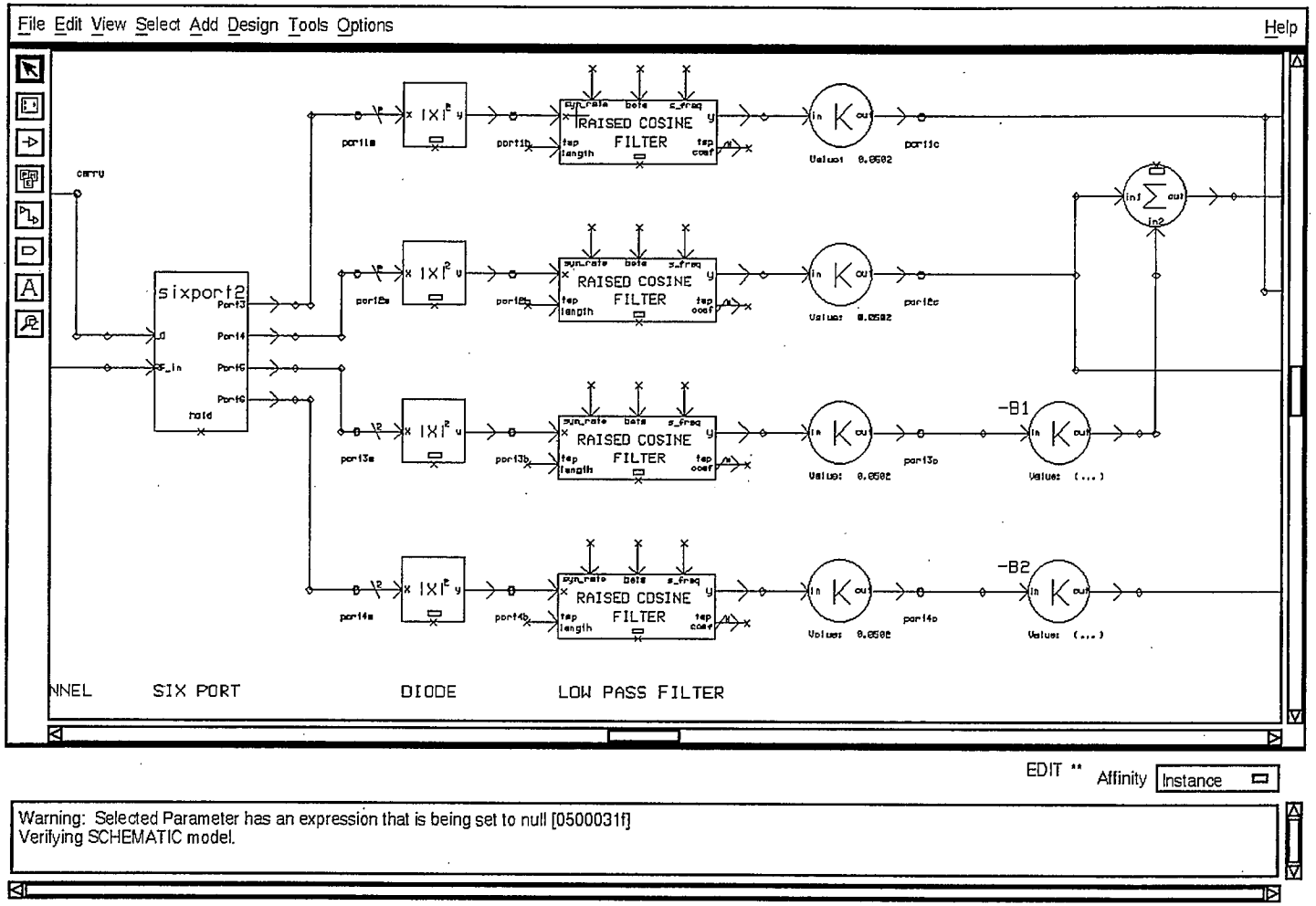
## Paramètres du six ports modélisé analogiquement

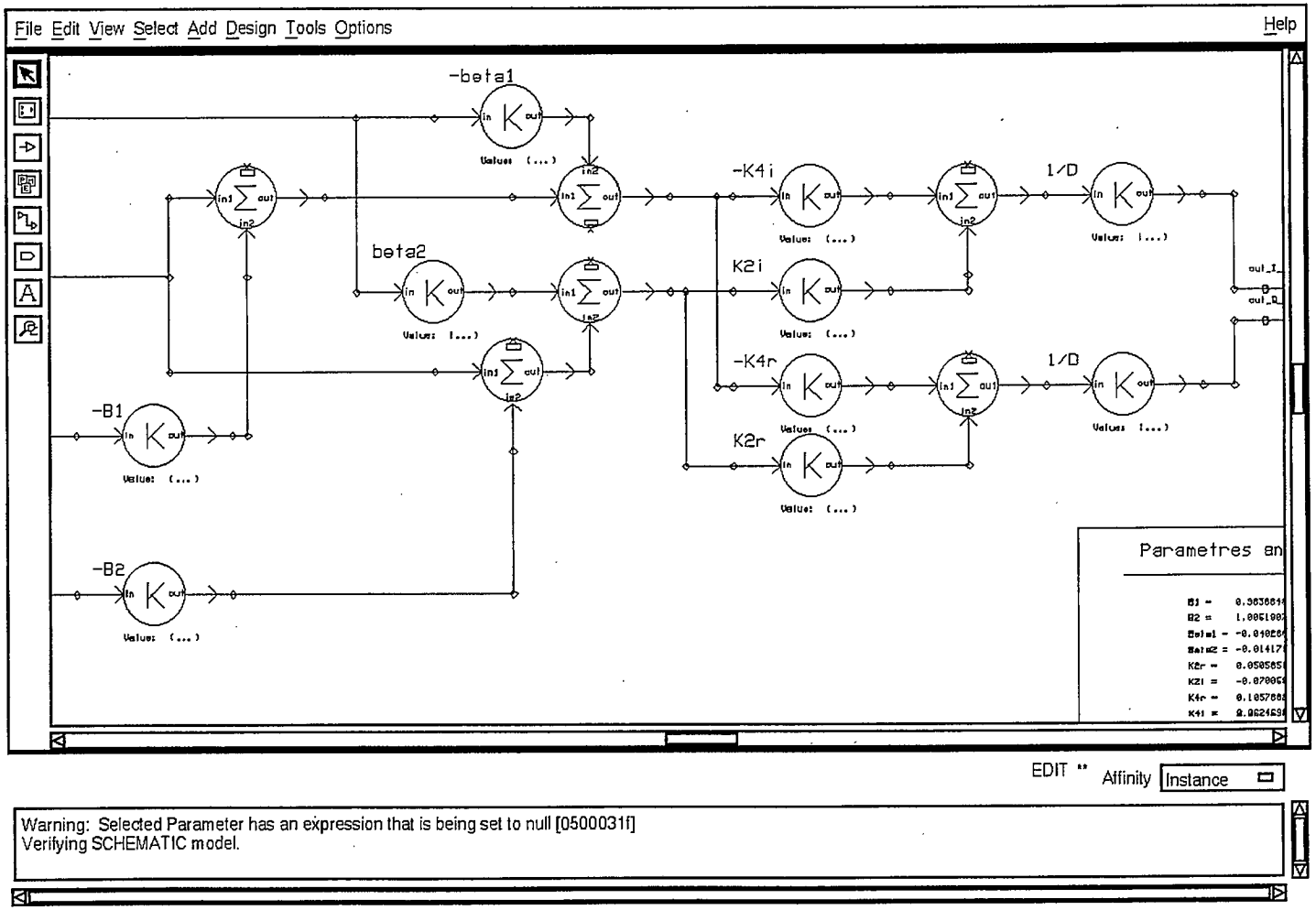

File Edit View Select Add Design Tools Options
Help
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.

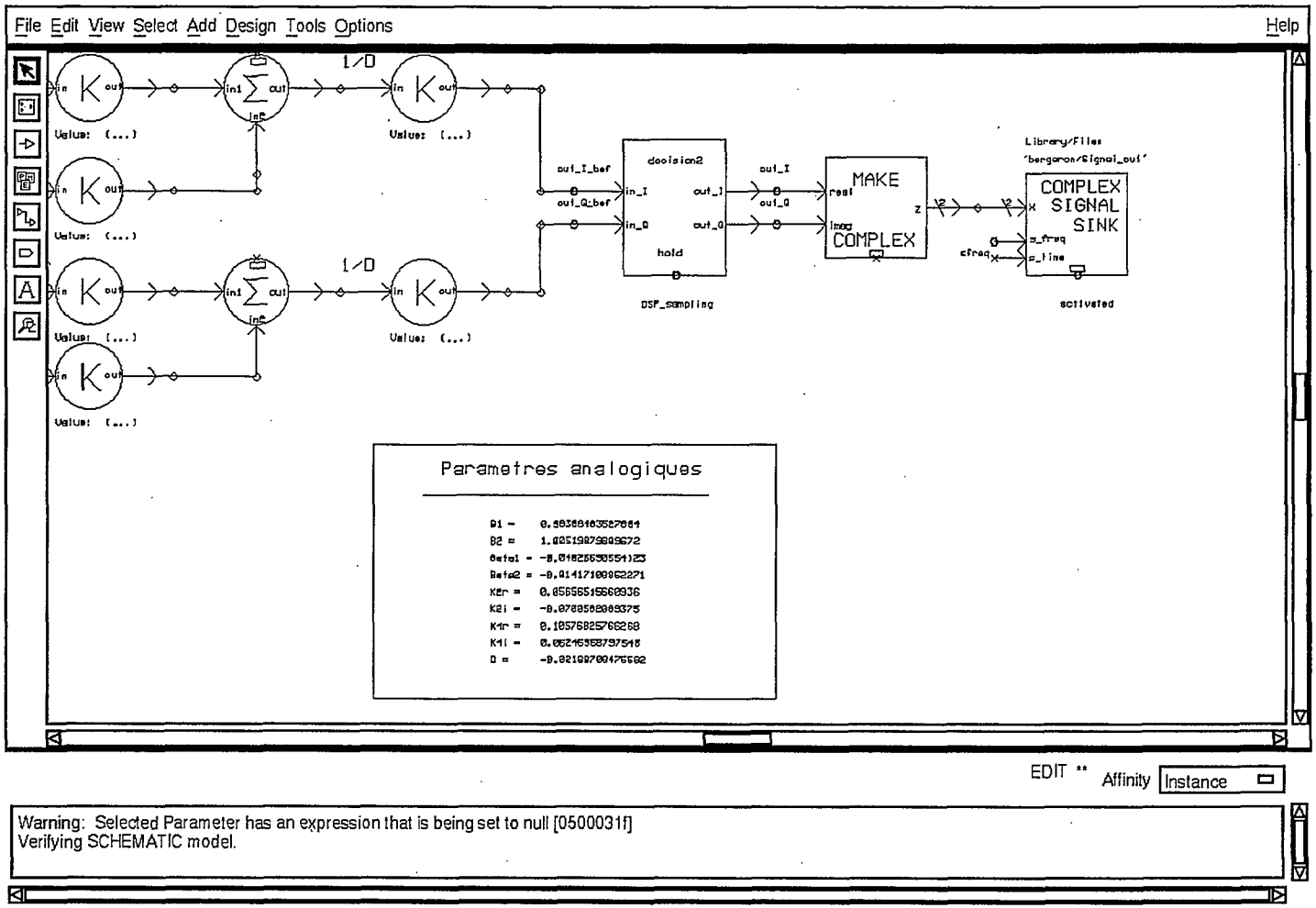



EDIT ** Affinity Instance

Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.


File Edit View Select Add Design Tools Options
Help
sixport2
RAISED COSINE FILTER
-B1
-B2
NNEL
SIX PORT
DIODE
LOW PASS FILTER
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.

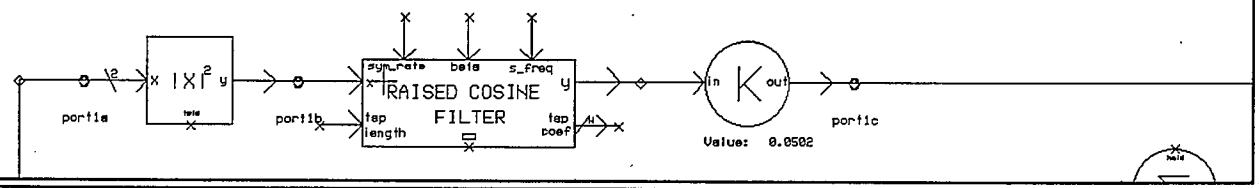

File Edit View Select Add Design Tools Options
Help
-beta1
beta2
-K4i
K2i
-K4r
K2r
1/D
1/D
-B1
-B2
Parametres an
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.


File Edit View Select Add Design Tools Options
Help
1/D
Value: (...)
out_I_bef
out_Q_bef
decision2
in_I
in_Q
out_I
out_Q
hold
DSP_sampling
MAKE
real
imag
COMPLEX
Library/Files
'bergeron/Signal_out'
COMPLEX
SIGNAL
SINK
s_freq
s_time
sfreq
activated
Parametres analogiques
B1 = 0.90368403527864
B2 = 1.00519879809672
Beta1 = -0.04826530554123
Beta2 = -0.01417100062271
K2r = 0.05656515660936
K2i = -0.0700508089375
K1r = 0.10576825766268
K1i = 0.06246568797548
D = -0.02189700476682
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.

File Edit View Select Add Design Tools Options Help

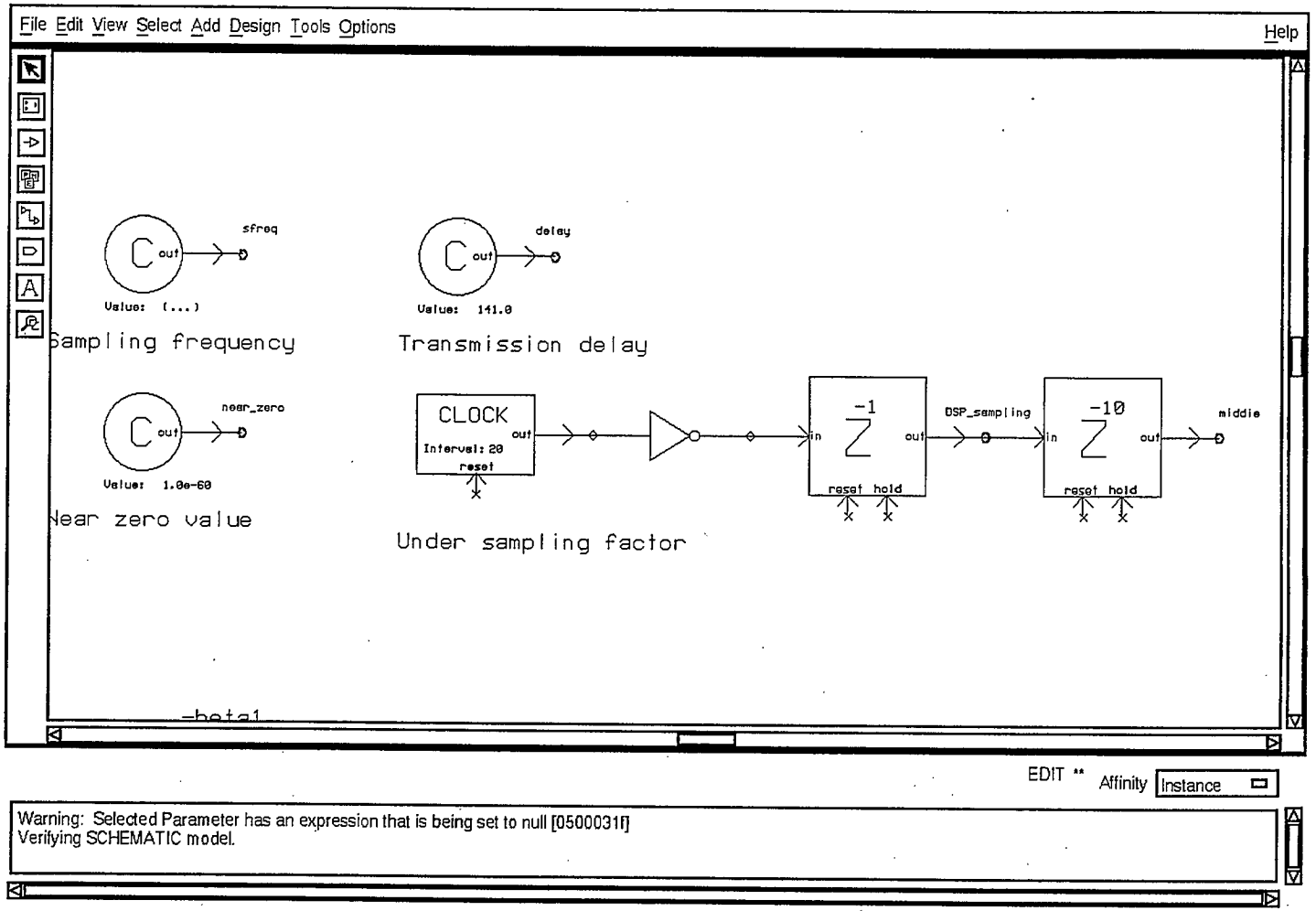
## SIX PORT MODEL PARAMETERS

| | | | |
|---|---|---|---|
| **MAIN PARAMETERS:** | | | |
| Sampling frequency (MHz) | 1160.0 | Lowpass filter edge (MHz) | 58.0 |
| Carrier frequency (MHz) | 100.0 | Number of bits de resolution das A/D's | 16 |
| Baud rate | 58.0 | | |
| **NOISE CHANNEL:** | | **MISCELLANEOUS PARAMETERS:** | |
| Signal to noise ratio (dB) | 6.8 | Initial value | 0.0 |
| Symbol period (usec) | (...) | Overflow value | 0.0 |
| Normalisation switch | 1 | Error count before action | 1 |
| **FILTER PARAMETERS:** | | Action taken (stop or continua) | 'stop' |
| Number of tap | 12 | | |
| Attenuation at passband edge in dB power | 3.0 | clock delay | -134 |
| Default values for unconnected inputs: | | hold out delay | -5 |
| Passband edge frequency in MHz | 80.0 | | |



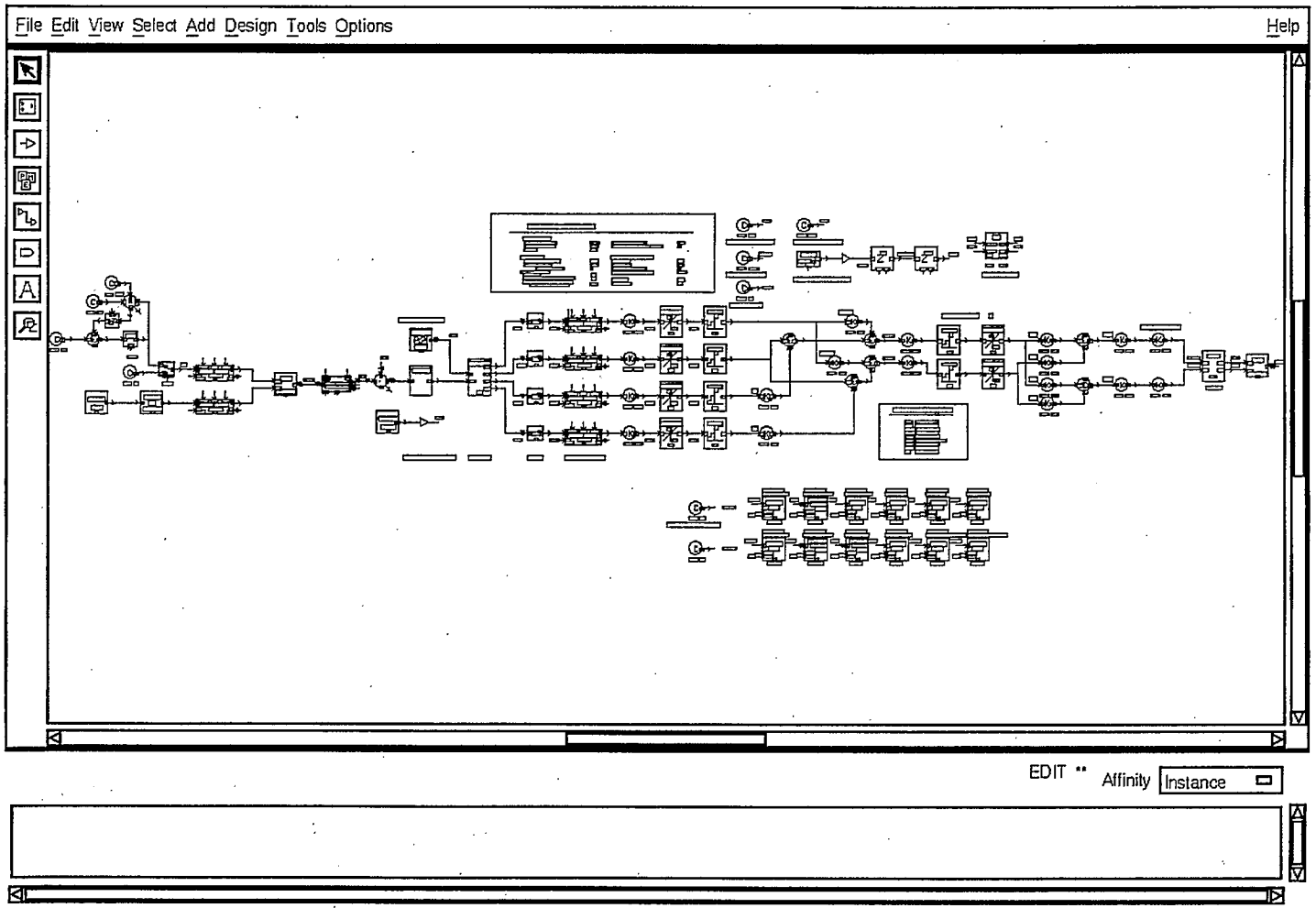

EDIT ** Affinity Instance

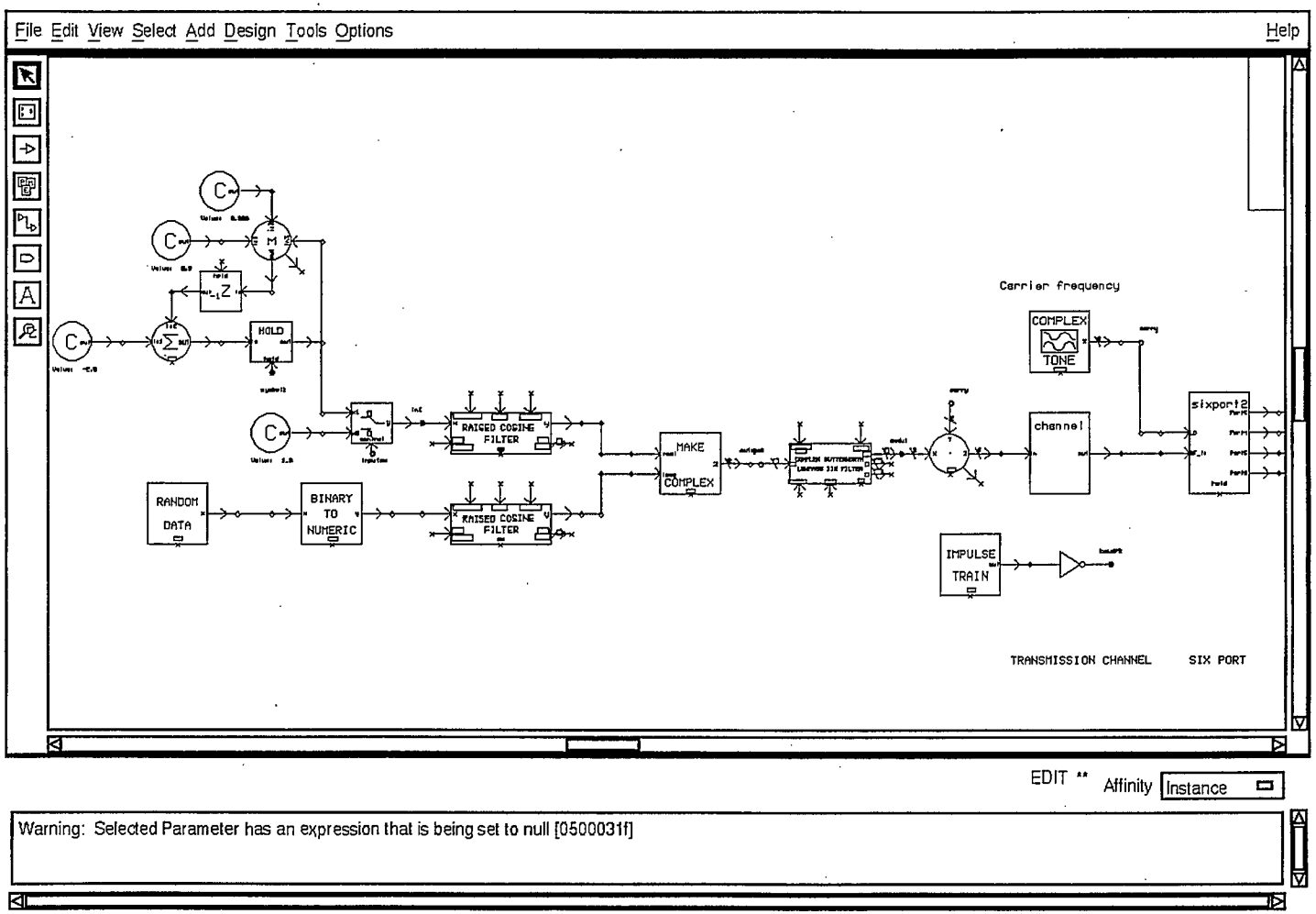
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.

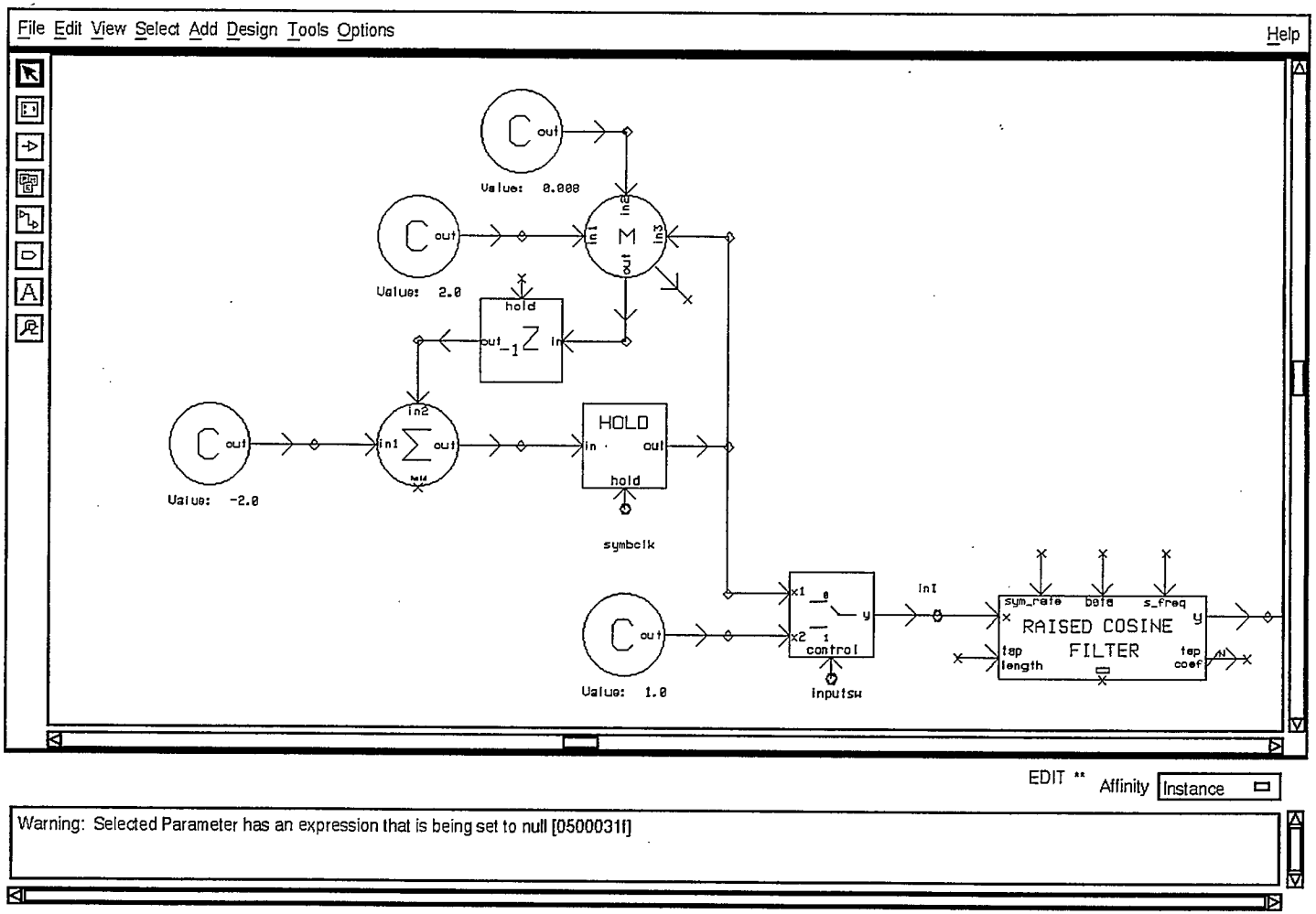

File Edit View Select Add Design Tools Options
Help
sfreq
out
Value: (...)
Sampling frequency
delay
out
Value: 141.0
Transmission delay
near_zero
out
Value: 1.0e-60
Near zero value
CLOCK
out
Interval: 20
reset
-1
in
out
reset hold
DSP_sampling
-10
in
out
reset hold
middle
Under sampling factor
-beta1
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]
Verifying SCHEMATIC model.

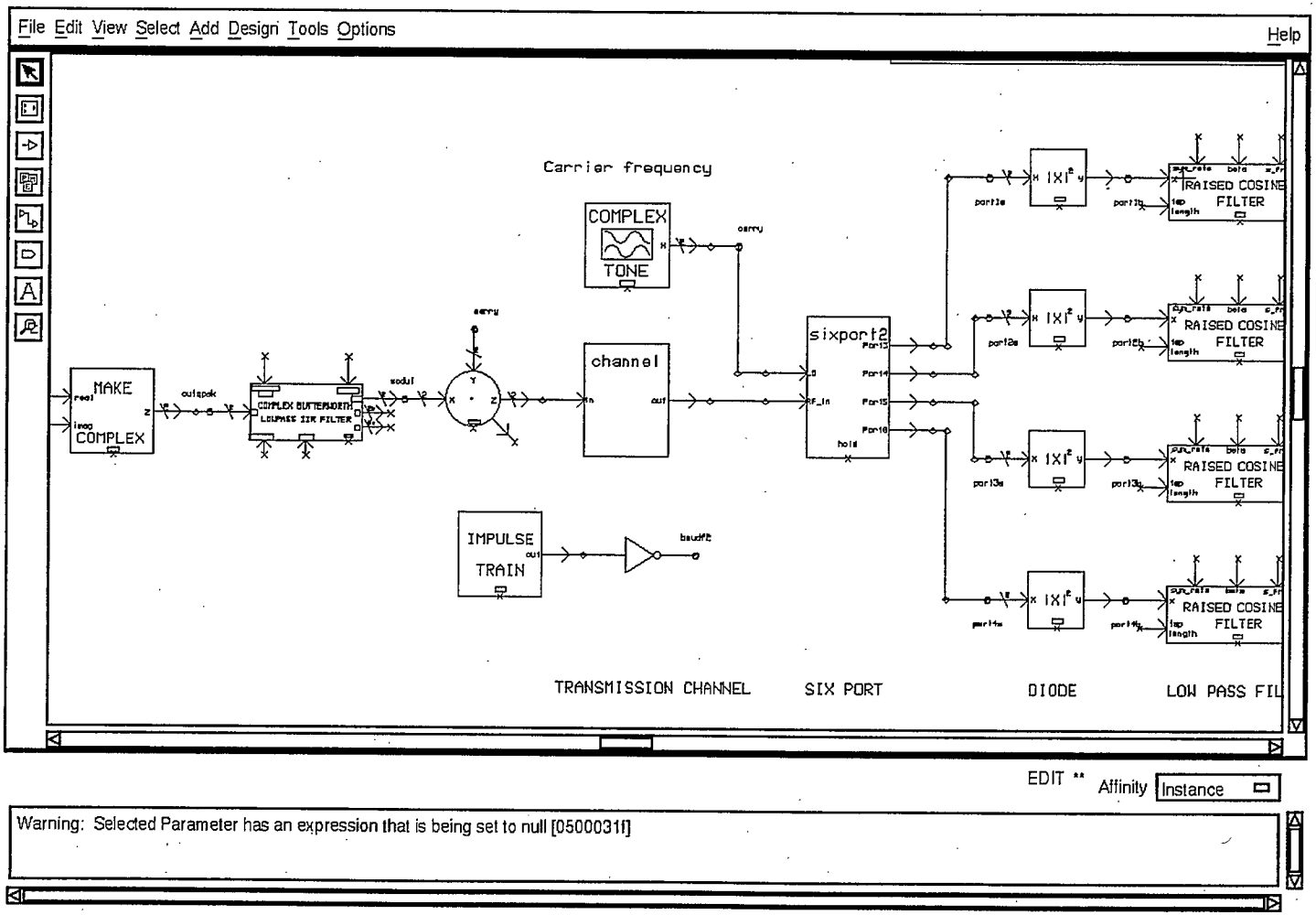
# Section A6

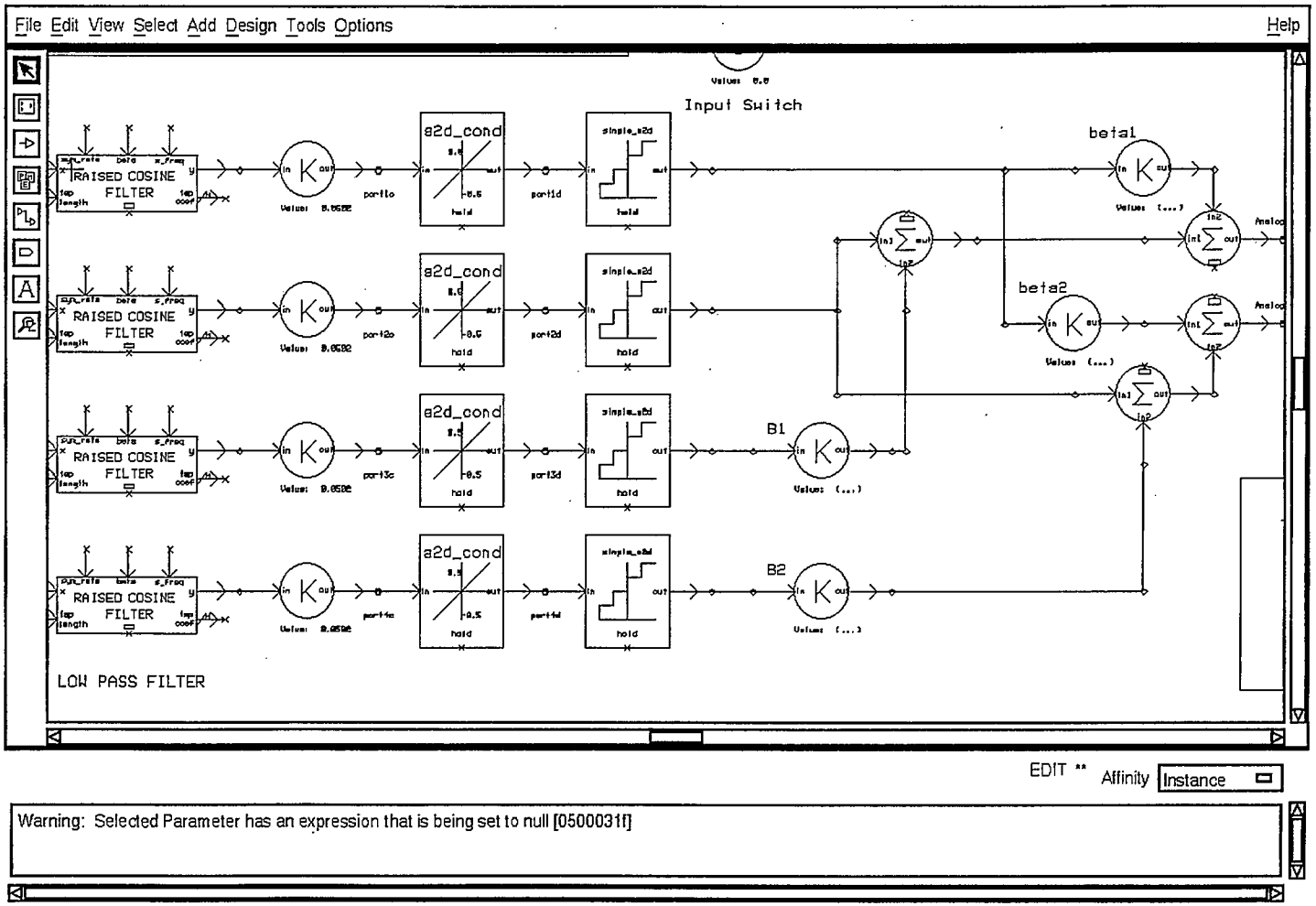
## Paramètres du six ports modélisé et numérisé

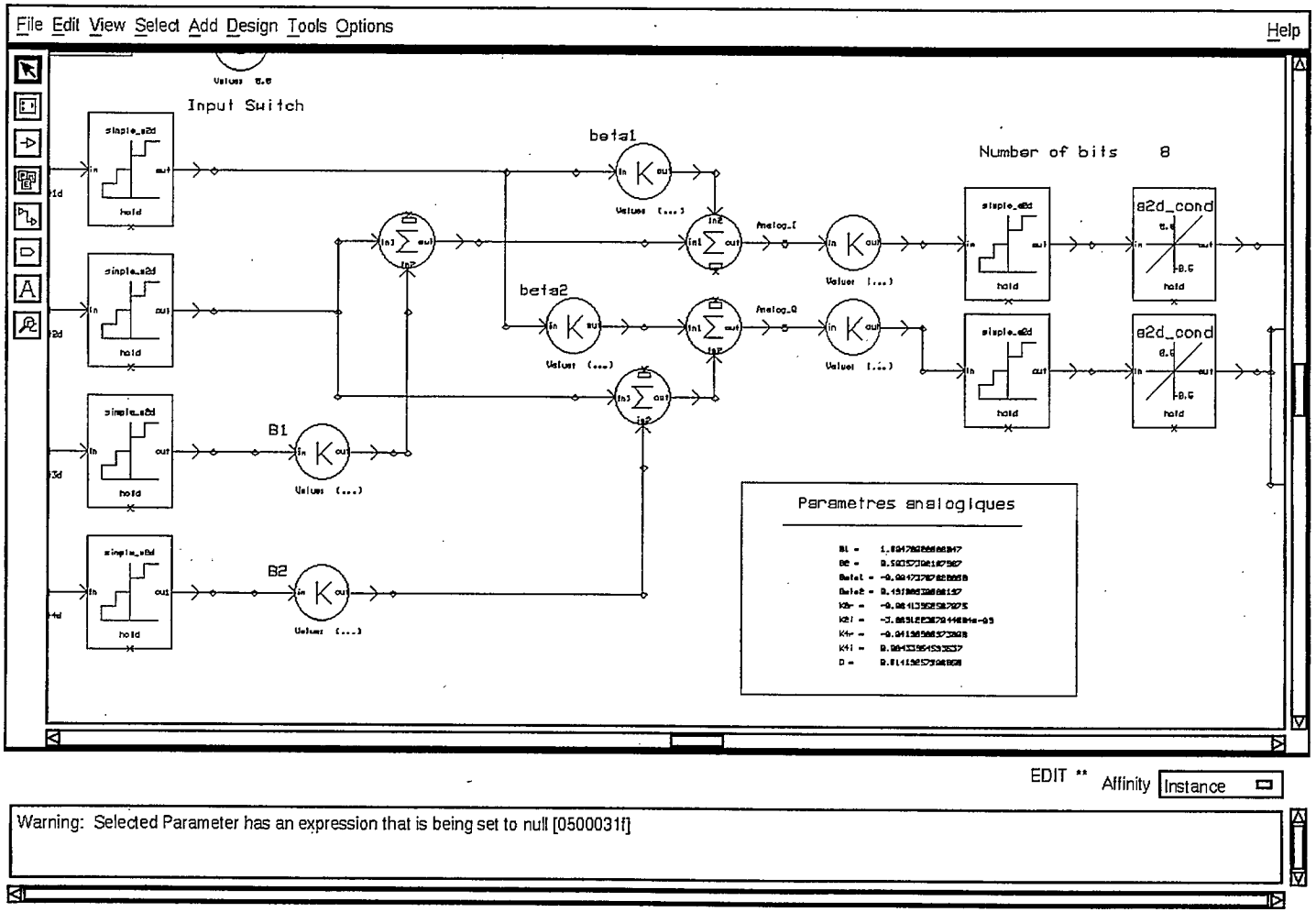

File Edit View Select Add Design Tools Options
Help
EDIT **
Affinity
Instance

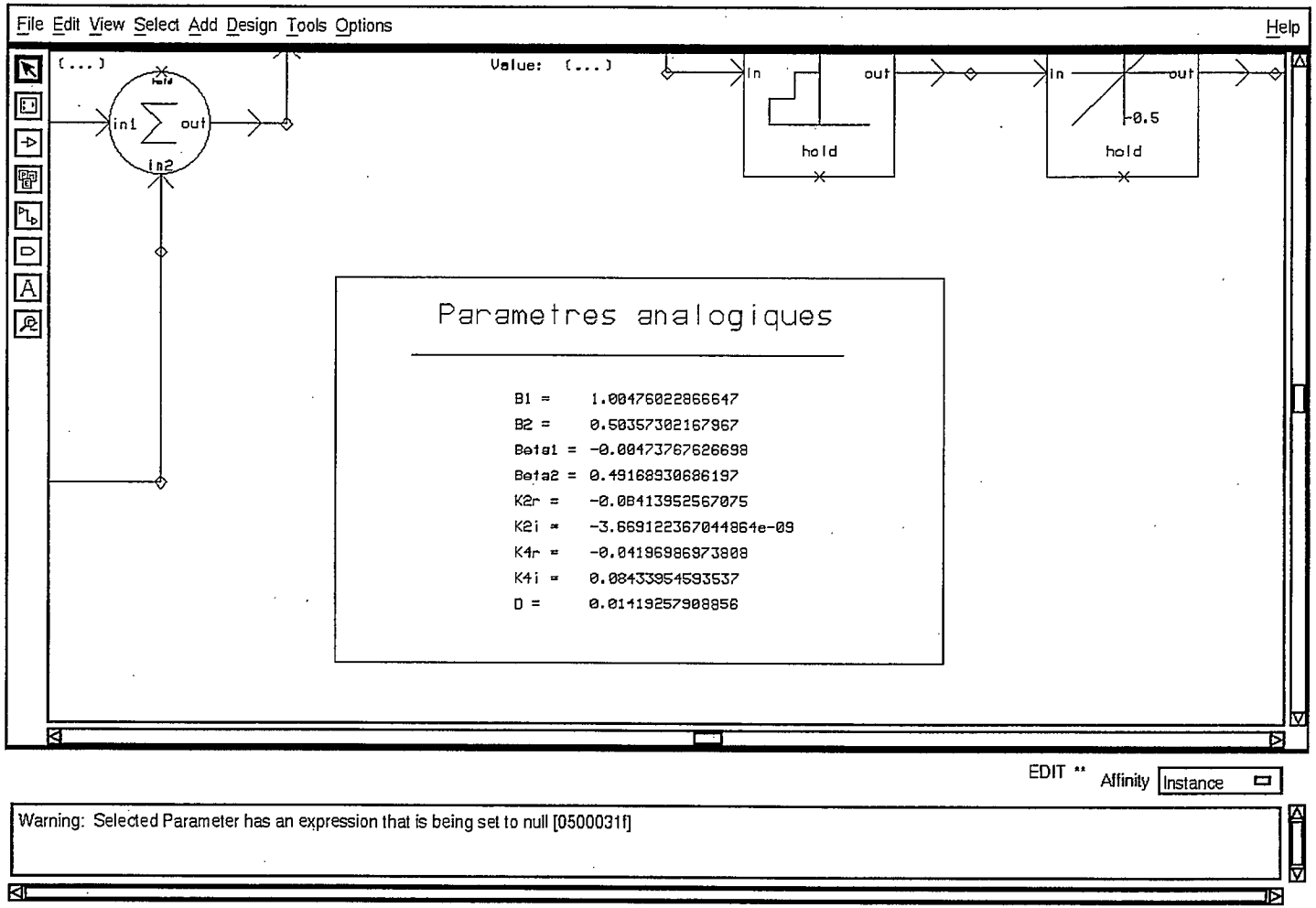

File Edit View Select Add Design Tools Options
Help
Carrier frequency
COMPLEX
TONE
HOLD
RAISED COSINE FILTER
MAKE COMPLEX
channel
sixport2
RANDOM DATA
BINARY TO NUMERIC
RAISED COSINE FILTER
IMPULSE TRAIN
TRANSMISSION CHANNEL
SIX PORT
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]

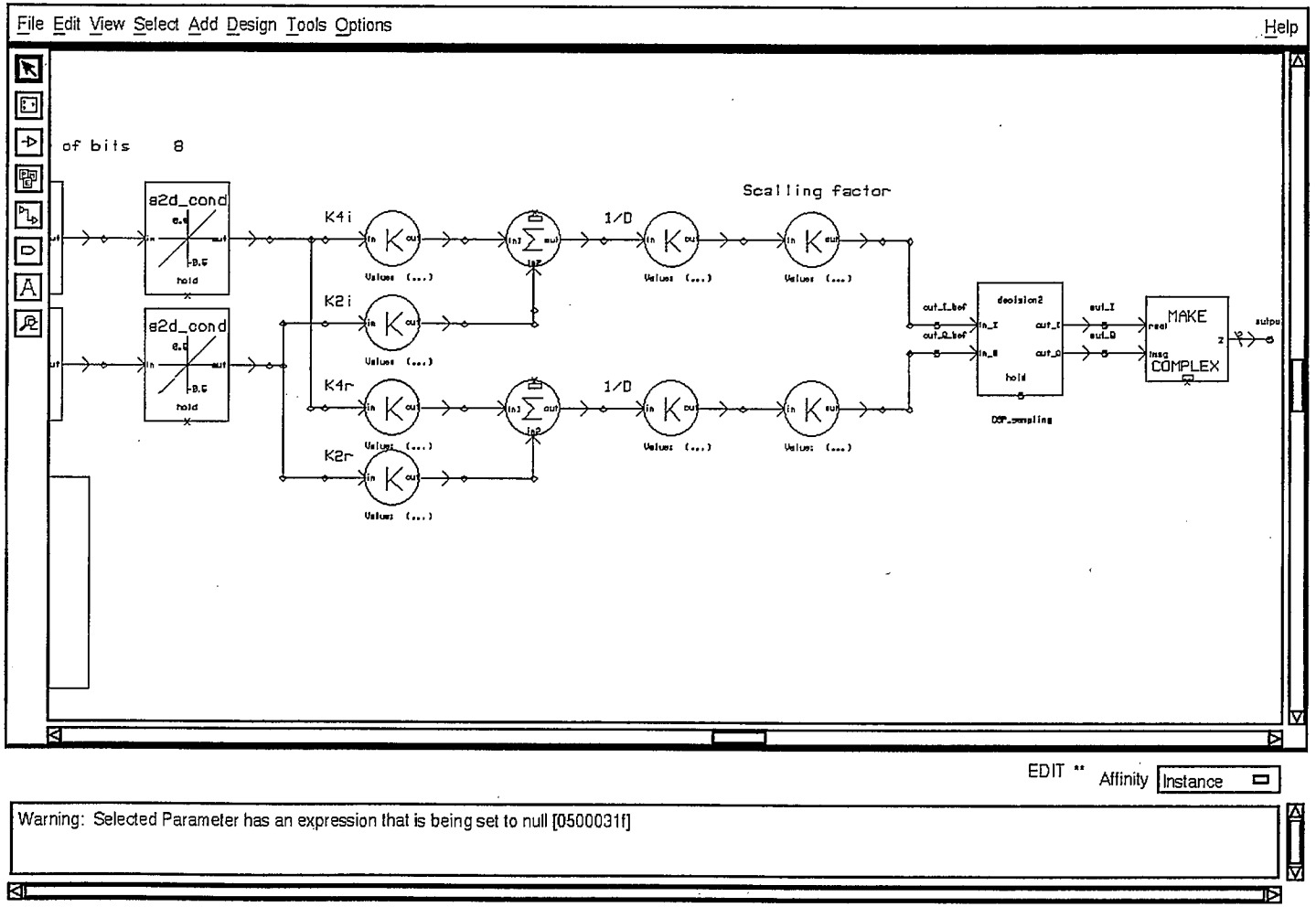

File Edit View Select Add Design Tools Options
Help
C out
Value: 0.000
C out
Value: 2.0
M
in1
in2
in3
out
hold
out -1 Z in
C out
Value: -2.0
in2
in1 Σ out
HOLD
in out
hold
symbclk
C out
Value: 1.0
x1
x2
y
control
inputsw
inI
sym_rate
data
s_freq
RAISED COSINE
FILTER
y
tap length
tap coef
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]

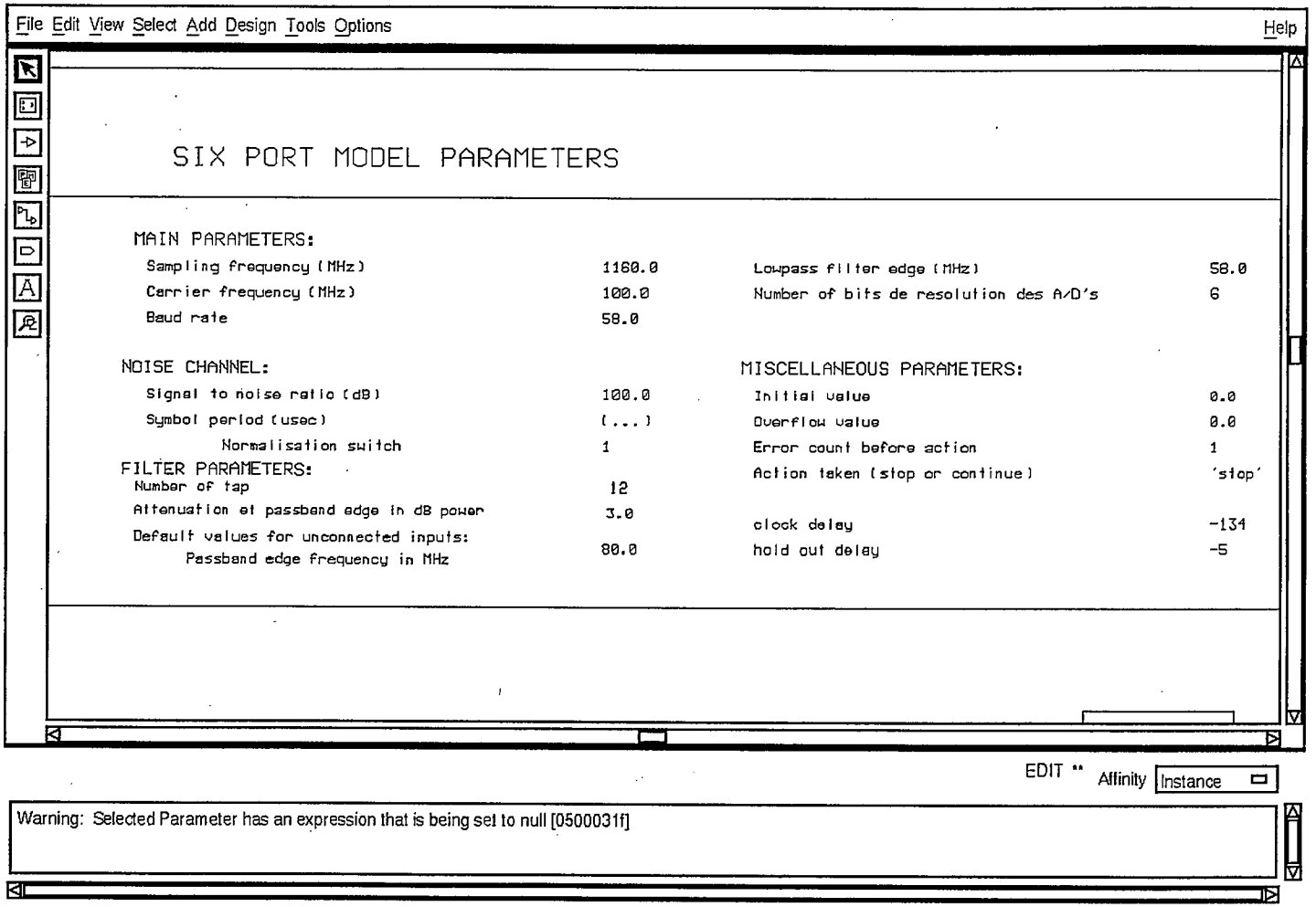

File Edit View Select Add Design Tools Options
Help
Carrier frequency
COMPLEX
TONE
carry
MAKE
real
imag
COMPLEX
outpak
COMPLEX BUTTERWORTH
LOWPASS IIR FILTER
modul
channel
in
out
sixport2
RF_in
hold
IMPULSE
TRAIN
baudRt
RAISED COSINE
FILTER
TRANSMISSION CHANNEL
SIX PORT
DIODE
LOW PASS FIL
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]


File Edit View Select Add Design Tools Options
Help
Input Switch
RAISED COSINE FILTER
a2d_cond
beta1
beta2
B1
B2
LOW PASS FILTER
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]


File Edit View Select Add Design Tools Options
Help
Input Switch
beta1
beta2
B1
B2
Number of bits 8
a2d_cond
Parametres analogiques
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]


File Edit View Select Add Design Tools Options
Help
[...]
Value: [...]
in1
in2
out
hold
in
out
hold
-0.5
Parametres analogiques
B1 = 1.00476022866647
B2 = 0.50357302167967
Beta1 = -0.00473767626698
Beta2 = 0.49168930686197
K2r = -0.08413952567075
K2i = -3.669122367044864e-09
K4r = -0.04196986973808
K4i = 0.08433954593537
D = 0.01419257908856
EDIT **
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]


File Edit View Select Add Design Tools Options
Help
of bits 8
s2d_cond
s2d_cond
hold
hold
K4i
K2i
K4r
K2r
Values (...)
Scalling factor
1/D
1/D
decision2
hold
DSP_sampling
MAKE
COMPLEX
EDIT
Affinity
Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]


File Edit View Select Add Design Tools Options
Help
SIX PORT MODEL PARAMETERS
MAIN PARAMETERS:
Sampling frequency (MHz) 1160.0
Carrier frequency (MHz) 100.0
Baud rate 58.0
Lowpass filter edge (MHz) 58.0
Number of bits de resolution des A/D's 6
NOISE CHANNEL:
Signal to noise ratio (dB) 100.0
Symbol period (usec) (...)
Normalisation switch 1
FILTER PARAMETERS:
Number of tap 12
Attenuation at passband edge in dB power 3.0
Default values for unconnected inputs:
Passband edge frequency in MHz 80.0
MISCELLANEOUS PARAMETERS:
Initial value 0.0
Overflow value 0.0
Error count before action 1
Action taken (stop or continue) 'stop'
clock delay -134
hold out delay -5
EDIT ** Affinity Instance
Warning: Selected Parameter has an expression that is being set to null [0500031f]

# Annexe B

# Modélisation et simulations du récepteur homodyne basé sur les jonctions six ports

**Marc Bergeron ÉTS/LACIME**
**Le 1 avril 1996**

# Table des Matières


B1.Introduction ..... 3
B2.Simulation du six ports ..... 3
B2.1.Transmission d'un signal sinusoïdal ..... 3
B2.2.Système classique de communication à démodulation QPSK ..... 5
B2.3.Transmission d'un signal QPSK avec six ports ..... 6
B2.4.Essais sur la quantification ..... 9
B2.5.Ajout d'interférence ..... 10
B2.6.Nouveaux paramètres du six ports ..... 12
B3.Réalisation du six ports ..... 15
B3.1.Réalisation analogique ..... 15
B3.2.Effet de la quantification ..... 18
B3.3.Suggestion de composantes ..... 19
B4.Conclusion ..... 19

# B1. Introduction

Ce document présente les résultats préliminaires de l'étude du récepteur homodyne basé sur les jonctions à six ports. Les résultats de simulation sont obtenus à l'aide du logiciel SPW. Une série d'essais a été effectuée afin de valider le fonctionnement de la démodulation basée sur les jonctions six ports. La validité de ce type de démodulation se fait par récurence. Les essais effectués afin de valider la démodulation à l'aide de jonction à six ports sont les suivants:

- Démodulation d'un signal sinusoïdal, afin de vérifier le recouvrement du signal sinusoïdal, section B2.1;
- Vérifier un système de démodulation classique QPSK utilisant des filtres à cosinus élevé et ajouter un filtre passe-bas de Butterworth afin d'éliminer les fréquences images générées par le filtre à cosinus élevé, section B2.2;
- Simuler le système QPSK utilisant la démodulation à l'aide du six ports, optimiser le système à l'aide de filtre passe-bas de Butterworth, section B2.3;
- Simuler en réduisant le nombre de bits des convertisseurs analogique/numérique au récepteur, section B2.4;
- Ajouter de l'interférence au système et vérifier son comportement, section B2.5;
- Simuler le système avec de nouveaux paramètres des jonctions à six ports, section B2.6;
- Réalisation et simulation d'un modèle de six ports analogique, section B3.1;
- Simuler et mesurer l'effet de la quantification du modèle analogique, section B3.2 et B3.3.

Les différentes sections démontrent la validité de chaque essai énuméré plus haut.

# B2. Simulation du six ports

## B2.1 Transmission d'un signal sinusoïdal

Dans la première étape, on vérifie le comportement du récepteur homodyne. Cette première étape consiste à transmettre un signal de forme sinusoïdale dans un canal à bruit blanc gaussien et de mesurer le rapport signal à bruit à la sortie du récepteur. Voici le schéma bloc de la cette étape.

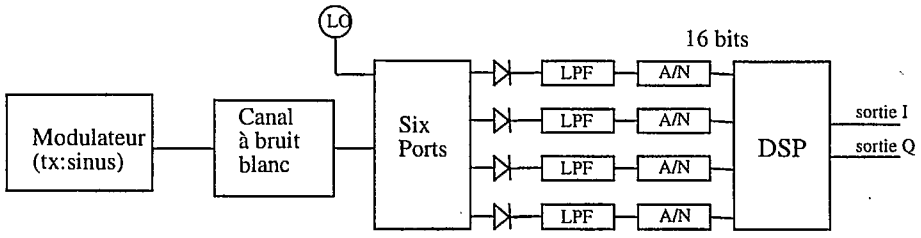



**Figure B2.1 : Système six ports utilisant les filtres passe-bas de Butterworth**

Deux types de simulations ont été effectuées pour vérifier le fonctionnement du six ports. Le premier type de simulation consiste à ajouter et à varier le niveau de bruit blanc gaussien à un signal en bande de base. Ce signal en bande de base est une onde sinusoïdale de 58 MHz. L'oscillateur local du six ports est donc ajusté à une valeur constante.

Le deuxième type de simulation est le même que le précédent, sauf que le signal transmis est une sinusoïde modulée. Le six ports nécessite donc un oscillateur local à la fréquence de la porteuse.

Dans les deux cas, la fréquence du signal est de 58 MHz et la fréquence d'échantillonnage est de 1000MHz. Dans le deuxième cas, une porteuse de 100MHz est rajoutée et la fréquence de l'oscillateur local du six ports est en phase et à cette même fréquence. On retrouve dans le six ports des filtres passe-bas de Butterworth d'ordre 8, dont la fréquence de coupure est de 80 MHz. Le signal à l'entrée est échantillonné à 1000MHz. À la sortie des filtres passe-bas, le signal est échantillonné et traité à 200MHz.

Les simulations consistent à vérifier et à calculer la puissance du signal reçu en injectant une certaine quantité de bruit à l'aide du canal à bruit blanc gaussien.

Voici les résultats obtenus lors des simulations :

**Tableau B1 : Résultats des simulations**

| | $SNR_{in}$ ($P_s/P_n$) | $P_{signal\ tx}$ | $P_{signal\ rx}$ | $SNR_{out}$ | Théorie démodulation cohérente $SNR_i$+10log(500/80) |
|---|---|---|---|---|---|
| Signal en bande de base | | | | | |
| | 2dB | 1.0 | 0.96952 | 9.81dB | 9.9588dB |
| | 6dB | 1.0 | 0.97935 | 13.47dB | 13.958dB |
| | 10dB | 1.0 | 0.981236 | 17.1dB | 17.958dB |
| Signal modulé | | | | | |
| | 2dB | 1.0 | 0.97092 | 9.71dB | 9.9588dB |
| | 6dB | 1.0 | 0.96574 | 13.56dB | 13.958dB |
| | 10dB | 1.0 | 0.97030 | 16.996dB | 17.958dB |

Théoriquement avec un récepteur classique, le bruit qui était présent sur 500MHz est filtré à 80MHz (si on avait un filtre passe-bas idéal). Ainsi, le rapport signal à bruit devrait s'améliorer de 10log(500/80) = 7.958dB. En effet, nous observons que la différence entre les résultats théoriques et pratiques provient du fait que les filtres ne sont pas idéaux.

## B2.2 Système classique de communication à démodulation QPSK

La deuxième étape consiste à vérifier le comportement des filtres à cosinus élevé, afin de les utiliser dans le système six ports. Voici le schéma bloc du système simulé:

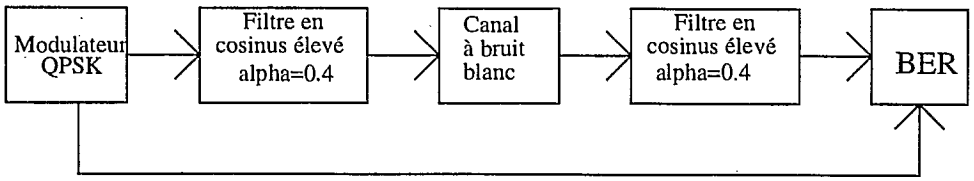



**Figure B2.2 : Modulateur QPSK classique utilisant des filtres à cosinus élevé**

Le modulateur QPSK classique de la figure B2.2 a un taux de transmission de 58 M sym/s. Le canal à bruit blanc gaussien est le même que précedemment. Le rôle de ces simulations consiste à comparer les taux d'erreurs de transmission des bits d'un démodulateur QPSK théorique typique, à celui d'un démodulateur QPSK utilisant des filtres à cosinus élevé.

Le taux d'échantillonage des filtres (incluant le filtre à cosinus élevé) au modulateur QPSK est de 116M éch/s et sur le canal, la fréquence d'échantillonnage est de 1160M éch/s. Le taux d'échantillonage du module de décision est à 58MHz. À ce taux, le moment d'échantillonnage doit être pris au moment opportun, ce qui implique que ce moment d'échantillonnage doit être fixé à l'aide du diagramme de l'oeil du signal à la sortie des filtres en cosinus élevé et de l'horloge.

Après analyse des résultats des simulations du tableau B2, on remarque une certaine dégradation du signal causée par l'utilisation de filtres en cosinus élevé sous-échantillonnés à l'émétteur. Il faudra enlever les images des signaux en bande de base à n*(116MHz) à l'aide de filtre. Afin d'enlever les images des signaux en bande de base, on ajoute un filtre passe-bas de Butterworth à la sortie du modulateur QPSK, comme le démontre la figure B2.3.

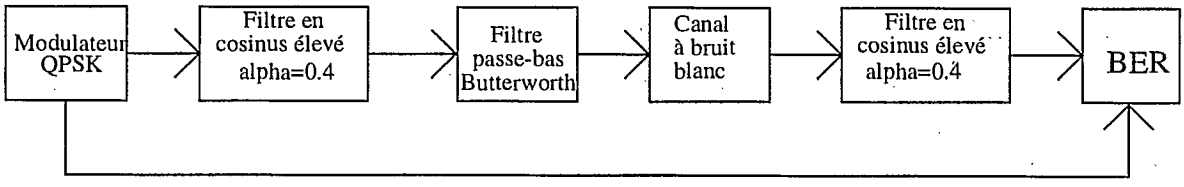



**Figure B2.3 : Modulateur QPSK classique utilisant des filtres à cosinus élevé et Butterworth**

Nous avons effectués les mêmes simulations et avec les mêmes paramètres que dans le système de la figure B2.2. Par contre, on remarque que dans la figure B2.3, nous avons ajouté un filtre passe-bas de Butterworth à la sortie du filtre à cosinus élevé et ce, afin d'éliminer les images des signaux

en bande de base.

**Tableau B2 : Résultats des simulations**

| $E_s/N_o$(dB) | $BER_{pratique.}$ (#err/#bits_tx) de la fig.B2.2 | $BER_{pratique.}$ (#err/#bits_tx) de la fig.B2.3 | $BER_{théorique}$ |
|---|---|---|---|
| 6 | 0.0344763 (6485/188100) | 0.0278256 (5234/188100) | 0.02300713 |
| 7 | 0.0196279 (3692/188100) | 0.0161085 (3030/188100) | 0.01250078 |
| 8 | 0.011547 (2172/188100) | 0.00773869 (1605/378100) | 0.00595388 |
| 9 | 0.00532663 (2014/378100) | 0.00296482 (1121/378100) | 0.00238835 |
| 10 | 0.00170854 (2646/378100) | 0.00125628 (475/378100) | 0.00077274 |
| 11 | 0.000603015 (228/378100) | 0.000400802 (380/948100) | 0.00019095 |
| 12 | 0.000220441 (209/948100) | 8.2969e-05 (114/1374000) | 3.3643e-05 |

Comme nous le constatons, en comparant les résultats du BER pratique de la figure B2.2 et B2.3, l'ajout du filtre passe-bas de Butterworth améliore le taux d'erreur de transmission des bits (BER).

## B2.3 Transmission d'un signal QPSK avec six ports

La troixième étape consiste à utiliser les filtres en cosinus élevés dans le démodulateur homodyne utilisant le six ports. Ainsi, nous simulons le même système qu'en B2.2 mais, avec une démodulation utilisant les jonctions à six ports. Voici le schéma bloc du système:

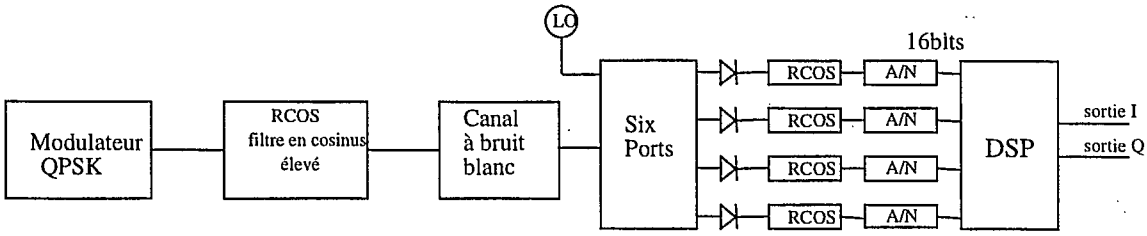



**Figure B2.4 : Système six ports utilisant les filtres a cosinus élevés et Butterworth**

Le taux de transmission du modulateur QPSK est de 58 M sym/s. Ce modulateur, ainsi que les filtres en cosinus élevé qui le suivent sont échantillonés à 116M éch/s.

Le signal à la sortie des filtres est échantillonné et est traité à 58M éch/s. Ceci implique que le DSP dans le module six ports fonctionne à 58M éch/s. Pour les mêmes raisons que dans l'étape précédente, l'instant d'échantillonage doit être fixé à l'aide du diagramme de l'oeil. Les simulations effectuées ont été faites avec des porteuses de 100 et 200MHz.

L'analyse des résultats du tableau B3, démontre qu'une dégradation est causée par l'effet du filtre à cosinus élevé qui est situé à la sortie du modulateur QPSK.

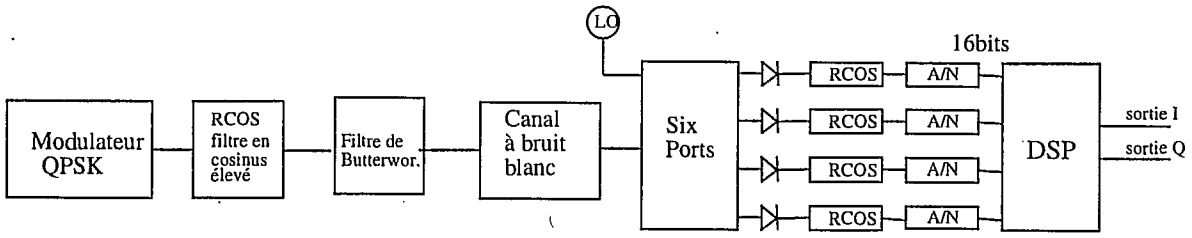



**Figure B2.5 : Système six ports utilisant les filtres à cosinus élevés et Butterworth**

:

**Tableau B3 : Résultats de simulation**

| $E_s/N_0$(dB) | $BER_{pratique.}$ de la fig.B2.4 (#err/#bits_tx) $F_c$=100MHZ | $BER_{pratique.}$ de la fig.B2.4 (#err/#bits_tx) $F_c$=200MHz | $BER_{pratique.}$ de la fig.B2.5 (#err/#bits_tx) $F_c$=100MHZ | $BER_{théorique}$ |
|---|---|---|---|---|
| 6 | 0.0351515 (6612/188100) | 0.037193 (6996/188100) | 0.0277774 (5225/188100) | 0.02300713 |
| 7 | 0.0150505 (2831/188100) | 0.0143434 (2698/188100) | 0.0135334 (2546/188100) | 0.01250078 |
| 8 | 0.00787879 (1482/188100) | 0.0086867 (1634/188100) | 0.00605638 (11495/1.898e6) | 0.00595388 |
| 9 | 0.00286432 (1083/378100) | 0.00386935 (1463/378100) | 0.00240253 (4560/1.898e6) | 0.00238835 |
| 10 | 0.00110553 (418/378100) | 0.00140281 (530/378100) | 0.00081085 (1539/1.898e6) | 0.00077274 |
| 11 | 0.00035175 (133/378100) | 0.00040201 (152/378100) | 0.00025026 (476/1.898e6) | 0.00019095 |
| 12 | 0.0001002 (95/948100) | 0.00010612 (101/948100) | 5.00263e-5 (190/3.789e6) | 3.3643e-05 |

L'ajout du filtre passe-bas de Butterworth, à la figure B2.5, améliore considérablement le comportement du circuit. Avec l'ajout de ce dernier, nous pouvons conclure que le système est comparable à un démodulateur simple QPSK. De plus, la variation de la fréquence de la porteuse ne change en rien le comportement du circuit.

À la figures B2.6, nous pouvons observer les résultats de performances comparatifs avec et sans

utilisation de six ports sans filtre de Butterworth. Nous observons, à la figure B2.7, les résultats de performances comparatifs avec et sans utilisation de six ports, avec filtre de Butterworth. Dans les deux cas la fréquence de la porteuse est de 100MHz.

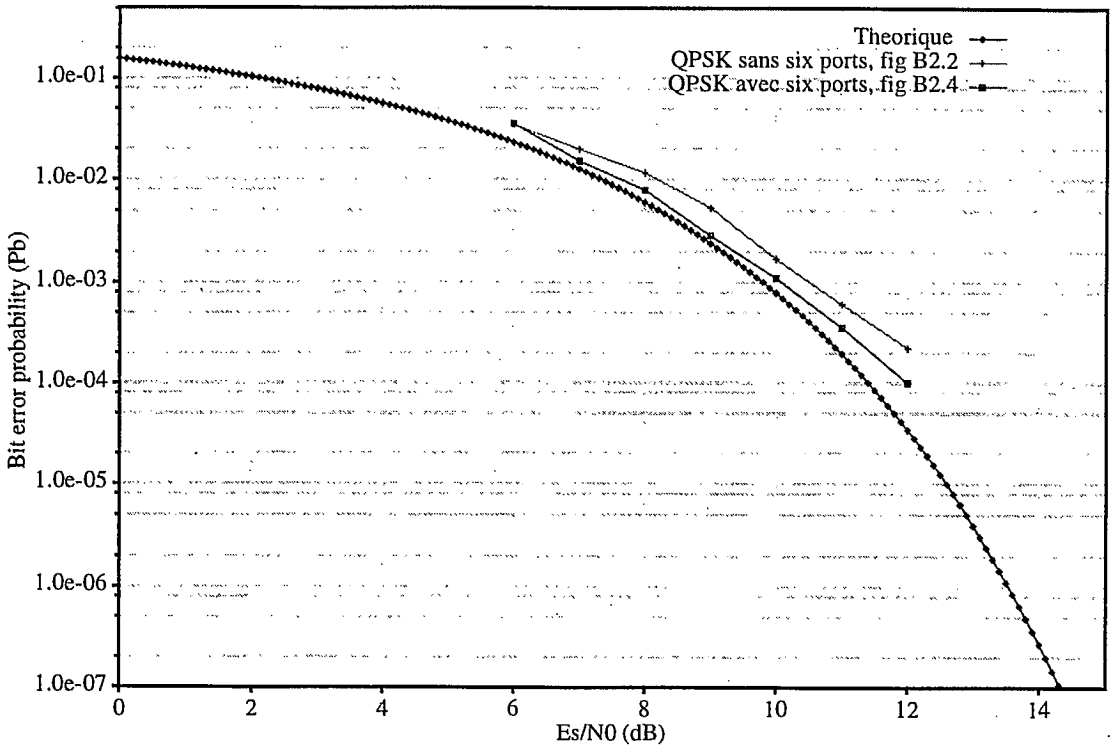



**Figure B2.6 : Comparaison des systèmes sans filtre de Butterworth**

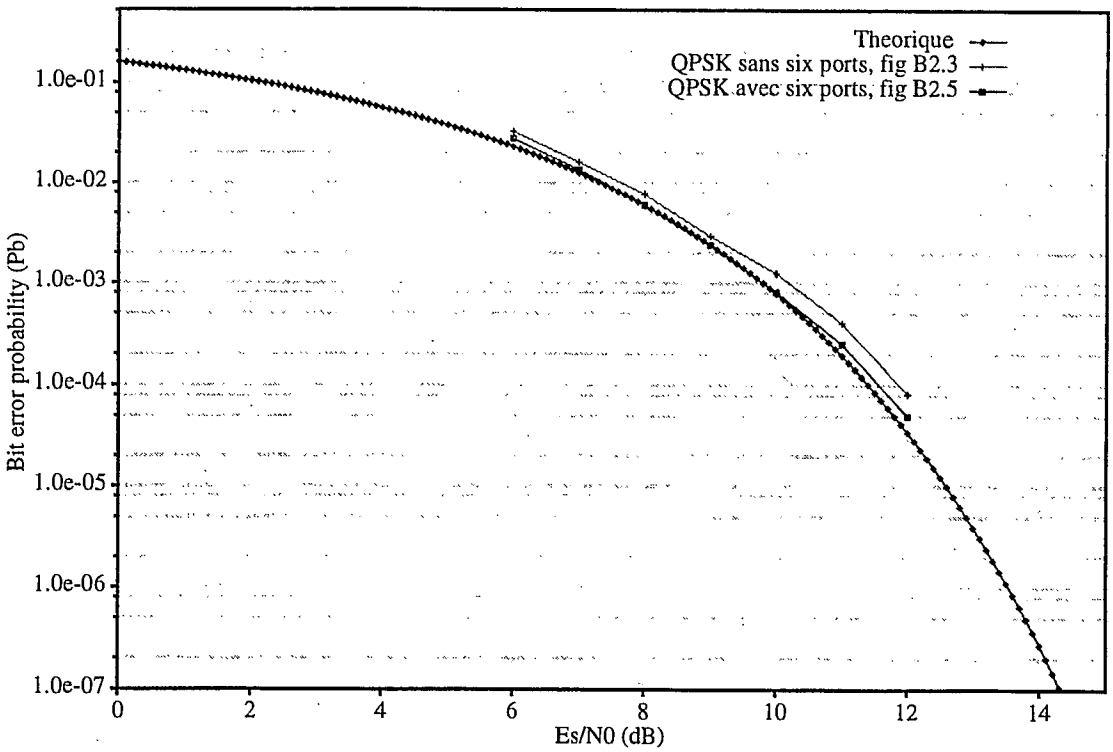



**Figure B2.7 : Comparaison des systèmes avec filtre de Butterworth**

## B2.4 Essais sur la quantification

Utilisant le système optimal montré à la figure B2.5, nous avons diminué le nombre de bits de quantification aux convertisseurs analogique/numérique A/N. Ayant fixé le rapport signal à bruit Eb/No = 11 dB, nous avons varié le nombre de bits de quantification de 16, 8, 6, 5, 4 et 3 bits, et, mesuré le taux d'erreur de transmission des bits (BER). Le tableau B4, nous donne les résultats des différentes simulations effectuées:

**Tableau B4 : Variation sur la quantification**

| Nombre de bits de quantification | $BER_{pratique}$ (#err/#bits_tx) Es/N0 = 11dB |
|---|---|
| 16 | 0.000250263 (475/1.898e9) |
| 8 | 0.000250263 (475/1.898e6) |
| 6 | 0.000300316 (570/1.898e6) |

**Tableau B4 : Variation sur la quantification**

| Nombre de bits de quantification | $BER_{pratique}$ (#err/#bits_tx) Es/N0 = 11dB |
|---|---|
| 5 | 0.000480506 (912/1.898e6) |
| 4 | 0.00141149 (2679/1.898e6) |
| 3 | 0.0243056 (43132/1.898e6) |

Afin de maintenir un taux d'erreur de transmission acceptable, il serait préférable de conserver un minimum de 5 bits de quantification.

## B2.5 Ajout d'interférence

Le système de la figure B2.9 a pour but d'injecter une interférence au signal modulé. Cette interférence est espacé de 90 MHz, de même modulation, de même débit et à une puissance égale au signal principal, voir la figure B2.8.

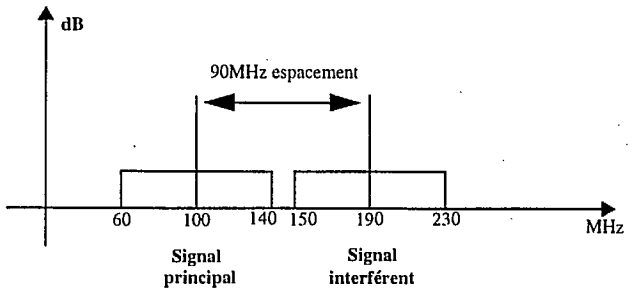



**Figure B2.8 : Vue spectrale de l'ajout du signal interférent**

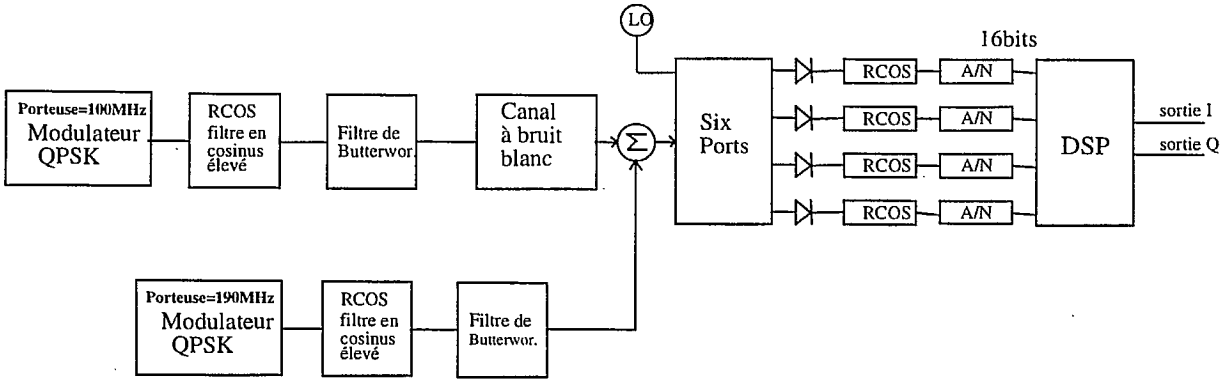



**Figure B2.9 : Système six ports optimal avec ajout d'interférence**

**Tableau B5 : Système six ports avec interférence du canal adjascent**

| $E_s/N_o$(dB) | $BER_{pratique}$ de la fig.B2.9 $F_c$=100MHZ (#err/#bits_tx) avec int. du canal adj. | $BER_{pratique.}$ de la fig.B2.5 $F_c$=100MHZ (#err/#bits_tx) sans int. du canal adj. |
|---|---|---|
| 6 | 0.046545 (17860/378000) | 0.0277774 (5225/188100) |
| 7 | 0.0170899 (6460/378000) | 0.0135334 (2546/188100) |
| 8 | 0.00721519 (6840/948000) | 0.00605638 (11495/1.898e6) |
| 9 | 0.00285304 (3572/1.25e6) | 0.00240253 (4560/1.898e6) |
| 10 | 0.00091482 (1729/1.898e6) | 0.00081085 (1539/1.898e6) |
| 11 | 0.00026069 (988/3.789e6) | 0.00025026 (476/1.898e6) |
| 12 | 5.00527e-05 (950/1.898e7) | 5.00263e-5 (190/3.789e6) |

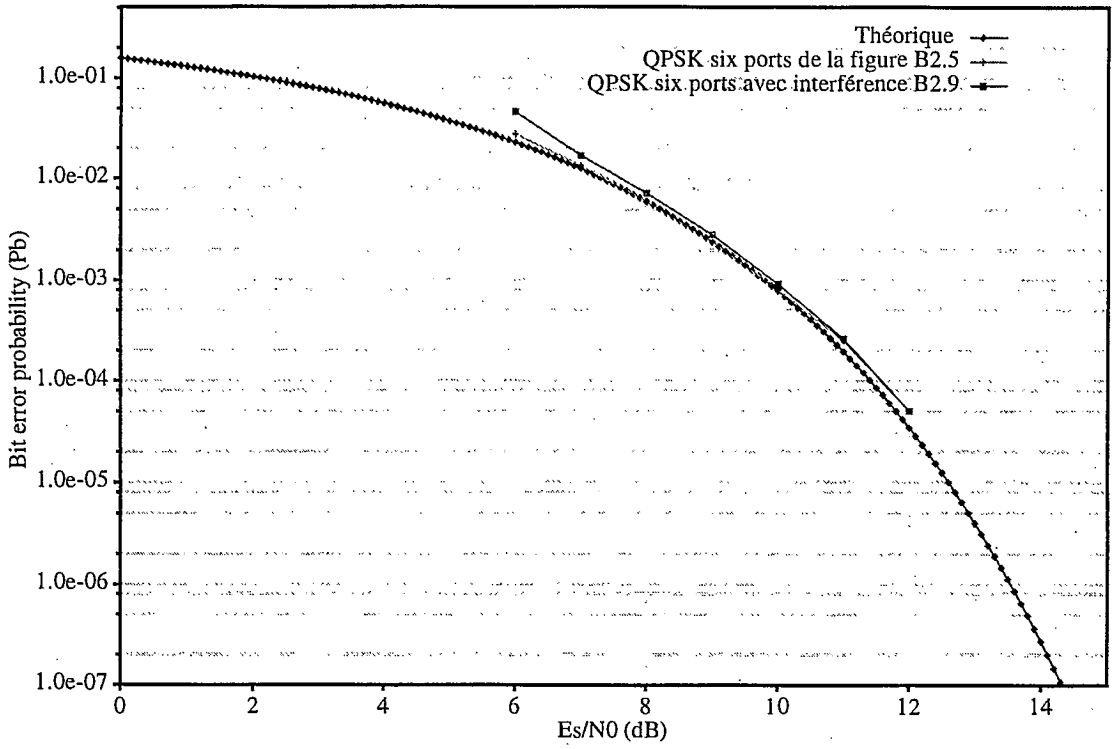



**Figure B2.10 : Comparaison du six ports avec et sans interférence**

Nous observons des résultats de performance comparatifs avec et sans interférences (comparaison entre les résultats obtenus de la figure B2.5 et de la figure B2.9). L'ajout de l'interférence augmente, de façon très négligeable, le taux d'erreur de transmission des bits (BER). Donc, nous pouvons conclure que le système se comporte de façon comparative à un système de démodulation QPSK classique.

## B2.6 Nouveaux paramètres du six ports

Ayant reçu une nouvelle série de paramètres des jonctions six ports, nous avons effectué une nouvelle série de simulations afin de confirmer la validité du simulateur. Les simulations consistent à utiliser les systèmes de la figure B2.5 et de la figure B2.9, et de comparer les résultats obtenus avec les paramètres initiaux et les nouveaux paramètres.

Voici le tableau comparatif des résultats:

**Tableau B6 : Comparaison avec de nouveaux paramètres du système six ports**

| $E_s/N_o$(dB) | $BER_{pratique.}$ de la fig.B2.5 **Paramètres initiaux** (#err/#bits_tx) $F_c$=100MHZ | $BER_{pratique.}$ de la fig.B2.5 **Nouveaux Paramètres** (#err/#bits_tx) $F_c$=100MHZ | $BER_{pratique}$ de la fig.B2.9 **Paramètres initiaux** (#err/#bits_tx) $F_c$=100MHZ | $BER_{pratique}$ de la fig.B2.9 **Nouveaux Paramètres** (#err/#bits_tx) $F_c$=100MHZ | $BER_{théorique}$ |
|---|---|---|---|---|---|
| 6 | 0.0277774 (5225/188100) | 0.0235238 (8892/378000) | 0.046545 (17860/378000) | 0.0266402 (10070/378000) | 0.02300713 |
| 7 | 0.0135334 (2546/188100) | 0.0135714 (5130/378000) | 0.0170899 (6460/378000) | 0.0143757 (5434/378000) | 0.01250078 |
| 8 | 0.00605638 (11495/1.898e6) | 0.00614647 (11666/1.898e6) | 0.00721519 (6840/948000) | 0.00707489 (6707/948000) | 0.00595388 |
| 9 | 0.00240253 (4560/1.898e6) | 0.00241254 (4579/1.898e6) | 0.00285304 (3572/1.25e6) | 0.00282487 (5339/1.898e6) | 0.00238835 |
| 10 | 0.00081085 (1539/1.898e6) | 0.00078082 (1482/1.898e6) | 0.00091482 (1729/1.898e6) | 0.00082717 (3135/3.789e6) | 0.00077274 |
| 11 | 0.00025026 (476/1.898e6) | 0.00022023 (836/3.789e6) | 0.00026069 (988/3.789e6) | 0.00025126 (969/3.789e6) | 0.00019095 |
| 12 | 5.00263e-5 (190/3.789e6) | 4.00425e-5 (152/3.789e6) | 5.00527e-05 (950/1.898e7) | 4.80506e-5 (912/1.898e7) | 3.3643e-05 |

Les résultats de simulation utilisant la nouvelle série de paramètres des jonctions à six ports confirme la validité du modèle du simulateur six ports.

À la figure B2.11 et B2.12, nous avons la comparaison des résultats des systèmes de la figure B2.5 et B2.9 entre les paramètres initiaux et les nouveaux paramètres du six ports. Il est à noter que nous obtenons les mêmes résultats avec les nouveaux paramètres.

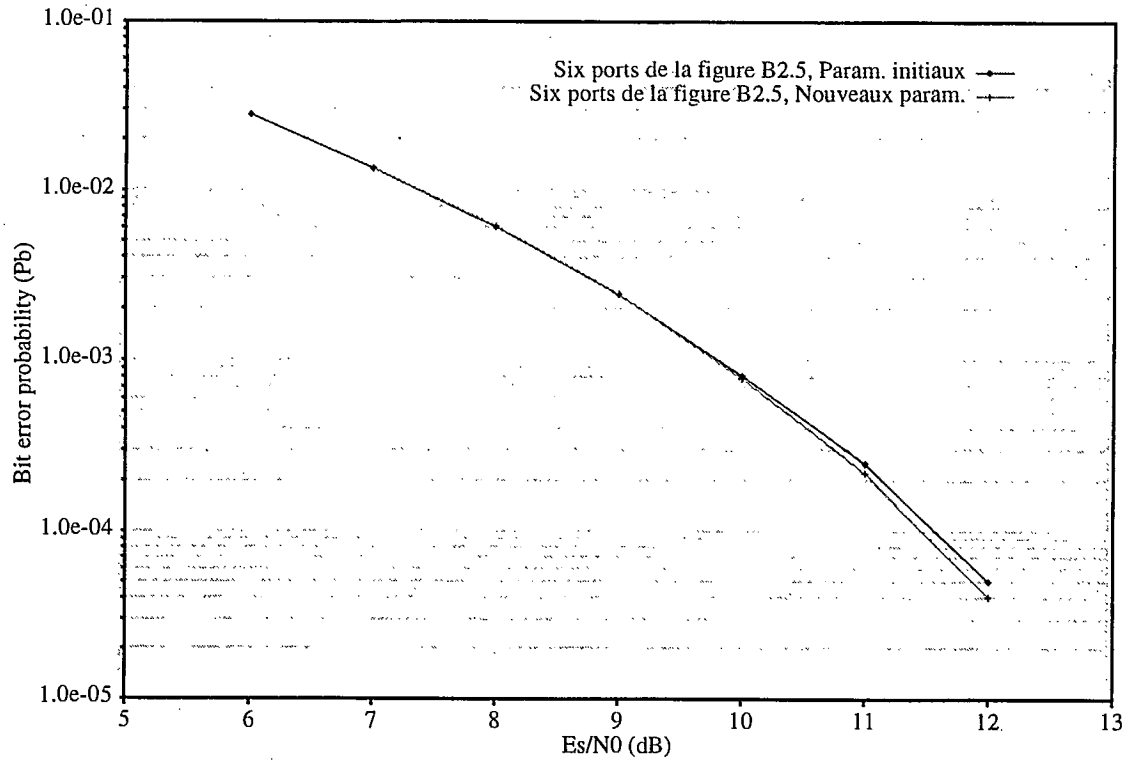



**Figure B2.11 : Comparaison des paramètres du système de la figure B2.5**

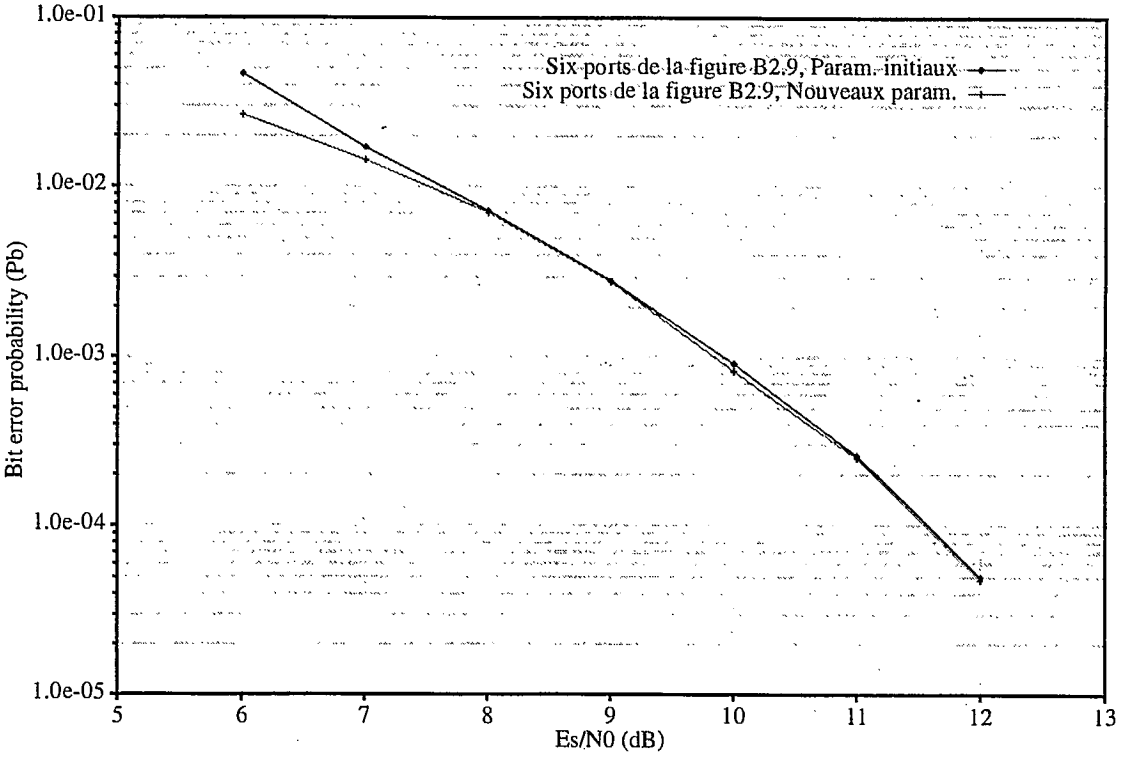



**Figure B2.12 : Comparaison des paramètres du système de la figure B2.9**

## B3. Réalisation du six ports

### B3.1 Réalisation analogique

La figure B3.1 montre une réalisation analogique proposée du six ports. Cette réalisation est faite à l'aide des équations proposées[1] pour la réalisation de la démodulation cohérente à l'aide de jonctions six ports.

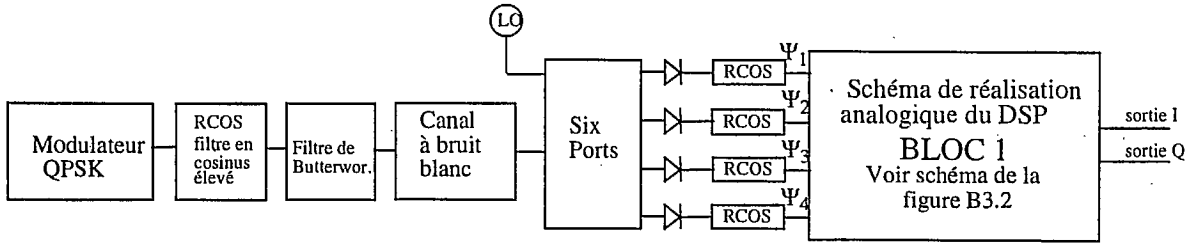



**Figure B3.1 : Système six ports utilisant les équations du DSP**

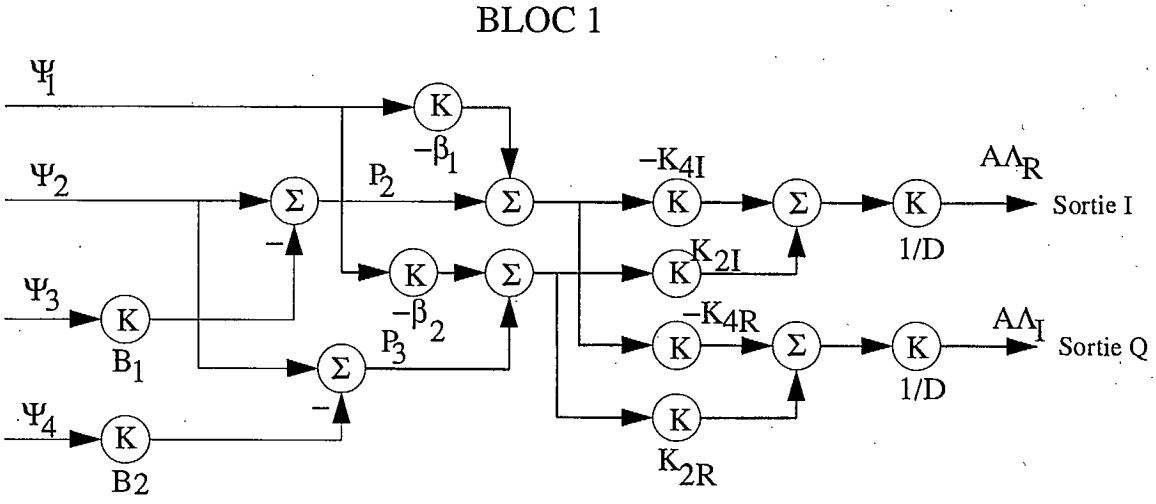



**Figure B3.2: Schéma de réalisation des équations du DSP**

On retrouve, à la figure B3.2, le circuit réalisant les équations représentant le DSP. Les simulations démontrent que le comportement du circuit est quasi-théorique, validant ainsi le fonctionnement de celui-ci.

1. Démodulation cohérente à l'aide du six ports, équations du DSP, Annexe C

**Tableau B7 : Résultats des simulations de la figure B3.1**

| $E_s/N_o$(dB) | $BER_{pratique.}$ (#err/#bits_tx) de la fig.B3.1 | $BER_{théorique}$ |
|---|---|---|
| 6 | 0.0236489 (4446/18800) | 0.02300713 |
| 7 | 0.0134206 (5073/378000) | 0.01250078 |
| 8 | 0.00605638 (11495/1.898e6) | 0.00595388 |
| 9 | 0.00240253 (4560/1.898e6) | 0.00238835 |
| 10 | 0.000810854 (1539/1.898e6) | 0.00077274 |
| 11 | 0.000250263 (779/3.789e6) | 0.00019095 |
| 12 | 4.80506e-05 (456/9.49e6) | 3.3643e-05 |

Les résultats obtenus, et présentés au tableau B7, sont comparables aux résultats théoriques. N'ayant aucun convertisseur analogique/numérique, nous n'obtenons aucune dégradation due à la quantification. Donc, le circuit se comporte de façon pratiquement théorique.

Avec l'ajout de convertisseurs analogique/numérique de 8 bits, voir la figure B3.3, les résultats de simulations présentés au tableau B8, concordent avec le résultats obtenus auparavant.

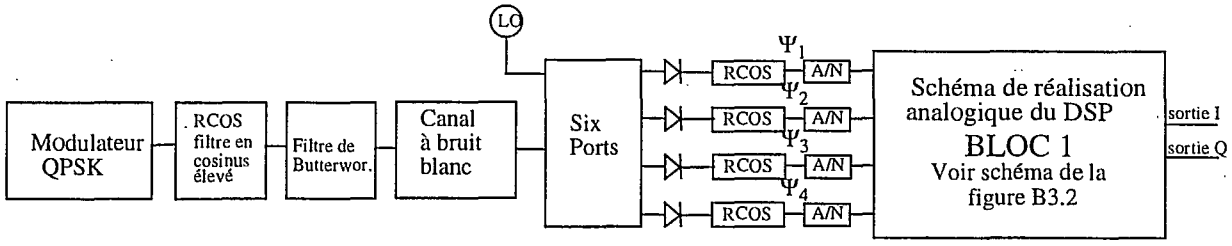



**Figure B3.3 : Système six ports utilisant les équations du DSP, avec convertisseur A/N**

**Tableau B8 : Résultats des simulations de la figure B3.3**

| $E_s/N_o$(dB) | $BER_{pratique.}$ (#err/#bits_tx) de la fig.B3.3 | $BER_{théorique}$ |
|---|---|---|
| 6 | 0.0273439 (10336/378000) | 0.02300713 |
| 7 | 0.0132698 (5016/378000) | 0.01250078 |
| 8 | 0.00610643 (11590/1.898e6) | 0.00595388 |
| 9 | 0.00242255 (4598/1.898e6) | 0.00238835 |
| 10 | 0.000840885 (1596/1.898e6) | 0.00077274 |
| 11 | 0.0002210554 (798/3.789e6) | 0.00019095 |
| 12 | 4.20443e-5 (399/9.49e6) | 3.3643e-05 |

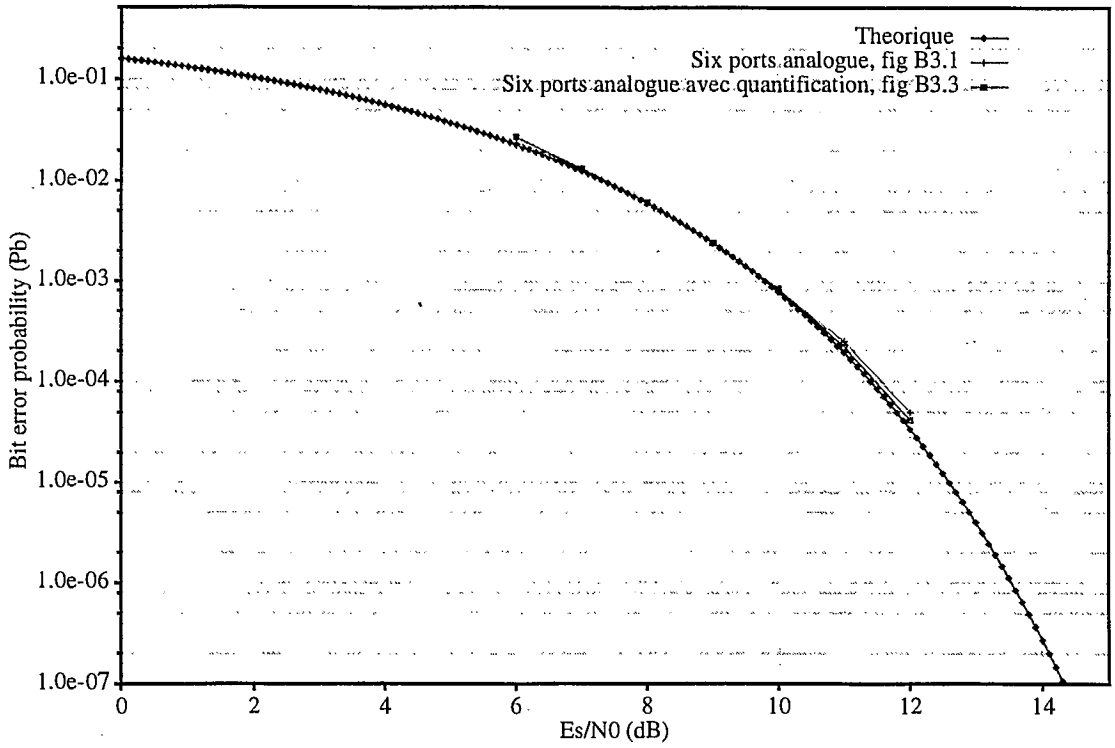



**Figure B3.4 : Comparaison du six ports analogue avec convertisseur A/N**

## B3.2 Effet de la quantification

Afin de vérifier l'effet de la quantification, nous avons procédé de la façon suivante (voir la figure B3.5): Sur l'entrée Q, nous retrouvons des bits aléatoires et sur l'entrée I, nous avons généré une rampe variant de -2 à 2. En comparant les rampes d'entrée et de sortie, nous avons calculé le bruit de quantification engendré par les convertisseurs A/N.

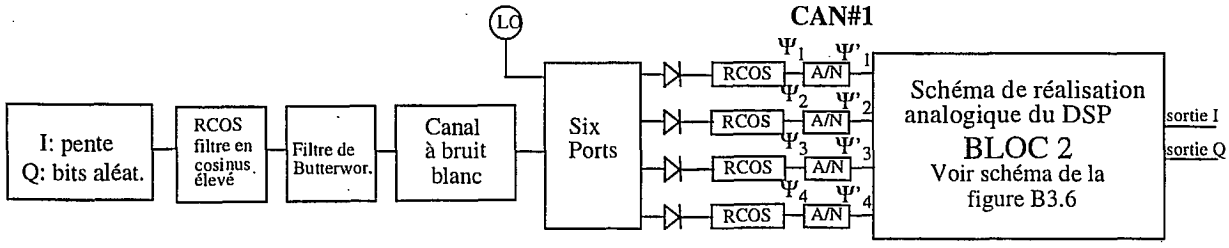



**Figure B3.5 : Système six ports utilisant les équations du DSP, avec convertisseur A/N**

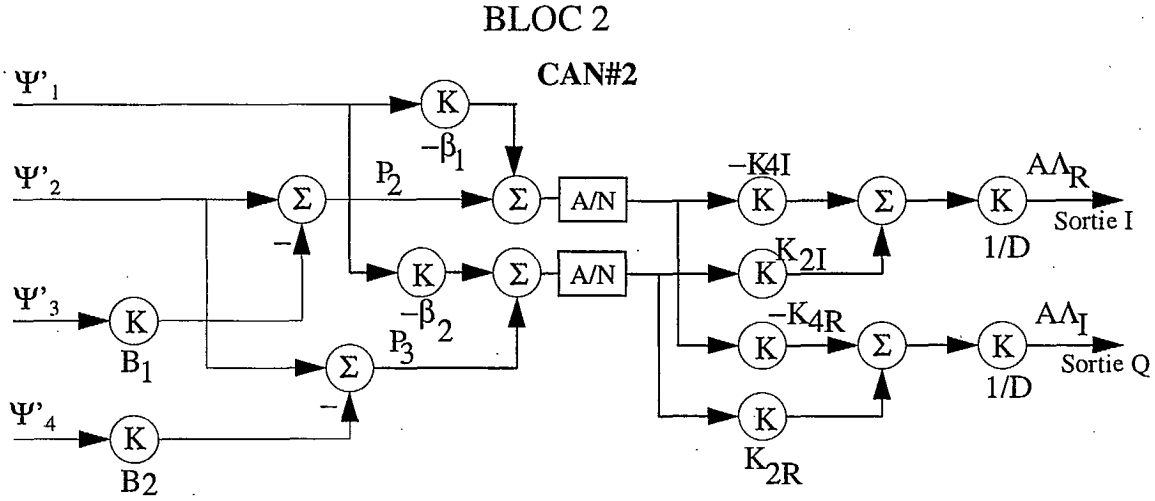



**Figure B3.6 : Schéma de réalisation des équations du DSP avec convertisseur A/N**

Plusieurs simulations ont été effuctuées en variant le nombre de bits de quantifications des convertisseurs analogique/numériques CAN#1 et CAN#2, voir le tableau B9.

**Tableau B9 : Mesure du bruit de quantification**

| Nombre de bits au **CAN#1** (fig B3.5) | Nombre de bits au **CAN#2** (fig B3.6) | $SNRQ_{dB}$ |
|---|---|---|
| 10 | 10 | 39.6dB |

**Tableau B9 : Mesure du bruit de quantification**

| Nombre de bits au **CAN#1** (fig B3.5) | Nombre de bits au **CAN#2** (fig B3.6) | $SNRQ_{dB}$ |
|---|---|---|
| 10 | 8 | 37.5dB |
| 8 | 10 | 38.2dB |
| 8 | 8 | 34.8dB |
| 8 | 6 | 23.9dB |
| 6 | 8 | 31.1dB |
| 6 | 6 | 23.0dB |

Avec ces résultats, nous remarquons l'importance du nombre de bits de quantification du convertisseur analogique/numériques CAN#2. Ce dernier doit, pour obtenir des résultats probant, avoir au minimum 8 bits de quantification.

## B3.3 Suggestion de composantes

Afin de réaliser l'ensemble du système, voici quelques suggestions de composantes:
Suggestion de mémoire SRAM:

- EPLD, Altera, EPM7032, 36 I/O, 125 MHz
- Cypress CY7C1009 (128Kx8), Taa=12ns
- Cypress CY7C1021 (64Kx16), Taa=12ns

Suggestion de convertisseurs numérique/analogiques:

- Analog Devices AD9002, High speed8 bits, 150MPS
- Analog Devices AD9012, High speed8 bits, 100MPS
- Maxim MAX100, 8 bits, 250MPS
- Harris semiconductor, HI386, CXA1386, 8 bits, 75MPS
- Harris semiconductor, HI396, CXA1396, 8 bits, 125MPS
- Harris semiconductor, HI5714, 8 bits, 75MPS

# B4. Conclusion

Dans ce document, nous avons développé un modèle du récepteur homodyne basé sur les jonctions à six ports. Ce modèle a été validé et des simulations ont été faites afin de calculer les performances

du modèle (Es/No vs Pb).

Les essais qui ont été effectués sont les suivants:

1. Démoduler un signal sinusoïdal, vérifient le recouvrement d'un signal;
2. Vérifier un système de démodulation classique QPSK utilisant des filtres à cosinus élevé et ajouter un filtre-bas de Butterworth afin d'éliminer les fréquences images généré par le filtre à cosinus élevé;
3. Simuler le système QPSK utilisant la démodulation à l'aide du six ports en optimisant le système à l'aide de filtre passe-bas de Butterworth;
4. Diminuer le nombre de bits des convertisseurs analogique/numériques au récepteur;
5. Ajouter de l'interférence au système six ports et vérifier le comportement de celui-ci;
6. Simuler le système avec de nouveaux paramètres de la jonction à six ports et finalement;
7. Proposer une réalisation analogique du six ports à l'aide des équations du DSP;
8. Simuler la réalisation analogique et mesurer l'effet de la quantification.

Tout porte à croire que la démodulation à l'aide du six ports donne des résultats de performances robustes et aussi bons qu'un démodulateur hétérodyne classique. Notons toutefois que l'oscillateur local au six ports était parfaitement en phase avec le signal reçu.

# Annexe C

# Démodulation cohérente à l'aide du six-ports

# Équations du DSP

**Christian Cardinal ÉTS/LACIME**
**Le 1 avril 1996**

# Table des matières

C1. Introduction . . . . . 1
C2. Opérations mathématiques associées au six-ports . . . . . 1
C3 Développements des équations du DSP . . . . . 3

# C1. Introduction

Dans ce document, on propose des équations du DSP pour effectuer une démodulation cohérente à l'aide d'une jonction six-ports. Les développements de ces équations y seront présentés. On cherche essentiellement à vérifier que les termes non-linéaires filtrés peuvent être éliminés par des combinaisons linéaires des signaux disponibles. En utilisant d'autres transformations linéaires des signaux disponibles, on cherche à déterminer les composantes en phase et en quadrature du signal en bande de base.

# C2. Opérations mathématiques associées au six-ports

Le six-ports fournit quatre combinaisons linéaires complexes des signaux aux entrées. Par hypothèse, grâce à la calibration, nous supposerons que ces combinaisons linéaires sont connues. Par la suite, quatre diodes fournissent des signaux proportionnels à la puissance instantanée de ces combinaisons. Ces signaux sont ensuite filtrés et échantillonnés. La figure suivante montre un schéma de principe du démodulateur.

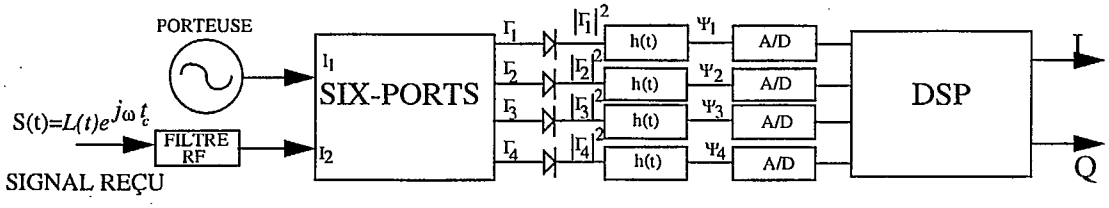



Figure C1. Schéma du principe du démodulateur

Le signal à démoduler est appliqué à l'entrée $I_2$ et a la forme:

$$L(t)\,e^{j\omega_c t} = (I(t) + jQ(t))\,e^{j\omega_c t} + \left(n_c(t) + jn_s(t)\right)e^{j\omega_c t} \qquad \text{(C2.1)}$$

où $I(t)$ et $Q(t)$ représentent les modulations en phase et en quadrature et $n_c(t)$ et $n_s(t)$ sont des signaux de bruits où d'interférences sur une largeur de bande quelconque. Pour accomplir une démodulation cohérente, il faut retrouver:

$$L(t) \otimes h(t) = \left[I(t) + jQ(t) + n_c(t) + jn_s(t)\right] \otimes h(t) = \Lambda(t) \qquad \text{(C2.2)}$$

où $\otimes$ représente une convolution

Si on peut retrouver $\Lambda(t)$, il est alors possible de générer une porteuse en phase avec le signal reçu et ce, à l'aide des techniques habituelles de récupération de la porteuse. Ainsi, on fixe

cette porteuse à $Ae^{j\omega ct}$ où $A$ est l'amplitude de la porteuse. Le six-ports fournit quatre combinaisons linéaires des signaux présents aux entrées:

$$\Gamma_i(t) = \alpha_{i,1} A e^{j\omega_c t} + \alpha_{i,2} L(t)\, e^{j\omega_c t} \tag{C2.3}$$

où les $\alpha_{i,j}$, $i$=1,2,3,4 et $j$=1,2 sont les coefficients du six-ports déterminés par calibration. Pour que le démodulateur fonctionne, ces équations ne doivent pas être co-linéaires. Les signaux à la sortie des diodes sont représentés par les relations suivantes:

$$\left|\Gamma_i(t)\right|^2 = \left|\alpha_{i,1}\right|^2 (A^2 + A a_i L(t) + A a_i^* L^*(t) + \left|a_i\right|^2 |L(t)|^2) \tag{C2.4}$$

où $\quad a_i = \dfrac{\alpha_{i,2}}{\alpha_{i,1}}$

Après l'opération de filtrage avec un filtre de réponse impulsionnelle $h(t)$, les signaux obtenus s'écrivent comme suit:

$$\Psi_i(t) = |\Gamma_i(t)|^2 \otimes h(t) = \left|\alpha_{i,1}\right|^2 \left( A^2 + A a_i \Lambda(t) + A a_i^* \Lambda^*(t) + |a_i|^2 (|L(t)|^2 \otimes h(t)) \right) \tag{C2.5}$$

En observant les valeurs des coefficients de la jonction du six-ports, on remarque que le module au carré de $a_1$ est de l'ordre de $10^{-32}$ et peut donc être négligé. Dans ce cas, on peut écrire:

$$\Psi_1(t) \cong \left|\alpha_{1,1}\right|^2 A^2 \tag{C2.6}$$

À partir de combinaisons linéaires de ces quatres équations, on élimine les termes non-linéaires après filtrage:

$$\begin{aligned} P_2(t) &= \Psi_2(t) - B_1 \Psi_3(t) \\ P_3(t) &= \Psi_2(t) - B_2 \Psi_4(t) \end{aligned} \tag{C2.7}$$

où $B_1 = \dfrac{\left|\alpha_{2,1}\right|^2 \left|a_2\right|^2}{\left|\alpha_{3,1}\right|^2 \left|a_3\right|^2}$, et $B_2 = \dfrac{\left|\alpha_{2,1}\right|^2 \left|a_2\right|^2}{\left|\alpha_{4,1}\right|^2 \left|a_4\right|^2}$.

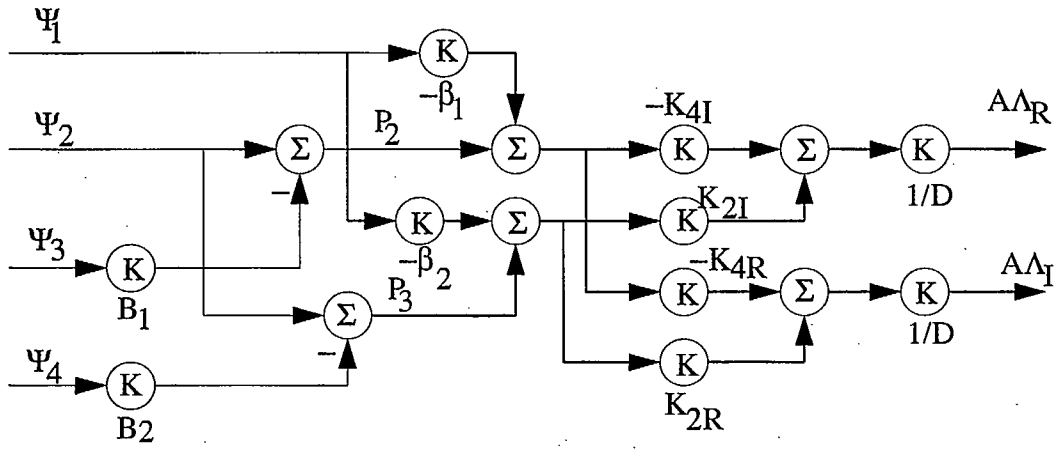
Par la suite, il suffit d'enlever les termes constants ($A^2$) et de résoudre le système d'équations fourni par (C2.7) pour obtenir:

$$A\Lambda_R(t) = \frac{-\left(P_2(t) - \beta_1 \Psi_1(t)\right) K_{4I} + \left(P_3(t) - \beta_2 \Psi_1(t)\right) (K_{2I})}{D} \tag{C2.8}$$

$$A\Lambda_I(t) = \frac{-\left(P_2(t) - \beta_1 \Psi_1(t)\right) K_{4R} + \left(P_3(t) - \beta_2 \Psi_1(t)\right) (K_{2R})}{D}$$

où les termes $K_{4I}$, $K_{2I}$, $K_{4R}$, $K_{2R}$,D, $\beta_1$ et $\beta_2$ sont des constantes pouvant être déterminées à partir des coefficients du six-ports. Le développement de cette équation est donné à la section C3.

La figure suivante montre un circuit réalisant ces équations. On retrouve donc à la sortie de ce circuit, les signaux en phase et en quadrature, I et Q, filtrés à l'aide de filtres ayant des réponses impulsionnelles $h(t)$. Notons que les signaux résultants correspondent aux signaux I et Q multipliés par l'amplitude $A$ de la porteuse. Toutefois, il est facile de retrouver les vrais amplitudes des signaux I et Q reçus simplement en divisant par la racine carré de l'expression donnée par l'équation (C3.6) en annexe. Ces équations ont été développées en supposant que l'approximation donnée à l'équation (C3.6) est valide.




## C3. Développement des équations du DSP

Le développement mathématique obtenu en utilisant l'équation (C2.5) dans l'équation (C2.7) donne:

$$\begin{aligned} P_2(t) &= K_1 A^2 + K_2 A\Lambda(t) + K^*_2 A\Lambda^*(t) \\ &= K_1 A^2 + 2K_{2R} A\Lambda_R(t) - 2K_{2I} A\Lambda_I(t) \end{aligned} \qquad \text{(C3.1)}$$

où on définit:

$$K_{2R} = \mathrm{Re}\{K_2\},\ K_{2I} = \mathrm{Im}\{K_2\}$$

$$\Lambda_R(t) = \mathrm{Re}\{\Lambda(t)\},\ \Lambda_I = \mathrm{Im}\{\Lambda(t)\}$$

et $K_1 = |\alpha_{2,1}|^2 - B_1|\alpha_{3,1}|^2$, $K_2 = |\alpha_{2,1}|^2 a_2 - B_1|\alpha_{3,1}|^2 a_3$ . De la même façon, on trouve pour $P_3(t)$

$$\begin{aligned} P_3(t) &= K_3A^2 + K_4A\Lambda(t) + K^*_4A\Lambda^*(t) \\ &= K_3A^2 + 2K_{4R}A\Lambda_R(t) - 2K_{4I}A\Lambda_I(t) \end{aligned} \tag{C3.2}$$

où $K_3 = |\alpha_{2,1}|^2 - B_2|\alpha_{4,1}|^2$, $K_4 = |\alpha_{2,1}|^2 a_2 - B_2|\alpha_{4,1}|^2 a_4$ et où les indices R et I représentent respectivement les parties réelles et imaginaires.

En supposant, en premier lieu, que l'amplitude de la porteuse regénérée au récepteur est connue, les équations (C3.1) et (C3.2) représentent un système à deux équations et à deux inconnues. Ce système d'équations s'écrit sous forme matricielle:

$$\begin{bmatrix} P_2(t) - K_1A^2 \\ P_3(t) - K_3A^2 \end{bmatrix} = \begin{bmatrix} 2K_{2R} & -2K_{2I} \\ 2K_{4R} & -2K_{4I} \end{bmatrix} \begin{bmatrix} A\Lambda_R(t) \\ A\Lambda_I(t) \end{bmatrix} \tag{C3.3}$$

La solution pour $A\Lambda_{R(I)}(t)$ est donnée par:

$$\begin{aligned} A\Lambda_R(t) &= \frac{\left(P_2(t) - K_1A^2\right)(-K_{4I}) + \left(P_3(t) - K_3A^2\right)(K_{2I})}{D} \\ A\Lambda_I(t) &= \frac{\left(P_2(t) - K_1A^2\right)(-K_{4R}) + \left(P_3(t) - K_3A^2\right)(K_{2R})}{D} \end{aligned} \tag{C3.4}$$

où D est le déterminant de la matrice de l'équation (C3.3):

$$D = 2(K_{4R}K_{2I} - K_{4I}K_{2R}) \tag{C3.5}$$

À partir de l'approximation donnée par l'équation (C2.6):

$$A^2 \cong \frac{\Psi_1(t)}{|\alpha_{1,1}|^2} \tag{C3.6}$$

on trouve:

$$A\Lambda_R(t) = \frac{-\left(P_2(t) - K_1\frac{\Psi_1(t)}{|\alpha_{1,1}|^2}\right)K_{4I} + \left(P_3(t) - K_3\frac{\Psi_1(t)}{|\alpha_{1,1}|^2}\right)(K_{2I})}{D}$$

$$A\Lambda_I(t) = \frac{-\left(P_2(t) - K_1\frac{\Psi_1(t)}{|\alpha_{1,1}|^2}\right)K_{4R} + \left(P_3(t) - K_3\frac{\Psi_1(t)}{|\alpha_{1,1}|^2}\right)(K_{2R})}{D} \qquad \text{(C3.7)}$$

Finalement, ce résultat peut se simplifier en le réécrivant comme suit:

$$A\Lambda_R(t) = \frac{-\left(P_2(t) - \beta_1\Psi_1(t)\right)K_{4I} + \left(P_3(t) - \beta_2\Psi_1(t)\right)(K_{2I})}{D}$$

$$A\Lambda_I(t) = \frac{-\left(P_2(t) - \beta_1\Psi_1(t)\right)K_{4R} + \left(P_3(t) - \beta_2\Psi_1(t)\right)(K_{2R})}{D} \qquad \text{(C3.8)}$$

où on définit les paramètres suivants: $\beta_1 = \frac{K_1}{|\alpha_{1,1}|^2}$, $\beta_2 = \frac{K_3}{|\alpha_{1,1}|^2}$ .

# Annexe D

# Étude de complexité matérielle

# Partitionnement du problème

**Christian Cardinal ÉTS/LACIME**
**Le 1 avril 1996**

Ce document porte sur l'étude de complexité matérielle concernant la réalisation des équations du DSP. Ces équations peuvent être réalisées selon le principe illustré à la figure suivante.

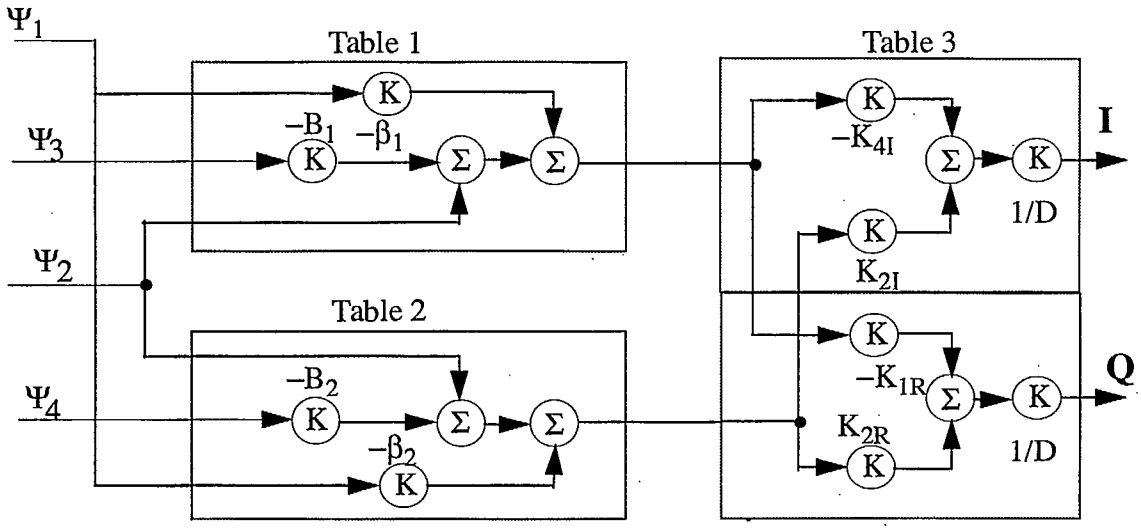



Figure 1. Partitionnement du problème

La figure 1 montre que les équations sont réalisées en trois parties. Chacune de ces parties pourront être implantées à l'aide de tables placées en mémoire. Le contenu de ces tables est initialisé à partir d'un micro-contrôleur lors du processus de calibration du circuit. Le schéma de la figure 2 illustre ce principe.

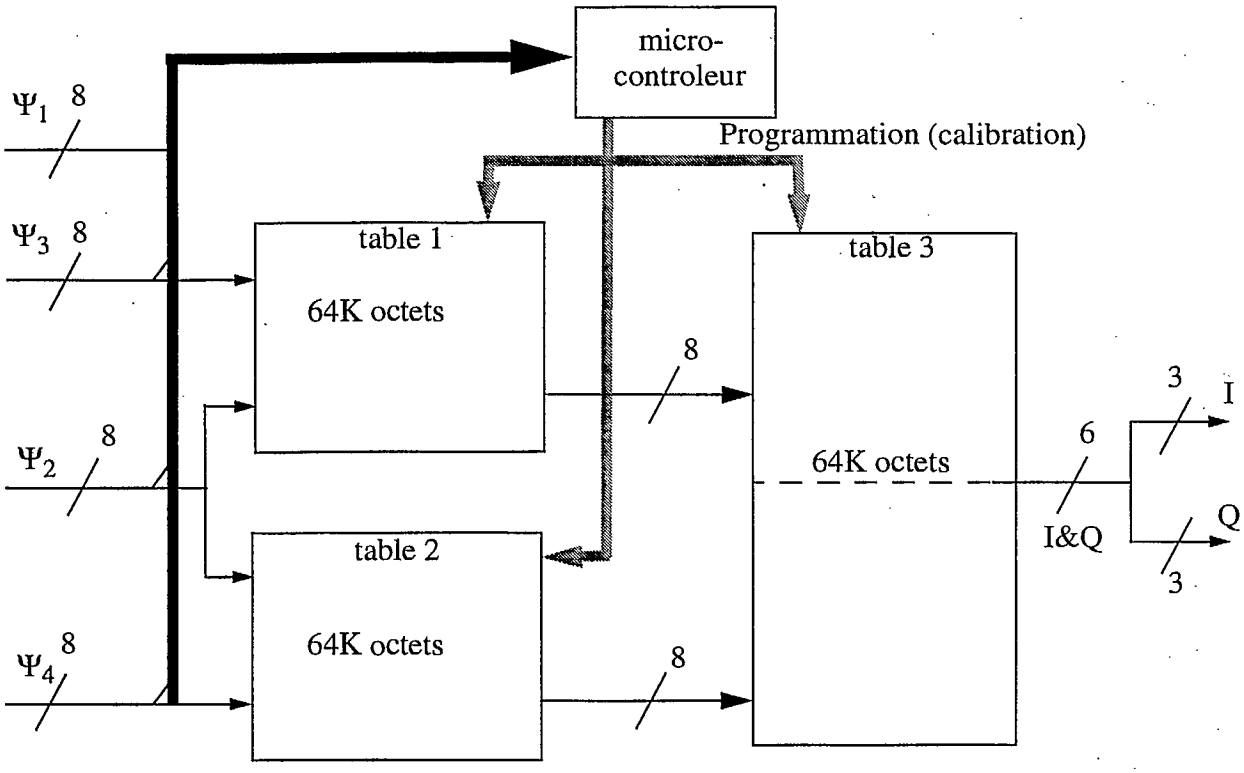



Figure 2. Schéma de principe du DSP

Avec une quantification sur 8 bits pour chaque entrée du circuit, on doit utiliser, pour chaque table, 64K octets de mémoire (64K = $2^{16}$). Puisque l'entrée $\Psi_1$ est par hypothèse constante[1], l'acquisition de cette valeur peut se faire qu'une seule fois, soit pendant la calibration du circuit. En utilisant la valeur de $\Psi_1$ ainsi obtenue, le micro-contrôleur calcule les valeurs contenues dans chaque table. Les sorties des tables 1 et 2 sont quantifiées sur 8 bits tandis que pour la table 3, chacune des sorties correspondantes aux signaux en phase et quadrature (I, et Q) utilisent 3 bits. Le premier bit correspond à une décision à quantification dure alors que les 2

1. Voir Annexe C «Démodulation cohérente à l'aide du six-ports, Équations du DSP».

autres bits correspondent à la fiabilité sur la décision. Il suffit donc de fournir au micro-contrôleur les paramètres du six-ports. Par la suite, en utilisant l'entrée $\Psi_1$, le micro-contrôleur entre dans une phase de calibration permettant ainsi de calculer le contenu des tables.

# Annexe E

# A NEW DIRECT DIGITAL RECEIVER PERFORMING COHERENT PSK RECEPTION

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## Abstract

**Coherent reception provides better CNR performance over its differential counterpart. However, this is generally obtained at the expense of increasing complexity of the receiver and more stringent specifications of circuits. In this paper, we describe a new coherent PSK direct receiver, in which a 'soft' phase reference is established by DSP, while the detection is performed directly at mm-wave frequencies. Both measurements and computer simulations validate the proposed new approach.**

## Introduction

It has been recently shown that a six-port circuit in conjunction with DSP (Digital Signal Processor) is capable of performing digital demodulation directly at frequencies ranging from microwave to mm-wave bands [1]. This new direct digital receiver promises reduced receiver complexity, loose fabrication requirements and fair performance in providing a cost effective alternative to the conventional heterodyne structure used in various digital terminals.

The most widely used modulation schemes in digital communication systems, such as satellite and personal communication systems, are PSK (Phase Shift Keying). There are two types of demodulation techniques: coherent and non-coherent (differential) [2]. In general, the differential detection brings about less complicated receiver configuration whereas the coherent detection is superior in error performance. However the complexity of a coherent receiver may be increased significantly due to the carrier recovery requirement. This task becomes particularly difficult when the carrier recovery has to be performed directly at microwave and millimeter-wave frequencies.

The presence of DSP in the six-port receiver gives us a flexibility of implementing receiver functions using simple software algorithms. In this work we introduce a simple method to establish a 'soft' phase reference needed for the coherent detection. In this way, only AFC (Automatic Frequency Control) is required for the local oscillator. Once the LO frequency is within the 'catching up' range of the receiver, the 'soft' phase reference tracks down and compensates the phase drift

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introduced by residual frequency difference such that the detected signal constellation becomes fixed as though the carrier recovery is achieved.

## Description of the Method

A block diagram of the six-port direct digital demodulator is shown in Fig. 1. The RF signal is fed into a six-port circuit. From the outputs of the four diode power detectors, the instant phase and frequency of the input RF signal are calculated by the DSP. The DSP controls the local oscillator to perform AFC. Once the carrier and clock recovery are achieved, the modulated data will be readily recovered.

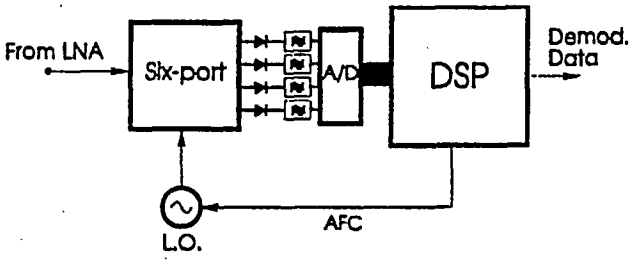


**Figure 1. Block diagram of the six-port direct digital demodulator.**

A received PSK signal is given by the following expression:

$$s(t) = A_c \cos(2\pi f_0 t + \Phi(t,a)) \qquad (1)$$

where $f_0$ is the carrier frequency and the instant phase $\Phi(t,a)$ is a function of time $t$ and the modulation data sequence $a$. Taking QPSK as an example and disregarding the band-limit, we have

$$\Phi(t,a) = 2\pi \cdot \frac{a_i}{4} + \phi_0 \qquad (2)$$

where $a_i = \{0, 1, 2, 3\}$, $\phi_0 = 0$ or $\pi/4$, $a_i$ is the $i$th symbol during $iT < t < (i+1)T$, and T is the duration of one symbol.
Suppose the LO frequency is very close to the incoming carrier frequency and the symbol clock synchronization is achieved, then samples detected by the six-port receiver are given by

$$s(i) = A_c \cos(2\pi \Delta f t_i + 2\pi \cdot \frac{a_i}{4} + \phi_0) \qquad (3)$$

where $\Delta f = f_c - f_{LO}$, and to simplify the problem, only one sample is taken for each symbol.
It is observed from (3) that due to the presence of residual $\Delta f$ the sampled constellation is still rotating at an angular speed of $2\pi\Delta f t$. In order to enable a coherent detection, a phase reference must be set up to counter this rotation.

For the case where $f_{LO}$ is sufficiently close to $f_c$, the phase drift introduced by the term $2\pi\Delta f t$ can be considered negligible during a certain period of time NT, and in this case the instantaneous samples $\theta_i$ represent the modulation data. Taking a sample $\theta_0$ as reference and denoting it by $P_0$, for every subsequent sample $\theta_i$, let $\varphi_i = \theta_i - P_0$ $(0 \le \varphi_i < 2\pi)$, such that the 4 states of data sequence can be recovered as follows:

$$a_i = (\varphi_i + \tfrac{\pi}{4}) / (\tfrac{\pi}{2}) \qquad (4)$$

In order to eliminate the noise, a FIFO (First-In-First-Out) register of length N is set up, and every latest $\theta_i$ that makes $a_i = 0$ is pushed into the register. Let the phase reference $P_0$ be the average of $\theta_i$'s in the register:

$$P_0 = \frac{\sum_{j=0}^{N-1} \theta_i}{N} \qquad (5)$$

In the stable state,

$$P_0 = P_0 + (\theta_{i\,latest} - \theta_{i\,earliest}) / N \qquad (6)$$

Obviously, $P_0$ will follow the $2\pi\Delta f t$ term and the $\varphi_i$'s will become relatively fixed regardless of $\Delta f$. In this way, once the test sequence is detected, the $a_i$'s will be mapped into corresponding bits in

conformity to the transmitting end. Although the example is given for QPSK demodulation, this method also applies to all other PSK and even QAM modulations.

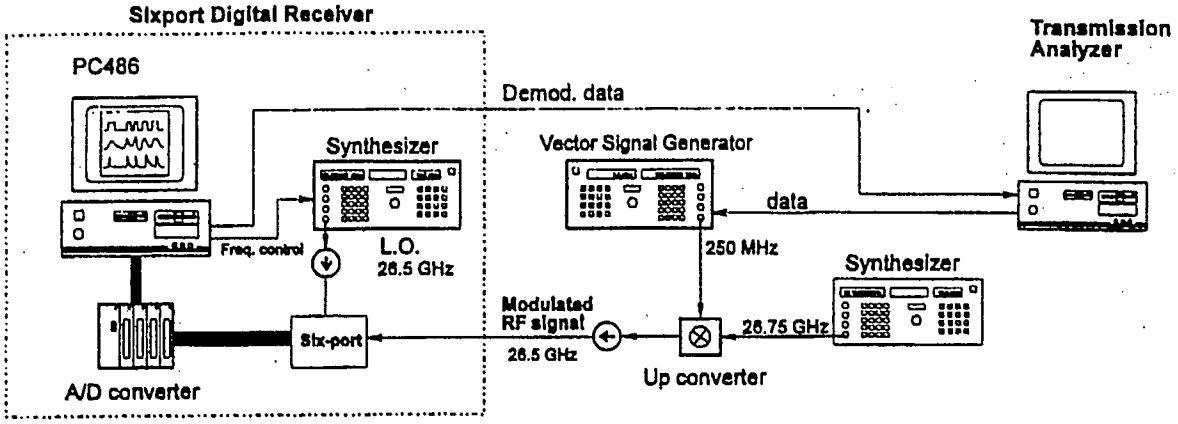


**Figure 2. Block diagram of the test setup for measurement simulation.**

## Results

A measurement simulation was made to verify the above procedure. Figure 2 is the block diagram of the test setup. The transmitter is composed of a HP8782B vector signal generator, a upconvertor and a RF source. The 26.5 GHz PSK is fed into the six-port receiver. No additional amplifier is placed before the six-port junction. The receiver LO power was -1.5 dBm. A PC486 was used to simulate the DSP functions. The input power level of the receiver was controlled by the internal attenuator of the vector signal generator which provides over 160 dB of variation in output level. Five basic PSK demodulations were tested: differential and coherent BPSK, QPSK and coherent 8PSK. A small random variable frequency deviation of the receiver LO was intentionally made to simulate the residual $\Delta f$.

A statistical computer simulation was also performed to verify the measurement results. It takes into account the phase noise of the signal generators and LO, the ADC quantitized noise. The interference brought in by DC path was also considered. It is noticed that for this measurement simulation the effect of Gaussian white noise is negligible. BER (Bit Error Rate) was simulated as a function of input power level, and a perfect carrier recovery was assumed during the coherent PSK simulation.

Figure 3 shows the measured and simulated BER versus input powers. It is found that the coherent PSK reception presents about 1 dB (BPSK) to 2 dB (QPSK) better than their differential counterparts. The agreement between measured and calculated data suggests a good performance of the proposed coherent demodulation method. It also shows that the demodulation can be performed at a power level as low as -35 to -45 dBm. It must be mentioned that the measurement results are by far not optimized. A significant improvement in performance can be expected once the six-port junction design and system configuration are optimized.

## Conclusion

A novel approach is proposed, which enables the coherent PSK demodulation directly at millimeter wave frequencies using a new receiver concept. This makes it possible for new six-port digital receiver to deal with various coherent and differential PSK modulation schemes. The receiver can be used in various wireless microwave/mm wave digital terminals to provide a cost-effective alternative to conventional heterodyne receivers.

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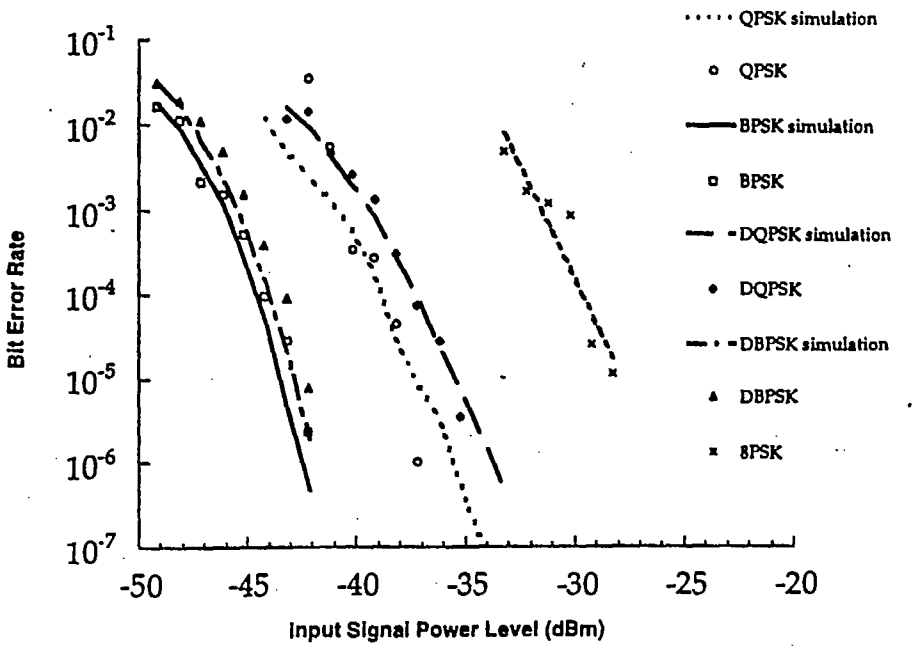


**Figure 3. Measured and computer simulated BER performance**

# A SIX-PORT DIRECT DIGITAL MILLIMETER WAVE RECEIVER

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## ABSTRACT

**A novel approach is proposed for direct demodulation of various digitally modulated signals at microwave/millimeter wave frequencies using a six-port phase/frequency discriminator (SPFD). The proposed six-port direct digital receiver is capable of handling PSK and QAM as well as their varieties. Preliminary measurements on demodulation of DBPSK signals at 26.5GHz, 33GHz and 40GHz have revealed great potential of this new receiver.**

## INTRODUCTION

Direct homodyne reception has been attracting constant attention due to its inherent advantages over its heterodyne counterpart. The recent development of personal communication systems (PCS) has ignited a new round of efforts to achieve low cost, robust and miniaturized versatile microwave/mm-wave digital terminals. Considerable effort has been made on digital direct conversion receivers (DCR) [1]-[3] in which conventional I-Q structure is adopted. However, the difficulties involved in implementing perfectly matched orthogonal I-Q circuits prevents such technology from applications at higher frequency bands.

Six-port technique has been known for its ability to accurately measure the scattering parameters, both amplitude and phase, of microwave networks. Instead of using heterodyne receiver a six-port junction accomplishes direct measurements at microwave and mm wave frequencies by extracting power levels at four of the six ports. The imperfections of the hardware can be readily eliminated by an appropriate calibration procedure. Very accurate measurements can be made over large dynamic range and wide frequency range. Six-port junction consists of passive microwave components such as directional couplers and power dividers as well as diode detectors. The circuit can be easily integrated as MHMIC or MMIC. Recently we have proposed a new approach, in which a six-port junction is used for accurate frequency comparison. The frequency differences are found by direct measurements of the derivatives of the phase variations. This features a new digital microwave/mm wave six-port phase/frequency discriminator (SPFD)[4].

In this paper we present a new six-port digital

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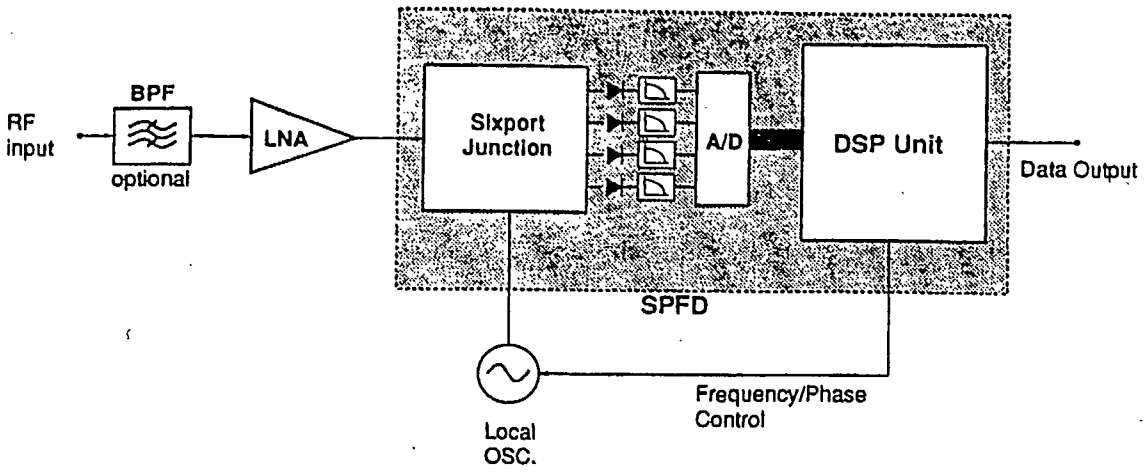


Figure 1. Block diagram of the sixport direct digital receiver

receiver (SDR). It performs direct phase/amplitude demodulation at microwave/mm wave frequencies. The receiver is simple and potentially low cost. Furthermore, the SDR can easily cover a wide frequency band by using a broadband design of the six-port junction. This SDR is proposed for low/medium speed receivers with data transmission rate lower than 15Mb/s.

## DESCRIPTION OF THE SDR

The functional block diagram of the SDR is shown in Fig.1. The traditional I-Q block in a receiver is replaced by a six-port phase/frequency discriminator (SPFD), which contains a six-port junction and a digital signal processing (DSP) unit. The incoming digitally modulated (e.g. PSK, QAM) RF signal is compared with the output of a digital controlled local oscillator. Carrier recovery is first performed. The DSP unit detects the frequency difference of the signals and then controls the local oscillator to track the incoming signal. Once the carrier is recovered the instantaneous phase of the received signal is detected and decoded so as to recover the original modulated data. Symbol synchronization can also be achieved simultaneously. Incoherent reception can be used where the LO frequency need not to be exactly the same as the carrier frequency. The maximum tolerable frequency deviation depends on the data transmission rate and the modulation scheme. The maximum data transmission rate is determined mainly by the sampling rate of the A/D converters and processing speed of the DSP unit.

Regarding the practical feasibility of the direct digital phase demodulation, the new SDR features some advantages over the conventional I-Q direct reception schemes. First, by performing a simple calibration procedure [5], the hardware imperfections such as phase error of the bridges, imbalance of the power detectors can be readily eliminated. This significantly eases the requirement of the hardware implementation and enables the SDR to operate over a wide band up to millimeter wave frequencies. Second, in the SDR, the magnitude and phase are acquired independently. Therefore the phase modulation of the incoming signal can still be correctly detected even though the amplitude of the incoming signal changes over a large dynamic range. Third, the DSP unit

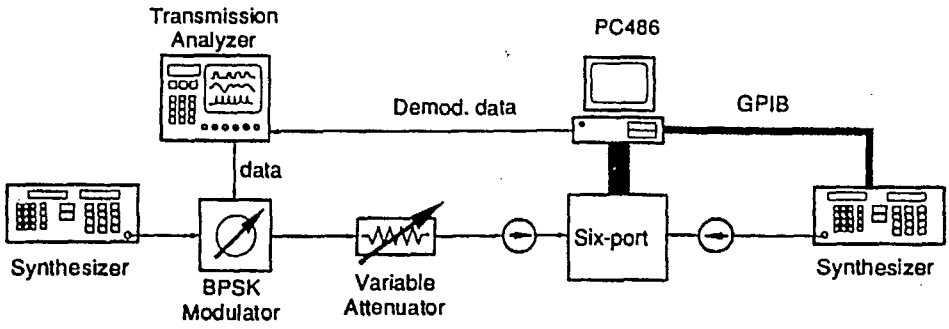


Figure 2. Test Set-up of the bit error rate measurement

gives much flexibility to the SDR. Switching between different modulations can be readily accomplished by slight alternations of the algorithm. Advanced error correction coding techniques can also be integrated into the same unit. Aside from PSK modulations, amplitude/phase modulation such as QAM is readily detectable by employing an algorithm which takes into account the fading effect in the transmission path.

## MEASUREMENT RESULTS

Measurements are performed to demonstrate the potential of the new SDR. The test setup is shown in Fig.2. A simple differential binary phase shift keying modulator generates a DBPSK signal. The LO frequency is controlled to track the carrier frequency. The output of the modulator was directly fed into the SPFD with no amplification additional. A PC486 equipped with a A/D converter is used as the DSP unit.

A constellation map measured at 33 GHz corresponding to different incoming signal levels is shown in Fig.3. It clearly indicates both magnitude and phase of the received signal. The imbalance of the BPSK modulator can also be clearly observed. The span of the phase might be introduced by phase noise of the two microwave synthesizers (The local oscillator and DBPSK signal generator). It is noticed that a coherent reception is also possible with a proper phase lock of the local oscillator. Bit error performance was measured at 26.5GHz, 33GHz and 40GHz using the same receiver. Fig.4 plots the BER versus incoming signal level. The levels between the saturation point of diode detectors and a specified BER point is considered as the operating dynamic range. The saturation point of the detectors used is about 10dBm. Counting the approximate 10dB insertion loss between the input port and the detectors the maximum

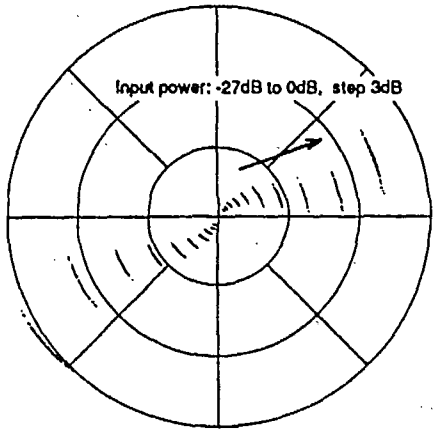


Figure 3. Measured constellation of the BPSK signal at different power levels (Freq.=33GHz)

power level at the input port of the six-port can be 20dBm so that the overall dynamic range is around 60~70dB without any additional level control. Note that the operating dynamic range is mainly determined by the resolution of the A/D converter. In this measurement a 16-bit A/D converter is used. The difference in BER performance at the three frequencies is believed to be caused mainly by the frequency response of the diode detectors.

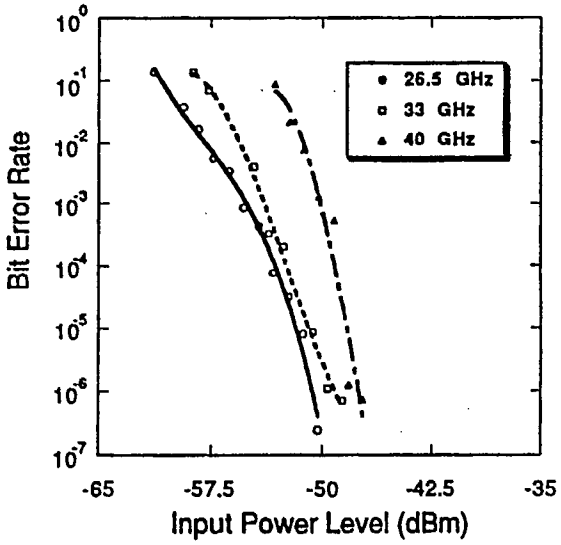


Figure 4. Measured BER performance of the six-port direct digital receiver

## CONCLUSIONS

A novel scheme for direct microwave/mm wave digital phase demodulation is presented. Some drawbacks of the conventional I-Q direct conversion digital receiver are overcome by using a six-port phase/frequency discriminator incorporated with a digital signal processing unit. This technology is potentially low cost and it is promising in various small/medium capacity digital communication systems such as point-to-point data links, micro-cell mobile terminals and wireless LAN's etc.

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# Computer and Measurement Simulation of a New Digital Receiver Operating Directly at Millimeter-Wave Frequencies

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## ABSTRACT

**A novel digital millimetric receiver (DMR) scheme is introduced. Using a six-port phase/frequency discriminator (SPD) in conjunction with a digital signal processor (DSP), the receiver performs various PSK and QAM demodulations directly at microwave and millimeter-wave frequencies. An important feature of the new DMR is that hardware imperfections such as phase/amplitude imbalance are readily eliminated by a simple calibration procedure. The concept is proved through computer simulation and measurements at 26.5GHz. This receiver scheme is proposed for small/medium capacity digital terminals typically found in various wireless communication networks.**

## INTRODUCTION

Due to the increasing demand of wireless communications, there have been persistent efforts to simplify the microwave/mm-wave digital transceiver structures to bring down their size and cost. Such efforts have been intensified recently due to fast emerging demands for personal communication services (PCS). Among various choices, the direct (homodyne) transceiver architecture is an effective way to significantly reduce transceiver complexity and cost. Both direct transmitter [1-3] and receiver [4-6] for different digital modulations using different circuits ranging from hybrid microwave integrated circuit (HMIC) to monolithic microwave integrated circuit (MMIC) technologies have been reported. All these direct transceivers have one point in common: a quadrature hybrid network (I-Q network). It is well known that, as the frequency increases, the corresponding wave-length decreases proportionally, and it is therefore more difficult to obtain a quadrature hybrid with acceptable phase and amplitude accuracy. This is particularly true when the frequency goes beyond microwave into the millimeter-wave band. Although additional circuits can be introduced to compensate phase and amplitude imbalances of the I-Q hybrid [7,8], this method is obviously cumbersome, and the long-term stability of such circuits is questionable.

As a result of the latest advancement in digital integrated circuit technologies, there is noticeable interest to replace analog circuit functions with their digital implementations [10,11]. This generally brings down the cost and increases the stability as well as the flexibility of the electronic systems; particularly when DSPs are used. The processing power of the latest DSP is reported to have reached 2 bops [12] which makes it possible to realize some very complex algorithms at high speed. Certain types of receivers sample signals in the IF band and implement the demodulation using DSPs [13]. These receivers, however, still retain all the microwave parts found in the conventional heterodyne receiver. For the design of microwave transceivers, it appears to be more reasonable to simplify the microwave circuit configuration at the expense of more complicated digital circuits, such as to make a better trade-off to reduce the cost and increase the yield of MMICs.

Six-port theory was first developed in the 70's as a new means of accurate automated microwave network analysis [14,15]. The vector ratio of the incident waves at two input ports can be calculated using the output power readings at the remaining four ports. In doing this there is no need of down-converting the signal to an IF to make phase comparison. A very interesting feature of the six-port is its ability to eliminate measurement errors introduced by hardware imperfections by a suitable calibration procedure [22]. After more than twenty years of development the six-port technology has become highly sophisticated and some commercial products are now available on the market [16]. In addition, recent progress in MMIC and MHMIC six-ports [17,18] renders such circuits better accessible for widespread commercial applications.

In this paper, we describe a novel concept of a direct digital receiver, in which a six-port replaces the I-Q quadrature hybrid as the phase detector. The block diagram of the new scheme is shown in figure 1. The demodulation is performed directly at microwave/mm-wave frequencies by a six-port discriminator (SPD) instead of the I-Q demodulator found in conventional digital receivers. This SPD is capable of detecting relative amplitude, phase and frequency of the received signal with respect to the local oscillator. A DSP unit executes computations necessary to perform the required demodulation in addition to

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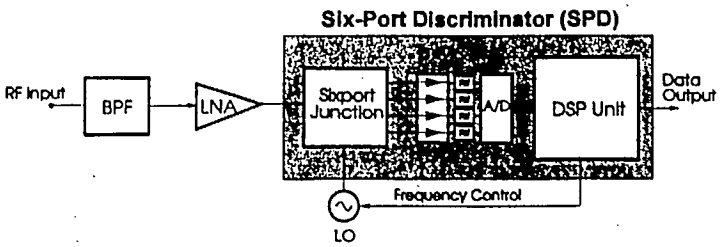


Figure 1. Block diagram of the new Digital Millimetric Receiver (DMR) with the six-port discriminator (SPD)

carrier and clock recoveries using algorithms that are already available [32-36]. Such a receiver benefits from all the advantages of six-port technology: First of all, the fabrication requirements of the hardware can be greatly eased. An auxiliary calibration algorithm [19] performs the required six-port calibration from the received signal itself, and monitors the real-time operation and updates the calibration coefficients as temperature and/or some other circuit parameters vary. This makes it possible to realize a direct millimeter wave digital receiver without stringent fabrication requirements; Secondly, the presence of a DSP provides a great flexibility to the receiver function: Switching between different modulations can be done by simply altering the software routines thereby avoiding hardware reconfiguration. Both differential and coherent detections are possible [24]. Furthermore, the demodulation and decoding functions can be combined together to further enhance the receiver system integration; Thirdly, the proposed six-port receiver possesses unique properties such as: a) Immunity to adjacent channel interferences, so that the specification of the channel bandpass filter can be relaxed; b) The six-port receiver allows variation in input power level. The dynamic range of the receiver is mainly a function of the A/D converter resolution. And c) Wide band operation is also possible by the use of a wide-band six-port design. After all, the maximum data transmission rate is limited by the A/D converter and DSP. The data throughput is expected to increase as the speed of the DSP chip escalates in time.

## SIX-PORT DISCRIMINATOR (SPD)

Previously reported six-port applications are mostly focused on microwave measurements such as network analysis [20] and parameter extraction [21]. These measurements involve only coherent signals, i.e. the incident and reflected waves of the microwave networks are generated from the same signal source. Consider the case of a six-port used as a microwave vector voltmeter, the complex ratio of the two input signals $a_1$ and $a_2$ in figure 2 can be obtained as follows:

$$\vec{A} = |A| e^{j\theta} = \frac{\vec{a}_1}{\vec{a}_2} = \frac{\sum_{i=3}^{6} (a_i + jb_i) P_i}{\sum_{i=3}^{6} (c_i + jd_i) P_i} \qquad (1)$$

where constants $a_i$ , $b_i$ , $c_i$ , $d_i$ 's are calibration parameters that depict the specific six-port and can be deduced from a popular two-step calibration procedure [22].

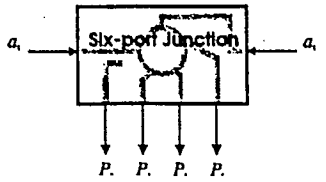


Figure 2. A six-port functions as a microwave vector voltmeter as $a_1/a_2$ is calculated from $P_i$'s.

To extend the scope of the six-port a little further, we define the two incident waves to be at different frequencies as follows:

$$\vec{a}_1 = |a_1| \cdot e^{j(2\pi f_1 t + \phi_1)} \qquad (2)$$

$$\vec{a}_2 = |a_2| \cdot e^{j(2\pi f_2 t + \phi_2)} \qquad (3)$$

Suppose the frequencies $f_1$ and $f_2$ are close enough to each other such that the difference in calibration coefficients is negligible for the six-port, the measured complex ratio $A$ will become a rotating vector in the complex plane:

$$\vec{A} = |A| \cdot e^{j\theta(t)} = |A| \cdot e^{j(2\pi(f_1 - f_2)t + \phi_1 - \phi_2)} \qquad (4)$$

Therefore, the frequency difference $\Delta f = f_1 - f_2$ can be readily obtained from the derivative of $\theta(t)$

$$\Delta f = \frac{\theta(t_2) - \theta(t_1)}{t_2 - t_1} \qquad (5)$$

where the time interval between two samples $\Delta t = t_2 - t_1$ is properly chosen for best accuracy. It is to be noted that the sign of $\Delta f$ is a direct indication of relative position of $f_1$ and $f_2$ . In this way, the so-called six-port phase/frequency discriminator (SPD) [23] is capable of dealing with all basic receiver functions which are traditionally carried out by I-Q hybrids.

## COMPUTER SIMULATION: PERFORMANCE OF SPD VERSUS I-Q DEMODULATOR

The obstacles preventing conventional I-Q receiver from direct operation at higher frequencies are mainly [25]: (1) Phase imbalance due to circuit imperfections and reflections; (2) Amplitude imbalance due to I-Q circuit, gain imbalance of the two mixer branches, etc.; and, (3) DC offset of the I and Q channels. It is recognized that the new SPD can largely overcome such drawbacks. This will be demonstrated through a series of simulation and analysis in the following sections.

### Circuit Model of Six-Port

A six-port circuit originally designed as a reflectometer is adopted here for simulation purposes. The block diagram of the circuit is shown in Figure 3. It can be seen that the six-port consists of I-Q hybrids, an in-phase power divider and interconnecting transmission lines. These components are characterized by S-parameters, so that the hardware imperfections can be readily taken into account. A commercial microwave simulator (MDS*) was used to analyze the network. In all the simulations, a real

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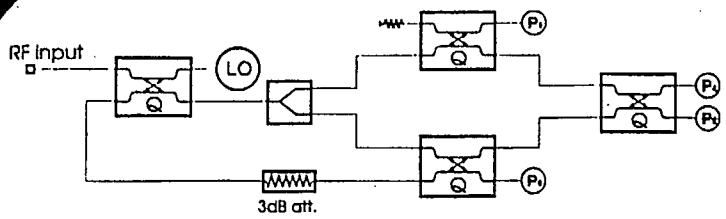



Figure 3. Block diagram of the six-port model used in the simulation of SPD.

calibration procedure was performed to obtain the corresponding calibration coefficients. Both the simulation and the analysis are performed to compare the SPD to a standard I-Q demodulator operating at the same mm-wave frequency.

Degradation of Receiver Performance Due to the Hardware Imperfections

Taking bit error rate (BER) as a straightforward measurement of the receiver performance, for a perfect digital receiver, the only factor affecting performance is noise. The degradation in performance due to various non-ideal factors such as hardware imperfections, synchronization errors and interferences can be regarded as equivalent to loss in signal to noise ratio (SNR or $E_b/N_0$). In order to demonstrate the advantages of using SPD over conventional I-Q hybrid, simulations have been made for a standard heterodyne QPSK receiver. The transmitter was considered perfect and the phase/amplitude imbalances were introduced in the I-Q demodulator. Figure 4 shows the BER as a function of $E_b/N_0$ in the presence of different order of amplitude and phase imbalances. The simulated transmission data rate was 10Mb/s. The role-off factor of the raised-cosine band-limit filter was 0.35. It is illustrated that the BER increases with the imbalance. The equivalent $E_b/N_0$ loss is approximately 1.5dB, 2.1dB, 2.9dB and 3.7dB for phase imbalances of 5, 10, 15 and 20 degrees respectively at $10^{-4}$ BER threshold. This $E_b/N_0$ loss becomes as large as 4.6dB when the phase imbalance reaches 25 degrees. It is expected that the higher level modulation schemes such as 8PSK and 16QAM. are even more sensitive to such imbalances. In some circumstances, the amplitude imbalance between I-Q branches is larger than 1dB. Therefore in order to maintain a reasonable performance of the receiver, it is absolutely necessary to find an effective way to counter these adverse effects.

Operating Dynamic Range as a Function of the ADC Resolution

In a conventional heterodyne digital receiver it is generally required that the input level of the I-Q demodulator be kept constant by using an IF automatic gain control (AGC) circuit. However, this becomes more difficult at microwave frequencies. One feature of the six-port direct digital receiver is its tolerance to input signal level variation. Therefore expensive microwave AGC amplifier can be exempted. The difference between the maximum and minimum signal levels, while maintaining a given BER margin for a specific modulation, can be defined as the operating dynamic range of the receiver. The minimum detectable signal level depends on the resolution of the A/D converters. On the other hand, an I-Q demodulator also allows variable input signal if the same A/D converters and DSP are used. Figure 5 illustrates the amplitude and phase errors of SPD and I-Q demodulator as functions of input signal level for 8bit, 12bit and 16bit A/D converters respectively. It is obvious that a high resolution A/D

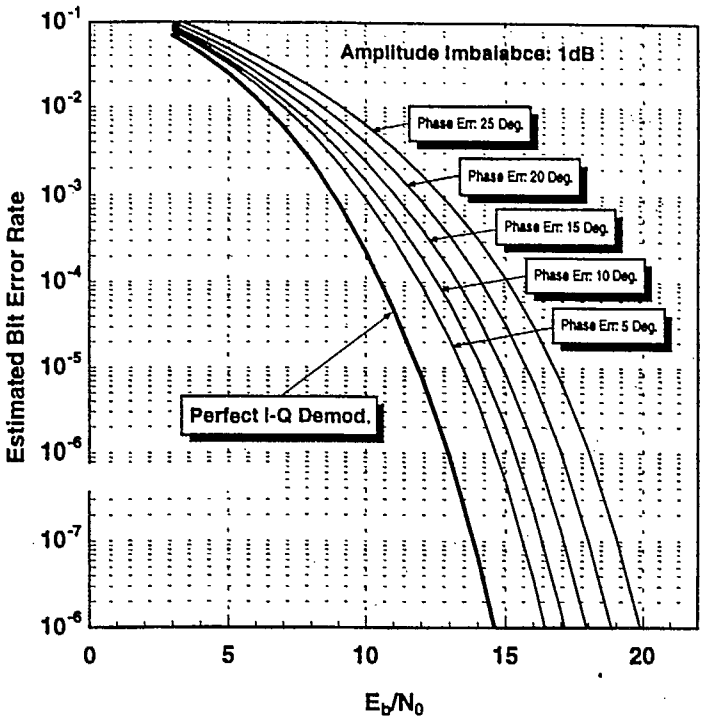
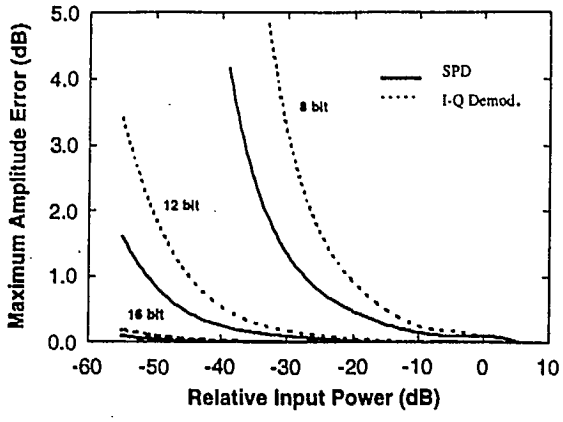



**Figure 4. BER performance of a QPSK receiver in the presence of amplitude and phase imbalance of the I-Q demodulator**

converter not only extends the dynamic range but also abates the gain requirement of the preceding low noise amplifier. Meanwhile, the maximum acceptable input level is determined by the saturation point of the power detectors or channel DC amplifier/ADC input limits. Therefore it is concluded that a 50dB of nominal dynamic range can be readily achieved for QPSK reception using 16bit ADC. In most applications it will be more interesting to increase the sensitivity of the SPD to facilitate the LNA design. It is also observed that SPD offers better accuracy than a digitized I-Q demodulator in all cases. For example, from Figure 5, at a relative input power level of -25dB, the SPD has maximum amplitude and phase error of 0.8dB and 5 degrees, respectively when a 8bit ADC is used, while these errors are 1.7dB and 8 degrees for the I-Q demodulator, respectively.

Accuracy of SPD in the Presence of Quadrature Imbalances

The SPD itself can be built up by quadrature hybrids and power dividers or other suitable circuits for phase dispersal. None of these components are perfect. The six-port calibration procedure is to extract the network parameters and eliminate errors from the final measurement results. As a result of noise, the limited resolution of A/D converters and so on, there will still be residual phase and amplitude errors. A statistical simulation has been accomplished to compare the residual errors of SPD with an I-Q hybrid. Random phase and amplitude errors are assigned to each component in the SPD (Figure 3), and the parameters are random at maximum tolerances for all the components. Consequently, the overall performance of the SPD is the worst possible case at the corresponding error level. Figure 6 shows the simulation results. A 1-dB amplitude imbalance is presented in all cases. The SPD has 16 bit resolution and the I-Q demodulator uses perfect A/D conversion in the simulation. It is clearly shown that the SPD is



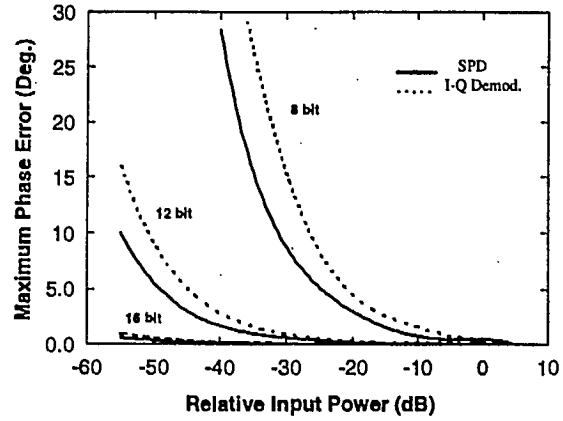
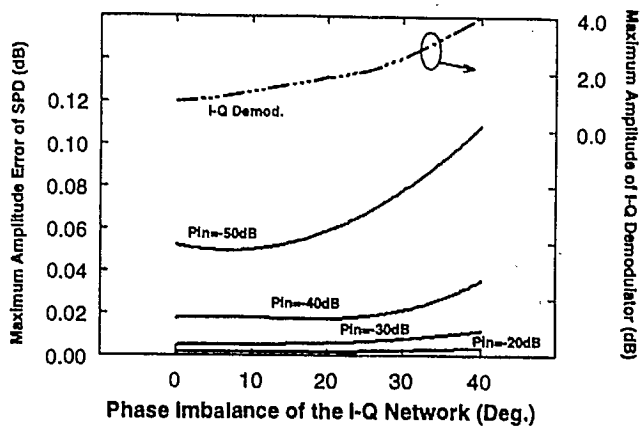




Figure 5. Maximum amp/phase errors vs. Input power level of SPD and I-Q Demodulator.



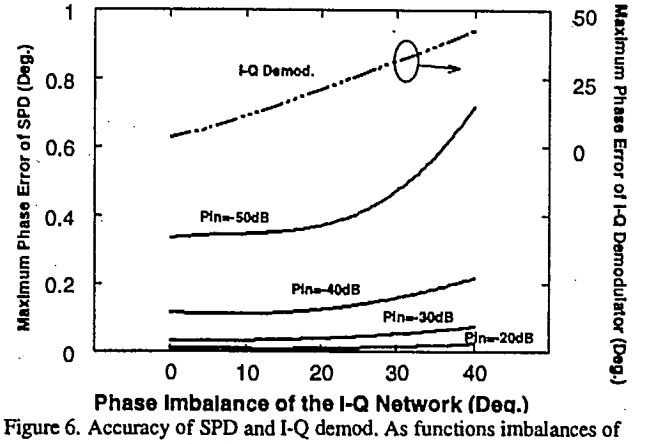




Figure 6. Accuracy of SPD and I-Q demod. As functions imbalances of quadrature hybrid (16bit ADC).

very powerful in countering hardware imperfections: in the phase imbalance range of 0 to 40 degrees with the relative input level as low as -50dB, the maximum residual amplitude and phase errors of SPD are only 0.1dB and 0.7 degrees, respectively. Therefore it is concluded the residual error can be considered negligible over the whole dynamic range of the SPD. In contrast, for I-Q demodulators, the errors are directly proportional to hardware errors, i.e. an amp./phase error of 1dB/25Deg. of the I-Q hardware will result in an error of 2.0dB in amplitude and 25 Deg. error in phase, respectively. Although the excellent accuracy of SPD will be degraded somehow in a real receiver due to other factors that have not yet been considered in the simulation such as imperfect calibration and noise, the conclusion that the SPD presents an accuracy several orders superior than I-Q demodulator is still valid. This is confirmed by the measurement simulation.

Effect of DC Offset on SPD Accuracy

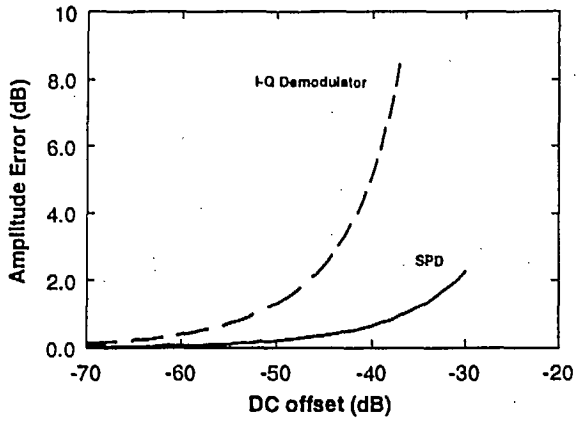
Fundamentally, the diodes in the SPD operate in a different fashion to their I-Q demodulator counterparts. In an I-Q demodulator the mixers behave like multipliers as the diodes act as nonlinear devices. In a SPD the diodes act as power detectors, and the emphasis is on linearity of the response. Consequently whilst at least a balanced diode pair must be used for the minimum specifications in an I-Q demodulator, a simple single Schottky diode detector is generally sufficient for a SPD.

The DC offset is primarily introduced by the diode detectors and the attached DC amplifiers, and its value is usually a function of temperature. A computer simulation reveals that, in the case of random offset, the SPD doesn't offer better accuracy than the I-Q demodulator. However, in situations where the offsets of all the channels are moving in the same direction, which is the actual case in single-chip ICs, the SPD comes up with a much greater accuracy.

Figure 7 displays the phase and amplitude errors as functions of the DC offset. The DC offset is defined as relative to the maximum output voltage of each channel. When the DC offset is at -40dB, the SPD maintains a minimum acceptable amplitude error of 0.6dB and a phase error of 3 degrees, while the I-Q demodulator has disastrous 5dB/26degrees amplitude/phase errors, respectively. Both amplitude and phase errors are more pronounced for the I-Q demodulator when the DC offset goes beyond -50dB. Evidently the SPD is much less sensitive to the DC offset than its I-Q demodulator counterpart.

Effect of Adjacent Channel Interferences

It makes common sense to use filters for most digital receivers to separate the signal from unwanted noise and interferences. While performance degradation caused by inband noise and interferences is inevitable, the SPD possesses unique immunity to out-of-band noise and interferences: For a single diode detector, let us suppose



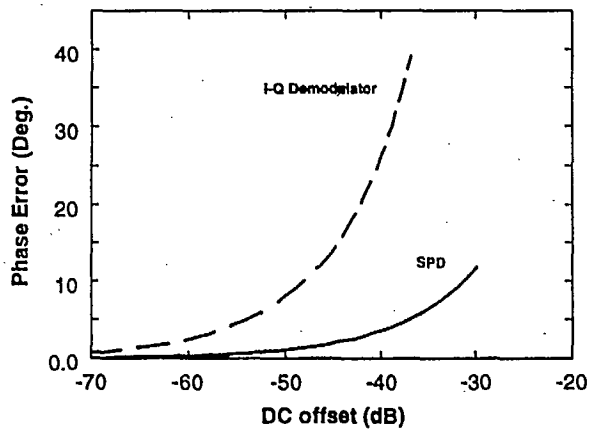




Figure 7. Accuracy of the SPD and I-Q demodulator versus DC offset.

the lowpass filters have stopped all the high frequency components, thus the interference acts only on the DC output. This DC component can be seen as an equivalent DC offset of the DC amplifier. As has already been concluded in the previous section, the I-Q demodulator is more vulnerable to such interferences.

Bit Error Rate (BER) Performance

Bit error rate is the ultimate indication of performance of a digital receiver. A statistical computer simulation model was established to help to predict the BER performance of the DMR for various types of modulations. The simulation takes into account several error sources in the real operation, such as phase noise of the local oscillator, resolution of the A/D converter and white noise introduced in diode detectors/DC amplifiers. The results are presented in figure 10 together with the measured simulation results.

## MEASUREMENT SIMULATION OF THE DMR

Measurement simulations are also performed. Figure 8 illustrates the measurement setup. A HP8782B vector signal generator produces the desired modulated signal at an intermediate frequency (250MHz). Then a upconverter brings this IF signal up to 26.5GHz and an isolator separates the transmitter from the receiver. There is no filter inserted to suppress the LO and image signal leakage. The variation of the signal level is accomplished

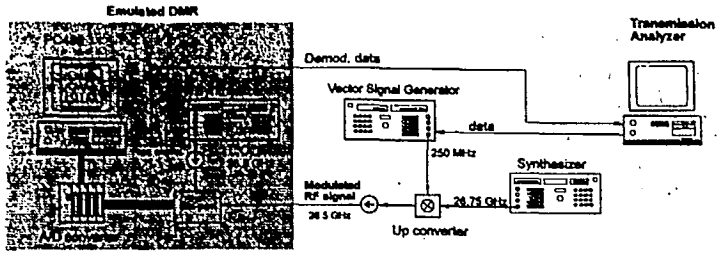



Figure 8. Test setup for measurement simulation of the new DMR operating at 26.5GHz.

by control of the output level of the vector signal generator which has over 160dB of output level range. No additional bandpass filter is inserted between the transmitter and the receiver. In the SPD, a PC486 with a 16bit plug-in A/D data acquisition board executes the DSP algorithms. The SPD is constructed using discrete coaxial components for the six-port configuration of Figure 3. The 3dB quadrature couplers have ±1.7dB of amplitude imbalance, ±10° of phase imbalance and a minimum isolation of 14dB. The in-phase power divider has ±0.6dB of amplitude imbalance, and ±4° of phase imbalance.

The receiver LO power was about -1.5dBm for all the measurements. A second PC486 was used as a transmission analyzer for BER tests.

Constellation Diagram

Figure 9 illustrates the measured constellation diagrams of BPSK, QPSK, 8PSK and 16QAM sampled by the SPD. It clearly proves the efficacy of the SPD in the correction of circuit imbalances. Neither the imbalances of the quadrature couplers nor the LO leakage impose noticeable distortion to the measured constellations. The phase spread in the constellation diagram is due to the phase noise of the oscillators, residual frequency difference and slow sample acquisition time.

It is also noticed that due to the absence of the bandpass filter at the output of transmitter, the LO component in the transmitted spectrum is more than 20dB higher than the desired signal when the output level of the IF vector signal generator is decreased. Even in this case the observed constellation diagram does not appear to be distorted, which reflects the power of the SPD in countering out-of-band interferences.

Bit Error Rate Measurements

Demodulation algorithms have been developed for both differential and coherent PSK modulations. The phase recovery for coherent detection is achieved by a simple DSP algorithm. This feature is a better alternative to the more difficult conventional hardware phase tracking directly at microwave/mm wave frequencies.

The measured BER for coherent and differential BPSK, QPSK demodulations are compared with the computer simulation results. Figure 10 shows the measured and calculated BER versus the input power level. It can be seen that, as anticipated, the coherent reception is better than the differential reception and the BPSK requires minimum energy to be detected. The input power level is about -44.5dB and -39dBm for BPSK and QPSK demodulations,

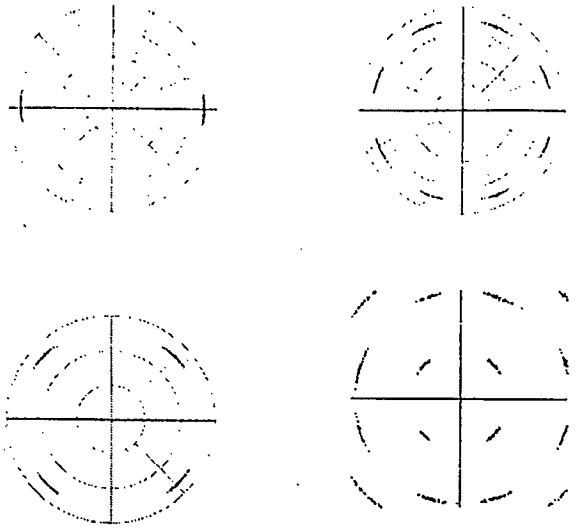


Figure 9. Sample contellation digram of different modulations measured at 26.5GHz by SPD.

respectively, when the BER is $10^{-4}$. It is also found that the measurement results are in general agreement with the computer simulations. The poorer agreement in the QPSK results is attributed to an unknown measurement error.

It must be mentioned that these measurements are meant to be "proof of concept" of the new receiver scheme as the transmission data rate was only in the order of several Kb/s due to equipment limitations. Thus it is primarily the ADC resolution, instead of noise, that determines the minimum detectable signal level. On the other hand, the SPD used in the measurements is far from being optimum for receiver applications. Significant improvements in sensitivity can be expected from an optimized design of the SPD.

## CONCLUSION

A novel six-port direct digital receiver is presented, and it is found to be rugged to hardware imperfections that normally prevent conventional I-Q receivers from direct operation in microwave/mm wave bands. Computer simulation and measurements at 26.5GHz validate the new receiver scheme. This work outlines a cost-effective alternative to the conventional heterodyne receiver with the following advantages: 1) High yield of circuit due to decreased fabrication requirements. 2) Low power consumption due to simplicity of the whole receiver and lower LO power demand. 3) Flexibility to switch between different modulation schemes. 4) Less stringent bandpass filter requirements. And 5) The maximum data rate heavily depends on the speed of the DSP unit and A/D converter.

It must be mentioned that although the work described in this paper focuses on mm-wave applications, the DMR can be readily adaptable to lower frequency bands such as the UHF band.

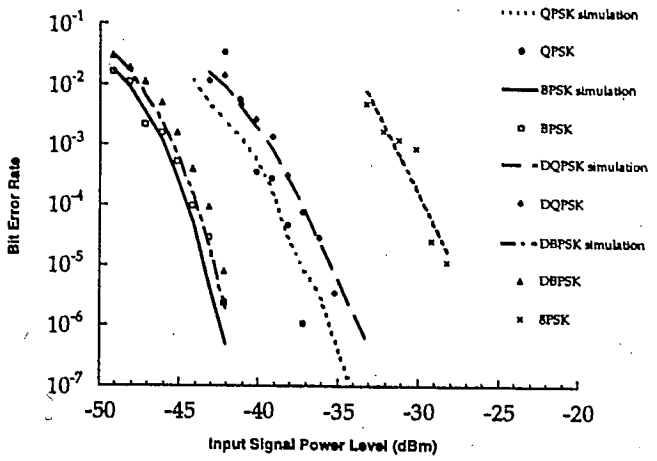



Figure 10. Measured and simulated BER performance of SPD for various PSK modulations.

## ACKNOWLEDGMENT

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