A REPORT ON THE RELIABILITY OF, AND OTHER ASPECTS OF, THE USE OF TRANSISTORS FOR A HIGH POWER UHF AMPLIFIER ON A COMMUNICATIONS SATELLITE

David M. Duncan

April 1975

Prepared for

Director General
Space Programs
Department of Communications
Ottawa
Ontario, Canada

under

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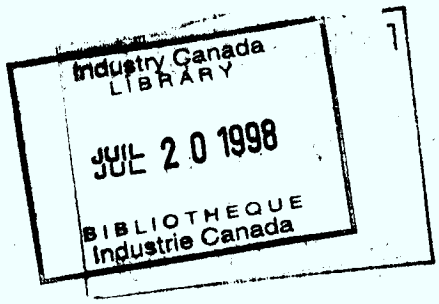

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INTRODUCTION

This report covers whether current state of the art RF power transistors can meet system requirements for a multiple carrier, high power, satellite amplifier with regards to reliability, power output, intermodulation distortion and efficiency. Then the report considers the question of how to do it.

Section #2 covers the step by step design procedure followed in developing a state of the art power transistor to ensure reliability, performance and manufacturability. Reliability hazards known or rumoured for this class of devices is covered in more detail in Section #3. Also covered is the high reliability processing procedures that need to be instituted for this application.

Section #4 considers the trade-offs which occur between, power output, the requirement to be able to vary power output, efficiency, intermodulation distortion and the modes of operation of various stages in the power amplifier. Also discussed are secondary circuits needed such as AGC systems, variable voltage supplies, and the need for much more data.

Then, in Section #5, the expected lifetime of the amplifier is considered. The questions of how many devices should be used, and if and how they should be combined are also considered.

Potential vendors are assesed in Section #6, and the report is concluded in Section #7. Appended to the report is the C.T.C. "Pre-seal Visual Inspection" specification and also a TRW Application Note on Gold Metallization. Also included with the report

are two C.T.C. publications. One covers reliability aspects of their devices and contains their MTF curves on their devices. The second one (Application Book #2.2.8.0A) is probable the best general publication available on the design of RF power amplifiers. This report was written to be used in conjuction with this book. Where topics overlap both should be read. Repetition is an indication of extreme importance. Also any references required will be found in this book. (Metallization references are given in the TRW note and the C.T.C. reliability book).

DEVICE DESIGN

Device design is a very empiric process in which the designer is trying to trade off between a mass of conflicting requirements. The three general areas of main concerns are:

I. Performance in the intended application(s)

II. Manufacturability

III. Reliability

In most cases there is generally more than one intended application for a given mask set. Also the designer will generally have a few experimental layers to try out his latest ideas, all of which impose more restrictions and compromises into the design.

The process is best illustrated by giving the normal step-by-step procedure followed in doing a particular design (with commentary on the significance of certain parameters).

STEP 1: SET SPECIFICATIONS

I. Decide RF performance specifications. (Power output, gain and efficiency at particular supply voltage and frequency).

II. Decide device configuration (common-base or common emitter) and whether to be internally matched. (Common-base traditionally gave higher gain than common-emitter and it also is considerably easier to fabricate a rugged die, particularly for high voltage operation. With internally matched modern packages this gain differential essentially disappears. Common-base stages are very difficult to forward bias, so are practically excluded from any linear type application. Common-base is the

way to make high power pulse parts. It is probably not possible to make common-emitter parts, for a 28 volt supply, work higher than about 1 GHz and manufacturers would rather be supplying common-base devices at these frequencies. At about 400 MHz or lower they prefer supplying common-emitter).

III. Decide package and Θ_{JC} MAX. (The choice of package immediately puts an upper limit on die size. Θ_{JC} tends to happen rather than be designed in i.e. the designer makes is as low as he can, subject to the constraints he is working under. It can be predicted quite early in the design process. If the prediction is unsatisfactory and there is room to increase the size of the die it can be lowered somewhat. Otherwise it is necessary to go to another package.)

IV. Decide DC specifications. The only DC specifications of any operational significance are, for common-emitter stages that the LV_{CEO} must be higher than the supply voltage (it is normally specified at 33 volt minimum for 28 volt operation) and for common-base stages that BV_{CES} be greater than the supply voltage. The only other purpose of DC tests should be to weed out faulty devices. The only DC parameter that occasionally causes problems between maker and user is if the user wants a very low collector emitter leakage current. There is a very common processing defect which results essentially in a bulk channel between collector and emitter. This defect

is no reliability hazard but it can result in currents of the order of many milliamps. Typically there are other DC specifications which I would class as traditional, which can be met easily though often some device performance was sacrificed to meet them.

STEP 2: DESIGN DIE

I. The first decision to be made is the number and size of the bond wires to be used. It is desireable for manufacturing and to minimize pad capacity to have as few wires as possible and as small a wire as possible. The limits on this process are set by the lead inductance you are left with and the current carrying capacity of the wires. With gold wires it is generally the inductive limit which controls while with aluminum it is the current carrying capability. Having decided the number and size of wires to be used we have, by manufacturing tolerance requirements, designed our bond pads on the die.

II. Having designed the bond pads, we now design the base cells which go between the pads. We will assume for the purpose of this exercise that it is a single long thin base running lengthwise across the die between two bond pads which it shares with the adjacent cells. This configuration is the most efficient use of silicon, certainly up to 500 MHz.

The designer know how much DC current each cell has to pass. He also knows from previous experience with this class of device, how much DC emitter current per unit emitter periphery the device will work optimally at. Consequently he calculates the total emitter

periphery needed in each base. The next decision is on the geometry of the internal basic cell within each base. This is the form that the emitter and the associated emitter and base contacts (and P+ if any) take and which is repeated throughout the base. These are normally fairly elaborate with differing names and each designer having his own favorite. The basic reason for the elaboration is to get the maximum emitter periphery per unit area associated with as coarse as possible oxide cut widths, alignment tolerances and metal finger width. The fundamental limitation is that if emitters are too wide, gain and efficiency suffer. Based on his experience, the designer comes up with a unit cell that he considers a satisfactory compromise between manufacturability and performance. We now have a unit cell of known size and known emitter periphery and known metal width. Hence, we know the DC current passed by one of the these unit cells and the total number needed each base. From the cross-section of the metal fingers we derive the maximum DC current we can pass along the emitter fingers to get a satisfactory life against electromigration failure (typical numbers used are 2×10^5 amps/cm^2 or 2ma/micron^2). Hence, we now know the maximum number of unit cells we can have along one emitter stripe. The initial tentative

design would be to use the maximum number of unit cells on each emitter stripe and then the number along the length of the base is known. We will assume this length is within what is allowed by the package. We now have a tentative base design where we know the internal structure and its dimensions. To this is now added to the peripheral structure. (P+ rings or whatever to control BV_{CB}, ballast resistors, busbars to connect the fingers to the bonding pads and give all the working tolerances). We now have the overall layout of the die which we again assume is within what is allowed by the package. The next step is to predict the θ_{JC} of the design. The easiest way to do this (other than with a suitable conPuter program) is to find some other device with a base the same width and hopefully the same length or half the length or a third the length etc. A large chip containing one or several of these devices is mounted in the intended package and one of these bases has DC power applied to it. By doing an extensive thermal map over this chip and then apply the principal of linear superposition we can predict what the θ_{JC} of the paper design we have done quite accurately. If the θ_{JC} and the calculated C_{CB} satisfactorily we now have a tentative design. If the θ_{JC} is unsatisfactory we have to make the bases longer and narrower (which also reduces the metal

current density) and/or seperate the bases further. Both these changes increase C_{CB}.

There is now an immense amount of detail work to come up with a working mask set design. Only two of these are of significance for reliabiltiy. One is that the structure should not be such that "necking" of stripes can occur. These are a function of optical second order effects both on the wafer and in the production of the work plates, the metal deposition process and the contours of the oxide surfaces over which the metal passes. The second procedure which helps reliability is grading the ballast resistors such that the temperature along each base and from base to base is more uniform than without the grading, thus reducing the peak temperature rise on the die.

STEP 3: TWEAKING IN THE DIE

After delivery of the working plates it becomes a matter of trimming in various process control parameters such as:

I. Starting material resistivity and thickness (affecting breakdown voltages power output and ruggedness mainly).

II. H_{FE} (affecting LV_{CEO}, gain and efficiency mainly).

III. Ballast resistor sheet resistivity (affecting ruggedness mainly for class C operation. For class A operation even higher values still are needed to increase the DC safe operating area, which will result in some reduction of gain.)

IV. For input matched devices the matching network is established to give a satisfactory compromise between gain, input impedance and manufacturability.

V. Reworking the masks or work plates to correct the inevitable errors, modify dimensions slightly and improve the resistor grading.

After this it is just a matter of putting runs through the line so that the alignment operators go through their "learning curve" on a new mask set and a better data base can be generated for establishing final specifications on the device and yield problems discovered.

MANUFACTURING AND RELIABILITY

In this section, manufacturing process where there are known reliability hazards or controversies will be considered.

Also the matter of package mounting on the heat sink and high reliability processing will be discussed.

I. DEVICE METALLIZATION

The dispute here is aluminum-copper-silicon alloy used by C.T.C.* versus titanium-tungsten, gold as used by TRW** The CTC process involves cold substrate evaporation of the alloy etching the metal pattern, alloying the metal and then over-coating it with C.V.D. silicon dioxide at about 400°. The TRW process involves sputtering platinum over the surface, forming platinum silicide in the contacts, etching off the unreacted platinum, sputtering tungsten-titanium alloy (approximately 10% titanium) and then sputtering gold. After metal etch I do not know what their process is.

The basic questions which have to be answered in this case are:

A. Is my expected M.T.F. satisfactory if I have "good" metallization on this particular device?

B. How do I know I have got "good" metallization?

In the case C.T.C. there are expected M.T.F. curves available. To my knowledge these C.T.C. curves are reasonable. For some TRW devices the M.T.F. curves are on the data sheet (e.g. for the JO2015 which is their direct competitor to the CM75-28). I am sure it could be obtained for their other devices if needed.

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** TRW Semiconductor, 14520 Aviation Blvd., Lawndale, CA. 90260

To the second question, have I got "good" metal, the answer is very easy to obtain in the case of C.T.C. devices. Put the wafer in a S.E.M. before the silicon-dioxide coating is applied and just inspect. If there are no tunnel, micro-cracks or peculiar etch-back phenomena where the metal passes over oxide steps or passes over the edge of the nichrome and the line width and thickness are within specifications, then you have good metal. There is not much else that can go wrong.

In the case of TRW's metal system I do not know how to evaluate the quality of the metallization. Obviously it has to meet the same requirements as the aluminum-copper-silicon, but I do not know how you evaluate the quality of the titanium-tungsten as a barrier layer against the gold geting in contact with the silicon and how you evaluate the adhesion of the gold to the titanium-tungsten; both of which can be severe reliability hazards.

This information can probably be found by talking to TRW and to users who have qualified TRW devices for high reliability programs. I do not want the above remarks to be construed as being negative to gold. My background is in aluminum systems and I know how to evaluate them. Gold systems have some additional problems which I do not know how to evaluate at this time. As anybody who has had processing experience will tell you, metal deposition and etching are probably the least well controlled processes in the whole of wafer fabrication and everybody's process goes haywire on occasions. I would consider a good gold system to be definitely superior to aluminum-copper-silicon.

II. BALLAST RESISTORS

C.T.C. uses nichrome which has no reliability problems that I know of which cannot be found with an S.E.M., provided it has glass over it to protect from the ambient in the package. TRW was using the tungsten-titanium layer as the resistor element. Again, provided this is passivated, I can not see any obvious reliability problems though I can see resistor control problems due to the low sheet resistivity of the titanium-tungsten. TRW is switching to diffused ballast resistors which they claim give increased reliability. The basis of these claims are that the resistors are better heat sunk (which is true but probably not significant) and that the resistors are proportioned so that they act as current limiters when the peak current rating of the device is exceeded. This certainly can be done and should improve ruggedness. This might also have interesting effects on intermodulation distortion.

III. DIE ATTACH

A nearly void free die attack is essential for a reliable device. C.T.C. discovered 2-3 years back the cause of the problem was impurities in the gold plating on the header. The only way they were able to bring the problem under control was to do their own plating. No outside vendor had this problem under control. Since that time they have had very little problems with voids in their die attach. TRW apparently still has the problem as in a recent discussion, they admitted that on their

microwave product line (which must be assembled as a pill i.e. with no stud or flange present during assembly but added afterwards.) they 100% X-ray all devices after die attach and rework the bad ones.

Whoever supplies the devices, they must be screened for bad die-attach. The non-destructive tests are:

A. V.S.W.R. testing (the bad ones only self-destruct if the die has sufficient intrinsic ruggedness.

B. X-ray on a 100% basis (this is only possible on a pill type package.)

Destructive tests are:

A. X-ray on stud or flange type packages (the stud or flange has to be removed before the X-ray is taken).

B. Hammer the die off the header. (It sounds crude but it works.)

C.T.C. 100% V.S.W.R. test all their products in these frequency ranges and are happy to do any X-ray work required. TRW is willing to V.S.W.R. test these days and do thermographic scanning and X-ray work. In the case of TRW I am not sure that V.S.W.R. testing will detect bad die attach as they have apparently been developing techniques which prevent high dissipation during V.S.W.R. The diffused ballast resistors are one of these methods and apparently they have another which works uner the high voltage condition.

IV. BOND WIRE AND WIRE BONDS

I know of no inherent reliability hazard in any of the bonding systems used. Purple plague is not one in the

situation where aluminum wire is bonded to the headers. Some claims have been made that there is a hazard in the matched devices of TRW where the bonds are passed over a glass rod. If there is any interest in using these devices, thermal cycling tests should rapidly clarify the matter.

All devices should have every bond inspected during the the precap visual. In the sample out of each batch manufactured that is destructively tested, bond pull strength measurements should be made.

V. PACKAGE SEALING TECHNIQUES

C.T.C. offers only packages that have a ceramic cap epoxied to the header. Apparently they have had no problem meeting high reliability specifications with this seal. TRW offers similar packages and also some hermetic packages for some devices.

VI. OTHER PACKAGE PROBLEMS

Leads have been known to fall off packages and voids have been found in the braze between the header and the stud or flange. I think that the quality standards used by the transistor manufacturer on incoming headers be checked. Lead pull strength and voids in the braze should be checked on a sampling basis.

VII. PACKAGE MOUNTING TECHNIQUES

As was mentioned earlier, most packages are available in stud, flange or pill form. There are difference in the junction to heat-sink thermal

resistances, stud being worst and pill the best. In some cases the improvement in thermal properties, with consequent expected increase of MTF, or the ability to 100% X-ray the die-attach may dictate the use of a pill package.

Now the user has the problem of generating a void free braze between the metallized bottom of the ceramic and the heat-sink.

A process that will give a void free braze except for a few small one at precisely controllable locations is as follows:

A. Pre-tin using the solder to be used (either gold-tin eutectic, or tin silver eutectic) the surfaces to be mated.

B. Put in brazing jig with small pieces of wire of the same alloy separating the pill and the heat-sink at points around the periphery where small voids will not matter.

C. Place in a vacuum oven until the solder melts.

D. Cool and remove.

The only voids that occur are where the pieces of wire were. The pieces of wire keep the two parts separated until they reach the melting point. This enables the vacuum to get rid of all entrapped gas.

If this process is used the heat-sink must be made of a material that is a composite of copper and tungsten. This material has the same expansion coefficient as BeO and about 80%

of the thermal conductivity of copper. If pure copper is used the braze will separate under thermal cycling due to the soft nature of the tin alloys.

VIII. HIGH-RELIABILITY PROCESSING

Both TRW and C.T.C. are willing to do almost anything to satisfy customer high-reliability requirements. The both suggested practically the same kind of processing.

A. S.E.M. qualification of wafers to be used, criteria being metal, resistors, alignment and whatever else.

B. Then 100% processing as follows:

(1) Precap visual. In some cases this is done by the customer. Copies of the standard C.T.C. precap visual specification is included. These could be tightened if desired.

(2) High Temperature Storage (e.g. 24hr at 150°).

(3) Temperature Cycle (e.g. 65°C to 125° @10 cycles).

(4) Centrifuge (20 Kg).

(5) Time leak test (1×10^{-7} ATM cc/sec).

(6) Gross leak test (1×10^{-5} ATM cc/sec).

(7) HTRB (168 hr.).

(8) Burn-in (168 hr.).

(9) Total electrical.

(10) Die attach check (if not V.S.W.R. probably somewhere else in the test sequence).

On a sampling basis, at least the following destructive tests should be run;

(1) Die-attach X-ray - (if not done on 100% basis).

(2) Lead pull strength on the package.

(3) Ceramic - to base braze voids (if not pill package).

(4) Wire bond pull strength.

EFFICIENCY, INTERMODULATION AND CIRCUIT DESIGN

In this section we will consider the inter-relationship between efficiency, intermodulation, circuit design and system requirements. We will use as our data base for this section, the report "A Study of Low Intermodulation Transistor Power Amplifiers" by R. G. Harrison and H. J. Moody. We naturally will accept all their measured data and also will accept that their computed predictions of behavior when the number of carriers increase beyond 4 are probably reasonably valid. We will also make the assumption that the behavior does not change significantly as the number of carriers is increased above 36 and that the efficiencies and gains achievable should be similar to the 4 carrier data at these higher numbers of carriers. We will make other sweeping assumptions along the way, as we need them.

Our starting point is system requirements. At start of life the transponder should be able to deliver 100 watts which correspond to something like 80-90 channels with a minimum EIRP of 30.5 db (1.1 watts). Under eclipse conditions the transponder should be able to reduce its power demand by 50% by reducing the number of channels it is carrying. To cope with end of life conditions as well, we will make the initial design objective that the transponder should reduce power consumption as close to proportional as we can make it down to 25% of its initial capacity. If actual traffic at any time is below 25% of initial capacity we do not care what the EIRP of the various channels are as long as they are above the minimum and the intermodulation requirement

is met and the power consumption does not rise above what it is at the 25% level. Whenever the traffic level is above the 25% level the power output of the individual channel should be as close to the minimum nominal levels as we can make them otherwise we are losing channel capacity at some time in the life of the satellite.

The other basic system requirements are that intermodulation does not get above -16db and that transponder bandwidth (for gain, power output, efficiency and intermodulation performance) be at least 2MHz for 25KHz channel spacing or for 4MHz if 50KHz channel spacing.

Consider now the design of the ouput stage. If we have a driver that is sufficiently low in intermodulation that the system requirement of less than -16db can be met by an output stage specification of less than -17db we can work with a class C output. This is desireable because of the higher efficiency of class C stages. To do this with the CM75-28R the input has to be restricted to the range of 38dbm to 43dbm which gives an output power range of 42.8dbm to 49.6dbm and efficiencies of 37.4% and 58.8% respectively. As can be seen the 49.6dbm is just about the required maximum transponder output power and the lower limit of 42.8dbm corresponds to 25% of initial capacity. Hence, by building into the transponder a compressor-HEC type system which holds the ouput level of the transponder at 42.8dbm for all traffic less than or equal to 25% and then keeps the system gain constant for higher traffic capacity we have a transponder that meets our system requirement.

The problems with this design are that:

(1) It is marginal on the intermodulation at full output and at 25% capacity. At less than 25% usage the intermodulation stays constant but the EIRP of each channel rises, hence improving the system s/n ratio.

(2) We may not be able to build a driver with any efficiency that has the required intermodulation.

(3) The DC power consumption of the final stage goes from 155 watt at full output to 51 at the 25% and less condition. This means that between normal and eclipse conditions there will have to be more than a 50% reduction in traffic capacity to meet our goal of 50% reduction of DC power consumption.

(4) This problem of power consumption not falling off nearly as rapidly as power output is due to the fall-off in device efficiency as power output drops. There is a way of reducing this problem. The output stage collector supply (and probably also its driver) is derived from the separate regulated supply which is connected to the AGC-compressor system such that the collector voltage is reduced as the power output of the transponder is decreased. This will help maintain the device efficiency as power output drops and consequently gives greater channel capacity as available power decreases. It would appear that it should be still possible to meet the intermodulation specification while doing

this.

If the intermodulation is too marginal then we have to go to one of the forward biased modes of operation such as class L. Here we have intermodulation in the output stage less than 20db at all input levels below 40dbm. The power output of the CM75-28R is 46.8dbm at 40dbm input which means that we need two of them in the final stage to get our required output. The efficiency at full output is 42.5% so we will need a DC input to the final of 224 watt with the efficiency at a 6db reduction in output dropping to 24%, so at the 25% level our power consumption is still 99 watts.

We have the situation that 2db of intermodulation improvement cost us nearly 2db of DC power.

We will not continue to calculate the tradeoffs involved in the design of a continuous service transponder such as this one because we do not have sufficient data to be meaningful. However, the general nature of the problem is very apparent.

The starting point of the design is DC power available under eclipse conditions at end of life. If the transponder is required to have a fixed traffic capacity over the whole of its life then it is designed on the basis that it radiates

at its designed total output power over the whole of its life (unless there is no traffic). An AGC system keeps the total radiated power constant whether is one channel or the maximum number of channels. The output stage and drivers are designed to give the best overall compromise between efficiency and intermodulation performance required at a fixed total power level and with a varying number of channels.

If it is desired to increase the system's channel capacity at times when there is greater power available than the compromise becomes much more difficult if it all has to be done in the one transponder with no switching. As the output device is operated over a wider power range its worst case intermodulation gets worse. Consequently if there is any problem meeting the intermodulation specification we probably have to go to a lower efficiency type of stage to get the required performance. In addition we get a marked drop in efficiency of the output stage as its total power output is decreased. Even though we can minimize this by decreasing collector supply voltage, we are still left with a considerable decrease in efficiency at our lowest power consumption. Essentially for a given power supply we can

trade channel capacity early in life for channel capacity later in life.

Another possible way of designing the final stages of the transponder so that the available power output varies with the condition of the power supply, which would probably gives a much better compromise on efficiency and intermodulation than the previous approach, is as follows:

The collector supply for the final stage and (probably its driver) is derived from a regulated supply (or maybe even directly from the unregulated supply) and is varied such that the power drain of the transponder equals what is available from the supply. Simultaneously the AGC system keeps the stage at the total power point where it has best intermodulation characteristics. Essentially what we are doing is varying its collector supply voltage. At any given supply voltage it radiates at constant power no matter how many channels it is carrying and is working at the operating point for that supply voltage which gives a good compromise. intermodulation characteristic.

Essentially it boils down to the fact that to make a single transponder work efficiently and

with low intermodulation over a reasonable range of pwer consumption, requires a fairly complex AGC system which also varies the collector supply voltage of the final stage. Whether we get any overall system advantage from this approach relative to having a transponder which operates at constant output power of the whole of its life requires more data than we presently have.

We will list what additional data is needed before it is possible to commence actual design work on the transponder final stages.

A. Class AB operation needs to be evaluated

Class AB operation is where the device is forward biased to the point where it is drawing a standing of the order of 1% of its maximum operating current. For this application the standing current is probably of no significance in terms of power consumption. The performance with two-tone intermodulation is to give better than -30db over a wide range of power levels. I have no information on how it performs with a large number of tones but suspect that it would probably at least equal Class L's best over a much wider range of input power. Consequently it may be a good candidate for a variable power output stage and probably also as a lower level driver stage where intermodulation is

more critical and efficiency not so important. C.T.C. makes a special device for biasing this kind of stage called a Byister. This device provides the correct thermal tracking of the bias to prevent thermal runaway. It needs a DC current drive of about 350 ma and has voltage drop on the order of one volt. Provided an efficient constant current power supply can be designed, the power consumption of the biasing circuit should be tolerable.

B. We need to know over what band-width the low intermodulation characteristics of class-L can be obtained. The band-width obtained by RCA was not adequate for this application. I would suspect that by designing the stage for much greater amplitude band-width, the inter-modulation band-width would be increased correspondingly.

C. Operation at lower supply voltages should be explored thoroughly. On the CM75-28R it appeared that efficiency was increased by reducing supply voltage and so apparently there is an optimum supply voltage for efficiency which should be the starting point for any design due to the crucial nature of efficiency in this application.

The efficiency that should be used to

compare efficiencies in this class of application is the so-called oscillator efficiency

$$\eta_o = \frac{\text{AC power out - AC power in}}{\text{DC power in}}$$

$$\eta_o = \eta \frac{G-1}{G}$$

When η= AC power out / DC power in.

G= Stage gain.

η_0 gives the overall system efficiency if an amplifier was made up of an infinite number of stages with identical gain and efficiency and is consequently more relevent than normal efficiency for comparing devices for this application. It is also for common emitter stages, a much better measure of the actual efficiency with which the die is converting DC power to RF power as most of the input power passes straight through to the output via the emitter lead inductance.

Besides finding out the most efficient supply voltage investigation should be made of performance at considerably lower supply voltages with the stage optimized for performance at the most efficient supply voltage.

D. Data needs to be taken of all likely candates for output stages and driver stages for

all the modes of operation of interest. This list can be weeded down very quickly. Probably only unmatched parts should be considered for reasons that will be discussed later.

It should be possible to obtain from suppliers, devices which have much higher gains and efficiencies than the catalogue devices for this application. CTC has a new range of die intended for use at frequencies a bit less than 1 GHz. These die would not be rugged for 300 MHz, 28 volt operation, but by reducing the supply and/or modifying the die this problem can be overcome. I am sure that TRW could do similar. In the case of the new CTC die the amount of evaluation needed should be reduced as the die are fabricated as "Power-Blocks". For example, they have 10 watt "blocks" so a 10 watt device has 1 "block" and a 40 watt device has 4 "blocks". In consequence, once you have characterized one device you have, for many parameters, also characterized several other devices.

E. Data needs to be obtained on the overall intermodulation characteristics of multi-stage amplifiers.

F. Data needs to be obtained on the inter-modulation characteristics of differing carrier

levels.

G. Data needs to be obtained on the effects of deliberately increasing the emitter lead inductance on unmatched devices. CTC claims that this increases system efficiency and improves intermodulation and is used by TRW Systems in FLEET SAT COM.

DESIGN OF THE OUTPUT STAGES

In this section we will go into whether the output stages should be as few and as large as possible devices or many small devices, whether these should be internally matched or not, how or if they should be combined, what mean time to failure to expect due to electromigration, other failure mechanism, whether the circuitry should be broadband or narrowband, weight, volume and trade-offs, etc.

I. MTF DUE TO ELECTROMIGRATION

We will calulate the expected MTF for the two specific output stage designs discussed in the previous section.

A. Class C using a single CM75-28R.

RF power output = 91.2 watt.

DC input power = 155.1 watt.

RF input power = 20.0 watt.

Power dissipation = 83.9 watt.

Collector current = 5.54 amp.

θ JUNCTION TO HEATSINK = 0.9°C/watt.

Junction to heatsink temperature rise = 75.5°C.

Junction temperature (at 55°C heatsink) = 130.5°C.

MTF at 130° and I_C at 4.5 amps = 570,000 hrs.

MTF at 130° and 5.54 amps = 380,000 hrs.

This probably is an adequate margin and also is probably the worst case ever likely. By going to a pill package the thermal resistance would be decreased by 0.1°C/watt and MTF would be increased by 50%.

B. Class L using a pair of CM75-28R.

RF power output = 47.9 watt.

DC input power = 112.6 watt.

DC current = 4.02 amp.

RF input power = 10 watt.

Power dissipation = 74.7 watt.

Junction to heatsink temperature = 67.2°C.

Junction temperature (@ 55°C heatsink) = 122.2°C.

MTF at 122°C and at 4.5 amps = 800,000 hrs.

MTF at 122°C and at 4.02 amps = 1,000,000 hrs.

As is apparent, electromigration does not appear to be a major hazard but has to be watched. Lower voltage operation would considerably reduce the dissipation per die.

II. OTHER HAZARDS

Assuming that correct mechanical and thermal techniques have been followed in mounting the transistors, the only other possible causes of device failure are too high a collector supply voltage, high voltage spikes on the collector supply or high VSWR loads. The over-voltage and spike problem can be taken care of either in the design of the power supply or with protective zeners. The high VSWR problem really only exists during the testing and installation phase in this application. Once in operation, any condition which causes a high VSWR load has already put the amplifier out of action.

The only other components used in design of this class of amplifier, whose ratings are being pushed hard, are the chip capacitors used right at the input and output of the transistors. Devices delivering 100 watt at 400 MHz have been known to destroy

these capacitors. Consequently if the final design involves high power devices the temperature rise on these capacitors should be checked and more capacitors in parallel used if it is excessive. In fact, for an application like this, it is probably a good idea to thermally scan the whole high power stage to find any potential problems.

III. THE NUMBER OF OUTPUT DEVICES AND COMBINING

As can be seen from the earlier sections, there is a possibility that the output stage could be a single device. However, the probabilities are that it will require more than one, and it may be desireable to make it considerably more than one.

Splitting the output power over several smaller devices rather than one larger device should result in the smaller devices having a longer MTF than the single larger device. The reason for this is that they should run cooler. If you put two identical die side-by-side in the same package the thermal resistance of the pair is not 1/2 that of a single die by itself due to the cross-heating ("linear superposition" again). In practice, for catalogue devices, this is not necessarily true. Typically lower power devices offered are older designs and possibly may even run hotter than later larger devices particularly if they are in stud packages. To get this increase in MTF it is necessary to look closely at the die type and package used.

Whether designing an amplifier with a larger number of devices with a longer MTF for the devices results in a longer MTF for the whole amplifier I do not know as I don't know how to do that kind of reliability analysis. This is on the assumption that the

devices are paralleled and that the failure of one device will result in the failure of the system (which is not necessarily true).

To ensure that the failure of one output device does not cause major disruption to the system it is necessary to use combiners. The biggest problem with combiners is the way the output power of the system drops off as amplifiers fail. This is illustrated in Table I.

TABLE I

Number of Amplifiers Combined	2	3	4	5	6	7	8	9
Power Loss When 1 Amplifier Fails (db)	6	3.5	2.5	1.9	1.6	1.3	1.2	1.0
Power Loss When 2 Amplifiers Fail (db)	-	9.5	6	4.4	3.5	2.9	2.5	2.2

Just from examining Table I it is apparent that the number of amplifiers that you would want to combine is probably in the region of 3 - 9. As the number of amplifiers goes up the size and weight and losses in the combining network all go up. As it is obviously only possible to split and combine once in the satellite, we would have to be sure that the driver, before splitting, had a much higher MTF than the final stages. This, in turn, means that this driver is probably fairly low power and that we probably need about 20 db gain in each module. Consequently, we are talking about a 2 or 3 stage module. This in turn means that these modules will have to be constructed very carefully, as any phase shift and amplitude differences between them will result in power loss in the combiner.

This requirement of having a 2 or 3 stage module with very close match of amplitude and phase characteristics can probably be met by using broad-band microstrip construction techniques

and closely matched discrete components and good thermal coupling between the modules.

There are basically two combining methods that can be used here; 90° hybrids and Wilkerson combiners. 90° hybrids can only combine two amplifiers at a time, so to combine 4 amplifiers requires 3 hybrids and to combine 8 amplifiers requires 6 hybrids. The same number of hybrids is also needed to split the input signal. The losses per hybrid are typically about 0.2db so combining 4 amplifiers gives us a loss of 0.4db and combining 8 amplifiers gives us about 0.6db. For a narrowband application such as this it may be possible to obtain lower insertion loss with careful design. Each hybrid require a terminating resistor which must be able to dissipate 1/2 the power coming into one of the input ports.

Wilkerson combiners are probably more compact and lower loss than hybrid combiners. They are narrow band, but that is no problem in this application. In theory, they can combine any number of stages, though their losses go up and their bandwidth becomes narrower as the number increases. Consequently, if combining a large number of amplifiers, it probably should be considered whether to do it in more than one stage. A Wilkerson combiner has a "star" connection of 50 ohm resistors to each input port with the common point of the resistors floating. Each resistor has to be able to dissipate half the power coming into one port. This resistor arrangement is awkward. However, it is possible to remotely site these resistors away from the input by using coaxial cable and by using this cable as a transmission line transformer. The outer conductor of the coaxial cables

can be grounded at the terminating resistors.

Both the Wilkerson combiner and the 90° hybrid, when one amplifier fails, isolate that amplifier's output terminal from the other amplifiers and leave the reamaining amplifiers working into a good 50 ohm load. Both, when working as splitters, do not isolate the other output ports and the driver from changes in the load presented at one of the output ports. Consequently, depending on the probability of a disruption of the input impedance of a module (most module failures would not have a large effect) and the method of splitting (a single stage Wilkerson will still give identical drive to the remaining stages; all others will not) it may be necessary to use circulators at the input of each module. Circulators as small as 2" x 2" x 1" and weighing 10 - 15 ozs. can be obtained from Western Microwave. However, I think they probably can be avoided.

The design of the AGC system has to be such, that if a module fails, the input power to the surviving output devices is still at its correct level for intermodulation performance and the loss of output power effects the system as a loss of traffic capacity, not a loss of S/N ratio.

If it does turn out that it is desireable to deliberately increase the emitter lead inductance to improve efficiency,

then it will definitely be necessary to use unmatched devices, which in turn limits them to being, at the most, 40 - 50 watt devices.

The use of multiple output stages and combiners would

definitely increase the size, mass, and complexity of the transponder; as well as produce a slight loss of efficiency, which are being traded off against increased reliability.

SUPPLIERS

The potential suppliers for a program such as this are:

I) CTC

II) TRW

III) Motorola

IV) RCA

Between them, CTC and TRW have the vast majority of the market, are qualified in many high-reliability and satellite programs, and make the best state of the art devices. These are the only suppliers that can be seriously considered.

Motorola is well behind the state of the art in performance (though you would not think so from their advertising) and does not have any significant market position.

RCA has essentially dropped out of the RF business. They have stopped all development and application's support and are continuing to manufacture products which they can make profitably, while the demand lasts. Their customers, in consequence, are feverishly seeking second sources or designing them out as fast as they can.

CONCLUSION

We have examined the following topics:

I. How to design a device to ensure both performance and reliability.

II. How to monitor the manufacturing process to ensure that we obtain reliable product.

III. How to design the output section of the transponder to meet system requirements.

IV. How to implement some aspects of the design of the output section to enhance operational life.

The conclusions that came out of this study are:

I. It appears feasable to build a single transponder which will carry a large number of channels with adequate intermodulation performance, lifetime and efficiency.

II. It is much easier to build a transponder which operates at a constant power output level controlled by the minimum available DC power, over its life, rather than one which varies its power output and channel capacity to take advantage of higher available DC power, available most of the time.

III. On the basis of the data which we have at this time, the loss of efficiency associated with the variable power feature may almost negate the advantages of this feature. However, there is so much data lacking that to make even a reasonable first attempt at a variable power transponder is impossible

at this time. With more data it may turn out that the variable power transponder is worthwhile.

IV. A tremendous amount of data will have to be taken before it is going to be possible to design anything like an optimum fixed power transponder, much less a variable power transponder.

PRE-SEAL VISUAL INSPECTION

1. PURPOSE

The purpose of this test is to check the internal materials, design construction and workmanship of semiconductor devices just prior to seal. The inspection is normally performed on a 100% basis as required by the contract.

2. APPARATUS

Low power microscope 20 - 80X
Metalurgical microscope 50-600X

3. PROCEDURE

The devices shall be examined under low magnification (less than 80X) for inspection of die attach and wire bonds and under high magnification (greater than 80X) for inspection of the semiconductor die.

3.1. Inspection of die attach and lead bond is as follows:

3.1.1. Ultrasonic bonds on the chip must be centered over pads with $\geq$ 50% of the bond on the pad.

3.1.2. Wire deformation must be between 1.2 and 3.0 times the wire diameter.

3.1.3. The wire must have a sufficient loop to clear the edge of the chip by at least two wire diameters.

3.1.4. DIE ATTACH

Gold silicon entectic must be visible around the

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1	Complete revision		10/4/3	

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PRE-SEAL VISUAL INSPECTION

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CHK'D:	SUPERSEDES	
ENGR. APPR.:		

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entire chip. Gold should appear smooth around the die (not granular).

3.2. Die inspection criteria.

3.2.1. METALLIZATION DEFECTS IN FINGER AREA

A die must have greater than 5% of the total emitter fingers affected by the defects as specified in 3.2.1.1 through 3.2.1.6; before it is considered a reject. The 5% can be an accumulation of all defects. (See Table I for die type and number of fingers).

3.2.1.1. METALLIZATION SCRATCHES

Any scratch in the metallization which reduces the width of the finger metal to less than 50% of the original width.

3.2.1.2. METALLIZATION LIFTING

Any evidence of lifting, peeling, or blistering metal.

3.2.1.3. METALLIZATION MISSING

a. Any void in the metallization which leaves less than 75% of the original metal on the finger.

b. Any void in the metallization over an oxide step (due to preferential etching) which leaves less than 75% of the remaining metal undisturbed.

3.2.1.4. FINGERS ISOLATED

Any finger which is not continuous through the nichrome resistor to emitter bus. May be due to blown resistor or preferential etching at nichrome - metal interface.

3.2.1.5. METALLIZATION ALIGNMENT

Any contact which has less than 75% of its width covered by the metallization.

3.2.1.6. METALLIZATION WIDTH ON FINGER

Any metal finger width narrower than 75% of its original design width. Under a low magnification, an undercut finger will normally appear as a darkened stripe.

NOTE: (1) An acceptable finger width normally appears as a light colored stripe with well-defined edges.

(2) Certain types of die may have darkened fingers under a low magnification and yet be acceptable. (See Table II for die types).

3.2.2. GENERAL METALLIZATION DEFECTS

No die shall be acceptable which appears to exhibit any of the following:

3.2.2.1. BONDING PADS

Any pad which has more than 15% of the metallization missing, lifting or blistering.

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3.2.2.2. EMITTER AND BASE BUS BARS

a. Any severe scratch which reduces the width of the bus bar to less than 90% of the original width. A severe scratch is one which exposes the underlying surface.

b. Any bus bar which has more than 10% of the metallization missing.

3.2.2.3. METALLIZATION BRIDGING

Any metal that bridges more than 5% of the total emitter fingers.

3.2.3. SCRIBING AND DIE DEFECTS

No die shall be acceptable which appears to exhibit any of the following:

3.2.3.1. CRACKED OR CHIPPED DIE

Any crack or chip from edge which extends greater than 50% toward any metallized pattern or other active portion of the die.

3.2.3.2. ATTACHED PORTIONS OF ADJACENT DIE

Length - Any die having attached portions of adjacent die which contains metallization.

Width - Any die having attached portions of adjacent die.

3.2.4. GENERAL

No die shall be acceptable which appears to exhibit any of the following:

3.2.4.1. FOREIGN MATERIAL

a. Any ink marks on surface of die.

b. Any foreign matter larger than 5 mils in any direction which can not be removed by a nominal gas blow (approximately 20 psig.)

3.2.4.2. PROBE MARKS

Any die which does not have probe marks on a base and emitter pad.

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PRE-SEAL VISUAL INSPECTION

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TABLE I

DIE TYPE	NUMBER OF EMITTER FINGERS TOTAL EMITTER FINGERS	MAXIMUM NUMBER OF DEFECTIVE FINGERS ALLOWED
A3-12,28	13	0
A25-12,28	200	10
A50-12,28	240	12
A65-12	240	12
A70-28,80	240	12
A150-12,28	984	50
S10-12,28	200	10
S30-12	240	12
S70-12	1216	60
S80-28	1216	60
S150-28	984	50
S150-50	1216	60
B3-12,28	32	2
B12-12,28	90	5
B25-12,28	200	10
B40-12,28	492	25
B70-12,28	896	45
B80-12,28	1216	60
C1-12,28	18	0
C3-12,28	36	2
C12-12,28	108	5
C25-12,28	220	11
C30-12	336	17
C40-12,28	336	17
C50-12	240	12
C50-28	528	26
C60-28	240	12
C75-28	1368	68
C80-12,28	360 (per die)	18
D1-28	18	0
D3-28	36	2
D10-28	108	5
D20-28	220	11
D40-28	336	17

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TABLE II

DIE TYPES WHICH MAY HAVE DARKENED FINGERS AND YET BE ACCEPTABLE

C50-12 (STD)

C50-28 (CD2007)

C60-28 (All types)

C80-28

C80-12

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1	Complete revision		10/4/73	[illegible]

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ENGR. APPR.:

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CHANGE —

TRW® SEMICONDUCTORS

A study of the advantages of GOLD METALLIZATION in the manufacture of microwave transistors

M. FLAHIE - M. WEISS

ABSTRACT

The development of a high reliability metallization system for R.F. power transistors has been TRW Semiconductor's continuing primary R&D and Manufacturing priority.

This priority, of course, is a necessary part of TRWS' goal to sustain its leadership in R.F. power transistors by continually advancing the state-of-the-art in power and frequency.

This report summarizes the reasons for TRWS' commitment to a GOLD metallization system for the manufacture of high power microwave transistors.

The conclusions are that the GOLD metallization system is superior to ALUMINUM systems in the following respects:

* Electromigration resistance
* Temperature stability
* Corrosion resistance
* Mechanical strength
* Oxide step ocverage
* Manufacturability

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SECTION 1 - ELECTROMIGRATION

The phenomena of electromigration occurs as follows.[1] For any given temperature, a certain equilibrium concentration of vacancies exists in all metal films. Self diffusion of metal ions throughout the film will arise due to the metal ions being thermally activated from their normal lattice sites into adjacent vacancies. In the absence of any external forces, the metal ion diffusion will be isotropic and will result in no net accumulation or depletion of mass in any given site. Upon the application of an electric field, however, the thermally activated metal ions will experience a force due to their charge and the electric field induc ing an ion flux toward the cathodic end of the film. In addition, the conduction flow of electrons in the metal due to the electric field will cause electron scattering off the activated ions and impart momentum to them inducing an ion flux toward the anodic end of the film. In good conductors, the momentum exchange force dominates the electrostatic force. This results in a net mass transport toward the anodic end of the film.

In the case of device interconnections, the net flux of mass due to momentum transfer causes void formation at the negative terminals. This void formation causes eventual contact opens resulting in destruction of the device. Void formation, hence, device failure, is accelerated by high temperatures (i.e., more metal ions will be activated) and high current densities (i.e., more electrons will collide with the activated ions and impart more momentum to them).

A simplified theory, Black[1], describing this phenomena provides the following expression for Median Time before Failure of device interconnections:

$$MTF = \frac{\omega \cdot t \; e^{\phi/KT}}{CJ^2}$$

Where
- ω = Stripe width
- t = Stripe thickness
- J = Current density
- ϕ = Activation energy for self diffusion of the metal
- K = Boltzmann's constant
- T = Temperature in °K
- C = Constant depending on degree of film crystallinity, resistivity, ion mass, density and stripe geometry

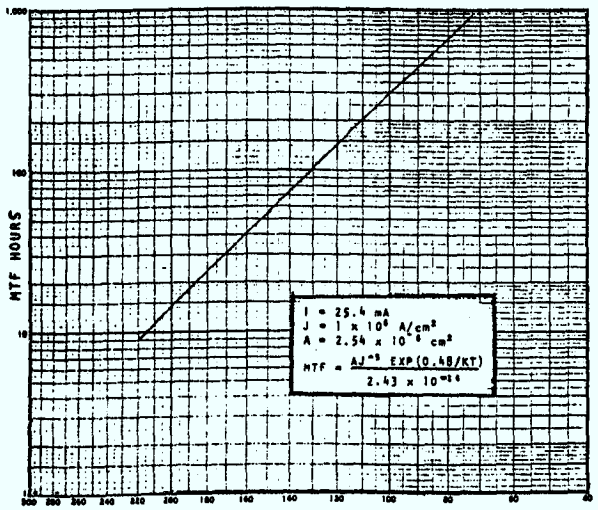


Figure 1

ALUMINUM SYSTEM

Figure 1 shows the expected best case MTF for an ALUMINUM stripe 1μ thick by 2.54μ wide, with a current density of 10^6 amps/cm^2 at various temperatures.

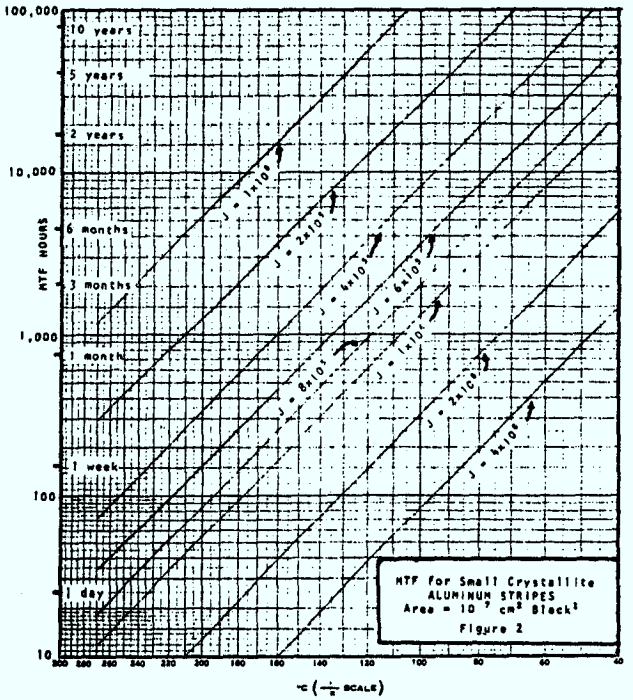
Figure 2 shows the effect of current density and temperature on life time of small crystallite ALUMINUM, Black[1].

GOLD SYSTEM

In order to increase the MTF of devices, two options exist:

1. Reduction of current density and/or device temperature.
2. Selection of a metal with a higher activation energy and higher mass (since electromigration is a momentum transfer process between the conduction electrons and metal ions thermally activated out of the crystal lattice).

Current density reduction cannot always be exercised due to device performance limitations (i.e., prerequisite geometry for frequency response considerations, etc.). Reducing the thermal stresses is possible; however, practical limits still make critical demands on the metallization. Utilization of a metal with a higher mass and activation energy is the remaining approach to increasing MTF.



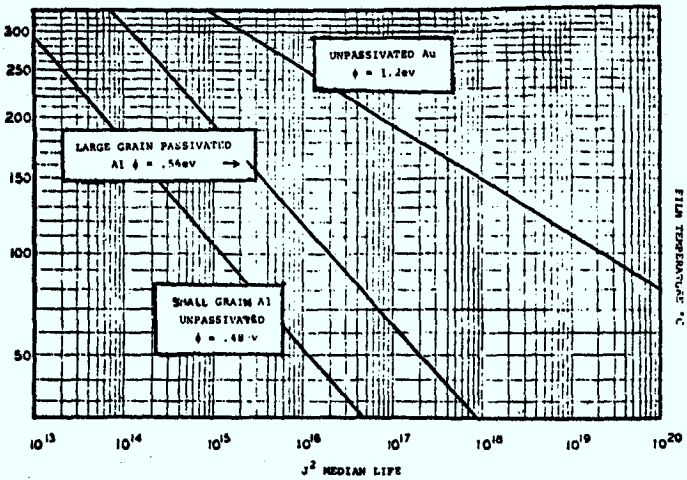
GOLD is preferred as the main conductor due to its high activation energy for self-diffusion, high mass and density, resistance to oxidation and corrosion, facility of chemical pattern delineation, and ease of lead wire bonding. Unfortunately, GOLD cannot be used as single layer metallization system due to its poor adherence to both Si and SiO_2, and the low Au-Si eutectic temperature of 367°C. To prevent the GOLD from alloying with the silicon, a barrier metal layer must be employed.

The composite system PtSi-Ti-TUNGSTEN-GOLD* meets all the aforementioned requirements for a superior metallization system. PtSi is used to provide a stable, ohmic contact to silicon. The TUNGSTEN layer is also used as a barrier against GOLD diffusion into, and eutectic alloying with Si, as well as to provide adhesion of the GOLD to silicon and SiO_2. Extensive investigation and life testing of the GOLD composite system has been done by TRW Semiconductors and others.[2,3,4,5,6]

The following discussion, figures, and tables (sections 1-5) are a summary of these investigations.

Figure 3 compares unpassivated small grain ALUMINUM and passivated large grain ALUMINUM to unpassivated TUNGSTEN-GOLD composite metallization.

The lifetime improvement for GOLD vs. ALUMINUM is dramatic, as shown in Table I. For example, the improvement is nearly two orders of magnitude in lifetime for GOLD vs. large grain ALUMINUM (passivated), even at an extreme of 200°C, and over three orders of improvement at 100°C. The data used to compile Figure 3 and Table I was obtained by accelerating the failure with high currents being passed through 0.5 mil by 13.5 mil dog bones[2] and using actual transistor structures.[7]



* First developed by Texas Instruments and described in U.S. Patents 3,575,570 and 3,601,666 and U.K. Patent 1,265,896.

TEMPERATURE °C	MEDIAN LIFETIME IMPROVEMENT	
	GOLD VS. SMALL GRAIN ALUMINUM UN-PASSIVATED	GOLD VS. LARGE GRAIN ALUMINUM PASSIVATED
200	1,250 TIMES	88 TIMES
150	4,750 TIMES	264 TIMES
100	17,000 TIMES	1150 TIMES

Table I.

A life test under severe conditions is under way at TRW. Identically processed, actual transistors made by both ALUMINUM and GOLD processes are base-emitter forward biased such that Tj = 200°C and $J = 1.4 \times 10^6$ A/cm^2. After 197 hours, 50% of the ALUMINUM transistors had failed. At 272 hours, all had failed due to open metallization.

At this writing the GOLD units have survived over 9000 hours of testing without degradation (as evidenced by regular power, gain, and leakage tests). This establishes 30 times life improvement for GOLD over ALUMINUM (a mathmatical model indicates 100 times) as a minimum.

Keep in mind that this test is a severe, accelerated life test and does not indicate that acceptable lifetimes cannot be realized from ALUMINUM in lower frequency, larger geometry devices. GOLD appears necessary in microwave, sub-micron geometry devices.

SECTION 2 - TEMPERATURE STABILITY

Temperature stability involves two areas of interest. The first and most important is the silicon-metal ohmic (non-rectifying) contact; secondly, is the formation of intermetallics or solid-solubility.

SILICON-METAL CONTACT

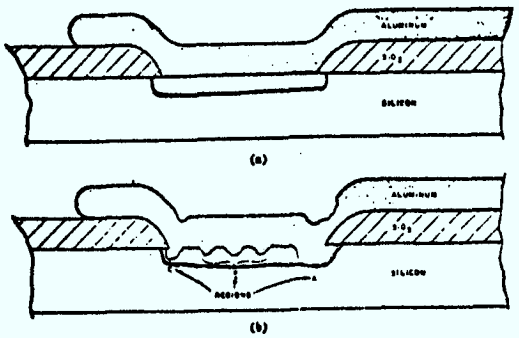
Previously (section 1) it was shown that transistors fail as "opens" due to electromigration. In this section, it will be shown how transistors fail as base-emitter "shorts" due to alloying of silicon with the contacting metallization.

ALUMINUM SYSTEM

Again, the problem is most severe with ALUMINUM. Figure 4 illustrates the etch-pit that forms when ALUMINUM is alloyed with silicon (caused by dissolution[1] of silicon into ALUMINUM). The alloying rate at 400°C is .021 angstrom/minute. Three gigahertz transistors have emitter diffusion depths of 3000-4000 angstroms.

Therefore, in 100 hours of operation under a hot-spot condition of 400°C, the transistor will fail as an emitter-base short. Output power will have degraded over time due to the even increasing base-emitter leakage.

E-B SHORTS DUE TO SINTERING OF Al INTO CONTACTS



	TEMP (°C)	Å/MIN
Silicon etch pit formation by: (a) As deposited	400	.021
(b) After alloying	500	6.36
	600	520.86

Figure 4. TYPICAL ALLOYING RATES OF Al INTO Si

At practical microwave device operating temperatures (150°C) and practical current density (1×10^5 A/cm^2), the calculated lifetime of ALUMINUM is limited to slightly over two years.

However, it is not uncommon with microwave geometries to have current densities of 2×10^5 A/cm^2, again at 150°C, the ALUMINUM lifetime in this case is limited to 5,500 hours or approximately 7.5 months.

Therefore, ALUMINUM metallization is deemed unsatisfactory for fine geometry device applications which approach the above conditions, especially those requiring practical lifetimes of over six months, and all high reliability applications.

GOLD SYSTEM

The GOLD composite metallization has lower alloying rates as shown in Table II, (2).

PtSi is used at TRW as the ohmic contact. Pt is sputtered on to the silicon, then PtSi is formed at greater than 500°C for times much in excess required to complete the reaction. Excess Pt, which was not exposed to silicon, is then etched away chemically. PtSi contacts are much less resistive than alloyed ALUMINUM contacts, thus reducing power loss.

With the use of TUNGSTEN to contact the Si-PtSi surface, a very stable connection is achieved which eliminates any etch-pit formation due to hot-spots.

ALUMINUM SYSTEM

"Although the alloying times given for Al in Table II were obtained without the use of a PtSi contact layer (450°C), it was found that a reaction occurred between the two materials which caused alloying in slightly more than thirty minutes."[2]

INTERMETALLIC FORMATION

Osborne, et al[2] investigated the change in contact resistance for various GOLD systems. This is shown in Figure 5. PtSi formed the preohmic contact. Again, the TUNGSTEN-GOLD composite is the most stable.

TIME TO ALLOY JUNCTIONS

AT 450°C AND 550°C (2)

METAL \ TEST	450°C	550°C
Al	20 min.	--
Mo-Au	3.5 hr.	40 min.
Ti-Pt-Au	5.0 hr.	50 min.
W-Au	4.5 hr.	50 min.

Table II.

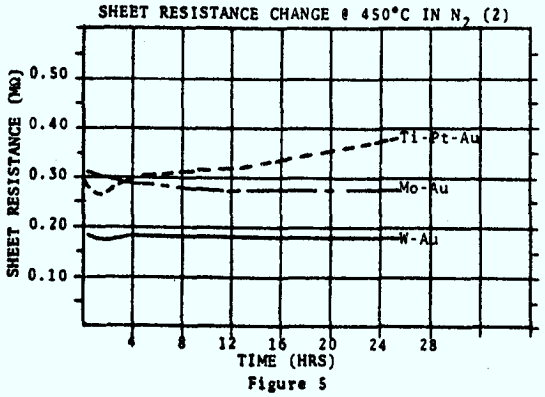


Figure 5

SECTION 3 - ELECTROLYTIC CORROSION

Osborne, et al[2] investigated electrolytic corrosion for Al, Mo-Au, Ti-Pt-Au, and W-Au as shown in Table III.

Two test conditions were used; (1) 85°C - 85% Relative Humidity, and (2) 98°C - 98% Relative Humidity. In each case, the test samples were two parallel 0.3 mil width stripes separated by 0.9 mils. A bias voltage of 3Vdc was applied across the two stripes under the above test conditions.

ALUMINUM SYSTEM

The ALUMINUM samples under test exhibited electro-chemical dissolution of ALUMINUM on the negative stripe while the positive biased side was nearly unchanged. Passivated ALUMINUM (6000 A SiO_2) was also tested with observance of the same reaction at the exposed bonding pad areas.

Biasing was shown to accelerate the ALUMINUM corrosion. In ten hours at 98°C - 98% R.H. no signs of corrosion was observed. However, with 3Vdc bias applied (98°C - 98% R.H.), severe corrosion was observed in one and a half hours.

GOLD SYSTEM

GOLD deplating from the positively to the negatively biased stripe was the limiting parameter for the TUNGSTEN-GOLD system (also for Ti-Pt-Au).

The time required for this failure is much longer than for ALUMINUM.

"The apparent differences in lifetime between Au on PtSi vs. Au on W as shown in Table III was attributed to a difference in surface topology of the GOLD resulting from different deposition conditions rather than any inherent effect of the underlying metallizations."[2]

CORROSION LIFETIME FOR Al, Mo-Au, Ti-Pt-Au, AND W-Au* (2)

METAL \ TEST	85-85	98-98	COMMENTS
Al**	4.5 hrs.	1.5 hrs.	Electro-chemical dissolution negative terminal
Mo-Au	--	.25 hrs	Mo-corrosion
Ti-Pt-Au	18 hrs.	4 hrs.	Au-deplating from positive terminal
W-Au	16 hrs.	3 hrs.	

* All tests were conducted with 3V dc bias. ** Unpassivated. Osborne, et al[2] Table III

SECTION 4 - ADHESION

Adhesion of the metal system to SiO_2 and Si is of a major importance to the mechanical and electrical reliability of any transistor.

Pull strengths of thermo-compression wire bonds were used to obtain a quantitative determination of adhesion.[2]

Figures 6 and 7 show the gaussian distribution of bond failures. The GOLD metallization systems all tend to show higher average wire pull strengths with GOLD wire than ALUMINUM with GOLD wire.[2]

Similar tests conducted at TRW Semiconductors on the PtSi-Ti-TUNGSTEN GOLD compared to ALUMINUM, also show higher average strength for GOLD vs. ALUMINUM (GOLD wire thermal-compression bonds).

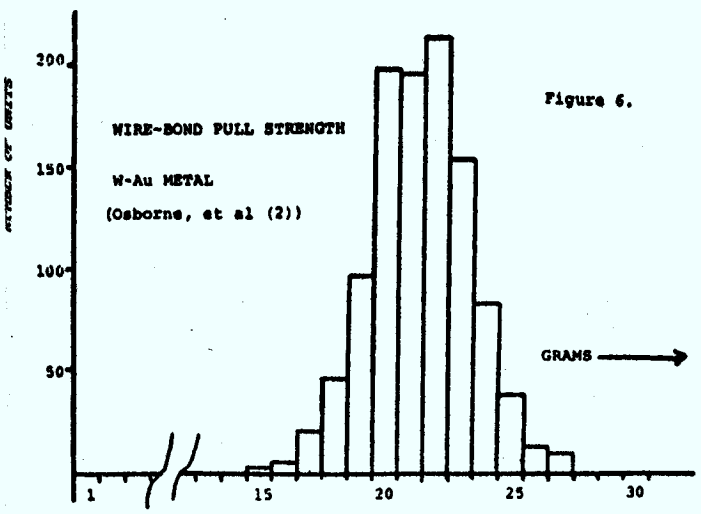


Figure 6.

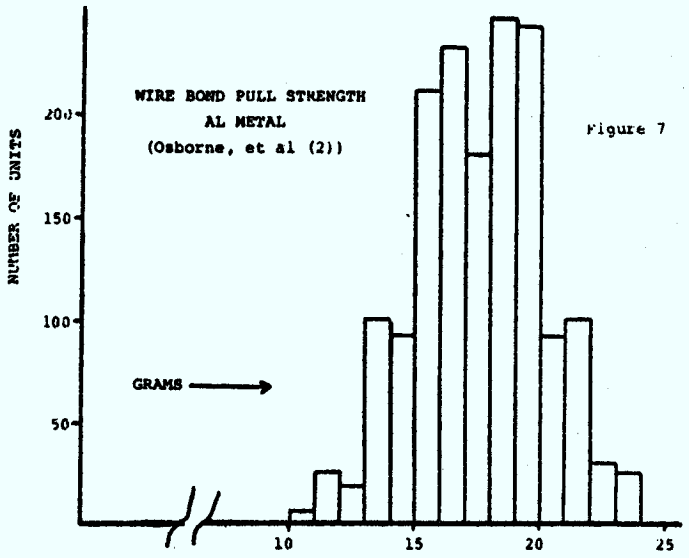


Figure 7

SECTION 5 - PROCESSING ADVANTAGES OF GOLD SYSTEMS COMPARED TO ALUMINUM

The reliability of all metal systems depends not only on those factors discussed in the previous sections, but the following three processing factors:

1. Deposition reproducibility,
2. Etchability to define metal geometries, and
3. Oxide step coverage, the ability to cover oxide steps without decrease of metal thickness or cracking.

The method of deposition makes the greatest difference between the quality factors of GOLD and ALUMINUM metallizations.

SPUTTERING is used at TRW Semiconductors for the PtSi-Ti-TUNGSTEN GOLD system, where vacuum evaporation is the industry-wide method to deposit ALUMINUM.

VACUUM EVAPORATION of ALUMINUM is usually accomplished via electron beam or resistive heating of the ALUMINUM to its vaporization temperature.

ALUMINUM SYSTEM

A point source for the ALUMINUM is used and since the mean free path of the ALUMINUM particle is long before collision, the wafer substrate must be rotated through all possible angles to achieve perfect coverage of all oxide steps. In practice, only an approximation to this ideal requirement is possible (see Figure 8).

OXIDE STEP COVERAGE
ALUMINUM VACUUM EVAPORATION

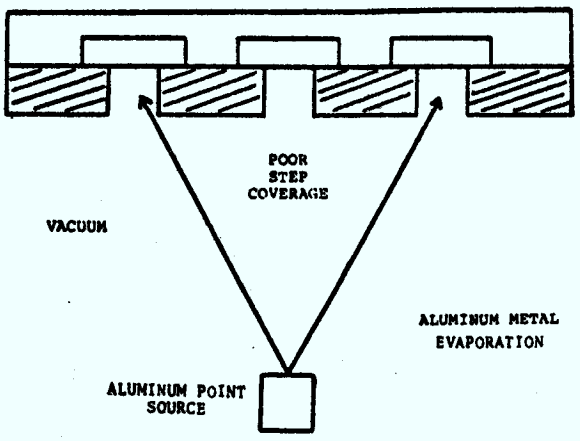


Figure 8.

This process problem alone is sufficient to justify an improved technique; but the task is only made impossible when the many difficult to control process variables are considered. A complete discussion of these process variables is beyond the scope of this paper; however, the impact on reliability of these process variables and problems is the subject of the Goddard Space Flight Center Specification S-311-P-12A entitled, "Scanning Electron Microscope Inspection of Semiconductor Device Metallization, Specification for."

Figure 9 shows a SEM photograph of an oxide step coverage problem with ALUMINUM.

Etchability of ALUMINUM is a problem which has been solved for large geometries, but is still (even though it has wide usage) a major process reliability problem with small geometry microwave transistors.

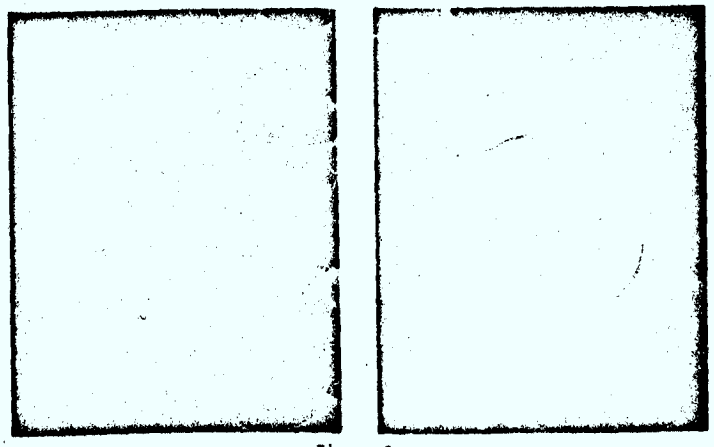


Figure 9

Photomicrographs of a transistor with ALUMINUM metallization showing poor step coverage. The blowup (6000X) shows a typical step with poor continuity in metallization. This gives rise to regions of extremely high current densities and the rasultant failures.

Figure 10A

6000X photomicrograph of a GOLD metallized transistor section. Note the uniform metallization without discontinuities.

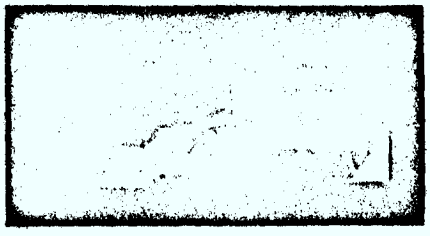


Figure 10B

Cross section photomicrograph of a GOLD metallized stripe showing uniform stripe thickness.

GOLD SYSTEM

The sputtering and etching processes used for PtSiTi-TUNGSTEN-GOLD (at TRW Semiconductors) solves these process-reliability problems.

Sputtering to deposit the metals is done in a high purity-inert gas atmosphere under pressure where the mean free path to collision of the metal particle is short.

The infinite number of metal particle to gas molecule collisions cause the metal to impinge on the wafer substrate surface at every possible angle. All oxide steps are easily and reproducibly covered (both sides of the substrate could be coated at one time!). Figure 10 shows a portion of the TRW 5 watt - 3GHz transistor.

This picture demonstrates that etchability is no longer a problem with the proprietary processas developed by TRW Semiconductors.

Sputtered PtSiTi-TUNGSTEN-GOLD forms the metallization. Step coverage and etchability is seen to be ideal, even though the device structure would be nearly impossible to process with ALUMINUM.

CONCLUSION

* TRW has Adapted the PtSiTi-TUNGSTEN-GOLD metallization system to solve the reliability problems which exist with ALUMINUM metallizations.

* The reliability problems with ALUMINUM are generally confined to R.F. power transistors designed for operation above 750MHz.

* PtSiTi-TUNGSTEN-GOLD metallization system removes the question of metal-reliability with microwave R.F. transiators.

* SUMMARY OF TEST RESULTS:

Section 1 - ELECTROMIGRATION

Median lifetimes of transistor metallizations can be improved over 17,000 times over ALUMINUM by using GOLD systems.

Section 2 - TEMPERATURE STABILITY

PtSi-W contacts to silicon have more than 100 times the stability of ALUMINUM contacts.

Section 3 - ELECTROLYTIC CORROSION

PtSiTi-TUNGSTEN-GOLD is over 3 1/2 times more corrosion resistant than ALUMINUM.

Section 4 - ADHESION

PtSiTi-TUNGSTEN-GOLD has better adhesion to Si and SiO_2 than ALUMINUM

Section 5 - PROCESSING ADVANTAGES OF GOLD METAL SYSTEMS

1. GOLD metal systems are more reproducible.
2. GOLD metal systems have improved etchability.
3. GOLD metal systems, sputter-deposited, solve all oxide step coverage problems.

The conclusion to be found within this report is:

* PtSiTi-TUNGSTEN-GOLD is a reliable, reproducible, and highly manufacturable metallization system which can increase the reliability (lifetime) of any R.F. power transistor, especially microwave transistors which are designed for operation above 750MHz.

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