MILLER
COMMUNICATIONS

STUDY, SPECIFICATION AND FABRICATION OF SIGNAL PROCESSING SYSTEM FOR TRANSPONDED EMERGENCY LOCATOR TRANSMITTER SIGNALS

(PHASE I)

FINAL REPORT

The work reported here was performed by Miller Communications Systems Limited for Communications Research Centre of the Department of Communications (Contract Officer M.D. Lambert) under DSS Contract No. OST76-00044

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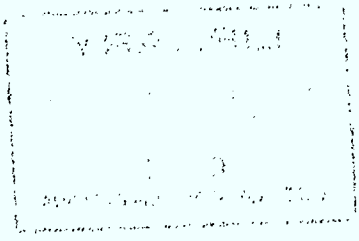

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EXECUTIVE SUMMARY

This report is the result of a comprehensive study of the requirements and alternative solutions for a signal processing system to identify and measure the frequency of up to eight ELT signals transponded through a Search and Rescue satellite. All conditions of the Statement of Work with regard to the Study Phase have been met, including:

- careful definition of the system requirements and constraints

- survey and evaluation of possible operational techniques, including analog, digital and hybrid alternatives

- development and detailed study of several promising candidate receiver types with all analysis required to determine key system parameters and estimate performance

- careful consideration of engineering and economic factors associated with the implementation of the receiver

- definition of a recommended receiver system to be designed and built in Phases 2 and 3.

The report is divided into four parts with two supporting Appendices as follows:

I RECEIVER SYSTEM DEFINITION

II SYNTHESIS AND ANALYSIS OF RECEIVER SYSTEM

III ENGINEERING - ECONOMIC EVALUATION OF CANDIDATE RECEIVERS

IV DEFINITION OF PROPOSED RECEIVER

APPENDIX A - DESIGN OF PLL'S FOR SIGNAL ACQUISITION

APPENDIX B - DIGITAL SIGNAL PROCESSING TECHNIQUES

Part I carefully re-examines all receiver performance specifications and the characteristics of the ELT signals themselves in order to bound the range of reasonable solutions and in fact verify that a solution is possible. Part I concludes that two basic receiver systems are feasible and merit in-depth investigation. The first, labelled Type A, employs one or more devices scanning the band and stopping only to measure the frequency of carriers detected. Good measurements can be sorted by software into ELT records unambiguously using known bounds on the first and second derivative of the ELT doppler characteristic. The second receiver configuration, labelled Type B, employs eight devices to track and measure each ELT detected. This approach requires more hardware and is clearly more complex from the control standpoint, but offers a greater ability to obtain measurements under more severe noise or interference conditions following initial detection. In neither case, however, does the receiver attempt to verify that the sinusoid

being measured is in fact an ELT.

Given the requirements of and constraints on the receiver system presented in Part I, Part II identifies and evaluates alternate schemes of realizing the functionally distinct Type A and Type B receivers. Performance, cost, operational flexibility, and technical risk are all taken into consideration in assessing alternate receiver designs.

Much of Part II is devoted to analysis of the detection and measurement processes, key elements of any Type A or Type B receiver. The phase locked loop (PLL) is the preferred device for both detecting and acquiring an ELT prior to measurement, and it is desired to

1. maximise the sweep rate in the search mode while maintaining low mis-detection and false alarm probabilities

2. minimize the acquisition time while ensuring the loop provides sufficient noise filtering to accurately measure frequency

3. ensure the PLL can track an ELT at the maximum doppler rate with the greatest possible noise and interference rejection

Part II determines that a second order PLL with loop bandwidth switching upon ELT detection can be designed to meet the requirements, and that two such devices operating in parallel in a Type A mode should be able to measure the frequencies of up to 8 ELT's at 10

second intervals.

The rms error in the measured frequency is estimated under nominal conditions, and the degrading effects of interfering carriers and sidebands, carrier pulsing, incidental FM, and phase noise are examined. Incidental FM generated in some ELT transmitters seriously degrades performance. PLL intervention is required to "track" pulsed ELT's and moderate degradation, statistical in nature, can be expected with pulsed ELT's unless elaborate detection and measurement techniques - not recommended in an initial receiver implementation - are employed.

Having examined in detail the fundamental signal processing elements of the receiver - detection, tracking and frequency measurement - Part II considers alternative overall receiver configurations. These are identified and the advantages and disadvantages of each stated. Section II.3.1.4 strongly recommends on the basis of simplicity and flexibility a receiver which employs two identical, independently controlled, frequency stepping "test instruments" capable of searching for, detecting, and measuring ELT's, interfaced with a PDP-11 microprocessor. Such a receiver can be operated in either a Type A or limited Type B mode with appropriate microprocessor software, and expansion to a full capability Type B receiver is accomplished by adding six more devices. (The Type B program and control interface can be designed to accommodate this addition). The input/output for each test instrument is rather simple, consisting of the incoming

noise filtered signal at appropriate centre frequency, an outgoing frequency measurement, and four logical control variables, namely:

i lock indicator status

ii stepper (synthesizer) frequency

iii PLL loop filter bandwidth (2 states)

iv counter start/stop command .

The critical timing parameters (sweep rate, allowed acquisition time, and measurement period), which can only be finalized experimentally, are under complete control of the computer and can easily be varied.

Since the signal-to-noise ratio required to achieve satisfactory performance trades off with the allowable sweep speed, and since neither can be quantified exactly at this time, it is also recommended that the instrument be able to operate with either 47 Hz steps/50 Hz pre-detection bandwidth or 94 Hz steps/100 Hz pre-detection bandwidth. This requires only that two sets of band pass and PLL loop filters be designed and built.

While priority will be given to developing a working Type A receiver, it is clear that extending its capability to the Type B mode consists only of developing the appropriate real time program. This task, however, should not be underestimated.

Part III of the report considers the candidate receivers from the standpoints of ease of implementation and hardware cost. A breakdown into major sub-systems is given, design tradeoffs are identified and quantified, and potential problem areas investigated. The results of Part III reinforces the recommendations of Part II, and concludes that the Type AB receiver is realizable within the time frame and budget constraints of this contract.

Part IV gives a concise specification of the Type AB receiver, and summarizes its expected performance under a variety of input conditions. This section will serve as the approved baseline as we enter the detailed design and implementation phases.

Appendices A and B are the results of background studies commissioned early in Phase I to get a handle on Phase Locked Loop operation and the availability and performance of digital processing hardware which might find application in the Sarsat receiver.

Lists of references which proved useful over the course of the study are also included on a chapter by chapter basis.

I. RECEIVER SYSTEM DEFINITION

I.1 Introduction

As part of its program to investigate the application of a low orbiting satellite to assist in locating downed aircraft, the Canadian Government's Department of Communications has awarded a contract to Miller Communications to study and develop a receiver system capable of detecting and measuring to an accuracy of 1 Hz the Doppler frequencies of up to eight Emergency Locator Transmitter (ELT) signals nominally sharing the same 12 kHz frequency band. The work is to be carried out in three phases:

(i) study to survey and evaluate possible operational techniques for ELT access recognition and signal reduction

(ii) performance specification and detailed design for the receiver system

(iii) breadboard design and fabrication of an approved developmental model

The problem of multiple access by ELT's can be broken into two parts. First, there is a requirement to continuously examine the downlink transmission from the SARSAT satellite to monitor the occurrence of ELT carriers. Secondly, when an ELT is found, its

carrier frequency must be measured and logged at regular intervals to a time-frequency accuracy of better than $\pm$100 msec, $\pm$ 1 Hz, at an operating C/N_o of 26 dB-Hz. It has been both theoretically and experimentally shown that this permits the position of the downed aircraft to be determined within several miles. Several types of candidate receivers have been proposed for examination, employing one or more of the following candidate analog and digital elements:

- swept filter or phase lock loop (PLL) detector(s)

- tracking narrow band PLL(s)

- frequency counter(s) and synthesizer(s)

- digital hardware processing elements such as Fast Fourier Transform (FFT), digital PLL(s), digital filter(s) and interpolators, etc.

- microprocessor or minicomputer used for real time software processing and data input/output.

An output record of frequency vs time is required at the completion of each satellite pass. This record must be in machine readable form for immediate automatic processing and/or transmission to a remote computer facility for final position determination of each ELT.

I.2 System Requirements

I.2 The system requirement calls for the following basic functions:

1. Search
2. Detect
3. Measure
4. Identify and track
5. Store

Only functions 1 and 3 require appreciable time; 2, 4, and 5 are essentially instantaneous, although 4 and 5 may require computation time.

Information pertinent to the design and performance analysis of the system is:

1. Up to 8 ELT signals must be simultaneously handled. These exist in a 12 kHz band at an input IF frequency of 70 MHz.
2. Carrier frequency must be measured to a relative accuracy of 1 Hz rms and time tagged to an absolute accuracy of 100 msec.
4. This dual measurement must be stored for later retransmission in machine readable form.
5. Each signal has a doppler shift range of $\pm$2.75 kHz.

6. Signals need not be resolved when within 100 Hz of each other.

7. Minimum peak doppler rate is 5 Hz/sec, the maximum is 14 Hz/sec, and the doppler rate can approach zero.

8. If tracking is lost, search must continue for 30 to 60 seconds.

9. On the average, 10 seconds between frequency readings is called for, but these need not be synchronous.

10. The maximum length of a satellite pass is 1200 seconds.

11. The Carrier-to-Noise density ratio will exceed C/N_o = 26 dB-Hz.

12. ELT modulation is of the "chirp" variety, either sinusoidal or square wave with duty cycles between 1/3 and 1/2, and with up to 100% modulation. The sweep width is 700 Hz in a band from 300 to 1600 Hz, and the rate is between 2 and 4 times per second. As well, the signal may be continuous, or pulsed with a minimum "on" period of 2 complete sweeps and an off/on ratio of up to 2, limited to 4 sweeps. Thus the signal may be "on" for a minimum of 0.5 seconds and "off" for a maximum of 2 seconds.

13. Carrier uncertainty is about $\pm$3.5 kHz and there is the possibility of incidental FM modulation accompanying the chirp. This modulation appears to be linear with an observed maximum

peak-to-peak deviation of 80 Hz. Phase noise ±15 Hz from the carrier has an observed 3 dB bandwidth of 4 Hz and an rms deviation of 5°.

These requirements and signal specifications will imply fundamental limitations on ELT receiver performance. For example, if the C/N_o of an ELT signal is such as to require a frequency measurement period of 1 second, then it would not be possible to measure a pulsed ELT signal with an "on" period of 0.5 seconds.

Various alternatives are available in terms of the functional devices used, their implementation, and the overall strategy inter-relating the several system functions. Devices available to implement the system include:

a. filter banks,
b. swept (or stepped) filters,
c. phase locked loops,
d. counters,
e. digital and computational units,

and analog, hybrid or digital alternatives are available for the construction of these sub-systems. The sequencing, or inter-relating, of the five primary system functions gives rise to numerous possibilities. One is the sequence "scan and detect ELT's across the whole band, measure, store" once every 10 seconds; although this would mean, for example, that the scanning device

would not be interrogated during the measurement period, and so this is intrinsicly inefficient. More effective methods would be "search in a swept or stepped mode, detect, measure, resume search", or "search in a swept or stepped mode, detect, assign measuring device, continue search while measuring". A single, or several search and measuring devices could be used in each case, and so the alternatives are numerous, particularly as each function has several candidate devices as possibilities.

As a consequence of the multiplicity of candidate systems, the fundamental constraints on the processes to be implemented were determined. This resulted in the elimination of a number of alternatives, and set the stage for a more detailed consideration of the more promising approaches.

I.3 Constraints on the Search Process

Initially it is assumed that the ELT signals are sinusoids; further limitations due to the particular properties of these signals will be introduced later.

The search process consists of identifying a possible ELT signal on an energy or amplitude basis in a background of ambient noise. The relevant specifications affecting this task are:

1. ELT signals separated by more than 100 Hz must be separately measured.

2. C/N_o = 26 dB-Hz.

While the bank of filters or swept filter approaches are different in detail, and while this difference would be taken into account in more detailed analysis, the same first order analysis suffices for both.

Minimum filter bandwidth cannot exceed 100 Hz and this would yield a SNR of 6 dB in the band giving marginal detection performance. Alternatively, a 30 Hz bandwidth would yield an 11 dB SNR and ease the detection of adjacent signals of different strengths. For incoherent (i.e. envelope) detection with a decision threshold of 0.6 relative to a typical signal, false alarm and miss probabilities would both equal 0.02 compared to 0.18 for the 100 Hz case (see Figures 1 and 2). Coherent detection would provide 3 dB improvement in effective signal strength.

To simultaneously cover the 12 kHz band would require 400 filters, or 800 to avoid a further 3 dB loss for signals located mid-way between filters. Alternatively, a 512 point FFT could be employed. As noted, continuous monitoring of 100 Hz or less contiguous bands across the full 12 kHz is unnecessary and would be costly no matter how implemented. (see FFT processor costs at end of Appendix B).

The time required to detect the presence of a signal however could be taken to be the inverse of the pre-detection filter bandwidth, or about 33 msec. for the 30 Hz filter. Alternatively, assume a white noise background and an averaging time T; then at the input

Figure 1

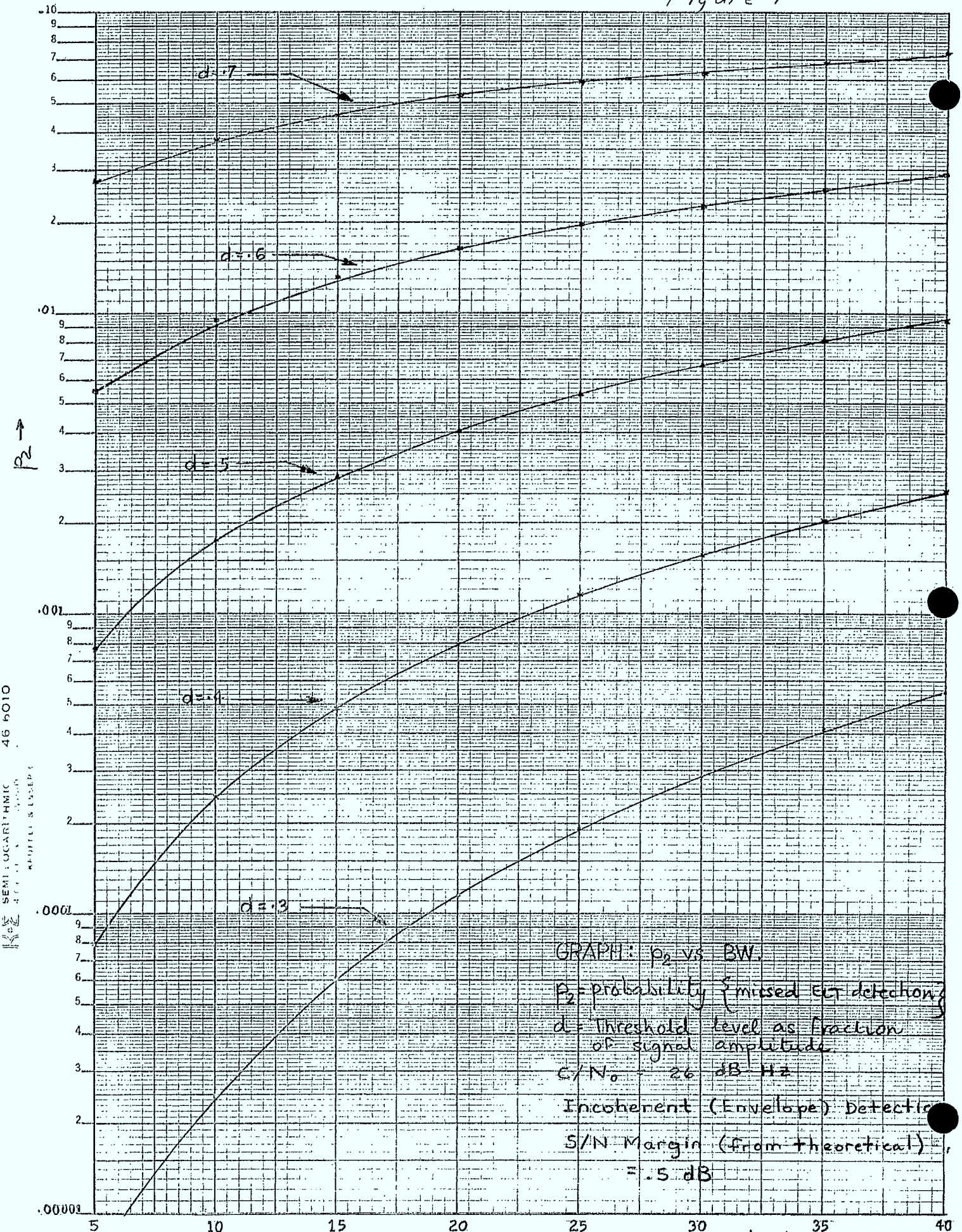
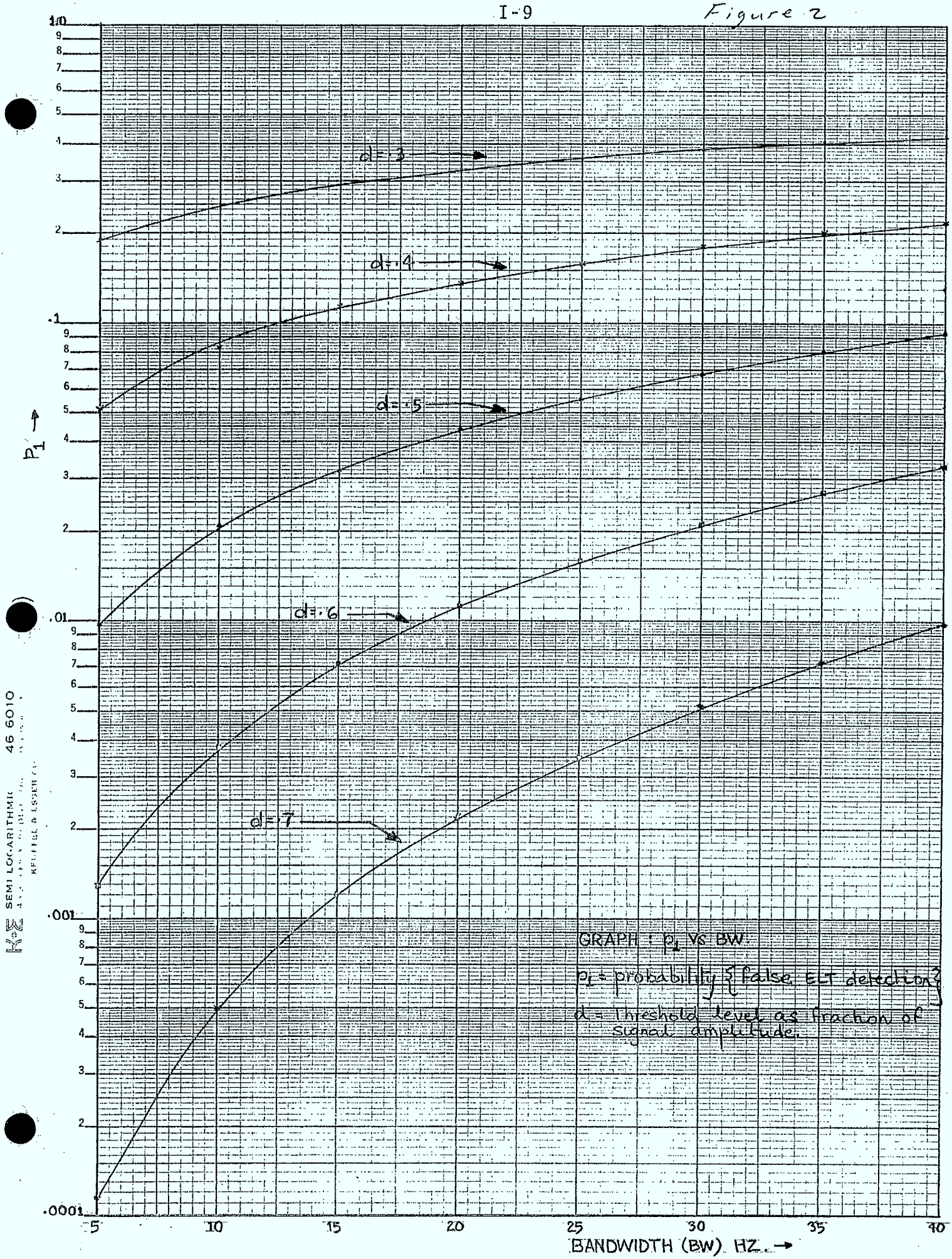


Figure 2



GRAPH : p_1 vs BW.

p_1 = probability of false ELT detection

d = threshold level as fraction of signal amplitude.

to the decision device

$$SNR = \frac{C}{N_o} T$$

assuming a 3 dB loss due to incoherent detection. A detection probability of 0.98 would be achieved in about 20 msec, thus allowing measurements to be spaced at 25 Hz if the whole 12 kHz band were covered in 10 seconds. If, to be safer, 50 msec. or 1.5 of a time constant were allowed per 30 Hz of bandwidth, two devices would be needed in simultaneous operation to sweep the band.

A phase locked loop performs, in effect, coherent detection, and initial estimates, based on published experimental data, indicate that a single PLL with a 20 Hz loop bandwidth could be swept across the band in 10 seconds with about a 95% detection probability. It would appear, then, that a single PLL could suffice for detection.

I.4 Constraints on the Measurement Process

The measurement of frequency can be achieved by narrow band filtering and energy detection, or by filtering followed by cycle counting. Relevant basic specifications are:

1. C/N_o = 26 dB-Hz

2. Measurement accuracy = 1 Hz

Assuming initial detection in a 30 Hz band defines the measurement range, final resolution could be accomplished by a bank of some 60 one Hertz filters, each requiring about 1 second to respond, or equivalently by a 64 point FFT with an initial response time of at least 1 second. (As the doppler rate can be as high as 14 Hz/sec, these alternatives will be discarded at once.)

The direct approach by counting devices is to count cycles over a fixed period T, and then the frequency is

$$f = \frac{N}{T}$$

Two sinusoids of frequency f and $f+\Delta$ differ in phase by $2\pi\Delta T$ after T seconds and these two signals will register the same count until this phase exceeds 2π. Thus T must be 0.41 seconds in order to assure an rms frequency error of 1 Hertz.

A more sophisticated technique is to measure the time required for a specified number of cycles, N, to occur. Then, the frequency is

$$f = \frac{N}{T}$$

and a noiseless sine wave is measured unambiguously. In practice, this will not be the case.

Signal distortion, resulting from carrier phase noise (statistical), incidental FM (periodic) and the doppler modulation itself, introduces the following rms frequency measurement errors:

1. $(\Delta f_{rms})_{\text{phase noise}} = (2\pi T)^{-1}\sqrt{2}\Delta p_{rms}\ (1-\exp(-(TB_p)^2)$ where Δp_{rms} and B_p are the rms deviation and 3 dB bandwidths respectively of phase noise components falling within the $\pm B_N/2$ pre-detection filter bandwidth. The 1-exp(.) factor here results from phase error correlation at start and stop counter trigger points, and tends to 1 as $T >> B_p^{-1}$.

2. $(\Delta f_{rms})_{FM} = (2\pi T)^{-1}\ \frac{\sqrt{2}\Delta F_s}{f_s}\ \sin(\pi f_s T)$ assuming the measurement starting time is randomly phased with respect to the chirp. ΔF_s and $2 \leq f_s \leq 4$ Hz are the peak deviation of the incidental FM (here assumed sinusoidal) and chirp rate respectively. Note that selecting T to equal an integral number of chirp cycles theoretically removes the degrading effect of incidental FM; however, f_s is a variable not immediately known to the receiver.

3. $(\Delta f_{rms})_{\text{non-linear doppler}} = \sqrt{E\left\{\frac{d^2 f(t_o)}{dt^2}\right\}}\ \left(\frac{T^2}{24}\right)$ where f(t) is the doppler frequency at time t and E {.} denotes an ensemble average over all doppler characteristics.

The rms phase error at the pre-detection filter output due to thermal noise is given by $\left(2\left(\frac{S}{N}\right)\right)^{-1/2}$ for $\frac{S}{N} >> 1$ where S/N = 26 - 10 log (B_N) dB. The corresponding rms frequency measurement is then

$$(\Delta f_{rms}) = (2\pi T)^{-1}\ \sqrt{2}\left(\frac{S}{N}\right)^{-1/2}\ (\ 1 - \exp(-TB_N)^2))$$

$$= (2\pi T)^{-1}\ \sqrt{2}\left(\frac{S}{N}\right)^{-1/2} \qquad \text{if } T >> B_N^{-1}$$

The final source of error is inherent to the measuring device itself. Evaluation of the HP model 5345A fast counter has revealed the following types of measurement error for an ideal sine wave input:

1. error uniformly distributed on $\pm$ 1 nsec at both start and stop triggering points (due to minimum of 2 nsec time base interval)

2. detection phase errors uniformly and independently distributed on $\pm$ .3% of a cycle at both start and stop trigger points.

3. relative time base error determined by 20 minute stability of time base generator reference oscillator.

Rms values for the resulting frequency measurement errors are as follows:

$$(\Delta f_{rms})_{\text{trigger error}} = 1.16 \times 10^{-9} T^{-1} f_c$$

$$(\Delta f_{rms})_{\text{phase detection error}} = .006T^{-1}$$

$$\Delta f_{\text{time base error}} = S f_c$$

where f_c is the incoming IF frequency and S is 20 minute reference oscillator stability.

Since the sources of errors described are statistically independent, the resulting rms error is simply the r.s.s. (root sum squared) of the individual components.

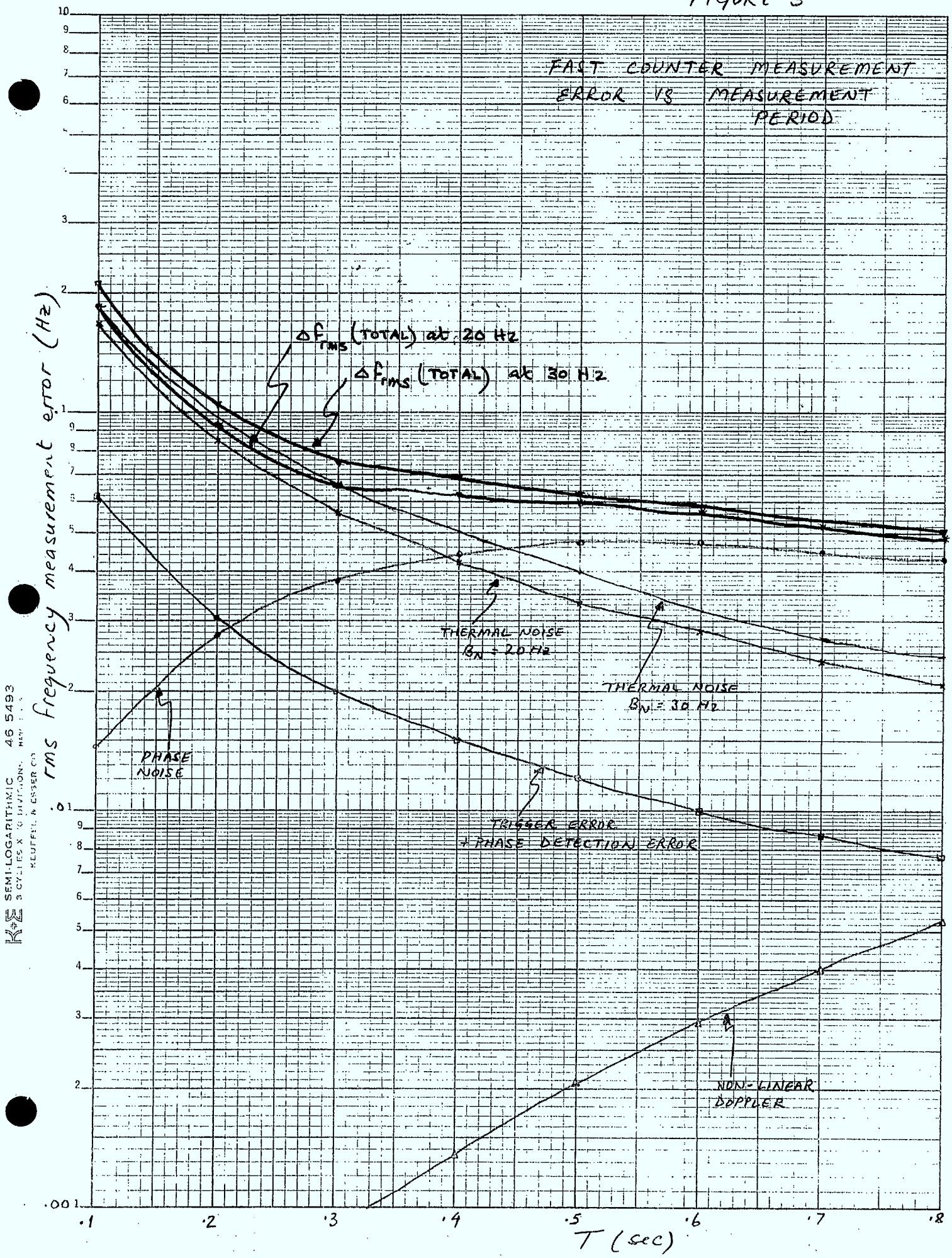
Assuming the following parameter values

Δp_{rms}	= 4.8° (1 to 15 Hz from the carrier typical of Garret ELT Spectra surveyed)
B_p	= 2 Hz
$a(t_o)$	= .2 Hz/sec^2 (worst case)
B_N	= 20 Hz, 30 Hz
f_c	= 100 kHz (worst case)
S	= 1 X 10^{-9}

Figure 3 plots the individual and net rms frequency measurement errors vs measurement period, neglecting incidental FM. All except the non-linear doppler and phase noise contributions decrease linearly with T, phase noise is controlling for T > 0.5 seconds, and time base error is negligible.

The preceding analysis presumes a sophisticated counter which measures the time, T, required for a set number of cycles, N, but the much simpler fixed period counter introduces the previously discussed ambiguity in frequency. This is equal to the inverse of the measurement period, but, if the frequency of the signal can be multiplied

FIGURE 3



from f to nf, and then measured by a fixed counter, the ambiguity is reduced by the factor n. It is, of course, necessary to consider accompanying signal-to-noise ratio effects.

If a PLL utilizes a counter in the feedback loop such that the input/output frequency ratio is n, then the loop locks with an output frequency which is n times that of the input. However, the standard deviation in the output phase error is also increased by the factor n, but this should not cause real difficulty. For example, the previous analysis shows that if n=4 and the measurement period is 0.25 seconds, then the rms frequency error (neglecting incidental FM) is 0.4 Hz for a 30 Hz pre-detection bandwidth.

Another approach is to twice square and filter the signal with the result that (Davenport and Root, p. 262)

$$\frac{\text{SNR out}}{\text{SNR in}} \approx \frac{1}{16}\left(1 + 2.5/\text{SNR}_{in} + 2/\text{SNR}_{in}^2 + .5/\text{SNR}_{in}^3\right)^{-1}$$

While measurement error due to phase distortions is necessarily quadrupuled whether a PLL or power law device is used, the effect of thermal noise is quite different. In the PLL case, the net rms phase error is multiplied by four, corresponding to an SNR degradation of approximately 6 dB over a wide range of input SNR's. The two cascaded square-law devices, on the other hand, degrades the SNR by at least 12 dB, and exhibits a sharp threshold effect.

In all, a fixed period counter, with PLL frequency multiplication if needed, may well be sufficient for the measurement of the ELT carrier frequency.

The PLL required for the searching function has characteristics reasonably similar to that needed for pre-filtering the signal before the frequency measurement. An SNR in the loop of 3 dB would be expected (with a 100 radians/sec ω_n or 100 Hertz noise bandwidth), and a resulting mean square phase noise of 0.25 radians squared. This would not be troublesome if the measurement period were much less than 60 msec; nor would it be troublesome if the period were long, say several seconds. The mean time between cycle slips would be 6 seconds, the number of cycles slipped would average 1.5, and the frequency measurement specification would be met. Alternatively, to shorten the frequency measurement period to less than a second, the PLL bandwidth could be changed following ELT detection, or another loop could be utilized.

I.5 Effects of ELT Modulation

I.5.1 Up-Link Doppler

As the tracking error at the maximum doppler rate of 14 Hz/sec for a PLL with a 16 Hertz loop bandwidth would be 0.5 degrees, and this varies inversely as the square of the bandwidth, doppler does not set difficult design criteria on any phase locked loops used in the system. However, as mentioned, the doppler rate does preclude use of a filter bank to measure frequency within 1 hertz, simply because

the frequency will have traversed at least 14 Hz in the time required for the measurement.

Since carrier frequency is changing with time, and since an appreciable time is required for the measurement, there is a question of just when the "instantaneous frequency" of the carrier is measured. To resolve this question, take the signal being measured to be

$$A \sin \phi(t)$$

and the measurement period to be from t = 0 to t = T. Represent

$$\phi(t) = \phi_o + \phi_1 t + \phi_2 t^2 + \phi_3 t^3 + \ldots.$$

so that the instantaneous frequency expanded in a Taylor series about t = 0 is

$$f(t) = \frac{1}{2\pi} \frac{d\phi}{dt}(t) = \frac{1}{2\pi} [\phi_1 + 2\phi_2 t + 3\phi_3 t^2 + \ldots.]$$

$$= [f_o + f_1 t + f_2 t^2 + \ldots.]$$

$$\text{where } f_i = \frac{1}{i!} \frac{df^i(0)}{dt^i}$$

In the measurement period T, the number of phase resolutions will be

$$\frac{1}{2\pi}[\phi_1 T + \phi_2 T^2 + \phi_3 T^3 + \ldots]$$

and this divided by T will be the measured frequency

$$\hat{f} = f_o + \frac{f_1}{2} T + \frac{f_2}{3} T^2 + \ldots$$

The difference between the measured frequency and the instantaneous frequency at $t = \frac{T}{2}$ is then

$$\hat{f} - f(T/2) = f_2 \frac{T^2}{12} + \ldots$$

Should the change of frequency be linear i.e. $f_i = 0$ for $i \geq 2$, the measured frequency is that at $t = \frac{T}{2}$, and compensation for the measurement period is simple. Otherwise more complex correction is necessary.

Preliminary study of typical ELT data suggests a maximum doppler second derivative of about 0.2 Hz/sec^2 which gives corrections:

Measurement Time (sec)	Maximum Frequency Correction (Hertz)
10	4
1	0.04
0.1	0.0004

This indicates that if the measurement time is of the order of 1 second or less, the linear correction is sufficient.

I.5.2 Chirp Modulation

As indicated in the Request for Proposal, ELT signals have from 33% to 45% of their power in the modulation first sidebands, and up to 22.5% and 4.5% respectively in the second and third sidebands. The first sideband power is distributed reasonably uniformly over 700 Hz ranges beginning at least $\pm$ 300 Hz from the carrier, and so detection and measurement of an ELT is not disturbed by its own sidebands. The carrier-to-spectral density of the sidebands for 100% sinusoidal, 100% rectangular - 33 1/3% duty cycle AM modulations and equal ELT carrier levels are indicated below

Modulation	C/I_0(dB-Hz)		
	1'st harmonic	2'nd harmonic	3'rd harmonic
100% sinusoidal	34,5	X	X
100% rectangular, 50% duty cycle	32,4	X	55,6
100% rectangular, 33 1/3% duty cycle	30,2	39,2	48,0

The maximum spectral density of a sideband is 4.2 dB below the ambient noise, and so on an average power basis the modulation will not greatly interfere with ELT detection. Viewed in an alternate fashion, the instantaneous frequency of a first sideband is changing at least at the rate of 1400 Hz/sec. Thus a sideband signal spends some 21 msec or 4.2% of its time within the bandwidth of a 30 Hz filter with a time constant of 33 msec. This is sufficiently long to cause a response, but this response would peak roughly 9 dB below carrier level (equal ELT's assumed), be present for about 50 msec (10% of time) and degrade the false alarm probability to only about .10 for an incoherent detection threshold of .6 x signal amplitude. This could be reduced substantially by use of a more sophisticated detection device.

The following table gives the probability that one or more first sidebands will fall within $\pm$15 Hz of a wanted ELT assuming independent

and uniform distributions of ELT frequencies across the 12 kHz band. Note that the probability of more than one interfering sideband falling on an ELT is normally very small.

Number of ELT's Present	Probability of first sideband interference sweeping within 15 Hz of an ELT carrier		
	1 interferer	2 interferers	3 interferers*
1	0	0	0
2	.117	0	0
3	.229	.0049	0
4	.336	.0146	.0004
5	.548	.0353	.0016

The probability that an ELT is subject to sideband interference, at any instant of time is obtained by multiplying these numbers by .1, which is the fraction of time interfering power due to a sideband sweeping back and forth across an ELT is actually present at the output of the pre-detection filter. On the other hand, the numbers in the table are clearly optimistic due to the assumption of a uniform probability distribution of ELT's across the 12 kHz band.

* In this case the likelihood of direct interference between two of the sideband producing ELT's is also high.

Another possible difficulty occurs if the sideband of one ELT signal makes the measurement of another signal more difficult. However, if the amplitude of this interference is less than that of the signal being measured, and if the interference sweeps the entire pre-detection bandwidth an integral number of times during the measurement period, the net effect on a fixed period counter with an ideal pre-filter would be zero as the lengthening and shortening of the periods between zero crossings would cancel. Only if the sweep began or ended within the measurement band would there be a net effect, and this would occur with a probability.

$$P = 2\left(\frac{30}{700}\right) = 0.086$$

for a 30 Hz pre-filter. The level of the interference at the filter output has previously been calculated to be at least 9 dB below the carrier level or only 2 dB above the noise. Consequently, this event even when it does occur, will not cause appreciable error if the wanted and interfering ELT signals are of comparable amplitude.

I.5.3 Pulsed ELT's

Further potential difficulty arises if the ELT signal is pulsed. Such a signal could be "on" for as little as 0.5 seconds and "off" at least 2.0 seconds. The existence of such signals sets a premium on the time available for measurement. Were the measurement period more than a second, many signals could be lost due to inadequate opportunity for measurement. If a measurement period of 0.25 seconds is chosen, the probability that a 0.5 second "on" ELT can be measured during the "on" interval in which it is detected is

not more than 0,5. For various "on" times T_{on}, this probability varies as follows:

T_{on} (seconds)	Prob. of incomplete measurement
0.5	$\leq$ 0.5
1.0	$\leq$ 0.25
2.0	$\leq$ 0.13
3.0	$\leq$ 0.08

There may be no simple way of overcoming this, and so it is to be expected that pulsed ELT signals will be measured and tracked less effectively than continuous signals. Certainly it will be necessary to continuously confirm signal presence during frequency measurement.

I.5.4 Incidental FM

The carrier may also be subject to incidental FM modulation which will be assumed to be periodic at the modulation sweep rate. Short interval frequency measurements would be ambiguous over the range $(-\Delta F, \Delta F)$ where ΔF is the peak incidental FM deviation; successive randomly phased frequency measurements would therefore be subject to this range of relative error. If the incidental FM is approximately linear and can be tracked without distortion by the measuring device pre-filter, the frequency measured would be the average over the measurement interval. Taking that interval to be

$$T = (N + \alpha)\tau$$

where N is an integer, $\alpha<1$, and $.25 \leq \tau \leq .5$ is the sweep period, the variation in measured frequency is

$$\frac{\alpha(1-\alpha)\ \Delta F}{2N}$$

which has a maximum of $\frac{\Delta F}{8N}$. To hold this within one Hertz requires

$$N > \frac{\Delta F}{8}$$

As pulsed ELT's with 2 sweeps "on" would be limited to N=1, it would be necessary that

$$\Delta F < 8 \text{ Hz},$$

otherwise the specification could not be met without elaborate, and perhaps impractical schemes, e.gs. chirp synchronous measurement, estimation and post-measurement compensation etc. Study of a specific ELT signal indicated a ΔF of about 37 Hz, and the inescapable conclusion is that very degraded system performance will be inevitable with some ELT's.

Figures 4 and 5 plot the frequency error due to sinusoidal and linear incidental FM when time base measuring and cycle counting in a fixed period counters respectively are used. Note that given its initial 2π measurement ambiguity, the simple (fixed period) counter

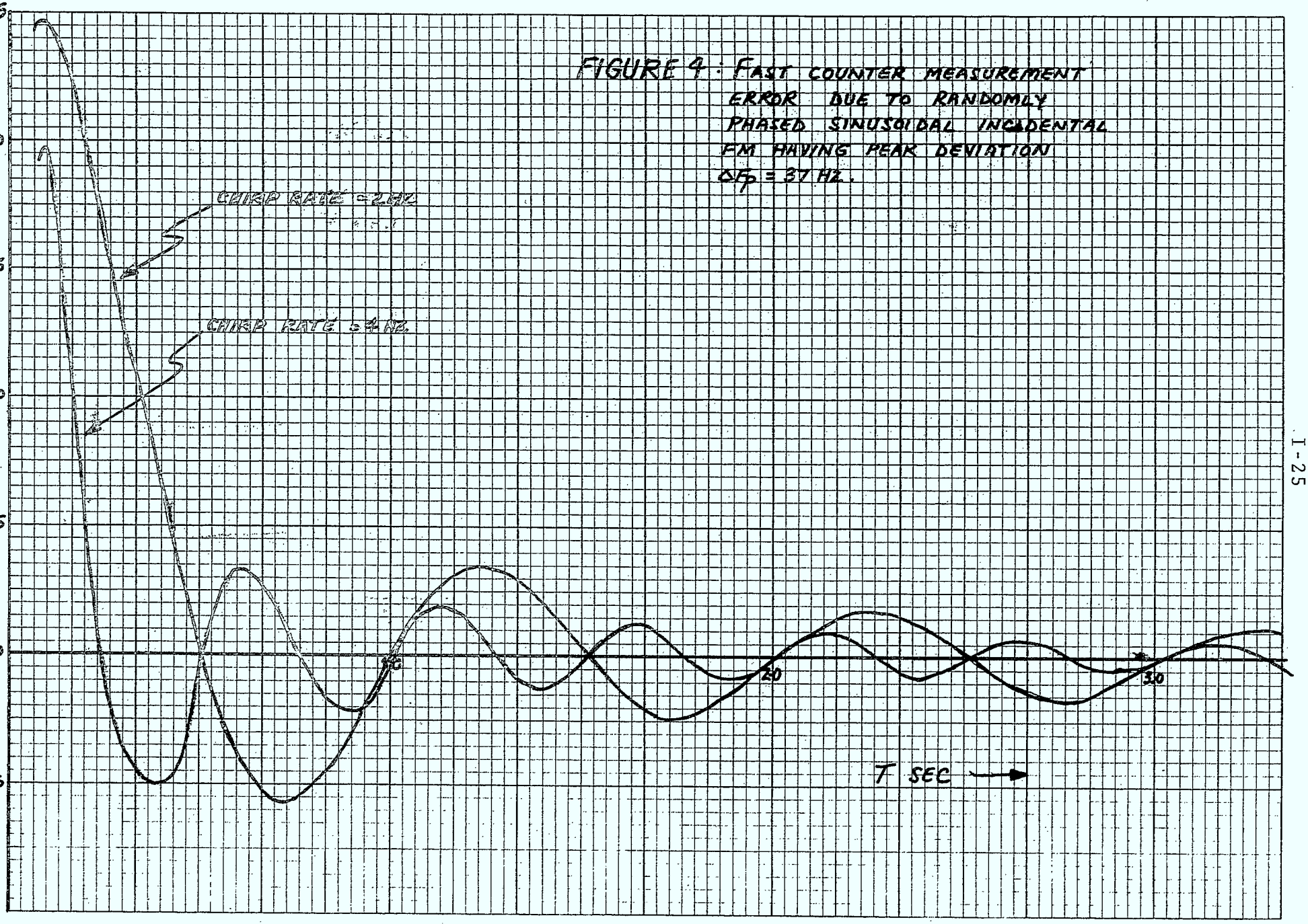
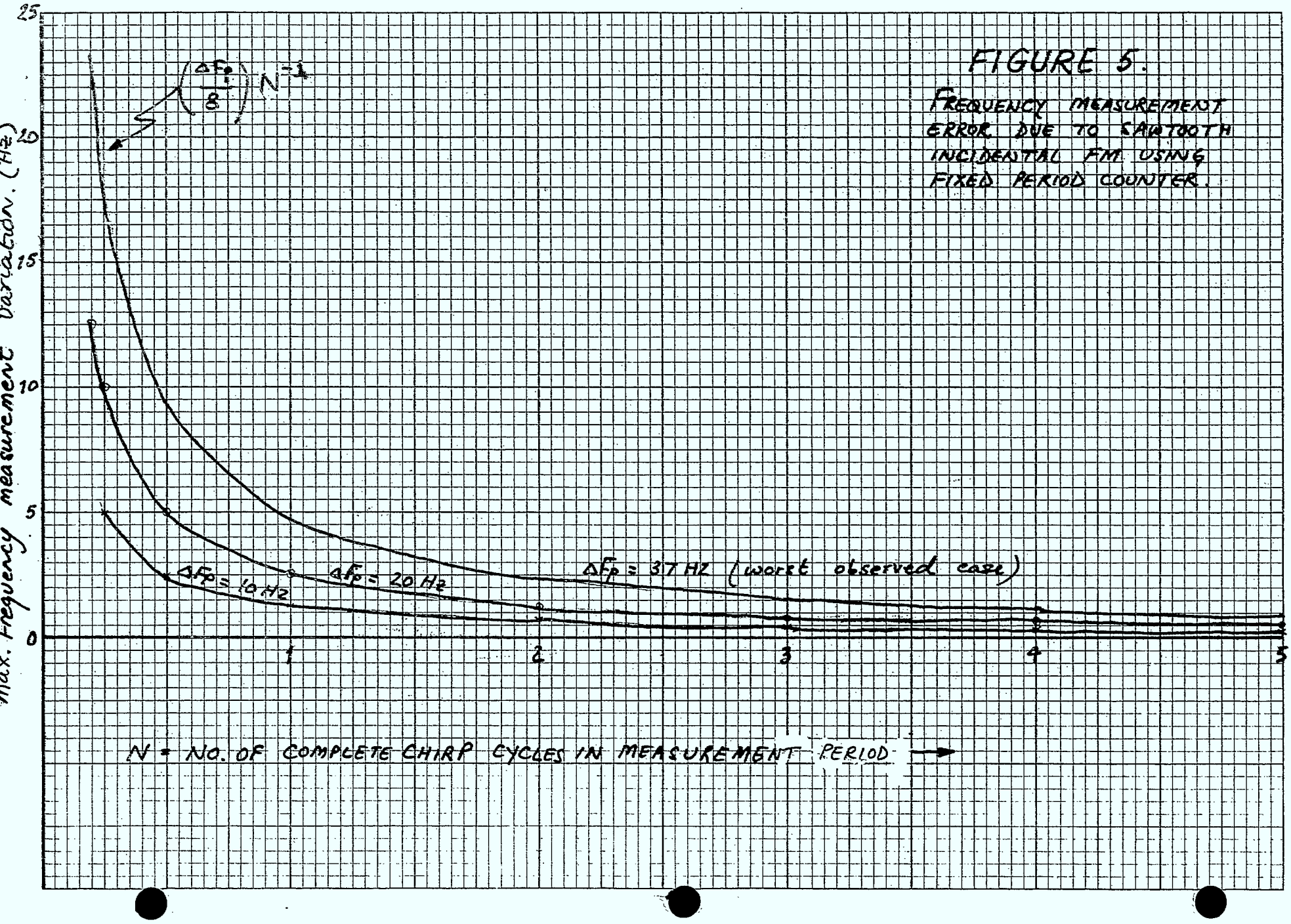


FIGURE 4: FAST COUNTER MEASUREMENT ERROR DUE TO RANDOMLY PHASED SINUSOIDAL INCIDENTAL FM HAVING PEAK DEVIATION $\Delta F_p = 37$ Hz.



is somewhat less sensitive than the time base measuring counter to additional degradation due to signal distortion.

I.6 Interference Effects of ELT Carriers Beyond 100 Hz Separation

This occurance can be modelled worst case by considering the effect of an interfering sinusoid on a single period T measurement where the estimate of frequency is

$$f = \frac{1}{T}$$

Here a phase change caused by an additive sinusoidal interferer Δf Hz from the wanted sinusoid is

$$\phi < 2\pi \frac{\Delta f}{f} \left(\frac{S}{I}\right)^{1/2}$$

where S/I is the signal-to-interference power ratio at the output of the pre-detection filter. A phase change ϕ corresponds to a period change of $\frac{\phi}{2\pi f}$ and a frequency change of $\frac{\phi}{2\pi T}$, so the specification is met if

$$\frac{S}{I} > (\Delta f)^2$$

If the wanted and unfiltered interfering ELT's have equal amplitudes and the pre-detection filter has a normalized amplitude characteric α (Δf), then we need

$$\alpha (\Delta f) < \frac{1}{\Delta f}$$

and for $\Delta f > 100$ Hz this is met by a three pole filter with a bandwidth of 30 Hz.

Thus, even the most disturbance sensitive frequency measurement technique does not require extraordinary pre-filters. For the 1 second counting method, a single pole filter suffices.

I.7 Control of Receiver Processing

In order to detect the occurence of ELT's, perform the required frequency measurements about every 10 seconds, and store the data in individual ELT logical fields, the following control processing is required.

I.7.1 Identification and Tracking

This is a single process and there are two basic approaches:

1. continuously track the ELT signal with a phase locked loop

2. measure each signal as detected and identify by extrapolation from previous measurements.

In each case no ELT signal would be identified as such until tracked over 30 seconds, nor declared "ended" until lost for over 30 seconds.

In the continuously tracking system, the detection device would have to be commanded to ignore signals which were already being tracked. As lock will be broken when ELT signals are pulsed, or approach within 100 Hz, an extrapolation system will be required for this method just as for the other.

Extrapolation can be accomplished by making

$$\hat{f}_3 = 2f_2 - f_1$$

the estimate of the signal frequency at the next sampling instant. This assumes periodic sampling and may have to be slightly modified for natural sampling. A survey of ELT records suggest that the next measurement would be within 25 Hz of this estimate. Thus signals separated by 100 Hz would not be confused, even over a 30 second period. An appropriate algorithm will have to be defined to identify and track distinct ELT's (continuously tracking system only), and initiate and terminate ELT records.

I.7.2 Signal Acquisition and Measurement Strategy

Previous analysis suggest that one or two detection filters be used to cover the band, rather than a bank of filters performing simultaneous detection. The filters could be in adjacent bands and stepped as a pair through the 12 kHz band in 10 seconds, separated by 6 kHz and swept (in 20 seconds) over the band, or each swept over a disjoint 6 kHz band in 10 seconds. In each case, all continuous

ELT signals present will be detected within 10 seconds with probability greater than 0.95. For a pulsed ELT with a two to one off/on ratio, the detection probability would be about 0.32 in 10 seconds, 0.54 in 20 seconds, 0.68 in 30 seconds 0.78 in 40 seconds, and so on, assuming that the pulsing and scanning were not synchronous. (If they were, the detection probability would remain at 0.32). In any situation, the missed detection probability can be improved by using more filters scanning at a lower sweep rate.

The simplest approach to acquisition and measurement is to have a number of devices capable of both these functions sweeping across the 12 kHz band. Were one of these devices to detect a signal, it would cease sweeping and measure the signal frequency. Once that was finished, sweeping would commence again. Were each device operating completely asynchronously, their distribution in time-frequency would be difficult to predict and undesirable distributions of measurements in time and frequency could occur. A simple solution for this problem is to stop all sweeping while any device is making a measurement. This would ensure the uniform spacing of the devices in frequency.

In fact, one such device could handle up to 8 ELT signals in 10 seconds by sweeping the band in 6 seconds and using up to 8 X 0.5 seconds for measurement. That assumes a PLL as the detection filter, a 0.50 second frequency measurement interval, and yields a detection probability of around 90%. Two or more devices would yield higher detection probabilities or longer measurement periods. This is a

viable approach and will be referred to as Option A. Note that the same device would be used for both signal detection and frequency measurement; that each device should sweep the 12 kHz band in 20 seconds, and be spaced at 6 kHz, if two were used; and that, if more than one is used, fixed bandwidth filters may be possible as an alternative to PLL's.

Other arrangements are available which would allow simultaneous search and measurement in such a system but at the cost of much additional complication and to no advantage. These alternatives will not be investigated further.

In the above approach, identification and tracking would be accomplished by extrapolation using frequency samples spaced about 10 seconds apart. A distinctly different alternative is to continuously track each detected ELT signal with a PLL. In this option, a signal detection device would be swept across the band (in 10, or perhaps more, seconds) and upon detection of a new ELT a PLL would be assigned to track that signal. Frequency measurements would be periodically obtained from the PLL output. Alternatively, if the PLL were used in both signal acquisition and tracking, a new PLL could be assigned to the search once the currently sweeping PLL had locked to an ELT signal. While this approach is intrinsically more complex than Option A, it may offer some performance advantages and so will be designated as Option B.

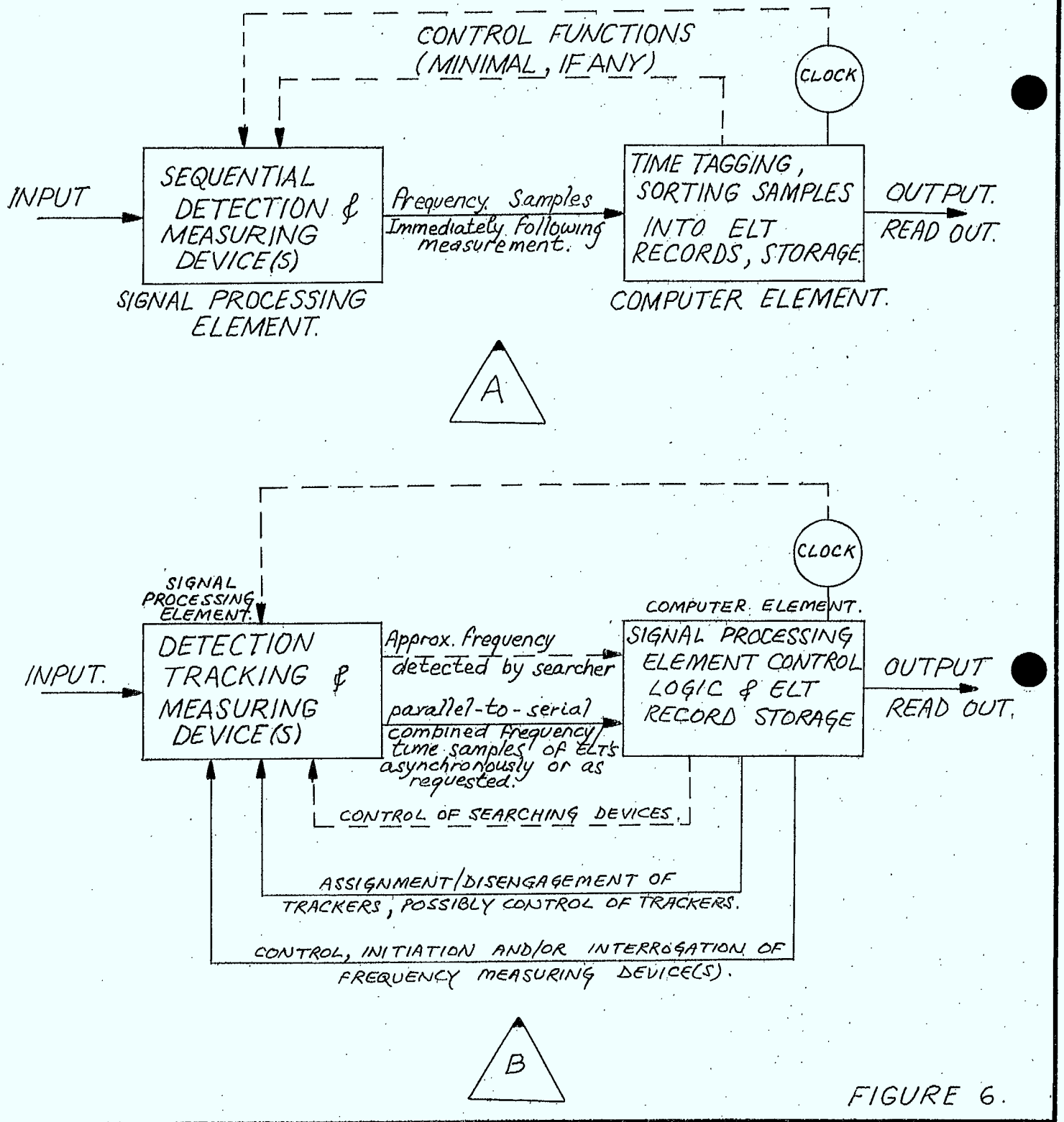


FIGURE 6.

	APP	TOLERANCES: .XX ± .XXX ± FRACT ± ANGLE ±	SCALE
NOV. 2, 1976	DATE	MAT'L	
	C.O. No.	FINISH	
	REV	DRN R. MISRA	
		DES	
		CH'D	
		ENG	

MILLER COMMUNICATIONS SYSTEMS LIMITED
KANATA - ONTARIO - CANADA

A TYPE "A" RECEIVER

B TYPE "B" RECEIVER

PART/DWG NO SAR-MCS-006

SHT- OF -

REV- 0

I.7.3 Software Element

The two basic types of receivers can functionally be broken into distinct parts, as shown in Figure 6. In its simplest form, the software/storage element of the Type A receiver "passively" accepts in serial form successive measurements of frequency as they are completed. The correct time tag for each measurement can be easily derived from the computer clock using the relation

time tag = mid-point of measurement interval
≃ computer time on receipt of sample
- 1/2 measurement period - constant delay (if any)

The software must sort incoming (time, frequency) samples into appropriate ELT records. Extrapolation from previous measurements and limits on the maximum doppler rate of change and second derivative can be used to define admissable regions of successive ELT measurements - overlapping decision regions can be bisected and samples falling out of admissable regions flagged as possible new ELT's. A suitable algorithm for initiating new and terminating old ELT records must be determined. After a satellite pass some apparently bad (time, frequency) samples may be retained, if desired, in a "mixed bag" data file.

Unlike the Type B case, control feedback from the software/storage element to the signal processing element is not essential to the Type A concept. Type A is therefore not only functionally simpler,

it permits largely parallel and independent development of the two constituent sub-systems.

In the Type B receiver, the computer element will have to exert some control over the assigning, sweeping and disengagement of 8 PLL's, and the start/stop, assignment/disengagement, and interrogation of measuring device(s). If the measuring device(s) are not under computer control, e.g. free-running, a variable delay between the mid-point of a measurement period and the instant the frequency sample arrives at the computer may be present, in which case external time tagging is required. This is avoided if the computer commands measurement start/stop, which also permits the computer clock to be used as the time-base for a fixed period counter and, if desired, facilitates the switching and time-sharing of a common measuring device among several tracking devices.

For the Type A receiver, simple computer control of the sweep and measurement taking devices may prove advantageous if this does not add greatly to the overhead time. However, it is clear that much more signal processor/software element interaction will be essential to the Type B receiver than in the Type A case.

Realizable performance advantages of the Type B, if any, lie in one or more of the following categories:

- regular measurement of pulsed ELT's following initial detection.

- measurement and correct identification of 2 previously detected ELT's now separated by less than 100 Hz

- improved frequency measurement accuracy in non-stationary S/N environment by repeated or selective measurement taking.

I.8 Recommendations

It is recommended that the systems designated as Option A and Option B be further investigated. This will first involve decisions regarding the various alternative approaches still open within the scope of the two systems which will result in at least two receiver structures to be further analysed. Detailed calculations of expected performance will be made, along with engineering and economic estimates of analog, hybrid and digital implementations.

I.9 References

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II SYNTHESIS AND ANALYSIS OF RECEIVER SYSTEM

II.1 Introduction

Given the requirements of and constraints on the receiver system presented in Part I, it is necessary to identify and evaluate alternate means of realizing the functionally distinct Type A and Type B receivers. Performance, Cost and risk factors will be taken into consideration in assessing alternate receiver designs.

It is required to establish the parameters and determine the performance of candidate receivers in a more exact fashion than that employed in Part I to bound the problem. Part II analyzes the constituent elements of either Type A or Type B receiver, and arrives at a total of ten possible basic approaches consisting of combinations of the following:

- Type A or Type B

- search and frequency measurement performed by a PLL having a bandpass filter preceding the phase detector and continuously swept over 12 kHz, or by a stepped programable frequency synthesizer beating the signal into a bandpass filter followed by a PLL.

- frequency measurement of the signal detected by PLL performed using a fixed period counter at the VCO output, or by a digitally controlled fine step (< 1 Hz) synthesizer replacing the VCO, or by direct measurement of VCO input (with the stepped sweep method only).

The functional devices involved will be suitably interfaced with and controlled by a PDP-11/03 microprocessor. All cases involve coherent detection of an ELT and reduction of the PLL loop filter bandwidth prior to frequency measurement.

Part III evaluates the candidate receivers from the practical design tradeoff, ease of implementation, capital cost and schedule standpoints. Part IV summarizes the results of the Study Phase, and recommends a single design approach.

II.2 Phase Lock Loop Analysis

More in-depth analysis of the detection and measurement processes, key elements of any Type A or Type B receiver is required. The combinations are as follows:

Detection
- swept PLL (coherent)
- swept filter (non-coherent)

Measurement
- analog PLL with counter
- hybrid PLL without counter
- analog PLL and measurement of VCO output

It is clear from Part I that the PLL offers both faster sweeping and a lower probability of failing to detect the signal than the swept filter, and therefore gives better performance as the detection device. In any event, system constraints dictate that a PLL must be used to filter the signal prior to measurement. A detailed study of the performance and tradeoffs associated with the design of Phase Locked Loops is therefore justified at this point.

Appendix A to this report examines quantitatively the behaviour and application of PLL's in signal detection. Results from that appendix have been applied in the following discussion which addresses problems in detecting and locking to an ELT signal in an environment of background noise and other ELT signals.

II.2.1 System Constraints

The carrier power-to-noise spectral density ratio is at least 26 dB-Hz and this value will be used in estimating (in a worst case sense) the performance of the system.

The noise is taken to be uniformly distributed over the band which is 12 kHz in width. The signal-to-noise ratio of the carrier in a band of Ω Hz is then

$$SNR = 26 - 10 \log \Omega \text{ dB}$$

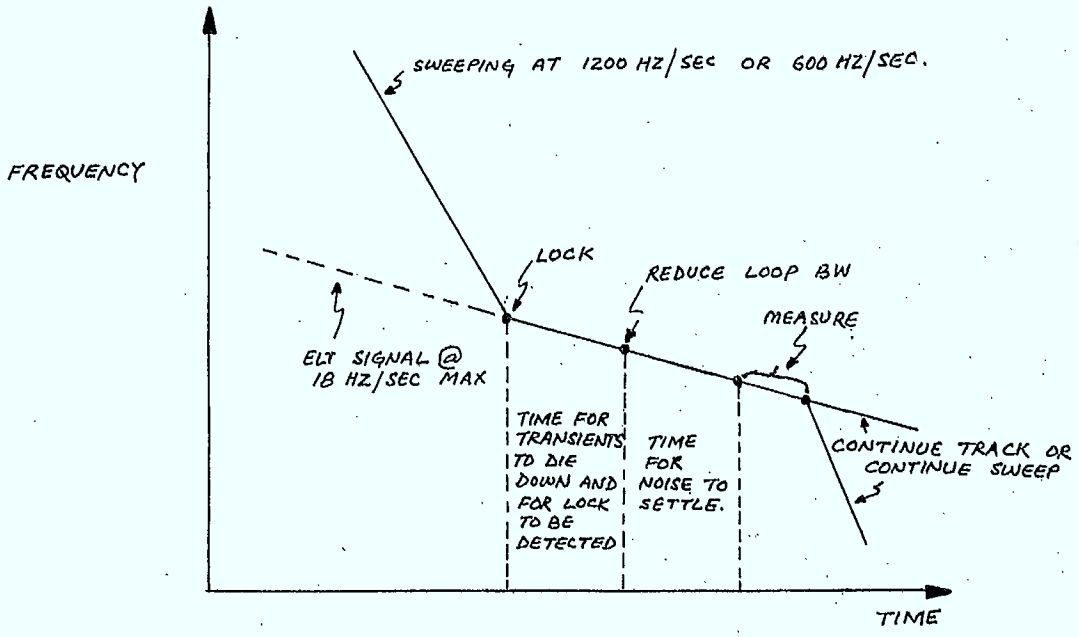
which yields

Filter Noise Bandwidth	SNR
Hz	dB
12,000	-14.8
1,000	- 4.0
100	+ 6.0
50	9.0
30	11.2
10	16.0
5	19.0
1	26.0

In order that the characteristics of the PLL not depend on the amplitude of the ELT signal, it would be desirable that the bandwidth of the "IF filter" preceding the PLL be no more than 200 Hz which would yield an output SNR of +3 dB.

Were a single detection device to be used to cover the 12 kHz band in 10 seconds, an ELT signal would be in the bandwidth of a 200 Hz IF filter 167 milliseconds, and the filter would have a "response time" of 5 milliseconds. Thus, there would be ample time for the filter to respond. Were a 100 Hz filter used, the time would be 84 msec. and 10 msec. respectively and again there would be no problem with response time.

Several alternative methods for acquisition, tracking and measurement are possible, but in general the sequence of operations in time-frequency would be as shown in the following diagram:



and a critical requirement on the PLL is its capability to track the doppler. The steady state tracking error for the second order loop best able to track a frequency ramp is

$$\phi_e = \frac{R}{\omega_n^2}$$

where ϕ_e is in radians, R is the doppler rate in radians/sec, and ω_n is the loop natural frequency in radians/sec. This yields errors:

Loop Natural Frequency Hertz	Tracking Error Degrees
100	0.013
16	0.50
5	5.1
1	128
.1	12,800

for the maximum doppler rate of 14 Hz/sec. Clearly the minimum natural frequency is a few Hertz, which limits the maximum SNR from the loop.

To estimate this maximum, the noise in the loop will be reviewed again. For comparable results it will be assumed that the natural frequency ω_n in radians/second is numerically equal to the PLL noise bandwidth in Hertz, and this yields the following loop SNR's:

Natural Frequency Hertz	SNR dB
16	6.0
5	11.0
1	18.0
0.3	23.3
0.1	28.0

It would appear that an SNR in excess of 10 dB, but less than 18 dB, is to be expected.

The question of acquisition time also requires more detailed consideration. If lock is identified by synchronous detection, then the time constant of the detection system will determine how quickly lock can be determined. The minimum time is influenced by the signal to noise ratio, but the tracking rate and the settling time are also relevant, as the previous diagram shows.

II.2.2 The Process of Lock Acquisition

Two major approaches for acquiring lock are available. In the sweeping method, the incoming signal is mixed with a reference sinusoid whose frequency is linearly swept, continuously or in fine steps, across the 12 kHz range. The stepping approach calls for the frequency of the reference to be moved across that same range in coarse steps which are, however, not so large that "instantaneous" lock is precluded. In both cases, when lock is detected the stepping or sweeping process is halted.

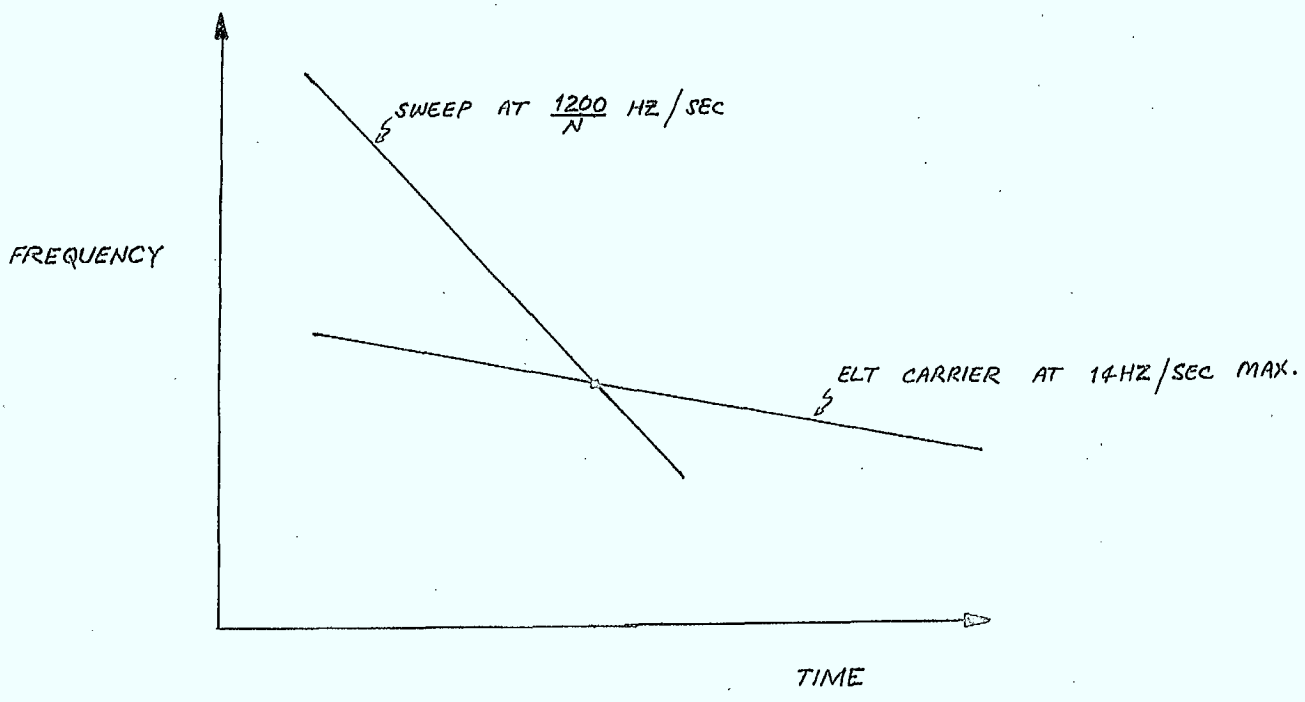
In this analysis, certain basic facts may be taken to apply. The PLL will be of second order with an input which is a "noisy sinusoid", i.e. a sine wave plus lower power, narrow band (100 Hz) noise, when an ELT carrier is present. This carrier will exhibit a linear doppler shift ranging from 0 to 14 Hz/sec, and the sweep rate will be $\frac{1200}{N}$ Hz/sec, where N is the number of detection devices being used (say 1,2, or 4).

The detailed processes of acquisition require complicated analysis which has only been successful in restricted circumstances. Fortunately this detail is not needed here where we shall be guided by a few basic concepts. First, if the frequency deviation, Δw, between the PLL input (psuedo) sinusoid and the VCO output is considerably greater in magnitude than the loop natural frequency, w_n, then lock will be acquired only gradually. The time required for this "natural" acquisition is given approximately by:

$$T_a = \frac{(\Delta w)^2}{2\zeta w_n^2}$$

where ζ is the loop damping ratio and the loop has high gain, There is an upper limit on Δw which will not be of importance here, but a lower limit exists which is very significant. If $\Delta w < 2\zeta w_n$, then lock is "instantaneous" which means (to quote Gardner, page 44) "the loop locks on immediately without skipping cycles. The lock-up transient occupies a time on the order of $1/w_n$ seconds."

The acquisition process can be illustrated by a diagram of frequency vs time which, if there were no acquisition and lock by the PLL, would be:



As the sweep approaches the carrier, the natural acquisition process may come into effect. To check this we must make some assumptions about the system being used and these are:

$$w_n = 2\pi f_n = 2\pi\ (16) = 100 \text{ rad/sec}$$

and $\zeta \simeq 1$

In that case, the formula for acquisition time gives an acquisition rate of*

$$\frac{\Delta w}{T_a} = \frac{2\zeta w_n^2}{(\Delta w)^2} = \frac{2 \times 10^4}{(\Delta w)^2} \quad \frac{\text{radians}}{\text{second}^2}$$

but to be a noticeable phenomena this must exceed the sweep rate of

$$2\pi \ \frac{1200}{N} \ \text{rad/sec}^2.$$

That means

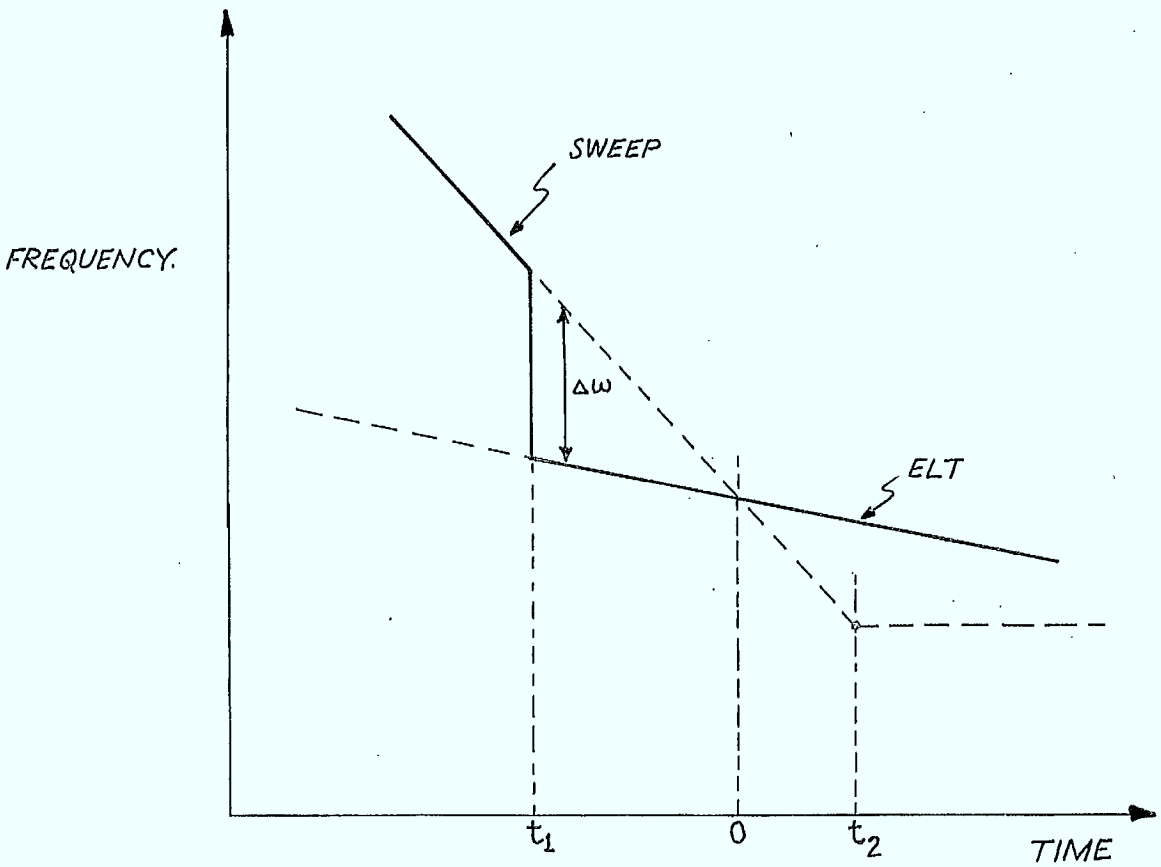
$$\Delta w < 1.6 \sqrt{N} \quad \text{rad/sec}$$

but since f_n = 16 radians/sec, it is clear that this effect will not be felt outside the range of instantaneous lock.

---

* "Pull-in" is also very sensitive to d.c. offsets, pick up, coloured noise and other contributions not accommodated in this model but which might affect the design.

Consequently, only when $\Delta w \tilde{>} 200$ rad/sec will acquisition commence and the frequency-time diagram becomes



where time 0 is taken to be the time of intersection between the sweep and the carrier, t_1 is the time when instantaneous lock occurs, t_2 is the time when the sweep is stopped and Δw is the frequency off-set of the VCO. The solid line is the trace of the sum of all demodulator frequencies used to obtain the low pass signal at the input to the PLL filter.

Since

$$\Delta w \approx 2\zeta w_n \approx 200 \text{ rad/sec},$$

$$t_1 = \frac{200\ 10^3}{2\pi\ \frac{1200}{N}} = 26.5\ N \text{ msec}$$

and the settling time for the loop is

$$\frac{1}{f_n} = \frac{10^3}{16} = 62.5 \text{ msec}$$

then it is apparent that t_2 will be positive given a lock detection time of $\frac{1}{f_n}$ seconds, unless $N \geq 3$. This assumes, naturally enough, that the sweep is stopped as soon as lock is detected. For $N = 1$, $t_2 = 36$ msec, for $N = 2$, $t_2 = 9.5$ msec, and since two or more detectors are most likely to be used, it may be concluded that there will be little overshoot of the sweeping frequency unless reliable lock detection requires considerably more time than assumed.

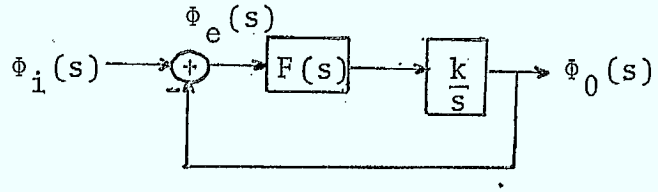
In the stepping method, the frequency of the local oscillator preceding the PLL is changed in coarsly quantized steps, and if these steps are less than $4\zeta f_n \simeq 64$ Hz, then instantaneous lock will occur if an ELT is within that band.

Following the previous assumptions, 62.5 msec would be needed to detect lock and this sets a minimum time between steps. Assuming $2^8 = 256$ steps of 47 Hz width gives 78 msec between steps if two detection devices are used, and this would be marginally viable.

To obtain more time for the measurement of ELT's detected, and for false detections, the natural frequency of the PLL could be somewhat increased. This has the advantage of both increasing the step size and reducing the loop settling time. For example, if 128 94 Hz steps were used, and f_n set at 25 Hz to allow a 6% overlap in the lock-in ranges, the settling time would become only 40 msec.

II.2.3 Lock Detection

Given the equivalent PLL model:



where $\Phi(s)$ is the Laplace Transform of $\phi(t)$, and $\phi_i(t)$ is the phase of the input signal, $\phi_o(t)$ the phase of the VCO output, and $\phi_e(t)$ is the difference in phase between the two signals, then:

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{\frac{kF(s)}{s}}{1+\frac{kF(s)}{s}} = H(s)$$

and

$$\Phi_e(s) = [1-H(s)]\ \Phi_i(s)$$

Now, if the PLL is well designed and locked to an input, then

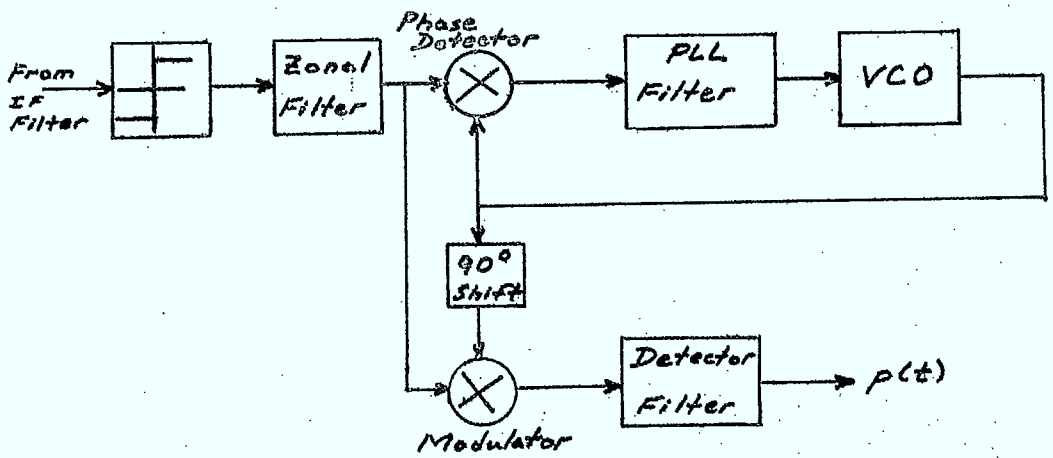
$$H(jw) \simeq 1$$

for $w < w_n$, where w_n is the natural frequency (in radians/second) of the loop. Consequently

$$\Phi_e(jw) \simeq 0$$

for $w < w_n$.

Now take the lock detector to be activated by the signal p(t):



where the bandwidth of the detector filter equals that of the PLL (i.e. w_n radians/second). It follows from the above that, when the loop is locked, p(t) consists of a d.c. signal with no (or more realistically very little) additive noise because in the band of the detector filter

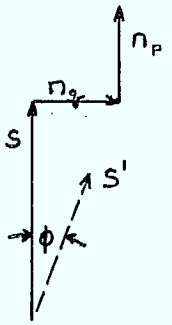
$$\Phi_e(jw) \simeq 0$$

and there is no phase error . In the other situation, when there is no ELT carrier present, the VCO output is drifting slowly in the vicinity of its nominal "zero-input" output frequency, and so the noise in the band is that in the IF filter bandwidth,but "beat to zero".

Without reducing the generality of the results, the VCO output (pseudo) sinusoid may be taken to have unity amplitude. Now, the signal from the IF filter when an ELT signal is present is

$$S \cos wt + n_p(t) \cos wt + n_q(t) \sin wt$$

and this may be shown in a phasor diagram as



The total noise is a narrow band process:

$$n(t) = n_p(t) \cos wt + n_q(t) \sin wt$$

where

$$\overline{n^2} = \overline{n^2}_p = \overline{n_q^2}$$

and $n_p(t)$ and $n_q(t)$ are independent low pass processes occupying the same bandwidth as the PLL.

As shown in the previous analysis, when locked the PLL tracks the limiter output, shown as S' on the diagram and taken for convenience also to be of unity amplitude. The modulator output is then

$$\{\cos[wt + \phi(t)]\}^2$$

which gives

$$p(t) = \frac{1}{2}$$

in the steady state. There is, as noted before, ideally no noise variance associated with this signal. The main effect of the noise lying outside the band of the PLL and the detector filter is simply to somewhat modify the effective characteristic of the limiter/phase

detector circuit.

However, when an ELT carrier is not present, the limiter output is a sinusoid of unity peak amplitude and randomly varying phase, i.e, $\cos[\omega t + \theta(t)]$, with a noise bandwidth the same as that of the IF filter. Consequently the mixer output is

$$\cos[\omega t + \theta(t)] \cos[\omega t + \Delta t + \gamma(t)]$$

taking the VCO output frequency to be offset Δ and phased at $\gamma(t)$. Since Δ is small by comparison to the bandwidth of the IF filter, and $\gamma(t)$ is a very slow process, the statistics of the signal when viewed in the detector filter bandwidth is just as if the mixer output were

$$\cos [\omega t + \theta(t)] \cos \omega t$$

$$= 1/2 [\cos \theta(t) + \cos (2\omega t + \theta(t))]$$

The power of the limiter output (0.5) is then equally split between the two bands. In the lower band, it is distributed from 0 Hz to the half noise bandwidth of the IF filter, and so the average power level of the random signal p(t) is

$$\frac{1}{2}\left(\frac{1}{2}\right)\frac{f_n}{W_{IF}}$$

where the detector bandwidth is taken to be $f_n = \frac{\omega_n}{2\pi}$ Hz, and W_{IF} is the IF filter bandwidth in Hz.

Since the noiseless d.c. power out when a signal is present is 0.25, the relative noise power when the signal is absent is

$$\frac{f_n}{W_{IF}}$$

When tabulated, taking W_{IF} = 100 Hz, this is:

Detector Bandwidth f_n Hz	Relative Noise Power dB
100	0.0
50	-3.0
16	-8.0
10	-10.0
5	-13.0
3	-15.2
1	-20.0

An alternative approach to obtaining a signal for a detection decision device is to obtain a modulator input directly from the IF filter output rather than from the limiter output as in the case just analysed. Then the noise at the output of the detector filter is

the same whether or not the signal is present. For comparative purposes, take the ELT carrier to have unity peak amplitude so that the d.c. level of p(t) when signal is present is 1/2, as before. Following the previous analysis the noise power in p(t) is given by

$$\frac{1}{2}\left(\frac{1}{2}\right) f_n \qquad \text{(noise power density)}$$

To achieve some form of comparison between this and the previous case, this noise power should be doubled as it is present when the signal is present and the loop locked, and when it is not. If we also note that the noise density (per Hz) is at least 26 dB below the carrier (which here has a relative level of -3 dB) then the effective noise power is (10 log f_n - 32); and the d.c. signal power is -6 dB. The result is a 6 dB advantage over the previous case:

Detector Bandwidth f_n	Relative Noise Power
Hz	dB
100	-6.0
50	-9.0
16	-14.0
10	-16.0
5	-19.0
3	-21.3
1	-26.0

From this analysis it is not immediately clear which lock detection process should be used. Use of a simple level detector suggests that the second method would be superior for any signal greater than -6 dB with respect to the typical value specified. Alternatively, a more sophisticated device taking advantage of the rather different situations of "signal present" and "signal not present" in the first case could prove to have overall superiority.

Finally, it should be noted that these are steady-state calculations requiring about f_n^{-1} seconds after the signal is present (and lock first acquired) to become valid. That same amount of time will be needed before the phase transients in the PLL associated with lock acquisition become negligible.

II.2.4 Signal Acquisition and Tracking

In this section it will be assumed that in the search mode the PLL is moved in precise steps across the 12 kHz band, and that a compensated integrator is used for the loop filter. Both the A and B type of system will be covered.

1. Step Timing

A first consideration is the number of steps to be used in searching across the band, and the time taken for the search. This is most critical for some Type A systems where there is a severe timing

constraint, Since frequency measurements are needed every 10 seconds, on the average, the search period cannot exceed 10 N seconds, when N is the number of search devices. If 2^n steps are used, the time per step is $\frac{10N}{2^n}$ seconds, and the size of each step is $\frac{12000}{2^n}$ Hz.

As the bandwidth of the IF filter will be about the same as the step size, a settling time for this filter of about $\frac{2^n}{12000}$ seconds will be needed. A further settling and detection time of $\left(\frac{2^n}{12000}\right)2.8$ seconds will be needed for the PLL, since the "instantaneous" acquisition range of the loop is $4\zeta\ \omega_n$ rad/sec. and this range must equal the step size. Consequently, the loop settling time is of the order of

$$\frac{2\pi}{\omega_n} = 2\pi\left[\frac{12000}{2^n}\ 2\pi\ \frac{1}{4(0.707)}\right]^{-1} = \left(\frac{2^n}{12000}\right)2.8 \text{ secs}$$

and the minimum time per step should be in the order of the sum of these times, i.e. $\left(\frac{2^n}{12000}\right)3.8$ seconds.

The relative size of these quantities may be seen from the tabulation:

Nbr. of Steps	Step Size	Min. Time Needed	Time per Step msec				
	Hz	msec	N=2	3	4	6	8
128	94	41	156	234	312	468	626
256	47	81	78	117	156	234	313
512	23	162	39	59	78	117	156
1024	12	324	20	30	39	59	78

From there it is immediately seen that no more than 256 steps are possible unless 8 devices were used at which point 512 steps would be marginally possible. For 2 devices, 256 steps are similarly marginal.

2. Noise Constraints

Ambient noise sets an upper limit on step size as the ω_n of the loop is necessarily proportional to step size as pointed out in the last section. For 128 and 256 steps ω_n is 211 and 106 rad/sec respectively yielding loop SNR's of 1.5 dB and 4.5 dB from the standard formula for a single sided PLL noise bandwidth B:

$$B = \frac{\omega_n}{4\zeta} (1 + 4\zeta^2) \quad \text{Hz}$$

assuming C/N_o = 26 dB-Hz, a 1 dB loss in the phase detector, and ζ = 0.707.

This is a relatively large noise bandwidth for a second order filter and stems from the roll-off outside the band of only 6 dB/decade. As the IF filter would have the same nominal bandwidth, even a single pole filter would add another 6 dB/decade to the roll-off and improve the SNR by 1.8 dB to 3.3 and 6.3 dB respectively. A double pole IF filter would yield 3.7 and 6.7 dB. (By approximate asymptotic calculations, the noise bandwidth of a filter of nominal bandwidth W is $(1 + \frac{1}{n})$ W where the high frequency roll-off is 6 n dB/dec.).

As at least 6 dB SNR in the loop is recommended for satisfactory performance, 256 steps of 47 Hz and a PLL natural frequency of 17 Hz is strongly indicated. This assumes the necessity to sweep the band once each 10 seconds. If that requirement is relaxed, narrower filters could be swept more slowly, and some improvement in performance would be experienced.

3. Unlocked Conditions

The loop filter being used has a pole at the origin so there is a stability problem when the loop is unlocked. In this section the extent of this difficulty will be established.

An integrater with input white noise at density N_o watts/rad/sec (single sided) produces output noise power $\frac{N_o}{2}$ t, where t is the time from the start of integration. Since the VCO output frequency is related to the input phase difference by the transfer function

$$\frac{K\ (1 + \Gamma s)}{s}$$

The random fluctuations of the frequency of the VCO will grow with time when the loop is unlocked.

When the loop is not locked, the output of the phase detector will be randomly distributed between $+\frac{\pi}{2}$ and $-\frac{\pi}{2}$ with an average power

of $\frac{1}{3}\left(\frac{\pi}{2}\right)^2 = 0.82$. This power will be mainly distributed over the half noise bandwidth of the IF filter. Taking this filter to be of a nominal 47 Hz double sided bandwidth with 12 dB/dec roll off, the bandwidth of the noise from the phase detector is

$$\frac{1}{2}\ (1.33)\ 47\ (2\pi) = 196 \text{ rad/sec}$$

and so has a single sided density of $\frac{0.82}{196} = 4.2$ mwatts/rad/sec.

The resulting noise power from the VCO (in terms of its output frequency in radians/sec) is

$$(K\Gamma)^2 \overline{n^2} + K^2\ \frac{N_o}{2}\ t$$

and the filter constants, in terms of the loop parameters, are

$$K = \omega_n^2 = 11400 \text{ or } 247$$

$$K\Gamma = 2\zeta\omega_n = 151 \text{ or } 22.2$$

$$\Gamma = \frac{2\zeta}{\omega_n} = 13 \text{ or } 90 \text{ msec}$$

for the two cases: $f_n = 17$ Hz, $\zeta = 0.707$ and $f_n = 2.5$ Hz, $\zeta = 0.707$. The noise power is then

$$(151)^2\ 0.82 + (11400)^2\ \frac{4.2}{2}\ \frac{t}{(1000)}$$

$$= (18,7 + 273\ t)\ 10^3$$

and $$(22.2)^2\ 0.82 + (247)^2\ \frac{4,2}{2}\ \frac{t}{(1000)}$$

$$= 404 + 128\ t$$

for the two cases, and where t is in seconds.

The rms frequency from the VCO is then given by $522[t + 0.068]^{1/2} > 137$ for the search phase and $11.3\ [t + 3.2]^{1/2} > 20$ for the tracking phase. The minimum value almost equals the VCO operating range of about $2\pi\ (25) = 157$ rad/sec during the search phase, with the result that initially the VCO will be rapidly switched back and forth between the positive and negative extremes of its range of operation. As time progresses, the integrator output will cause a drift toward one limit or the other. The rms drift will equal the VCO operating range when

$$522t^{1/2} = 157 \text{ or } t = 90 \text{ msec}$$

at which time the probability of the device being in saturation would be high. However, since the minimum acquisition time is less than 100 msec no serious difficulty will be experienced if the filter capacitor is discharged at the beginning of each step and the loop not released until the IF filter output has settled. In the tracking phase, the corresponding interval is given by

$$11,3t^{1/2} = 157 \text{ or } t = 193 \text{ seconds}$$

and drift would not be a problem.

4. Adjacent ELT Carriers

Given two carriers within the bandwidth of the phase locked loop it would be expected that the loop would track the stronger signal. However, the VCO would be modulated at the difference frequency and the frequency measurement would be in error. Since the measurement period is 0,25 sec. and the frequency difference less than about 3 Hz, phase error ϕ is

$$\phi < 2 \frac{D}{S}$$

where D is the amplitude of the interference, and S is the amplitude of the signal being measured. A phase change ϕ corresponds to an error in count (assuming the particular fixed period counter proposed) of $\frac{\phi}{\pi}$ since there is one count for each π radians of phase. In our case, since frequency is twice the count, the frequency error is

$$\Delta f = \frac{2\phi}{\pi} < \frac{4}{\pi} \frac{D}{S} < \frac{4}{\pi} = 1,3$$

since this analysis is not valid if D > S as the loop would not then maintain lock on the signal. Such an error bound is outside the system specifications, although average performance would be considerably better.

Unfortunately, the lock detector would not identify that this phenomina was occuring as the loop will continue to maintain close to zero phase error. The best procedure would appear to be to use extrapolation methods, to be described later, to inhibit measurements when ELT's intersect. If two ELT's inhabit the same band when first detected, the poor fit of the ELT trace during later data processing would indicate the presence of an interference signal.

Such procedures would also handle the situation where the PLL jumped lock between two competing signals in the loop bandwidth.

Signals separated by more than the loop bandwidth, but less than the IF filter bandwidth pose a different problem. Following Kliger and Olenberger, a loop locked to a signal of amplitude S will "jump" to a signal of amplitude D if

$$\frac{D}{S} > \frac{\Delta\omega}{2\zeta\omega_n}$$

approximately, where $\Delta\omega$ is the difference in frequency (rad/sec) between the two signals. The approximation is good if $\Delta\omega > 4\zeta\omega_n$.

As a consequence, once two signals of different amplitude co-exist within the IF bandwidth there is a high likelihood that the lock on the weaker signal will be lost. The more equal in amplitude the signals are, the closer together they will approach before the phenomena occurs. It should also be noted that, while this is a

jump in frequency, it is not a jump in time and takes place relatively slowly. Little appears to be known about the time required except that the jump takes longer the greater the separation. As the basic phenomena are similar, it may be that the times are similar to those taken for natural lock acquisition.

When the disturbing signal is outside the band of the IF filter, the same jump can occur, however the disturbance must have sufficient amplitude to overcome the attenuation due to the IF filter. If that filter has a 50 Hz bandwidth and 12 dB/dec roll-off, then with a 100 Hz separation, the ratio of magnitudes would have to be in the range:

$$10 \log\left(\frac{100}{3}\right)+24 > \left(\frac{D}{S}\right)_{dB} > 10 \log\left(\frac{100}{3}\right) + 12$$

or

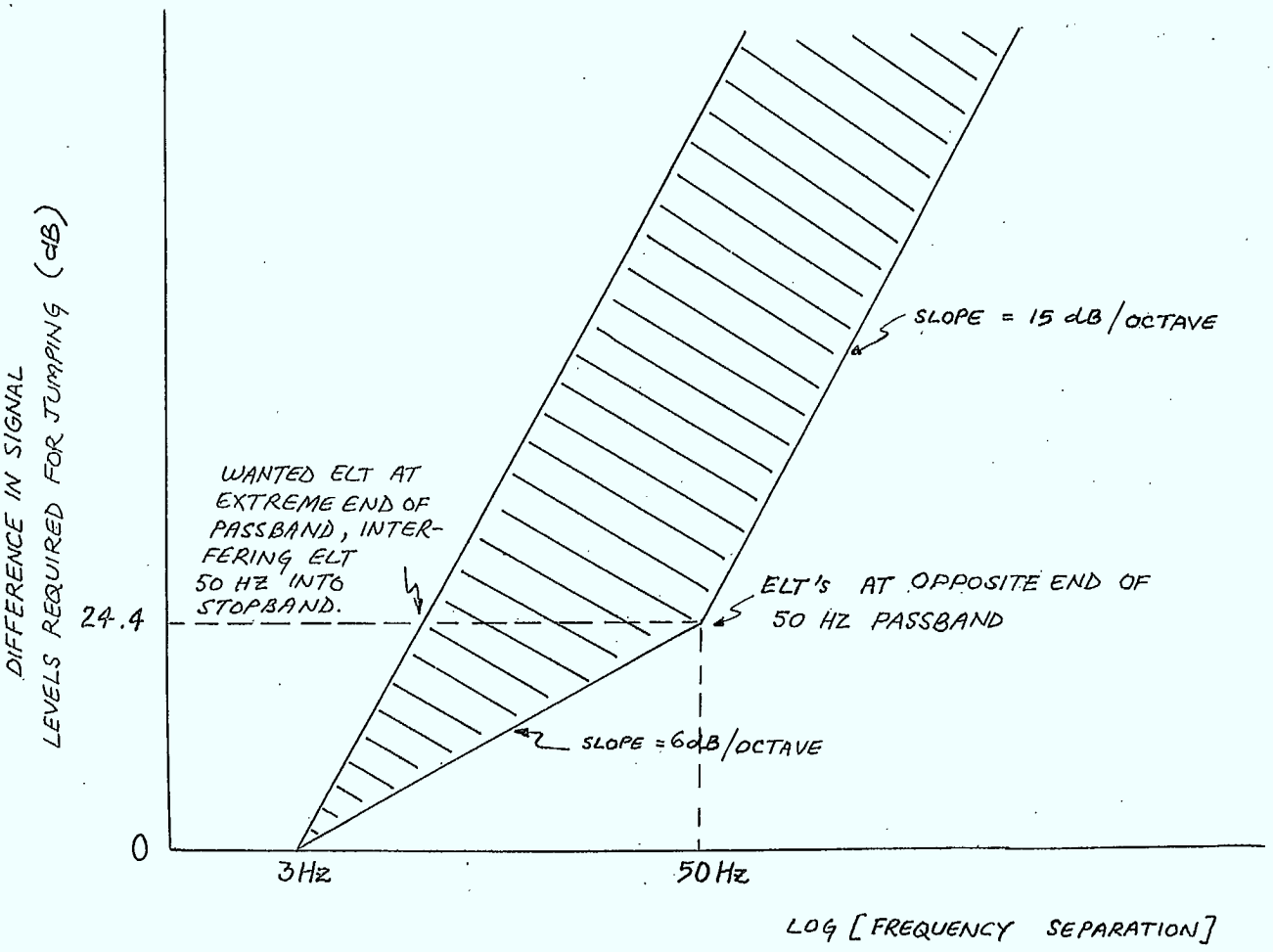
$$39 > \left(\frac{D}{S}\right)_{dB} > 27$$

depending on the detailed circumstances and a 3 Hz tracking bandwidth. For a 200 Hz separation, under the least inhibiting circumstances a 54 dB differential would be needed.

It may be concluded that these jumps can be expected in and somewhat beyond the 50 Hz IF filter bandwidth. They would be unlikely, although possible, beyond the 100 Hz separation specified. As well,

unlike the situation within the tracking bandwidth, they would result in a loss of lock as the VCO would be pulled away from the frequency of the smaller signal being tracked. Even within the band of the tracking loop this would result in a beat tone in the synchronous lock detector output. Designing the detector to respond to this would ensure that lock would be broken with the result that measurement would cease and no errors made.

The following graph illustrates the situation:



and if the relative amplitudes of two signals exceed these values, lock will be lost. The shaded area is a range of ambiguity where loss of lock is not certain, but depends on the detailed situation.

The above discussion pertains primarily to the Type B systems. Although the same phenomena will occur, the effect on a Type A system will be very different as each measurement is preceded by an acquisition phase where the loop has a lock-in range of 50 Hz. Initial "instantaneous" lock can only occur within that range, although thereafter the signal may be pulled out of lock by a larger, out of band signal. However, a relatively long time is taken for this jump in frequency to occur, and the loop filter is soon switched (within 100 msec) to the tracking mode. This leaves little time for the drift to occur, and after the loop bandwidth is reduced the drift from lock is even slower. If the formula for natural acquisition is approximately valid, then for a 50 Hz separation the time for the frequency jump is

$$\frac{(\Delta\omega)^2}{2\zeta\omega_n^3} = \frac{(50)^2}{2\ (0.707)\ 2\pi\ \ (2.5)^3} = 18 \text{ seconds}$$

but only about 1/3 of a second is needed for the completion of the measurement process, which is consequently likely to be completed without loss of lock.

Within the loop acquisition range, however, the PLL will track the

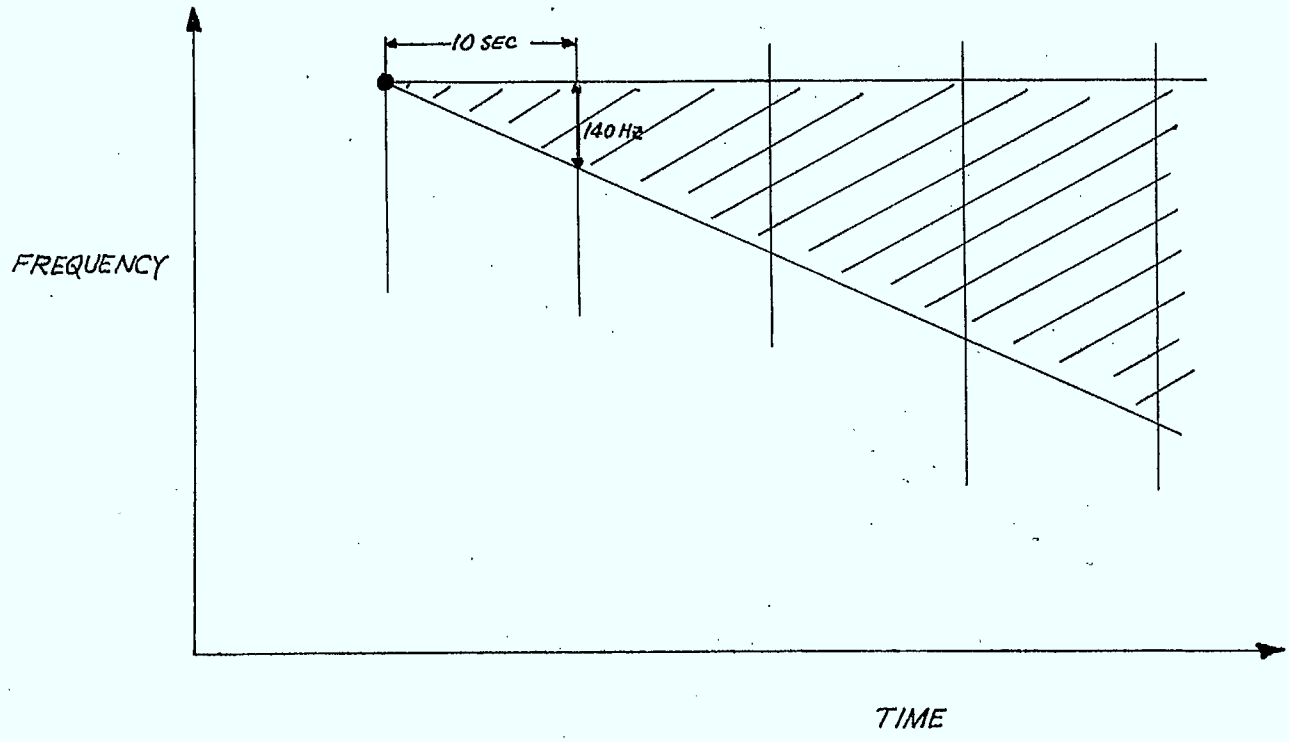
sum of the two signals as noted previously. As a result, when the loop bandwidth is narrowed for the tracking phase, it is unlikely that lock will be maintained. It follows that the Type A system would not operate satisfactorily with two signals within the same 50 Hz step unless one were considerably the smaller. It should be noted, however, that for the same reasons, a type B system with a comparable acquisition process would fail to acquire these signals unless they were previously detected when not in the same step interval.

5. Acquisition of New ELT's

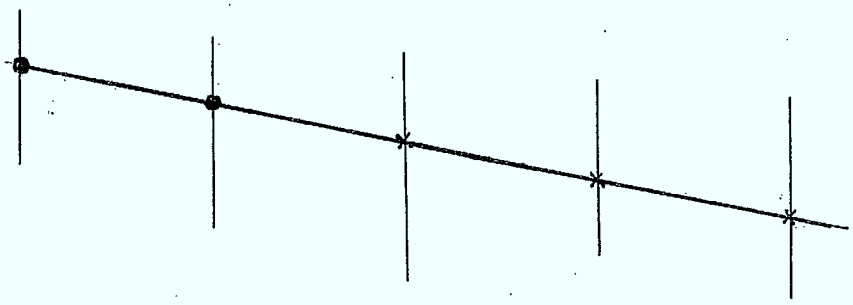
With both system types there is virtually no likelihood that a spurious signal detected during the acquisition stage would remain in lock through the first measurement stage. Hence, any successful measurement may be taken as the acquisition of an essentially modulated carrier. There is somewhat more of a problem in associating a sequence of measurements with a particular ELT.

A Type B system poses less of a problem, and no problem at all if continuous lock is maintained. If lock is lost, however, it is necessary to track the ELT as will later be described in more detail. This necessitates a nearly identical extrapolation system for both types following the process which will now be described.

A time-frequency diagram eases visualisation of the process;

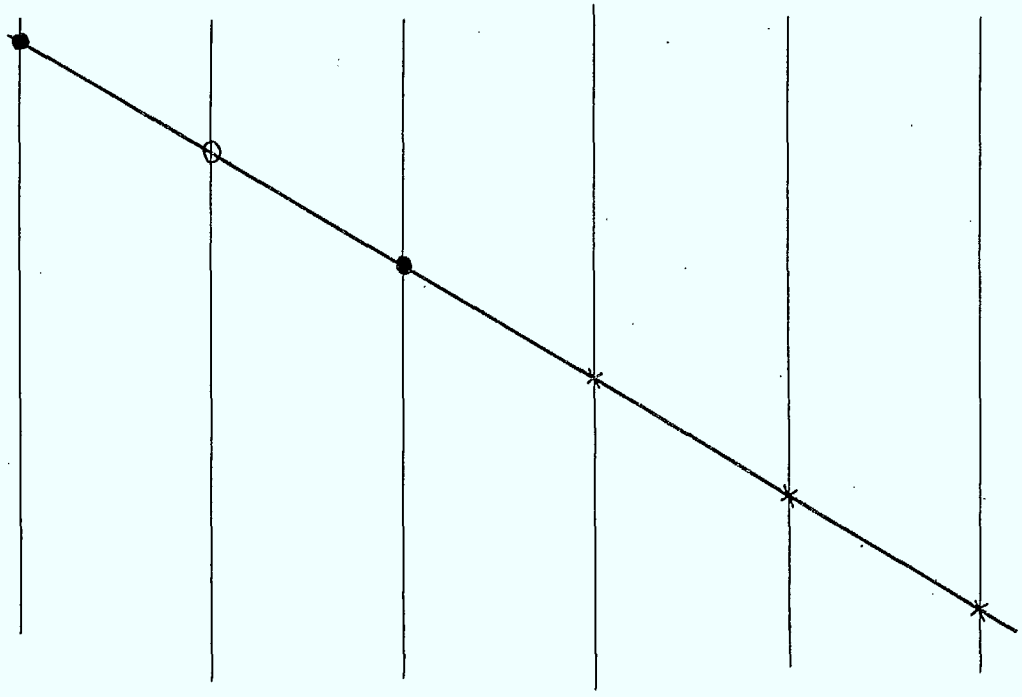


The solid dot indicates a detected ELT and the shaded area gives the range of the possible next measurement. If a measurement is completed approximately 10 seconds later it will be possible to anticipate the next (say) 3 measurements as shown.



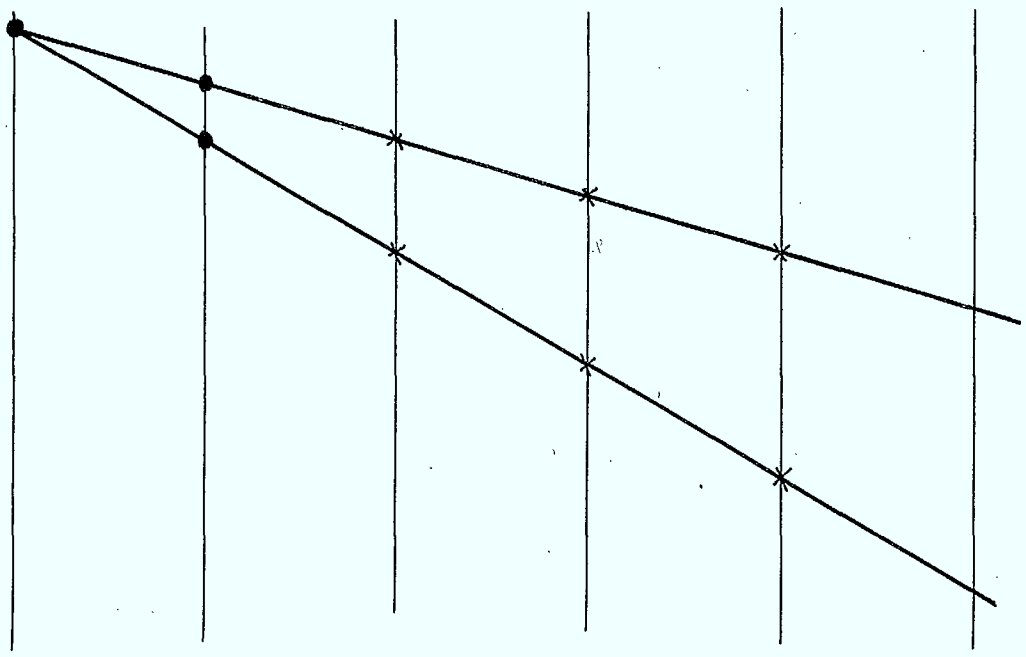
where the x's are the expected future measurements (within an ambiguity of 20 Hz due to the second derivative of the ELT traces).

If the second measurement were not made, the process would become:



with the solid circle being an interpolated data point, and with the assumption that a measurement was made in the next period. This process would be continued even if that did not occur and no ELT would be declared lost until (say) 3 periods had passed without a valid measurement.

Should two measurements occur within the shaded area;



then two projections would be made as shown. A single future measurement would be needed to resolve the ambiguity. Three consistent measurements, each separated by not more than 3 measurement periods, would confirm the identification of a new ELT.

7. Missed Measurements

Measurements not completed for whatever reason would be replaced by interpolated values. Three "misses" in a row would terminate the tracking of an ELT.

Similarly, when two ELT traces approached within the range of possible confusion of the system, and were projected to remain within that band for 3 measurement periods, the ELT records would be terminated. If the traces were projected to be sufficiently separated after 1, 2 or 3 periods, tracking would continue by the projections and the PLL's not "released" until the necessary separation had occurred.

However, these projections are not error free, and ELT data indicates a maximum doppler second derivative of 0.2 Hz/sec^2 and hence projection uncertainties:

Projection Interval	Uncertainty
Secs	Hz
10	20
20	80
30	180

Since a Type A system is only capable of distinguising and measuring ELT carriers spaced at least 50 Hz apart, there is no possibility that the software will incorrectly sort measurements taken every 10 seconds. Only when one or two measurements of closely spaced ELT's are missed, a rare event, do the projected admissable regions for two ELT's overlap. Even, then, with the region of overlap bisected, it is highly likely that resumed measurements will be correctly sorted. Therefore, we can conclude that no information is lost in "shuffling the deck" of frequency measurements for ELT's

more than 50 Hz apart; i.e. the Type B offers no sorting advantage over the Type A in the common operating range ($\Delta f > 50$ Hz).

The Type B receiver is capable of tracking and measuring ELT's at frequency separations much less than 50 Hz. Since, under such circumstances, it cannot be assumed that the PLL's will remain with their assigned ELT's, sorting may be required in which case the above uncertainties are significant. This problem will be addressed in the following section.

8. Loss of Lock

As just mentioned, loss of lock in the Type B system is a problem. Three events occur: broadband noise (with the same half-bandwidth of the IF filter) appears at the VCO input with rms value(in terms of frequency output) of $\frac{20}{2\pi} = 3.2$ Hz; a random drift away from the previous lock frequency develops and increases with time, giving an rms drift of $1.8\ t^{1/2}$ Hz; the ELT signal frequency changes at a rate as high as 14 Hz/sec. If the signal reappears (when the ELT is pulsed, for example) a second or two later, it is quite probable that the 3 Hz lock in range will be exceeded.

At least two solutions are possible. In the simplest, the filter would simply be switched back into the broadband mode. As several seconds would be required before an ELT with the fastest doppler would be beyond lock-in range, lock would be readily required so long as the situation were not complicated by another signal in the band. With this method, a Type B system would essentially perform as a Type A system for pulsed ELT's.

A more elaborate method would re-initialize the VCO output to a projected frequency every (say) half second after lock was lost. This would maintain doppler uncertainty within $0.05n^2$ Hz, and drift within 0.45 Hz rms, where n is the number of half-seconds since the last frequency measurement. Clearly this would suffice for n as large as 10, but would not cover the inter-measurement period of 10 seconds. This means that a frequency reading would be needed every second or so to provide input for this projection, or that the second derivative of the ELT trace would have to be projected, although a fairly rough projection would suffice.

The other difficulty associated with intermittant loss of lock is the possible disruption of a frequency measurement. For some ELT's this can result in very deteriorated performance, but it will be shown later that techniques are available which may greatly ameliorate this problem.

Unfortunately, loss of lock cannot be detected immediately, but once it is lost the VCO is subjected to a burst of noise (rms amplitude 3.2 Hz referred to the VCO output) and to a drift ($1.8\ t^{1/2}$ Hz). Assuming that the lock detector circuit dynamics operate in the acquisition (broadband) loop settling time of $\frac{2\pi}{17} = 0.37$ seconds, the measurement may well be completed before the loss of lock is known. As well, the output of the synchronous demodulator, as seen in the bandwidth of the acquisition loop, will be noisy during the tracking mode as the bandwidth of zero phase error will be that of the tracking loop - which is almost an order of magnitude smaller. That noise will complicate the detection of lost lock.

However, assuming that loss of lock can be detected with an accuracy much better than the (perhaps) inevitable detection delay, it may well be possible to salvage these interrupted measurements.

9. Effects of Signal Modulation

As just described some pulsed ELT's will be less well measured by both system Type A and B unless special - and for the moment hypothetical - techniques are implemented.

Incidental FM in the ELT carrier is characteristic of some signals. This appears to be a sawtooth sweep synchronized to the modulation sweep rate which lies between 2 and 4 times per second. If the maximum frequency deviation is Δ, the rate is between 2Δ and 4Δ Hz/sec, and should this exceed several times the maximum doppler rate, the loop would be unable to retain lock. Taking the peak rate for lock to be about 40 Hz/sec, the maximum Δ would be in the range of 10 to 20 Hz. For deviations beyond that, lock could not be held and no measurements could be made.

However, assuming that lock is maintained, further difficulties are encountered which were analysed in the mid-term report. There it was shown that it was necessary that $\Delta F < 8$ Hz for the peak frequency error to be less than 1 Hz. Signals beyond this range, but still within the locking capabilities of the PLL would produce measurements with unusual error variance.

The slowest ELT sidebands are swept in frequency at 1400 Hz/sec which is far beyond the tracking capability of the narrow band filter (which would exhibit a static error $\frac{1400}{(2.5)^2 2\pi}$ = 36 radians). The acquisition loop would exhibit a static error of only $\frac{1400}{(17)^2 2\pi}$ = 0.8 radians and so would be capable of following a sideband. In both cases the spurious signal would have to pass through the IF filter which with a 50 Hz bandwidth would pass the signal for only $\frac{50\ 10^3}{1400}$ = 36 msec. Since the settling time of that filter is $\frac{10^3}{50}$ = 20 msec, there would be an output into the PLL.

If this occurred during the tracking phase with a settling time of 400 msec and a 2.5 Hz bandwidth, the signal would spend just $\frac{(2.5)10^3}{1400}$ = 1.8 msec in the band. Since that is but 0.5% of the settling time, the effect will be insignificant. (The signal as seen at the phase detector output in the loop bandwidth will be a short pulse, of random height depending on the phase difference between the two signals at the time of intersection, and of length of about 2 msec.)

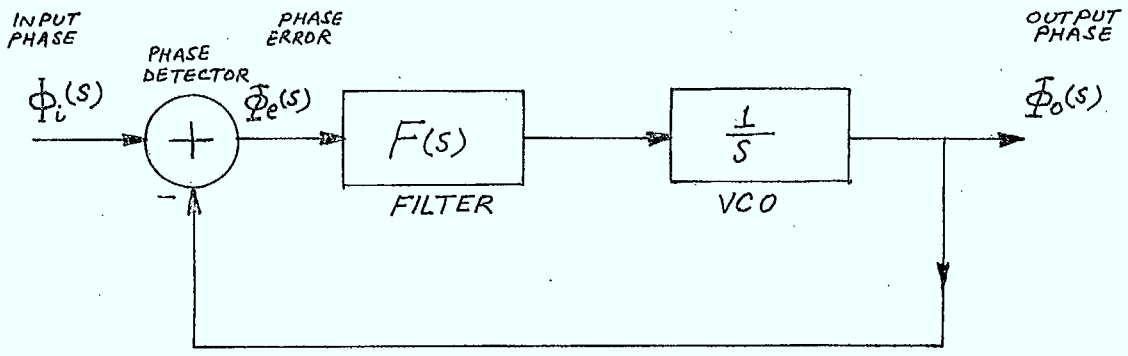
The occurrance of an ELT sideband within the bandwidth of the IF filter at the same time as an ELT carrier is an uncommon event (see p. I-21), but it if does occur, the phase swing as the two signals "close together" is $[(1400)(2\pi)(20)10^{-3}][(20)10^{-3}]$ = 3.5 radians, or just slightly more than π radians. The resulting phase swing would probably not be sufficient to prevent lock although confirmation must await experimental studies.

I.2.5 Third Order PLL's

The second order PLL suffers from the critical limitation that it is not possible to independently control the noise bandwidth of the loop and the steady-state phase errors in tracking a frequency ramp. As bandwidth is reduced to improve the accurate tracking and measurement of the ELT carrier frequency, the phase error increases to the point that lock is lost.

While a compromise has been achieved in the system design, some alternatives have had to be discarded. A third order loop presents a way of overcoming the need to compromise, but at a price. The considerations which lead to a rejection of the third order loop as a possible sub-system will now be developed.

The following diagram will define the symbols being used,



so

$$\Phi_e(s) = \frac{s}{s + F(s)} \Phi_o(s)$$

For a very particular second order system, this becomes

$$\Phi_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \Phi_o(s)$$

where generally $1 < \zeta < 2$, and the noise bandwidth is proportional to ω_n for a given ζ. However, with a frequency ramp input at Ω rad/sec^2, the steady state phase error is

$$\Phi_e = \lim_{s \to 0} \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{R}{s^3} \cdot s$$

$$= \frac{R}{\omega_n^2}$$

and the conflict between an allowable tracking error and low noise bandwidth is clear.

As mentioned, this is true for a certain second order loop. In particular, it is required that

$$F(s) = \frac{k(1 + \alpha s)}{s}$$

For all other second order loops, the tracking error increases indefinitely with time and lock can be held for only a limited period of time.

However, if the filter transfer function becomes

$$F(s) = \frac{k\ (1 + \alpha_1 s)\ (1 + \alpha_2 s)}{s^2}$$

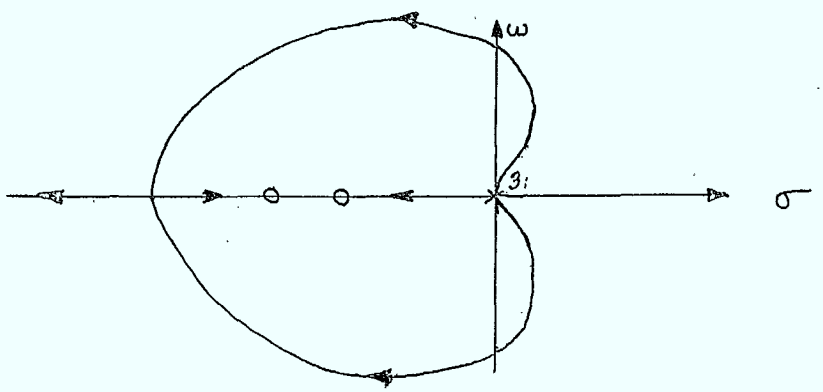
then the conflict no longer occurs, because the tracking error is then

$$\Phi_e = \lim_{s \to 0} \frac{s^3}{s^3 + \alpha_1\alpha_2 s^2 + (\alpha_1 + \alpha_2)\ s + K} \cdot \frac{R}{s^3} \cdot s$$

$$= 0$$

Consequently, no matter what loop parameters are selected there is zero tracking error. It should be noted that this is the only third order loop which exhibits this property.

As was stated, this is not obtained without cost and one component of this cost is the additional design complications to obtain satisfactory loop performance. A rough sketch of the root locus diagram for the system



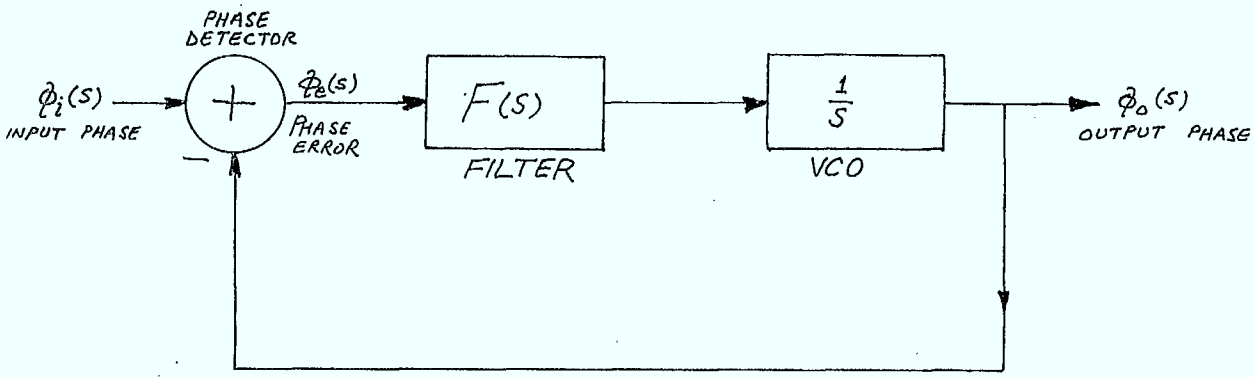
is sufficient to suggest the degree of complication, and it serves also to make the point that the system is only conditionally stable. If the effective loop gain were to become small, as would happen with a very small input ELT carrier, the loop would become unstable. Finally it appears that very little is known about the acquisition properties of third order loops.

The conclusion taken is that the third order loop is not a viable alternative.

II.2.6 Design Considerations for Second Order Loops

1. Filter Type

As explained in the section dealing with third order PLL's a particular kind of second order loop is needed to continuously track a frequency ramp. Using terms defined by



the loop filter needed for tracking is

$$F(s) = \frac{1 + \Gamma_1 s}{s} \quad K_1$$

An alternative is to use a single pole filter so that

$$F(s) = \frac{K_2}{1 + \Gamma_2 s}$$

and the relative advantages of these two filter types will be exposed in the light of the two requirements: acquisition and tracking. Only the first type is a possible candidate for continuous tracking, but both could perform in the acquisition mode.

Looking first at the first situation,

$$\Phi_o(s) = \frac{K_1 (1 + \Gamma_1 s)}{s^2 + K_1 \Gamma_1 s + K_1} \quad \Phi_i(s)$$

and following standard notations for second order systems:

$$\text{damping ratio } \zeta = \frac{K_1^{1/2} \Gamma_1}{2}$$

$$\text{natural frequency } \omega_n = K_1^{1/2}$$

The second case gives

$$\Phi_o(s) = \frac{K_2/\Gamma_2}{s^2 + \frac{1}{\Gamma_2}s + \frac{K_2}{\Gamma_2}} \quad \Phi_i(s)$$

so that

$$\zeta = \frac{1}{2(K_2 \cdot \Gamma_2)^{1/2}}$$

$$\omega_n = \left(\frac{K_2}{\Gamma_2}\right)^{1/2}$$

Clearly the two filters give rather different results, in terms of their performance, even if the damping ratio and natural frequency are identical. Since the time for phase transient to die out is about $\frac{2\pi}{\omega_n}$ seconds, and the range of suitable ζ is the same in both cases, these parameters will be held constant while making comparisons.

A distinctive difference is seen in the two frequency responses, and this is reflected in the noise bandwidths. From Blanchard, page 159, the single sided noise bandwidth of the first type is

$$B_1 = \frac{\omega_n}{4\zeta}(1 + 4\zeta^2) \quad \text{Hertz}$$

and of the second,

$$B_2 = \frac{\omega_n}{4\zeta} \quad \text{Hertz}$$

Taking ζ to about unity, the first type operates at a 7 dB disadvantage under this criterion. For our particular case, assuming a 1 dB loss of SNR in the phase detector, the SNR ratio in the VCO output for the type 2 filter is

$$25 - 10 \log B \qquad \text{dB}$$

which gives

$\frac{\omega_n}{2\pi}$	Type 1 SNR	Type 2 SNR
Hz	dB	dB
30	1.3	8.3
25	2.1	9.1
15	4.3	11.3
10	6.0	13.0
5	9.1	16.1

As this covers the range of ω_n required to acquire lock in a sufficiently short time, a type 2 filter would experience fewer noise problems while acquiring lock. Gardiner (page 23) notes that 6 dB SNR is needed, in general, to obtain lock.

Tracking bandwidths will have to be much smaller, as type 1 is required, and here:

$\frac{\omega_n}{2\pi}$	Type 1 SNR
Hz	dB
5	9.1
4	10.0
3	11.3
2	13.0
1	16.0
0.5	19.1

This indicates a suitable SNR for the measurement of the frequency of the VCO output, given a natural frequency of a zero Hertz.

Another difference between the two types is found in their response to a frequency step. This will govern their response to an ELT when it appears in their instantaneous lock range. For a PLL with a loop filter of the first type, the steady state phase error with a step input of frequency is zero, and for the second type is $2\zeta \frac{\Delta\omega}{\omega_n}$ radians (from Chapter 5 of Blanchard). $\Delta\omega$ is the size of the ω_n frequency step, and if lock is to be maintained, then

$$\frac{\Delta\omega}{\omega_n} < \frac{\pi}{2\zeta} \simeq 1.6$$

given a phase detector operating over a $-\pi$ to $+\pi$ range. By contrast, the maximum phase error in the other case is about $0.3 \frac{\Delta\omega}{\omega_n}$ for $\zeta = 1$, and so lock would be maintained if

$$\frac{\Delta\omega}{\omega_n} < \frac{\pi}{0.3} \simeq 10$$

This result suggests strongly that the acquisition characteristics of the first type of loop will be superior in that the range of frequencies over which instantaneous lock will occur will be larger. On the other hand, it is more susceptable to noise, as might be expected. On balance, since the SNR calculations are conservative, and the steady state phase error is a firm limitation, the first type of filter will be chosen.

2. Filter Parameters

Two parameters, ω_n and ζ, must be chosen and these govern the performance of the PLL in terms of the instantaneous acquisition range

$$\Delta\omega \simeq 2\zeta\ \omega_n$$

and the SNR in the loop as determined by the noise bandwidth

$$\frac{\omega_n}{4\zeta}\ (1 + 4\zeta^2)$$

If ζ is in the typical range from 0.5 to 1, then

$$\omega_n < \Delta\omega < 2\omega_n$$

and SNR could range up to 3 dB greater than given in the last subsection. Choice of ω_n for the acquisition phase is bounded on one side by the desire to maximize the lock in range and minimize the time to acquire lock, and by the loop SNR on the other side. A choice between 10 and 20 Hz would seem probable. Final choices of these parameters will be the result of empirical decisions during implementation.

Since the SNR likely to be obtained for acquisition will not be sufficient for tracking and filtering prior to frequency measurement, the filter bandwidth will have to be reduced to a couple of Hertz in order to obtain a SNR above 10 dB. The limit to which this bandwidth can be reduced will be governed, at least in part, by the tracking error. Given a maximum doppler rate of 14 Hz/sec, the resulting phase error is

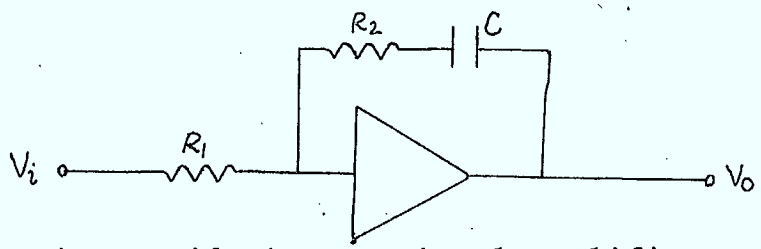
$\Phi_e = 2\pi(14) \frac{1}{\omega_n^2}$ in the steady state. Tabulating this in the probable range of interest gives:

$\frac{\omega_n}{2\pi}$	Φ_e
Hz	radians
5	0.09
4	0.14
3	0.25
2	0.56
1	2.23
0.5	8.91

and it is seen that the phase error will not be a problem for natural frequencies greater than 2 Hz.

3. Filter Switching

The basic filter needed may be realized



and assuming an ideal operational amplifier

$$\frac{V_o}{V_i}(s) = \frac{1 + sR_2C}{sR_1C}$$

and $\Gamma_1 = R_2C$, $K_1 = \frac{1}{R_1C}$. It follows that since $\omega_n^2 = K_1$ and $2\zeta\omega_n = K_1\Gamma_1$, then

$$R_1 C = \omega_n^2$$

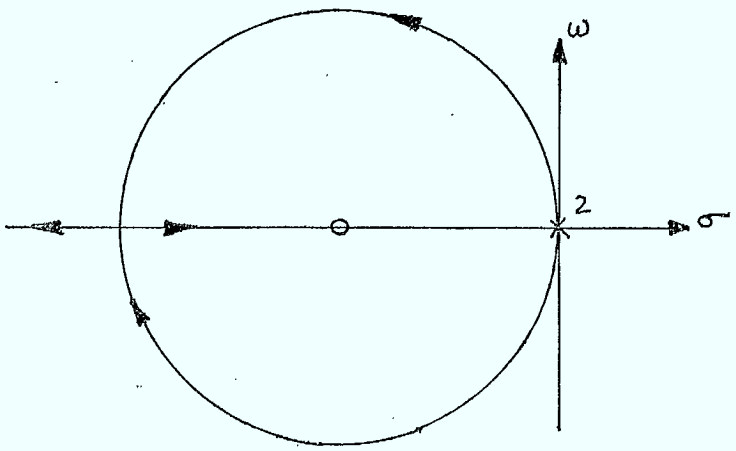
and $R_2 C = 2\zeta/\omega_n$

From this R_1 and R_2 can be determined for an arbitrary choice of C, and any desired system parameters. It is clear that if the resistor values are switched the filter characteristics can be changed as desired.

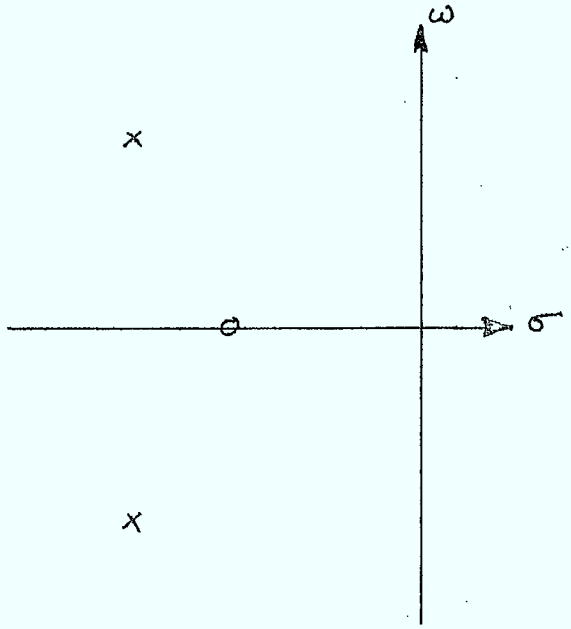
II.2.7 Stability of the Heterodyne Loop

Some PLL sweeping configurations include the IF filter within the overall loop. The result is to complicate the loop design and introduce problems of stability. In our case this is particularly relevant since the IF filter bandwidth and the loop bandwidth are comparable during the acquisition phase.

Without this additional filter in the loop the root locus diagram for our case is

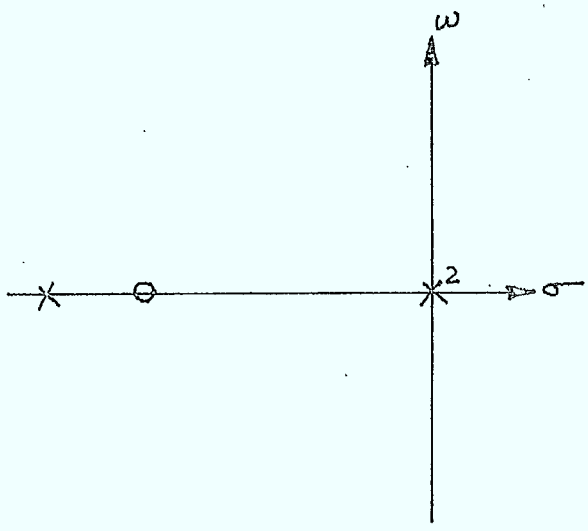


and the loop gain is set to give the following configuration

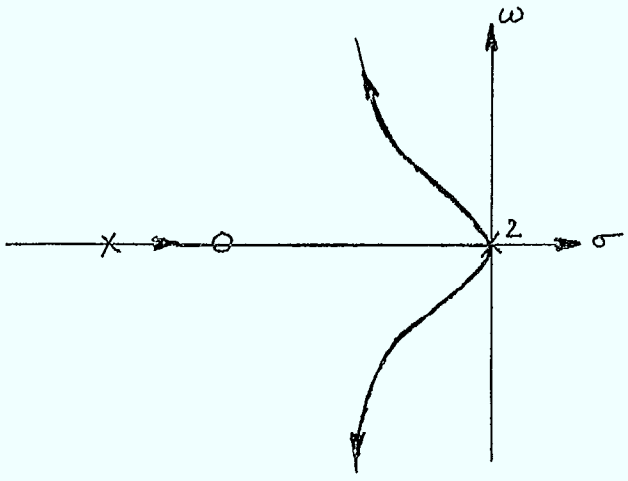


of the poles and zeros of the loop transfer function.

If a single pole IF filter is used, and if the frequency offset between the centre frequency of the band and the PLL lock frequency is $\Delta = 0$, then

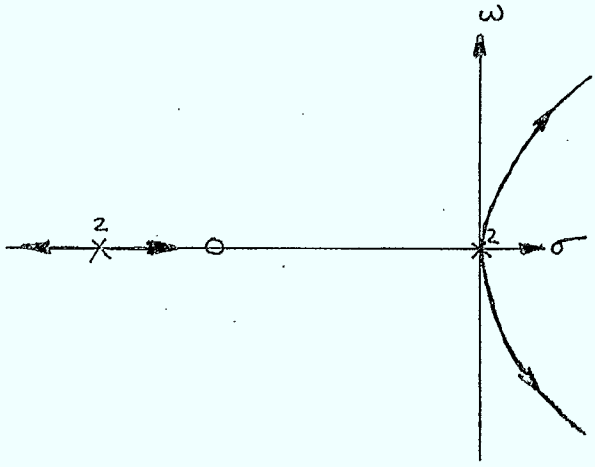


shows the poles and zeros of the open loop low pass equivalent. The resulting root locus diagram is



The design complication is obvious and the additional pole will seriously limit efforts to obtain a suitable system response with such a narrow IF bandwidth. If $\Delta \neq 0$, the process is yet more complicated and system response itself will be dependent on Δ.

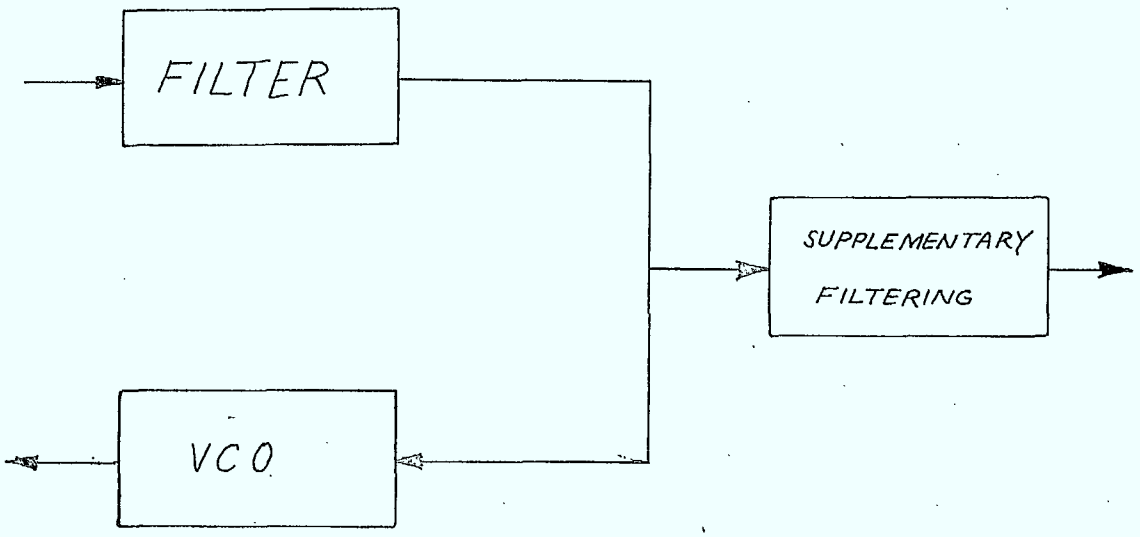
A further complication arises when yet more poles are introduced in that the system way be only conditionally stable or even unstable. For example:



II.2.8 Measurement by FM Demodulation

A direct approach to measuring the VCO output frequency would be to measure its input voltage which could then be directly converted to a frequency reading. Unfortunately, as the PLL locks on phase, and the VCO input voltage is the derivative of this phase, the VCO input is noisy.

As noted in Blanchard, page 183, some improvement may be gained with supplementary filtering



with a transfer function

$$\frac{1}{1 + 2\zeta\left(\frac{s}{\omega_n}\right)}$$

This gives an output noise power

$$2.2 \left(\frac{C}{N_o}\right)^{-1} f_n^{\ 3}$$

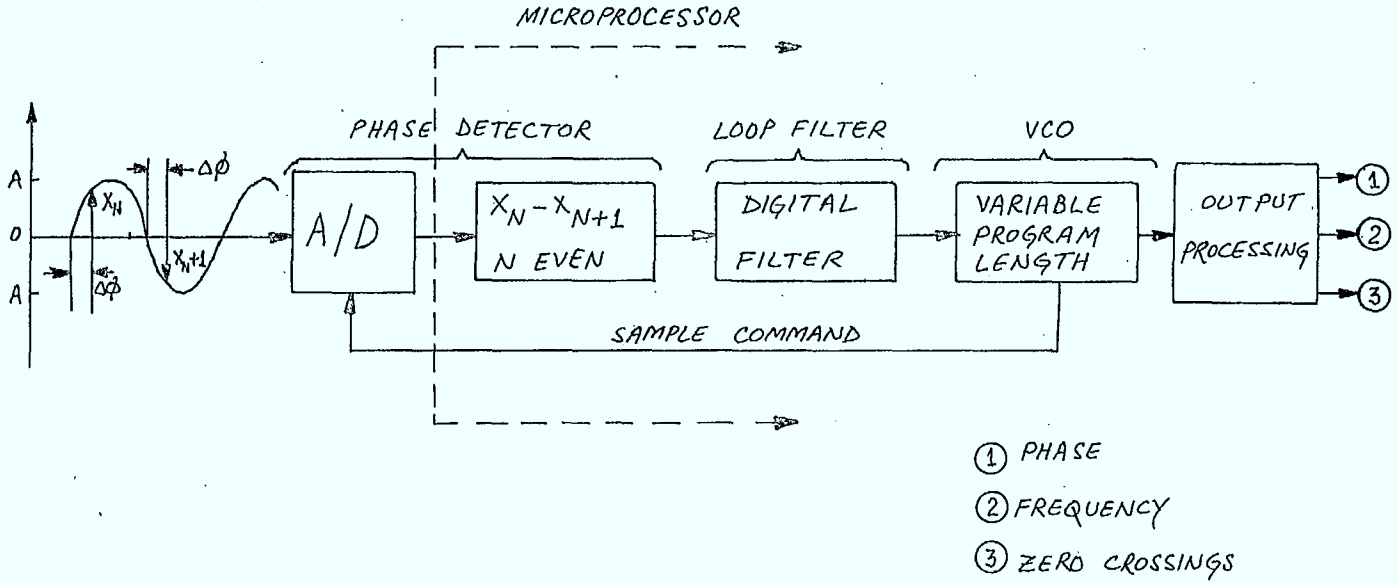
with unit amplitude corresponding to 1 Hertz, and $\zeta = 1$. The resulting noise level is

f_n Hz	Noise level (dB-Hz rms)
20	19.0
16	16.0
10	10.0
5	0.9
3	-5.7
1	-20.3
0.3	-36.7

and bandwidths of less than about 4 Hz would yield a suitably low noise level. It has been previously determined that bandwidths greater than 2 Hz are satisfactory for tracking 14 Hz/sec doppler, and so this approach is theoretically feasible.

II.2.9 All Digital PLL

The functional diagram of a digital phase locked loop is shown below (reference Bjerede,AES Newsletter, Sept. 1976). All functions except the A/D function are performed by the microprocessor. The approach is based on using the microprocessor itself as a variable oscillator the frequency of which is inversely proportional to the total number of program steps in a program cycle. The phase detector function is obtained by interrogating the A/D converter close to the zero-crossings of the periodic input waveform. For a sinusoidal input the phase error is then proportional to the difference between the samples taken at the positive-going and negative going zero-crossings.



ALL DIGITAL PHASE LOCK LOOP

A phase difference of $\Delta\phi$ radians is assumed to exist between the sampling pulse and the zero-crossing. The difference $X_N - X_{N+1}$ equals:

$$X_N - X_{N+1} = A \sin \Delta\phi - A \sin (-\Delta\phi) = 2A \sin \Delta\phi$$

and for small phase differences:

$$X_N - X_{N+1} \simeq 2A\Delta\phi$$

In other words the A/D, together with the block $X_N - X_{N+1}$ (N even), in Figure 1 is a phase detector. Furthermore because of the subtractor, $X_N - X_{N+1}$, this phase detector eliminates the effect of the dc component and even harmonics in the input samples and reduces the effect of low frequency noise.

Since the microprocessor program is synchronized to the input waveform, each point in the program corresponds to a particular value of the instantaneous phase.

Additive noise on the incoming samples will cause a phase error

$$\Delta\phi = \arcsin (X_N - X_{N+1})/2A$$

$\Delta\phi$ = phase error in radians

A = ELT amplitude

Assuming the additive noise n(t) to be white at an rms value of n_o and the ensemble average $(X_N \cdot X_{N+1}) = 0$, we have

$$\Delta\phi = \arcsin [n(NT) \cdot n[(n + 1) T]/2A$$

It follows that the standard deviation of the phase is

$$\sigma(\phi) = \arcsin \frac{n_o}{\sqrt{2A}}$$

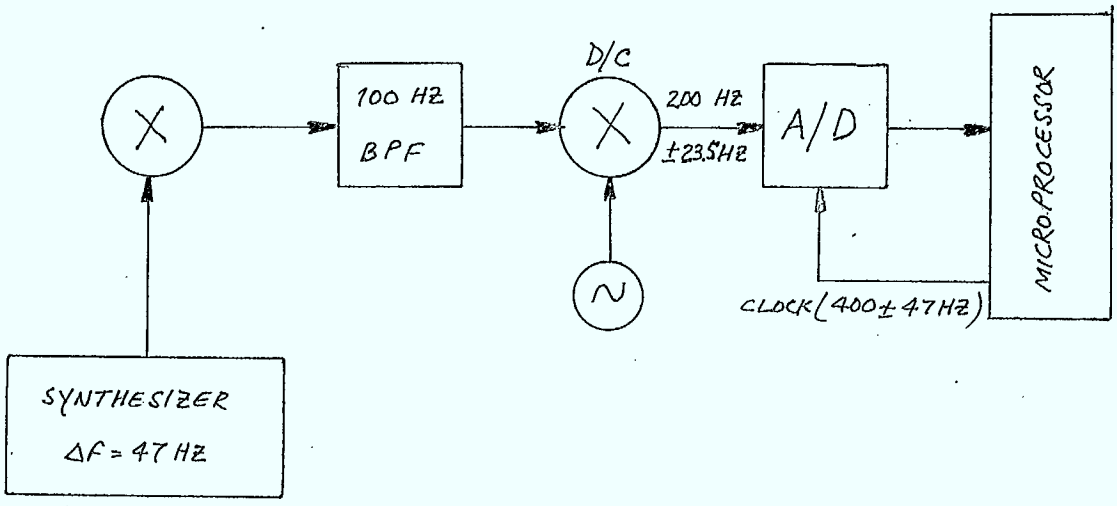
$$\simeq (2 \text{ SNR})^{-1/2} \quad \text{for SNR} >> 1,$$

i.e, equivalent performance of the analog phase detector.

The degrading effects of quantization and finite word length processing can be predicted using the results of Appendix B; however, these can be made arbitrarily small.

The effectiveness of such a digital PLL to track and measure the frequency of a sinusoid in the sub - kHz range has been demonstrated. The technique is therefore feasible in the Sarsat receiver providing a coarse stepper/filter/down-convertor is employed to restrict the range of the DPLL, and perform the coarse frequency estimate. The DPLL could also be used to detect the presence of ELT's within each step, with bandwidth switching of the loop digital filter performed following detection as before.

The reduction in signal processing hardware realized with the all digital PLL using a microprocessor does not provide a great cost advantage, and is probably more than offset by the complexity of software development and timing and interfacing requirements between the hardware and computer elements. The real advantage of closing the tracking loop through the microprocessor is the flexibility of control that can be exercised over the receiver to detect, acquire, track, and measure the frequency of up to 8 ELT's. As indicated in the following diagram, the computer selects the coarse synthesizer setting and provides the sampling clock to the low frequency A/D. Given this limited control, the job of the hardware is simply to generate and input digitized waveform samples to the computer, which in turn times the sampling (i.e. tracks the ELT) and estimates the frequency. However, as will be seen in Section II.3 a great deal of control flexibility can be obtained rather simply without resorting to this type of scheme.



II.3 Receiver Configurations and Performance Evaluation

II.3.1 Summary of Results to Date

The accompanying Table 1 summarizes the key results of the study to this point, and indicates viable signal processing techniques which theoretically can meet the Sarsat system requirements. Block diagrams of the corresponding receiver combinations are given in Figures 7-11, and are described below.

II.3.1.1 Receiver Types A and B

As indicated at the conclusion of Part I of the study, two distinctly different approaches to specifying the Sarsat receiver are possible. The first, labelled Type A, follows a simple repetitive operational sequence of sweep or step, detect, measure, resume sweep or step, and employs $N \geq 2$ identical devices spaced 12/N kHz apart, synchronized, and each taking about 10 N seconds to cover the band and perform frequency measurements. The essence of the Type A approach is that once an ELT is measured, it is of no further interest till 10 seconds later, at which time it must be redetected and re-measured. The sorting of measured frequencies into logical ELT records is performed exclusively by software. New ELT's are detected within 10 seconds of their first appearance.

TABLE 1

OPERATING MODE.	NUMBER OF DEVICES.	OPERATIONAL TECHNIQUE	DETECTION.	ACQUISITION	TRACKING	MEASUREMENT	TIME BETWEEN MEASURE-MENTS	REACQUISITION FOLLOWING LOSS OF LOCK.
A SEARCH, DETECT, STOP MEASURE, RESUME SEARCH.	2 IDENTICAL DEVICES OPERATED IDENTI--CALLY.	TWO PLL's SWEPT (BY HETERODYNING) OR STEPPED IN 47 HZ STEPS BY FREQ. CONVERSION USING PROG--RAMMABLE SYNTHESIZER. DEVICES STAGGERED 6 KHZ APART, SYNCHRONIZED AND EACH TAKING 20 SECS TO SWEEP BAND. (ELT INITIALLY DETECTED WITHIN 10 SECS NOMINALLY.)	COHERENT (USING REFERENCE PHASE FROM VCO OUTPUT) MISDETEC--TION PROBABILITY FOR CONTINUOUS ELT's ≃ 0.	2ND ORDER PLL WITH COMPENSATED INTEGRATOR LOOP FILTER. NOMINAL PARAMETERS: PULL IN RANGE = ±25 HZ DAMPING RATIO = .7 NATURAL FREQ. = 16 HZ	LOOP FILTER NARROWED BY SWITCHING RESISTERS FOLLOWING INITIAL DETECTION. NOMINAL PARAMETERS OF MODIFIED LOOP: PULL IN RANGE = ±3.75 HZ DAMPING RATIO = .7 NATURAL FREQ. = 2.5 HZ	FIXED PERIOD 1/4 SEC. COUNTING OF RECTIFIED VCO O/P WITH START/STOP FROM COMPUTER. OR FREQ. MEASUREMENT READ DIGITALLY FROM PROGRAMMABLE SYNTHESIZER REPLACING VCO IN LOOP. (SEE II.3.1.3) OR DIRECT MEASUREMENT OF VCO I/P VOLTAGE (STEPPER ONLY.) ********** NOMINAL DYNAMIC RANGE OF FREQUENCY MEASUR--ING DEVICE = { 100 HZ FOR STEPPED SEARCHER 12 KHZ FOR SWEPT SEARCHER	10-14 SECS.	TRACKING NOT REQUIRED. (ELT REDETECTED ON NEXT PASS.)
MODIFIED A SEARCH AND LOG, VISIT AND MEASURE IN SEQUENCE.	2 DEVICES 1 OPERATED AS SEARCHER/DETECTOR OTHER AS DETECTOR/ MEASUREMENT TAKER.	ONE PLL STEPPED ACROSS 12 KHZ. LOCATION OF ELT RECORDED AND TRACKED BY SOFTWARE (ELT INITIALLY DETECTED WITHIN 20 SEC. NOMINALLY) AND VISITED BY OTHER DEVICE FOR MEASUREMENT.					10 SECS.	TRACKING NOT REQUIRED. (ELT REDETECTED ON NEXT PASS.)
B SEARCH, DETECT, STOP TRACK AND MEASURE AS REQUIRED, RESUME SEARCH USING IDLE SERVICE	8 IDENTICAL DEVICES 1 OPERATED AS SEARCHER, SOME TRACKING, THE REST IDLE.	ONE PLL SWEPT OR STEPPED ACROSS 12 KHZ (ELT INITIALLY DETECTED WITHIN 20 SEC. NOMINALLY) AND ASSIGNED TO TRACK FIRST NEW ELT ENCOUNTERED.					10 SECS.	UPON LOSS OF LOCK OPEN LOOP FILTER AND REAQUIRE OR ADD a+bt VOLTAGE CHARACTERISTIC TO VCO I/P WHERE b IS EXTRA--POLATED INTERMEASURE--MENT RATE OF CHANGE OF ELT FREQ. AND a REPRESENTS STEP CHANGE (TO COMPENSATE COARSE FREQ. CHANGE FROM SYNTHESIZER - REQUIRED IN STEP TRACK MODE ONLY.) IF LOCK REAQUIRED WITHIN A SPECIFIED TIME, REMOVE SWEEP.
COMMENTS	TYBE B OPERATION CAN BE COMPLETELY DEMONS--TRATED USING ONLY 2 DEVICES. IDENTICAL DEVICES DESIRED FROM FLEXIBILITY /RELIABILITY STAND--POINT.	IN STEPPED MODE, VCO O/P FREQUENCY DRIFT MUST BE ZEROED ON EACH STEP TO ENSURE SATISFACTORY PULL IN. SIMILAR REQUIREMENT IN SWEPT MODE.			VCO MAY BE REPLACED WITH DIGITALLY CONTROLLED FINE STEPS (1HZ) SYNTHESIZER TO PERMIT DIRECT FREQUENCY MEASUREMENT.	SATISFACTORY MEASURE--MENT OF PULSED ELT's MAY BE OBTAINED BY CLAMPING FREQUENCY UPON LOSS OF LOCK AND AND (IF NECESSARY) POST-COMPENSATING MEASUREMENT BY SOFTWARE.		

A modified Type A receiver employs 2 stepped (possibly identical) devices, one used for detection of new ELT's and the other to measure previously detected ELT's. This nearly doubles the time required to initially detect the occurence of an ELT, but ensures that 2 devices can easily meet the 10 second between measurement specification (one which is very tight in the previous case with N = 2). The measuring device is programmed to consecutively step to and measure up to 8 ELT's in the band. The locating of an ELT to within one, or at worst two, coarse steps can be performed in software by extrapolating previous frequency measurements. Thus, while there is only one measuring device, it is not burdened with the necessity of stepping through the entire band and waiting for possible ELT detection on each step, and therefore has nearly 1.25 seconds to acquire and perform a frequency measurement. Meanwhile, the second searching device is continuously stepping across the entire band and logging the appearance of new (and old) ELT's. This second Type A scheme is obviously more complicated from a logical control standpoint, and implies that integer multiples of the fundamental step size must be accomodated by the control interface.

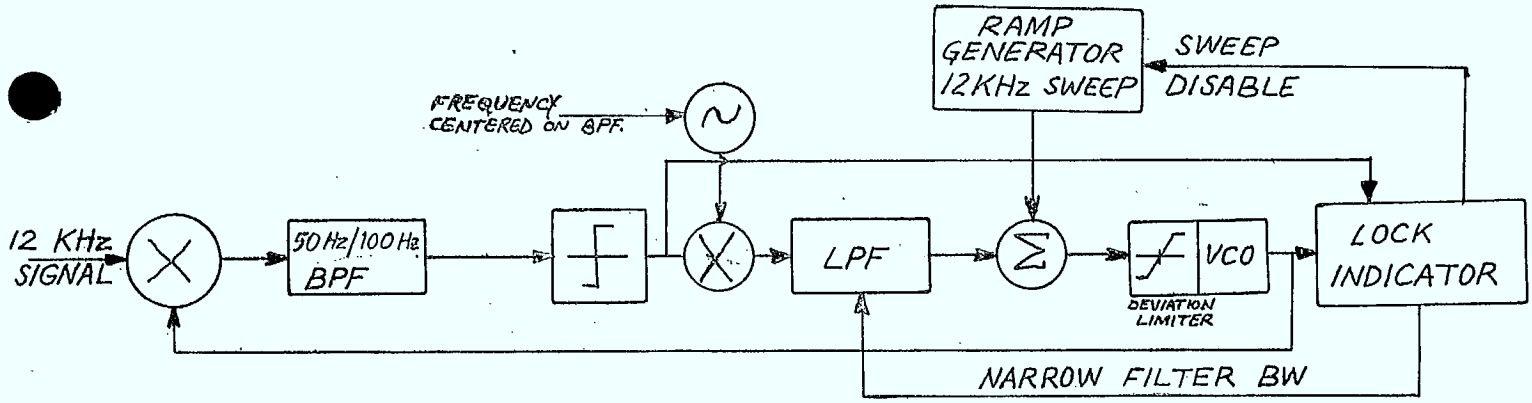
The Type B receiver operates on the principle that once an ELT is detected, it is tracked by the reduced bandwidth PLL as long as possible. This permits ELT frequency measurements to be obtained under more severe mutual ELT interference or noise conditions (following initial detection) than possible with the Type A scheme.

Eight identical devices each capable of searching or tracking are required - one will be swept till it detects a new ELT, and then is engaged to track it. Subsequently, an idle device resumes the search. With $N \leq 7$ ELT's currently detected, N devices will be assigned to track, 1 to search, and $8-N-1$ idle. In the limit when N=8, all devices are tracking and there is no searching.

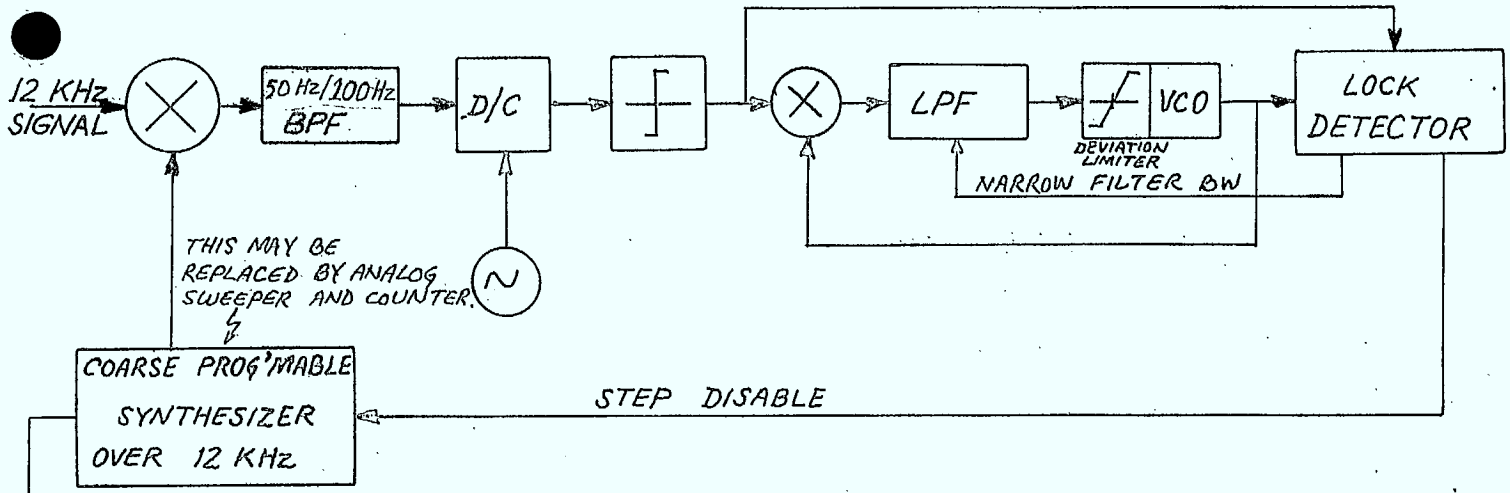
The Type A receiver can be designed to easily accomodate more than 8 ELT's, with a corresponding increase in the time between measurements of less than 10% for each ELT added. The Type B receiver cannot be made to "degrade" gracefully when the number of ELT's exceeds the number of devices, unless it can fall back to a Type A mode of operation. This suggests a third mode of operation which we might label as limited Type B/Type A; e.g. with 4 devices we can operate in Type B mode when 3 or less ELT's are present (i.e. most of the time), reverting to Type A operation when the 4'th ELT appears. This approach offers the advantages of a reduced number of devices, Type B performance most of the time, and a graceful degradation with increasing number of ELT's, with, of course, the disadvantage of increased complexity of control and software processing.

II.3.1.2 Searching and Detecting

As indicated in Figure 7, two approaches are available for searching the 12 kHz band for ELT's:

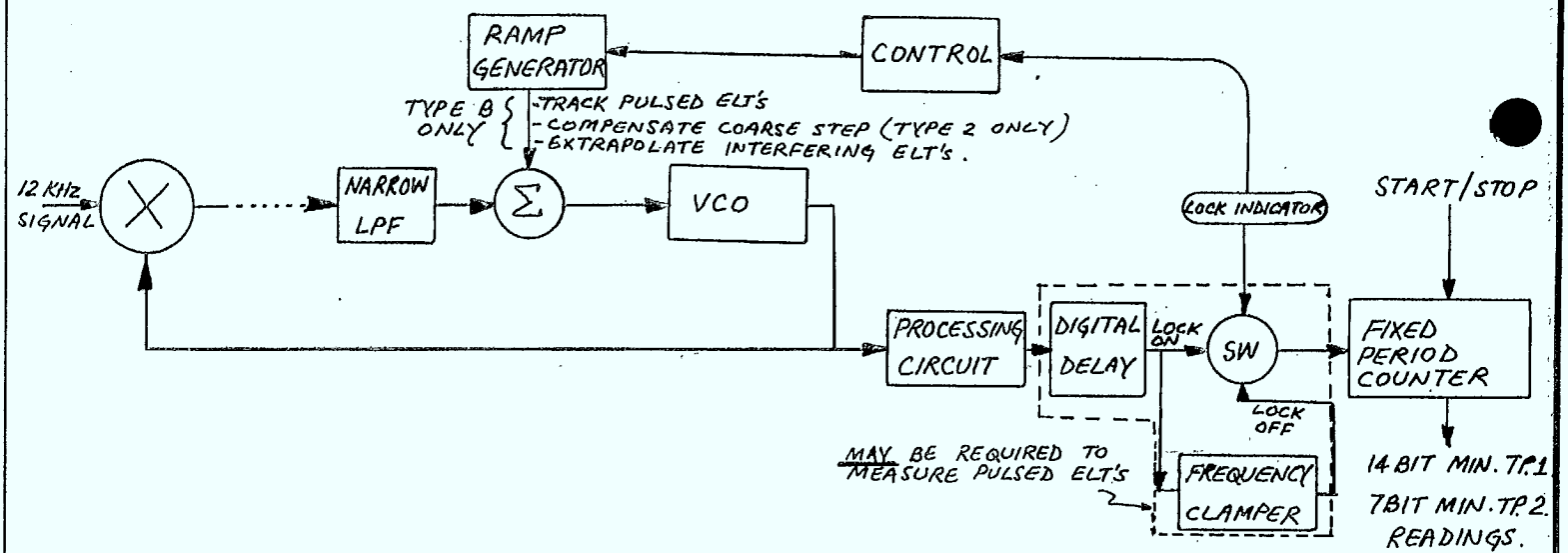


① SIGNAL HETERODYNED OVER FULL 12 KHz BAND.

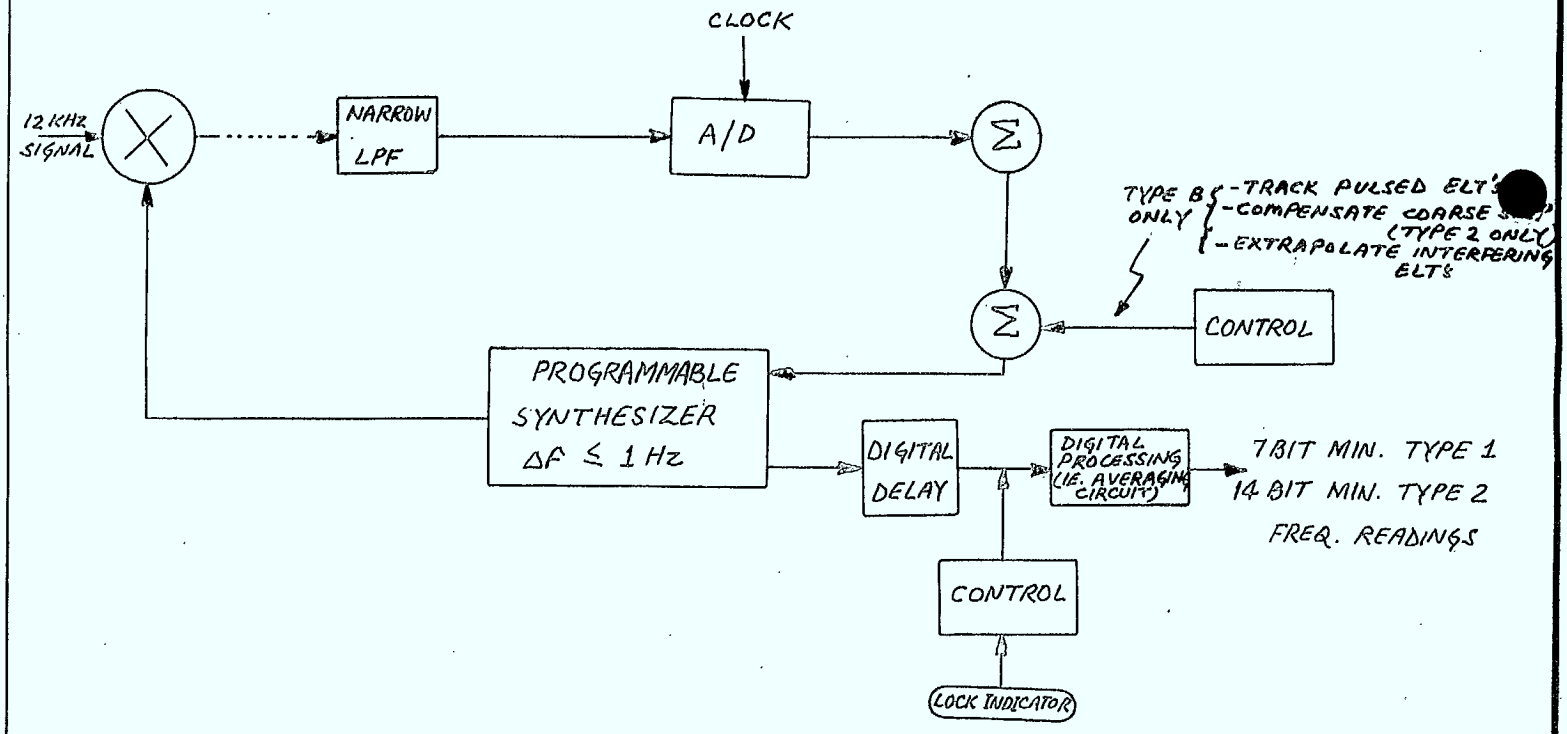


② SIGNAL STEPPED INTO 100 Hz FILTER / PLL.

	APP	TOLERANCES; .XX ± .XXX ± FRACT ± ANGLE ±	SCALE
NOVEMBER 8, 1976	DATE	MAT'L	MILLER COMMUNICATIONS SYSTEMS LIMITED KANATA - ONTARIO - CANADA
	C.O. No.	FINISH	FIGURE 7 SEARCH AND DETECT.
	REV	DRN R. MISRA; DES; CH'D; ENG	PART/DWG NO SAR - MCS - 007
			SHT - OF - REV - 0



(I) COUNTER MUST OPERATE OVER 12 KHZ (TYPE 1) OR 100 Hz (TYPE 2) RANGE



(II) SYNTHESIZER MUST OPERATE OVER 12 KHz (TYPE 1) OR 100 Hz (TYPE 2) RANGE.

	APP	TOLERANCES: .XX ± .XXX ± FRACT ± ANGLE ±	SCALE
NOVEMBER 8, 1976.	DATE	MAT'L	MILLER COMMUNICATIONS SYSTEMS LIMITED KANATA - ONTARIO - CANADA
	C.O. No.	FINISH	FIGURE 8 TRACK AND FREQUENCY MEASUREMENT.
		DRN R. MISRA.	PART/DWG NO SAR-MCS-008
	REV	DES / CH'D / ENG	SHT- OF - REV- 0

Type 1 - heterodyne sweep PLL over 12 kHz

Type 2 - step incoming 12 kHz signal into limited range PLL.

As indicated previously, the heterodyne sweeper has the following disadvantages in terms of performance:

- reduced loop stability due to presence of 100 Hz filter within loop (see II.2.7)

- two orders of magnitude greater dynamic range required for VCO and corresponding frequency measuring device

- other ELT's and noise 41 dB above the desired ELT present at the heterodyne mixer input implies that it must be linear over a very wide dynamic range (similar requirement for synthesizer controlled down converter).

- requirement to disengage sweep quickly following lock detection.

The stepper searcher uses a synthesizer with a 12 kHz range having frequency steps of less than 100 Hz with a short term stability of much better than 1 Hz (the first component of the frequency measurement) and has the following disadvantages:

- lock up time of stepping synthesizer adds to overhead of searcher (this can be minimized if necessary by switching between 2 synthesizers, with one locking to the next step)

- increased cost of synthesizer unit vs ramp generator (offset to some extent by reduced IF frequency into PLL and limited dynamic range of phase detector and frequency measuring device),

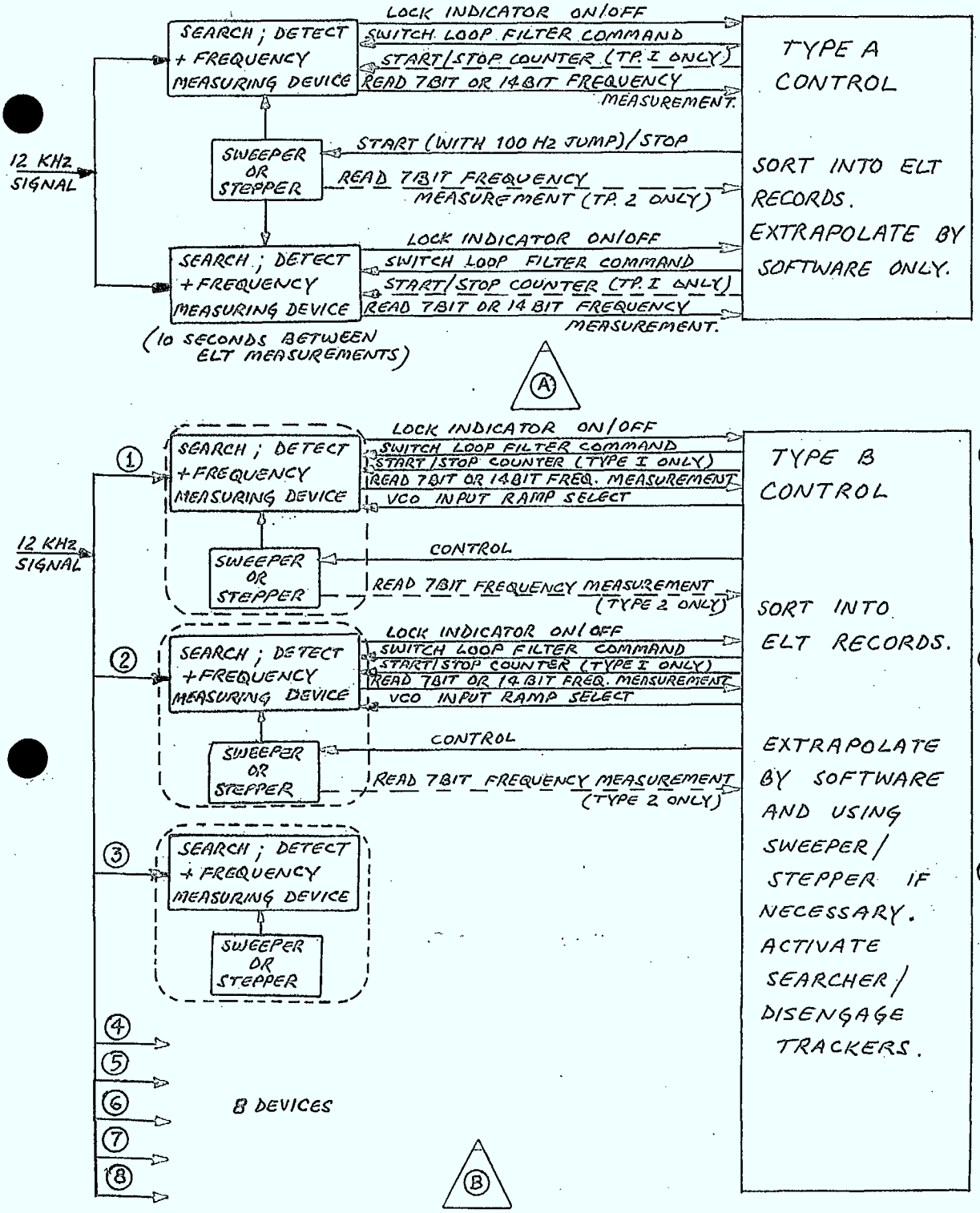
- difficulty of being used to track ELT's (Type B only - see II.3.1.3)

An additional advantage of the programmable synthesizer/stepped searcher is the variety of ways in which it can be controlled by the computer; e.g. stepping rate can easily be varied by software, steps in which ELT's are currently being tracked can be skipped (Type B only), stepping devices in the search mode are easily synchronized to maintain a fixed separation (normal Type A), jumping in sequence to steps in which ELT's are known to reside (modified Type A) is possible, etc.

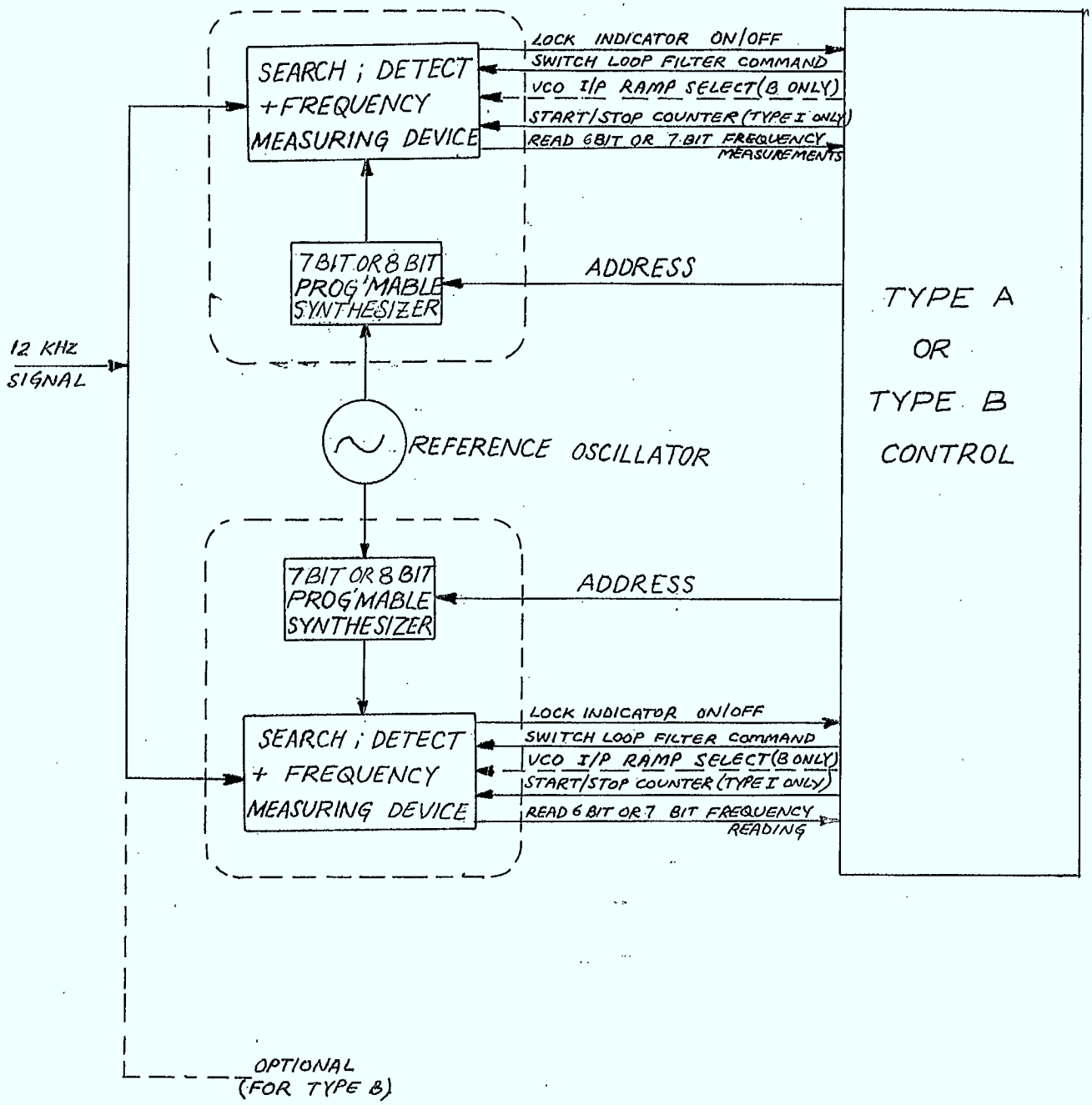
At this point in time, there is some uncertainty as to what parameters and control algorithms are optimum, and these may only be determined well into the implementation and field testing phases; the intrinsic flexibility of control that can be obtained with little penalty in hardware is what really clinches the argument for the stepper vs the heterodyned sweeper in the proposed receiver configuration (see Figure 10).

II.3.1.3 Measurement and Tracking

It has been determined that to acquire an ELT with sufficient S/N

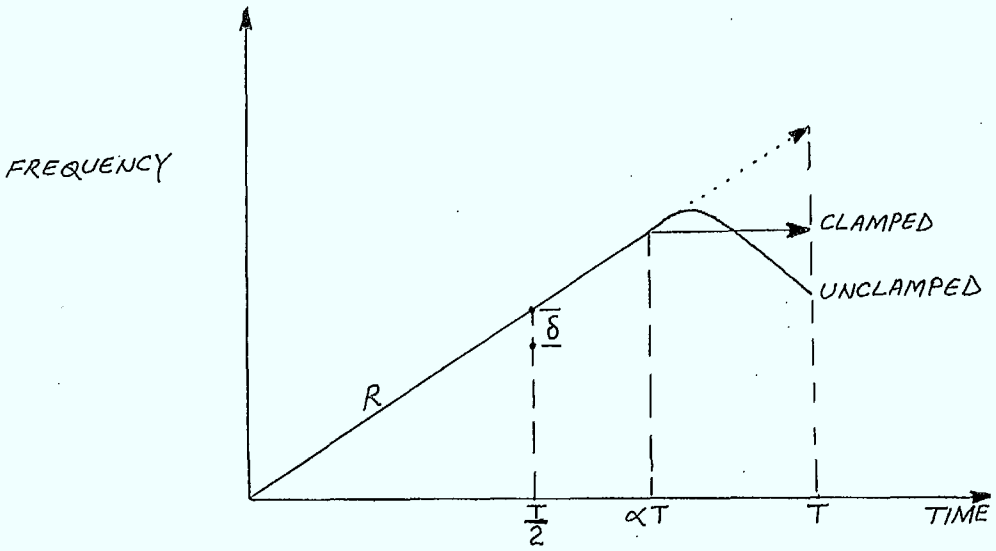


	APP	TOLERANCES; .XX ± .XXX ± FRACT ± ANGLE ±	SCALE	MILLER COMMUNICATIONS SYSTEMS LIMITED KANATA - ONTARIO - CANADA
NOVEMBER 8, 1976.	DATE	MAT'L		FIGURE 9
	C.O. No.	FINISH		(A) TYPE A RECEIVER (B) TYPE B RECEIVER
		DRN R. MISRA.		PART/DWG NO SAR-MCS-009
	REV.	DES / CH'D / ENG		SHT- OF- REV- 0



NOVEMBER 8, 1976.	APP / DATE / C.O. No. / REV	TOLERANCES; .XX ± .XXX ± FRACT ± ANGLE ±	SCALE
		MAT'L	MILLER COMMUNICATIONS SYSTEMS LIMITED KANATA – ONTARIO – CANADA
		FINISH	FIGURE 10 TYPE AB RECEIVER
		DRN R. MISRA. DES CH'D ENG	PART/DWG NO SAR-MCS-010
			SHT- OF- REV- 0

to perform an accurate frequency measurement, the PLL loop filter bandwidth must be narrowed following detection. At this point the PLL will be able to track an ELT in the 0 - 14 Hz/sec range and provide an S/N of about 10 dB at the VCO input for a C/N_o = 26 dB-Hz. Three schemes are possible for determining the frequency of the ELT: fixed period counting of the VCO output, interrogation of a digitally controlled synthesizer in place of the VCO (hybrid scheme), and direct measurement of the VCO input voltage (possible with Type 2 receiver only). As indicated in Figure 8 the VCO output signal may be measured by a fixed period counter started and stopped by computer command. With full wave rectification or its equivalent, the frequency can be measured to an rms accuracy of 1 Hz in 1/4 second as long as the loop remains in lock. If the loop becomes unlocked during frequency measurement, the VCO input voltage will drop and become subject to a slowly increasing level of noise (see II.2.4). To ensure satisfactory completion of measurement of pulsed ELT's, it may therefore be necessary to clamp the frequency currently being measured upon loss of lock; since there will be considerable delay between the actual loss of lock and its detection, a digital delay of the counter input is required to ensure that it can be clamped to the frequency present prior to loss of lock. The following diagram depicts the two sources of frequency measurement error resulting from a loss of lock $0 < \alpha \leq 1$ into a measurement period T, assuming a rate of change of doppler of R Hz/sec.



δ = measurement error with clamping

= instantaneous frequency at $t = \frac{T}{2}$ - average frequency with frequency clamped upon loss of lock

$\leq \frac{1}{2}(1-\alpha)^2 (14)(.25)$ Hz for T = .25 sec, $R \leq 14$ Hz/sec

ε_{rms} = additional rms error (due to noise) without clamping

$= (1-\alpha)(3.2 + 1.8((1-\alpha)T)^{\frac{1}{2}})$ (see II.2.4)

α	δ max (Hz) = max error with clamping	ε_{rms} (Hz) = additional error without clamping
.10	1.42	3.64
.25	0.98	2.98
.50	0.44	1.92
.75	0.11	0.91
1.00	0.00	0.00

These frequency measurement errors may be tolerable. If desired, the δ component could be largely removed in software by extrapolating a slope value from previous measurements. To do this the computer would have to know the moment of lock interrupt.

The advantage of the above scheme of measuring pulsed ELT's is that once a measurement is initiated (with lock indicator "on"), a "good" frequency measurement will be taken - i.e., there is only one sequence of measurement taking events. Even without frequency clamping or extrapolation, the degradation in measurement is less than 1 Hz rms for $\alpha > .75$. Taking this approach, pulsed ELT's have absolutely no impact on the receiver design, but are subject to 2 - 3 times the mean time to detect and rms measurement error associated with continuous ELT's.

Alternatively, successful measurement of a pulsed ELT during a complete "on" period is virtually assured over an interval of several seconds with non-interrupted repeated counting. The only exception to this is when the pulsed ELT cycle period ("off" plus "on" time) is very nearly an integer multiple of the measurement time (nominally .25 seconds). The following table indicates the probability of making a successful measurement versus time under the following assumptions

- minimum effective ELT on-time = 0.5 sec - PLL lock-up time assuming linear extrapolation
  $\simeq$ 0.45 sec.

- $0,5 \leq \frac{\text{ELT on-time}}{\text{ELT off time}} \leq 1,0$ uniformly distributed

- max. ELT off-time = 2,0 sec

- uninterrupted counting over N successive .25 second intervals

N	T	Likelihood of success after N tries (assuming lock indicator initially "on")
1	.25 sec	$\geq$.44
2	.50 sec	
3	.75 sec	
4	1.00 sec	$\geq$.74
5	1.25 sec	
6	1.50 sec	
7	1.75 sec	
8	2.00 sec	$\geq$.89

The operational sequence for this measurement technique is again rather simple - commence measurement taking if lock indicator "on" and continue till successful measurement is taken. It is of no interest in the Type A receiver, however, not only because of the unacceptable measurement overhead time introduced, but also because it imposes the need to track the ELT by extrapolation sweeping during the "off" periods.

The stability of the clock used to start and stop the fixed period counter must satisfy the following relation:

$$\Delta T = \text{time base accuracy over 1200 sec}$$
$$\ll 1 \text{ period of waveform being counted}$$
$$\approx \left(2f_{IF}\right)^{-1}$$

where f_{IF} is the VCO centre frequency and frequency doubling is assumed. Otherwise variations from the nominal value of T used to divide the number of cycles counted will contribute to measurement error*. For a 2 stepper (Type 2) system (see Figure 7) a reasonable lower bound for f_{IF} is 250 Hz, implying the absolute necessity that

$$\Delta T \ll 2 \text{ msec}$$

As indicated in Figure 8, an alternative scheme to counting the VCO output is to employ a digitally controlled programmable synthesizer in place of the VCO (continuously or during measurement period only). Assuming frequency steps $\Delta f < 1$ Hz, then instantaneous frequency can be read directly from the synthesizer or averaged over some time interval.

---

* Note that very long term variations are insignificant, as we are only interested in relative (i.e. measurement to measurement) accuracy over a satellite pass.

Phased locked loops are usually taken to be analog devices, but in fact can be realized also with digital hardware or with a hybrid mixture of analog and digital components. In the frequency range appropriate for the SARSAT system, analog implementations seem self-evident, but digital or hybrid loops were investigated in some detail in case some less obvious advantages were to be found in these approaches.

The potential advantage of the digital approach not only lies with the elimination of the fixed period counter, but also with the easy controllability of the loop as follows:

- the delay/frequency clamping scheme previously described is trivially realized by retaining memory of the synthesizer state at some previous instant

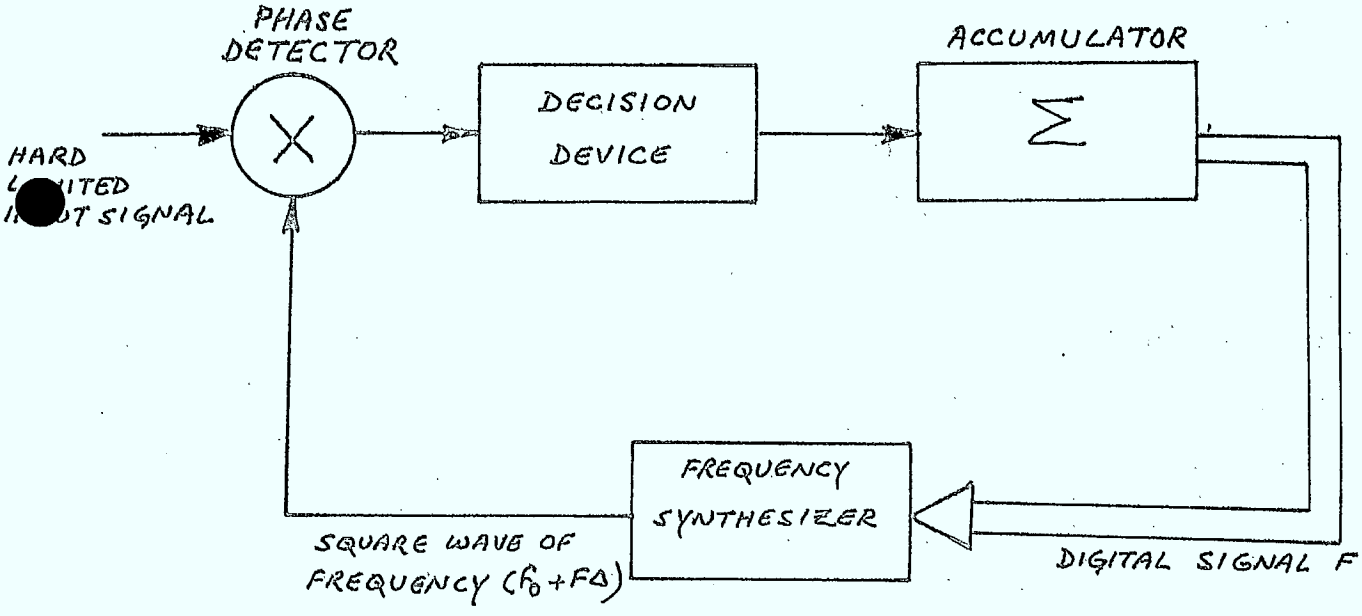
- variable slope sweeping in the search mode (Type 1 only) or tracking (i.e. extrapolation - Type B only); quantum stepping (to compensate coarse synthesizer stepping with Type B2 receiver - see subsequent discussion) can be realized without the problems of drift, gain variation etc. of corresponding analog circuits and with precision and dynamic range determined only by word length.

An obvious all-digital method is formed through direct digital simulation of an analog PLL. This could be realized by either hardware or software, but the most casual consideration of costs suggests

very strongly that this is not a viable approach.

A hybrid method in which computer software is a major element is possible, but the complexity associated with the multiple processing and complex control needed for the SARSAT receiver destroyed any potential this technique may have enjoyed.

Another approach based on hardware is described by the diagram:



Only the phase detector operates in an analog fashion and it is actually a hybrid device in which the incoming signal is gated by the square wave from the Frequency Synthesizer and the result is averaged

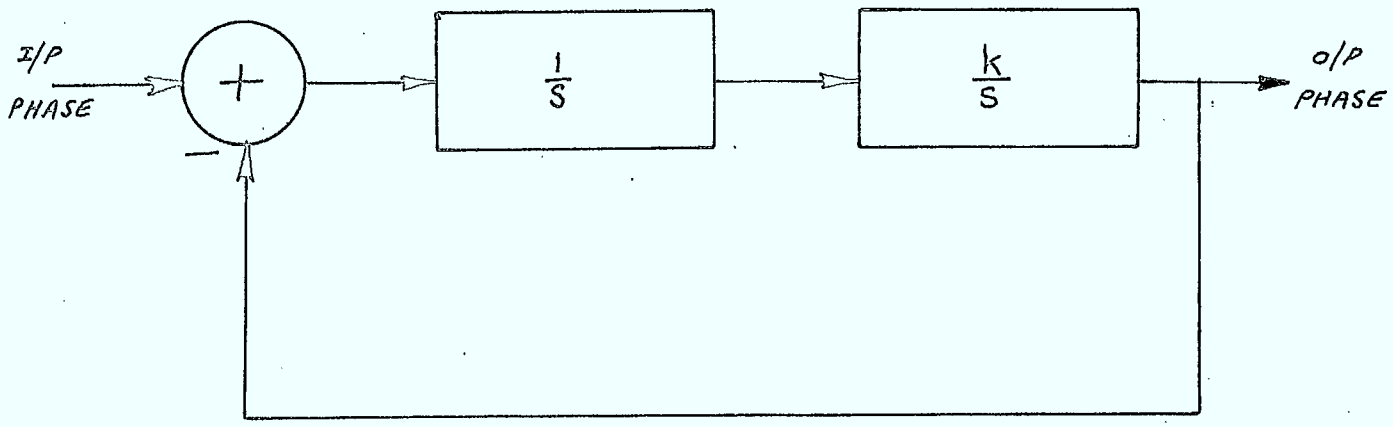
to give a measurement of phase difference over the range $-\pi$ to π. Based on this phase difference, the Decision Device increments or decrements the contents of the Accumulator whose output is a digital word determining the PLL's frequency. The square wave generated by the Frequency Synthesizer has frequency $(f_o + F\Delta)$ Hertz, and the synthesizer is actually a down-counting device which directly determines the period of the square wave rather than the frequency.

Such a frequency synthesizer has only a limited operating range but for a Type 2 (i.e. stepper) system with step size $\Delta = 1$ Hz, and F an integer with a range of ± 25, this is not a problem. For example if f_o is 10 kHz, obtained by dividing a 50 MHz clock by 5000, then the error in step size is less than 1% across the operating range.

Detailed study of the behaviour of this system determined that it is able to lock to both fixed sinusoidal inputs and sinusoids whose frequency varies linearly with time. The resulting phase error is not fixed but oscillates, usually in a somewhat random fashion, about a mean value. Similarly the frequency reading F is not fixed but varies slightly with time. Two approaches to obtaining a suitable reading were found to be possible: if $\Delta = 1$, and the system were designed so that the "bistable" variation in F were limited to ± 1, any reading of F would suffice; alternatively, this restriction on Δ and F could be relaxed if a suitable measurement time T were chosen over which the reading of F were averaged. In all, the SARSAT specifications can be achieved by use of a simple hybrid PLL of this type.

Unfortunately, it was also found that the system suffers from some problems of instability and large sustained oscillations could build up. In the tracking mode these can be controlled by designing an appropriate Decision Device, which in the most basic mode would simply be a hard limiter. Use of two thresholds, and a slightly complex method for modifying the input to the Accumulator when a threshold was exceeded, was sufficient. However, no reasonable method could be found to prevent excessive settling times when the loop was initially attempting to acquire lock. As a consequence, this interesting approach to the implementation of a primarily digital PLL was abandoned.

The essential problem can be identified in the analog version of this loop



which has a transfer function

$$\frac{\Phi_o}{\Phi_i}(s) = \frac{\frac{k}{s^2}}{1+\frac{k}{s^2}} = \frac{k}{s^2+k}$$

This is immediately seen to have poles at $\pm jk^{1/2}$ and so would have a highly unsatisfactory transient behaviour. (As indicated in Appendix B, the performance of the hybrid loop is not identical to its analog counterpart, due to sampling quantization, and arithmetic roundoff; however, these typically add noise to the system without affecting behaviour).

The third approach to measurement taking is direct linear A/D conversion of the VCO input. Due to a stringent frequency vs voltage linearity and stability requirement over the measurement range, this scheme is only feasible for the stepped receiver. For 47 Hz steps, the frequency must be measured to an accuracy of 1 Hz over say 64 Hz, implying at least a 6 bit A/D convertor.

This approach has been demonstrated to be theoretically feasible (see II.2.8); its practicability is largely determined by the linearity and stability (over 1200 seconds) obtainable for the PLL. Slight non-linearities and time variations in the VCO frequency vs voltage response, loop gain etc. do not affect output frequency , and hence a counter measurement, but will alter slightly the demodulated FM signal from which the measurement is derived in this case.

The tracking capabilities of the 12 kHz heterodyned PLL (Type 1) and the coarse stepping / 50 Hz PLL (Type 2) devices are somewhat different, and favour the former. Basically, the Type 2 device can only track within the 50 Hz pass band of the input filter without resorting to coarse stepping. (Beyond this band, the carrier is attenuated by the filter skirts and loss of lock occurs).

The coarse step is much larger than the pull-in range of the tracking PLL, implying loss of ELT acquisition over an extended period unless:

- the PLL filter is widened and the ELT redetected in the next step

- a compensating coarse frequency step voltage is applied to the VCO input at the moment the synthesizer is stepped, and the stepping takes place prior to loss of ELT lock (since the bandwidth of the filter is considerably wider than a frequency step, extrapolation can be used to control the synthesizer to keep the ELT within this bandwidth)

- the synthesizer is programmed to slew between steps at the maximum tracking rate of the narrow band PLL and measurement taking does not take place during this transition period.

The heterodyned PLL doesn't encounter this difficulty as it is free to track over the full 12 kHz band presented at the phase detector input.

The impact of this tracking difficulty with the Type 2 stepping receiver is quite different in the Type A and Type B modes of operation. In Type A, tracking is only required over the .25 sec. measurement period, implying a maximum frequency excursion of about 4 Hz. Only in the case of marginal detection at the very edge of band could lock be broken due to further signal attenuation during the measurement. This event occurs with very low probability, and when it does, the ELT will simply be redetected and remeasured successfully on the next step. In conclusion, there is no disadvantage to the stepper for Type A operation.

In Type B operation, a narrow band tracking capability equivalent to that of the 12 kHz hetrodyned PLL can only be achieved with the added complication of adding compensating jump steps to the VCO input (such successive steps accumulate in voltage) or slewing the synthesizer at a rate of 14 Hz/sec (transition time between stable points = 3.4 secs.) Alternatively, the narrow band PLL is stepped ahead of the ELT and awaits its predicted arrival. (If only a coarse step from the synthesizer is used, this jumping ahead scheme offers little interference rejection advantages to the wider PLL bandwidth/redetect approach since ELT frequencies are moving in the same direction, and certainly increases the loss of acquisition time).

The "widen PLL filter bandwidth/redetect" approach has no impact on the hardware requirements of the stepper receiver, but clearly results in inferior performance to the heterodyned receiver because

an ELT cannot be successfully tracked to a 47 Hz synthesizer step currently occupied by another ELT. This eliminates much of the advantage of the Type B receiver, namely the ability to track and measure ELT's initially separated by more than 47 Hz to within the 3.25 Hz pull-in half bandwidth of the tracking PLL. .

Finally, it has been shown that to track pulsed ELT's with a maximum off-time of 2 seconds and a maximum doppler rate of 14 Hz/sec, either a programmed step (corresponding to the ELT frequency expected when it re-appears) or a programmed ramp voltage based on extrapolated frequency measurements must be applied to the VCO input, or else the filter is widened and the ELT redetected within the same step or the next one. In the latter case, there will obviously be less time to measure the pulsed ELT due to the wide band acquisition delay incurred at the beginning of each "on" period.

II.3.1.4 Recommended Type AB Receiver

Assuming selection of the appropriate search and detect plus frequency measuring device, Figure 10 illustrates how it is employed in either a Type A or Type B mode. Rather surprisingly, apart from the requirement for 8 rather than 2 devices, the Type B receiver hardware differs from that required for Type A operation only in the following respects:

1. Separate and independently controlled sweepers or steppers for each device.

2. External control of the VCO input voltage to track ELT's during out of lock periods (optional)

Of course, the software used to control the receiver hardware in the two cases is quite different.

Without a serious engineering or hardware cost penalty, it is therefore possible to devise a receiver which can be operated in the Type A, modified Type A, or limited Type B modes (see Table 1) with the appropriate control program loaded into the microprocessor.

Assuming a stepped synthesizer (Type 1) receiver, which has the previously discussed advantages over a swept receiver, Figure 10 illustrates the Type AB receiver configuration recommended for implementation. While Type B operation is limited by the presence of only two devices, its performance can be fully demonstrated. Furthermore, addressing and control sequences, as well as the Type B microprocessor program, can easily be devised to accomodate up to 8 devices, and therefore the proposed receiver is immediately expandable to full-fledged Type B operation.

The control input/output between the receiver hardware and the microprocessor are fully identified in Figure 10 and listed below (per device):

Input: i lock indicator on/off (interrupt)

ii frequency measurement (6 or 7 significant bits)

Output: i new address to synthesizer (7 or 8 bits), also commands loop filter capacitor discharge if device is in searching mode

ii switch loop filter command

iii start/stop counter

As described in Section II,3,2, rather simple I/O links can be used to control the two devices in any of the desired modes. Control algorithms are facilitated by the fact that all doppler frequency characteristics vary monotonically in the same direction with time. The searching device will therefore be stepped in the same direction as the ELT's are moving, ensuring that if an ELT is just lost on one step it will be detected on the next. Similarily, for tracking, there is no ambiguity as to which adjacent step a lost ELT has moved, and back stepping is not required.

The advantages of the proposed receiver configuration can be summarized as follows:

- simplicity of hardware and control interface

- Type A or Type B operation (with change only to software)

- duplication of identical independently controlled devices eases engineering development, fabrication and testing

- easy expandibility up to 8 devices

- flexibility maximizes likelihood of success (both operating mode and critical timing parameters are under the control of the computer and can be varied)

- reliability (in an operating system, graceful fallback easily accomodated as devices are taken out of action).

II.3.2 Microprocessor Control

Many of the receiver functions are controlled by the computer subsystem or monitored by it for control purposes. Specifically, for the recommended Type AB receiver these items include control of the synthesizer, the counter, the loop filter and the VCO input ramp (Type B only); and the monitoring of the lock indicator.

As well as the control functions which interface directly between the receiver and the computer system, the computer system must be capable of keeping track of absolute time of day, storing the measurements and associating a time with them, sorting measurements according to BLT's, keeping track of devices, and additionally in the Type B receiver activating and disengaging devices and periodically polling devices that are tracking for measurements.

The microprocessor system selected was a PDP 11/03 (LSI 11) with two 16-bit parallel interface units, 8K words of memory, dual floppy disks, a dec-writer and a real time operating system. This is a versatile system that satisfies the requirements at comparative cost as well as facilitating the development of the software to perform the required tasks. The expected delivery date for the PDP 11/03 system is January 20, 1977.

Figure 11 shows the distribution of the control functions on the two PDP 11 interfaces for the recommended Type AB receiver. They

are organized in such a way as to accomodate up to 8 devices in parallel.

Figures 12 and 13 illustrate a typical control sequence for the Type A receiver system. In general the synthesizer is stepped by 47 Hz every 66.6 ms unless one of the two devices attain lock. This event results in the computer changing the loop filter from a wide band to a narrow band filter, whereupon the lock indicator should indicate that lock has been maintained or reacquired within a short period of time. If it does not relock the initial acquisition is treated as a false alarm and searching continues. On relock the counter is started and then stopped after a fixed interval period of 250 ms. The computer reads the count, converts it to a frequency measurement and associates a time with it. The counter is then reset, the filter is switched back to wide band and the synthesizer is stepped. The measurement is sorted into the correct ELT record in core and these records are periodically stored on diskette. It is possible that both devices encounter ELT's at the same time, in which case two measurements are taken in parallel.

Figures 14 and 15 illustrate a typical control sequence for the Type B receiver system. The device is transferred from an idle state (synthesizer not stepping and device not tracking) to an active searching state (synthesizer stepping). In this state the synthesizer is stepped every 66.6 ms until lock is achieved. As in the case of the Type A device lock must be reattained in order for the

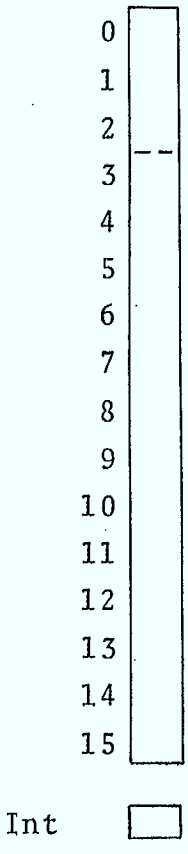
measurement to be made. However, the device is left to continue tracking the ELT, making measurements at regular intervals and another device is activated to continue the search for other ELT's. A device that is tracking an ELT is deactivated if it starts measuring the same ELT as another device or if it loses lock for an extended period of time. If lock is lost for a tracking device the VCO input ramp may be selected to assist in reacquiring lock (this option is accommodated in the data field but will not initially be available in hardware.)

The preceeding summaries were intended to give an indication of the software processing involved. The software for the microprocessor will be assembler programs that are expected to occupy approximately 2K of memory for the Type A receiver and an additional .5 to 1K for the Type B receiver. The resident operating system will occupy about 1.5K leaving up to 4K free. An indication of timing and delays between control functions is given in Figures 13 and 15. Absolute Time of day must be provided to the software at the time the software is activated.

FIGURE 11

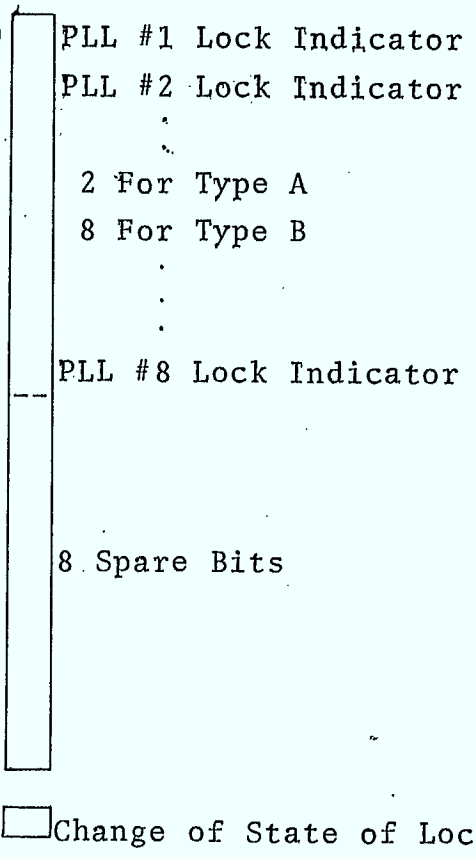
PDP 11/03 INTERFACES (DRV11)

DATA OUT OF PDP 11



Int

DATA INTO PDP 11



Int Change of State of Lock Indicator

Int

Int Clock Interrupt

TYPE A DEVICE

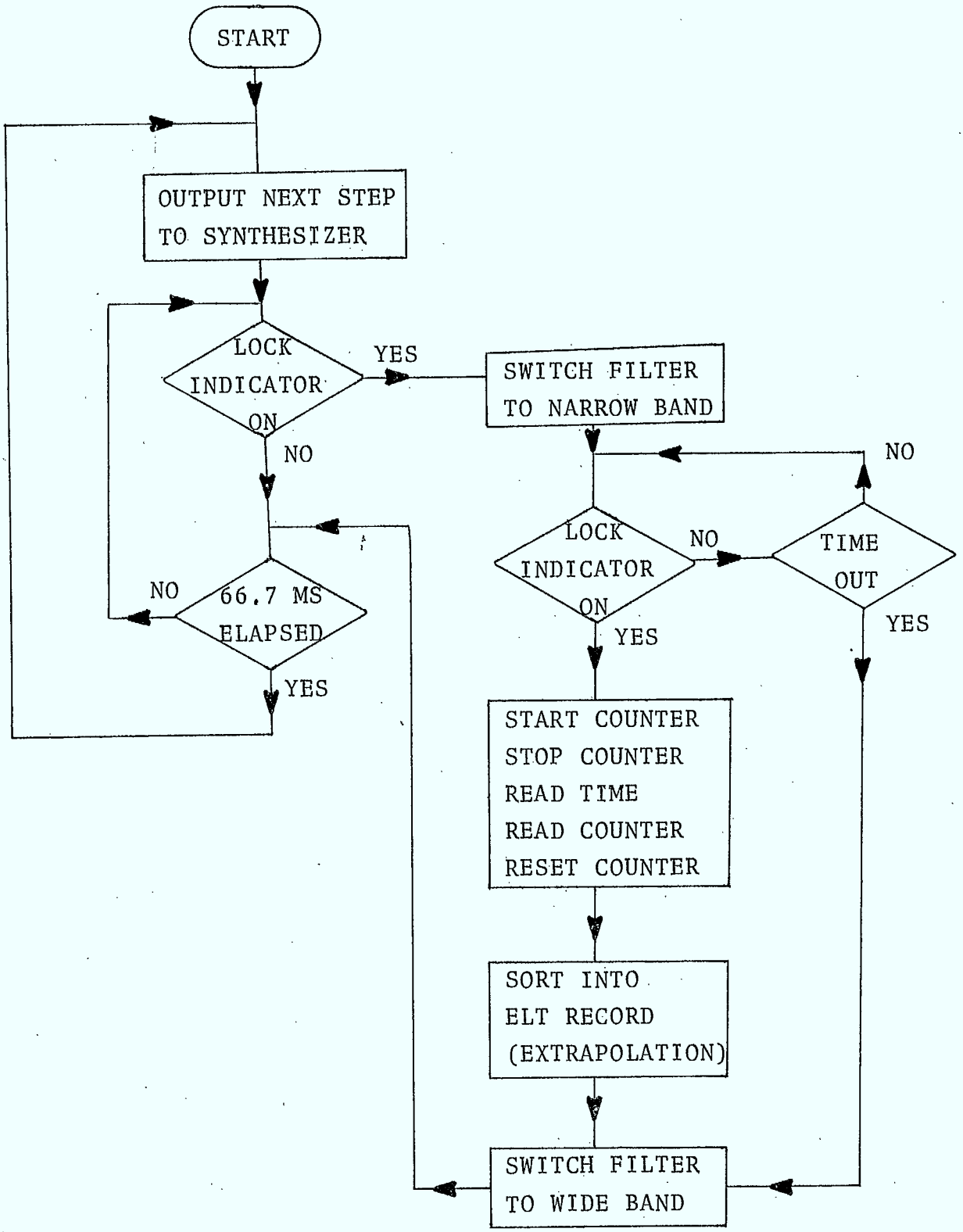


FIGURE 12

TYPE A DEVICE TYPICAL SEQUENCE

TIME RELATIVE TO PREVIOUS STEP (NOMINAL)	EVENT	#
0 - 20μs	Synthesizer Output Stepped	1
0 - 66 ms (-50μs)	Lock Indicator On Or Go To 1	2
<200μs	Switch Filter To Narrow Band	3
0 - 33.3 ms	Lock Indicator On Or Go To 1	4
0 - 16.6 ms	Start Counter	5
250 ms ± 9μs ± Clock	Stop Counter	6
<200μs	Read Time Read Counter Reset Counter	7
<16.6 ms	Switch Filter To Wide Band	8
	Go to 1	9

FIGURE 13

TYPE B DEVICE

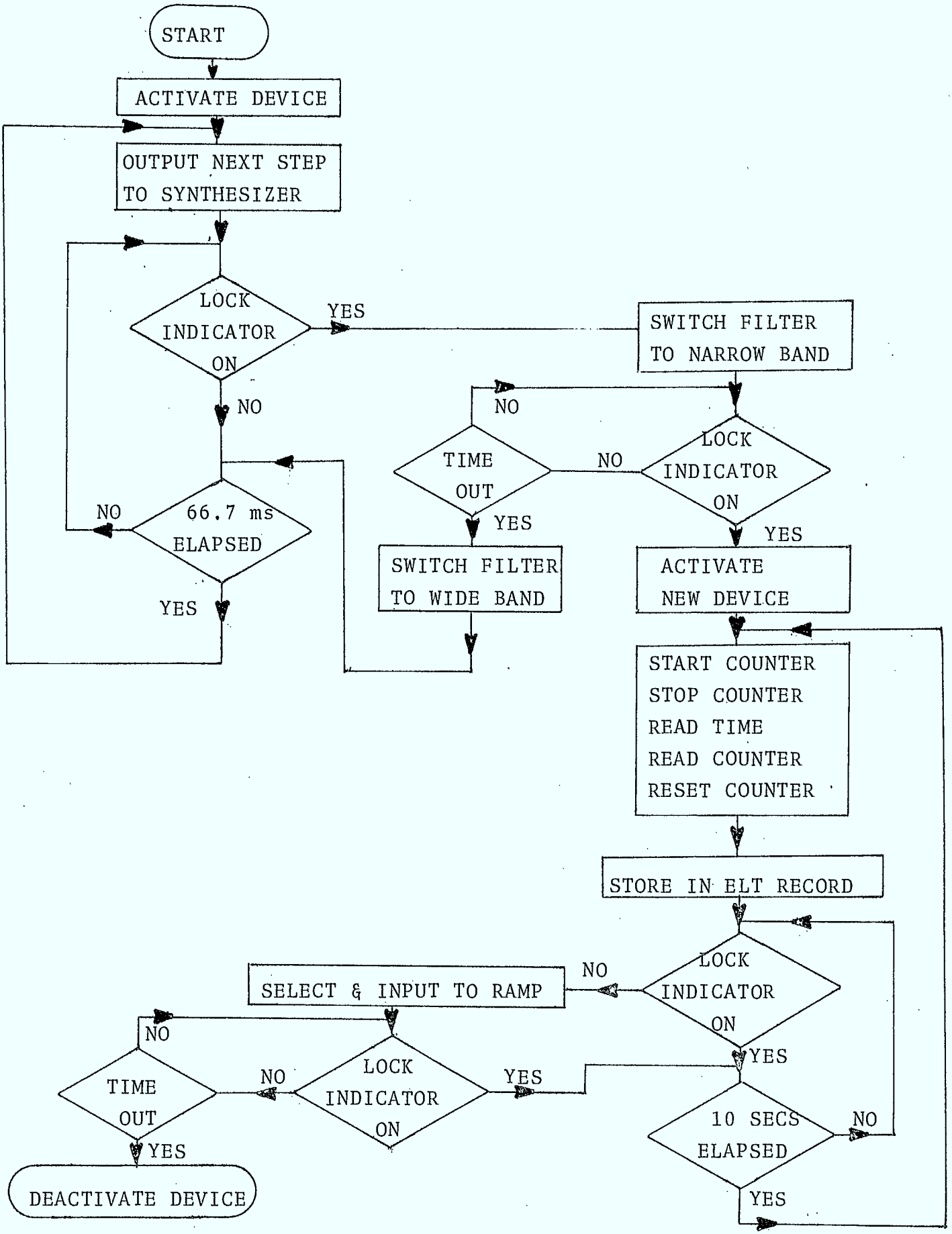


FIGURE 14

TYPE B DEVICE TYPICAL SEQUENCE

TIME RELATIVE TO PREVIOUS STEP (NOMINAL)	EVENT	#
0 - 20µs	Synthesizer Output Stepped	1
0 ≈ 66,7 ms (≈50µs)	Lock Indicator ON Or Go To 1	2
<200µs	Switch Filter To Narrow Band	3
0 ≈ 33,3 ms	Lock Indicator On Or Go to 1	4
0 - 16,6 ms	Start Counter	5
250 ms ± 9µs	Stop Counter	6
<200µs	Read Time Read Counter Reset Counter	7
10 seconds	Go To 5	8
.		
.		
.		
.		
.		
.		
.	Lock Indicator Off	7,4
<200µs	Select And Input to Ramp	7,5
0 ≈ N seconds	Lock Indicator On Or Deactivate Device	7,6

FIGURE 15

II.4 References

1. F.M. Gardner, "Phase Lock Techniques" Wiley New York, 1966.

2. Alain Blanchart, "Phase Lock Loops, Application to Coherent Receiver Design" Wiley, New York, 1976.

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4. I.E. Kliger & C.F. Olenberger, "Phase Lock Loop Jump Phenominon in the Presence of Two Signals" IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-12, No. 1, January 1976.

5. B.E. Bjerede, "A Fast Phase Lock Loop Algorithm with Applications to Microprocessor Implemented Communication and Navigation Systems" AES Newsletter, September 1976.

6. F.M. Gardner, "Acquisition of Phase Lock", Vol. I, ICC'76 Philadelphia.

7. L.J. Griffiths, "Rapid Measurement of Digital Instantaneous Frequency", IEEE Trans. on Acoustics, Speech and Signal Processing, Vol. ASSP-23, No. 2, April 75.

8. J.P. Frazier & J. Page, "Phase Lock Loop Frequency Acquisition Study", Trans IRE, Set 8 Sept. 62.

9. A. Blanchard, "Interference in PLLs", IEEE Trans. on Aerospace and Electronic Systems", Vol. AES-10, No. 5, Sept. 74.

III ENGINEERING AND ECONOMIC EVALUATION OF CANDIDATE RECEIVERS

III.1 Introduction

This section examines and compares the candidate receiver structures from the implementation standpoint. It addresses:

- Design approaches and technical tradeoffs
- Make vs buy options
- Technical and schedule risk
- Capital costs
- Engineering effort requirements

III.2 Receiver Configurations

The preceding sections of this report have identified receiver structures comprised of the following elements

a. Downconverter

b. Receiver - either (1) stepper
(2) sweeper

c. Counter - either (1) Fixed period
(2) A to D

In addition it has been shown that the above elements may be configured for Type A operation, or Type B operation. It is a design objective that both modes of operation be ultimately achievable with the same hardware building blocks, integrated differently where necessary and operated under control of the appropriately different software.

The candidate receiver structures may be broken down thus

Down Converter	+	Stepper or Sweeper	+	F.P. Counter or A to D	+	Type A or Type B

yielding 1 X 2 X 2 X 2 = 8 possible combinations.

The elements of these combinations are examined in detail in the following sections.

III.3 Detailed Assessment of Receiver Elements

III.3.1 Choice of Frequency Plan

A principal choice to be made for the Sarsat receiver is its operating frequency plan. This involves identifying the operating

frequency of the PLL, of the stepper or sweeper, and thence of the down converter. The factors which must be considered include;

i a lower operating input frequency limit of 6 kHz exists for the sweeper type of receiver. This is dictated by the need to avoid spectrum fold over.

ii No theoretical upper limit exists for the PLL operating frequency; however practical circuit design becomes progressively more difficult at higher frequencies. A broad statement of PLL operating frequency would be "in the tens or low hundreds of kHz range".

iii Other factors to be considered:

a. The VCO sweep range for the sweeper receiver should be maintained as a reasonably small percentage of operating frequency both to preserve reasonable voltage to frequency linearity (to ensure that loop gain does not become a function of frequency) and to retain predictable noise performance. This would suggest the sweeper VCO operating frequency should be in the "high tens of kHz or low hundreds of kHz".

b. The operating frequency of the stepper receiver synthesizer can be selected as desired, or, on the basis of commercially available units.

c. The realisability of a stable narrowband IF filter (of low order for the sweeper),

One notes that:

- active filters using operational amplifiers become progressively more difficult to realise above several kHz
- inductors with Q factors above 500-800 are difficult to realise. This means that L-C filters with a 3 dB BW of 50 Hz at frequencies exceeding Q X BW_{3dB} (i.e. 40 kHz) may yield practical problems
- crystal filters may not yield the design flexibility required for this phase of the work.

Based on c above a suggested centre frequency for the narrow band IF filter is 15 kHz

A suggested frequency plan for both types of receiver is given in the accompanying table. Clearly a considerable amount of designer freedom may be expressed and should be used to advantage if other design tradeoffs are required.

PARAMETER	STEPPER	SWEEPER
Down Converter Frequency Range (MHz)	70 ±.006	70 ±.006
Down Converter Output Frequency Range (kHz)	60 ± 6	60 ± 6 (455 ± 6)**
Synthesizer Frequency Range (kHz)	75 ± 6	N/A
VCO Frequency Range (kHz)	15* ± .025	75 ± 6 (470 ± 6)**
NB IF Filter Centre Frequency (kHz)	15	15
PLL Operating Frequency (kHz)	15*	15

SUGGESTED FREQUENCY PLANS

* can be lowered by having additional stage of down conversion between 47 Hz BPF and PLL input

** bracketed figures denote an alternative which may be attractive due to the fact that 455 kHz is a standard broadcast band intermediate frequency, for which IF filters are readily available.

III.4 The Down Converter

III.4.1 Make or Buy

The down converter is a clear case of 'make' since suitable units are not commercially available. The unusual features of this device are associated with frequency stability, frequency plan and filtering aspects.

III.4.2 Design Tradeoffs

The down converter tradeoffs are as follows:

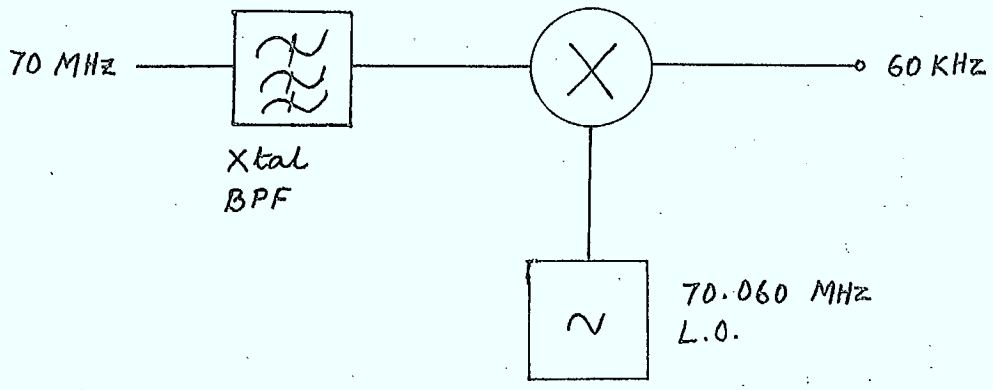
i Number of local oscillators should be minimised in order to reduce the potential sources of frequency error. This should be consistent with -

ii Realisable, stable economical filters capable of providing the required selectivity and image rejection

iii Price and lead times to procure components

a. Single Down Conversion

A single down conversion from 70 MHz to 60 kHz (or 455 kHz) is feasible if a crystal filter is used to provide image channel rejection at RF;



This approach employs one local oscillator, one stage of mixing and one bandpass filter.

The crystal filter employed will require at least 20 dB attenuation at the image ($2 f_{lo} - f_{signal}$) frequency i.e. at 70.120 MHz to ensure image noise degradation of less than 0.1 dB. This is well within crystal filter technology. A suitable filter quoted by McCoy is as follows:

1 dB passband:		70 MHz $\pm$ 6 kHz
Stop band	:	-20 dB @ $\pm$ 10 kHz
		- 60 dB @ $\pm$ 40 kHz
Size	:	2.4" X 1.0" X 1.3"
P & A	:	~ $350 US, 10-12 weeks

The 70,060 MHz local oscillator will require a stability of the order of 2×10^{-9} (= 0,14 Hz) over the duration of a pass and perhaps 2×10^{-7} (= 14 Hz per day). The Vectron CO-229 or CO-204 proportional oven controlled crystal oscillator should meet this requirement (P & A $425 US, 90 days).

b. Double Down Conversion

A double down conversion from 70 MHz to 60 kHz (or 455 kHz) is feasible using much less demanding RF filtering. In this case the image frequency is much further separated from the signal band.

Consider a 4 pole coaxial bandpass filter quoted by CIR-Q-TEL

1 dB passband:	70 MHz $\pm$ 0.5 MHz
Stop band	:	-20 dB at $\pm$ 2 MHz
		-45 dB at $\pm$ 5 MHz
P & A	:	~ $100 US, 5-6 weeks.

Assuming the first IF selected were 10,7 MHz, the IF filter response would require to be 20 dB down at the image frequency i.e. at 10,7 $\pm$,120 MHz (or 10,7 $\pm$,910 MHz). These requirements are not difficult to meet with either L-C tuned circuits or with a crystal filter.

The second conversion would translate the signal frequency to 60 kHz (or 455 kHz).

The stability requirements of the first L.O. are essentially the same as in the single stage down converter (hence similar cost). The second L.O. i.e. 10,760 MHz (or 11.155 MHz) should contribute no more to the net translation error than the first L.O. A temperature compensated crystal oscillator (TCXO) such as Vectron CO-252-3 will provide an aging rate of 1 X 10^{-8} (0.1 Hz) per day. Price for such a unit is $300-$400 U.S.

An advantage to the double down converter is the freedom to change the output frequency simply by changing the frequency of the 2nd L.O. This may be desirable in the design phase.

III.4.3 Conclusions

The single stage down converter possesses advantages of simplicity, lower parts count and thus a lower hardware cost and would probably be a first choice were it not for the long delivery of the crystal filter (10-12 weeks APO) and the first LO (90 days).

Should it not be possible to significantly improve the crystal filter delivery, the double down converter solution should be pursued. Whichever path is adopted, the development program can be expedited by temporary substitution of less stable but more readily available local oscillators, in lieu of the high stability units.

III.5 The Stepper Receiver

III.5.1 The Synthesizer

III.5.1.1 Make or Buy

Since suitable programmable synthesizers are commercially available a valid make or buy option does exist. The Fluke model 6010A (spec sheet appended) is priced at $3145 CDN including duty. Its key features are

programmability (0.1 Hz resolution)
fast settling (2-10 ms)
10 Hz - 110 kHz (Range I)
10 Hz - 11 MHz (Range II)
adequate stability 1×10^{-8}/day

Delivery is 8-10 weeks.

For purposes of cost comparison consider the Type AB receiver using two synthesizer units:

To Buy:	Synthesizer	$6290
	Estimated Interface Design Effort	$2500
	TOTAL	$8790

Specifications

Frequency

Range
10 Hz to 109.9999 kHz in the low range
10 Hz to 10.99999 MHz in the high range

Resolution
0.1 Hz in the low range
10 Hz in the high range

Range Selection
Automatic with manual override.

Annunciation
Units automatically justified in the LED display to indicate maximum resolution.

Accuracy
±3 parts in 10^6 for one year over the temperature range of 0°C to +50°C.

Aging Rate
Less than 1 part in 10^9 per day at constant temperature or 1 part in 10^6 per year.

Temperature
Less than ±2 parts in 10^6 from 0°C to +50°C (Less than ±5 parts in 10^7 from 0°C to +50°C with optional high performance oscillator)

Local Control
Keyboard selection of numerical data, magnitude (Hz, kHz, MHz) and functions. Rotary knob provided for modifying entry.

Remote Frequency Control
Byte serial, bit parallel, ASC II data format, two programming formats—fixed form and free form.

Frequency Display
Seven digit LED display of frequency set by local or remote control.

Frequency Storage
Facility to store and recall 10 front panel control settings including frequency, attenuator and modulaion.

Spectral Purity

Harmonics
—50 dB from 10 Hz to 1 MHz
—40 dB from 1 MHz to 11 MHz
(Except —35 dB for output levels within 2 dB of max output on each attenuation range from 1 MHz to 11 MHz.)
Total harmonic distortion less than 0.3% from 10 Hz—110 kHz. (Typical harmonically related outputs will be greater than 60 dB down.)

Spurious
All non-harmonically related outputs will be greater than 60 dB below the specified output or —110 dBm whichever is greater.

Signal to Phase Noise Ratio
Greater than 46 dB as measured in a 30 kHz band excluding 1 Hz centered on the carrier, including the effects of the internal standard. Residual (excluding internal standard) is greater than 50 dB down. Improvement on Low Range.

Phase Noise Spectral Density
SSB S/N Ratio at the output measured in a 1 Hz bandwidth at maximum output (typical). Improvement on Low Range.

Offset Frequency	SSB S/N
20 Hz	102 dB
200 Hz	108 dB
20 kHz	106 dB
1 MHz	130 dB

Amplitude

Range
0.25 mV rms to 5V rms (0.5 watts) into 50 ohms.

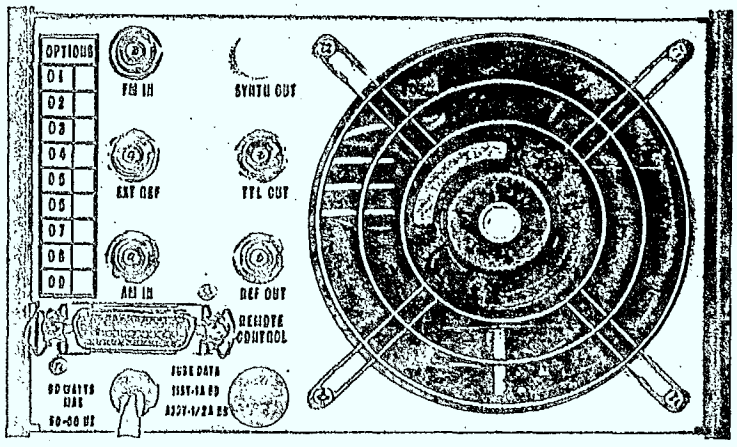
Attenuator
Consists of 20 and 40 dB sections providing 0 to 60 dB of attenuation in 20 dB steps.

Control
Rotary knob adjusts amplitude over a 26 dB range, keyboard selects one of four attenuator settings.

Frequency Response
±0.5 dB from 10 Hz to 11MHz within each band.

Stability vs Temperature

±0.25 dB	+18°C to +28°C
±0.75 dB	0°C to 50°C



FM IN
Frequency Modulation ±5 V peak-to-peak, deviates output frequency ±20 kHz in high range; ±200 Hz In low range. ZIn = 600 ohms.

EXT REF
A 10 MHz TTL compatible square wave can be used to reference the synthesizer. Internal Ref. is automatically selected in the absence of an Ext. Ref. (Int. Ref. error $<\pm 3 \times 10^{-9}$/yr., 0°C to 50°C).

AM IN
DC to 10 kHz; ±5V peak to peak corresponds to 100% modulation. Maximum modulation 90% Zin = 600 ohms.

Remote Control
Mating connector: Amphenol 57-30240.

Ref Out
Derived from the synthesizer frequency reference. 1 MHz output is standard; 5 or 10 MHz available by changing internal jumper. Output is TTL compatible square wave, 0 to 3.5 V peak amplitude.

TTL Out
Frequency is identical to SYNTH OUT; 0 to +2.5V minimum peak amplitude into 50 ohms

SYNTH OUT
Output for either option —04 or option —09.

Output Impedance
50 ohms

Remote Control
Byte serial, bit parallel.
External analog voltage (BNC connector on rear panel) will program output from 0.25 to 5 V rms. +0.25 VDC corresponds to 0.25V rms, +5 VDC corresponds to 5 V rms.

AM Modulation
Analog remote control input can be used to provide amplitude modulation. Bandwidth of this input is 10 kHz and maximum modulation is 90%. ±5V p-p corresponds to 100% modulation; Z_{in}=600Ω.

Switching and Settling Time

Frequency
Low range. Frequency settles to within 10 Hz of final frequency in less than 2 ms in fixed form and in less than 10 ms in free form upon update.

High range. Frequency settles to within 1 kHz of final frequency in less than 2 ms in fixed form and in less than 10 ms in free form upon update.

Range change, less than 10 ms to be within frequency settling specifications upon update.

Handshake cycle to accept one character other than update, less than 1ms in fixed form.

Auxiliary Outputs

TTL Output
TTL compatible square wave output (<0.5V to >2.4V p-p into 50Ω) at the synthesized output frequency. Symmetry is 45% to 55%, with rise and fall times less than 10 ns.

Reference
Derived from the synthesizer frequency reference. 1 MHz output is standard; 5 or 10 MHz available by changing internal jumper. Output is TTL compatible square wave, 0 to 3.5V peak amplitude.

Inputs

External Reference
Requires a 10 MHz TTL compatible square wave with symmetry between forty and sixty percent. Internal reference is automatically selected in the absence of an external reference.

General

Operating Environmental
0—50°C, 0 to 80% RH, 0 to 10,000 feet.

Non-Operating
—40°C to 75°C

Power
115/230V rms ±10%, 50—60 Hz
Power switch disconnects both sides of power line.

Weight
25 lbs. (11.4 kg)

Size
5¼" x 8½" x 19"
(13.3 cm x 21.6 cm x 48.2 cm)

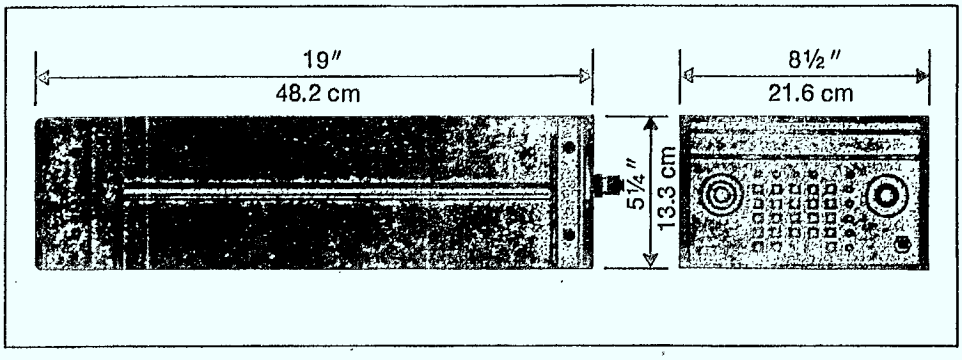
Options

High Performance TCXO (Option —01)

Frequency Accuracy
±1.5 parts in 10^6 for one year over the temperature range of 0°C to +50°C.

Aging Rate
Less than 1 part in 10^8 per 24 hours at constant temperature, or 1 part in 10^6 per year.

Temperature Dependence
Less than ±5 parts in 10^7 from 0°C to +50°C



Phase Lockable Input (Option —02)

Input Frequency
1, 2, 2.5, 5, or 10 MHz

Input Level
Greater than 100 mV, less than 5V rms into 50 ohms
May be used with either the standard oscillator or the optional high performance oscillator.

Frequency Modulation (Option —03)

	High Range	Low Range
Deviation about dialed frequency:	±20 kHz	±200 Hz
Accuracy 0-50°C:	±1.5 kHz	±15 Hz
Linearity at Const Temp:	±1 kHz	±10 Hz
Rate:	DC to 10 kHz	DC to 10 kHz
Stability:	±400 Hz	±4 Hz
Zin:	600Ω	600Ω

Rear Panel Output (Option —04)

IEEE P488 General Purpose Bus Interface (Option —05)
(Byte serial, bit parallel) Compatible with proposed IEC TC 66, WG 3 Interface.

EIA Standard RS-232 C Interface
(Option —06) (Byte serial, bit serial)

50 to 400 Hz line power (Option —07)

100V, 50 to 60 Hz line power
(Option —08)

20-31 MHz Tracking Output
(TTL Level) (Option —09)

Prices:

6010A	**$2,495**
Options	
01 High Performance TCXO	95.
02 Phase Lock Input	195.
03 Frequency Modulation	495.
04 Rear Panel Output	10.
05 IEEE 488 General Purpose Bus Interface (Byte serial, bit parallel)	200.
06 EIA Standard RS-232 C Interface (Byte serial, bit serial)	250.
07 50-400 Hz Line Power	150.
08 100V, 50-60 Hz Line Power	NC
09 20-31 MHz Tracking Output (TTL Level)	30.

To Make;	Estimated Parts Cost	$ 750
	Estimated Design Effort	$7700
	TOTAL	$8200

Conclusion: The relatively small cost difference and reduced program risk favour the 'buy' approach.

III.5.2 The Narrow band IF Filter

III.5.2.1 Make or Buy

This is a low cost impact item and two or more approaches may be examined:

a. crystal filter (buy)
b. Active filter e.g. bi-quad (build)
c. L-C High Q filter (build)

III.5.3 Phase Locked Loop

III.5.3.1 Make or Buy

The 'make' decision is necessary since the specific SARSAT requirements are unique and will require a considerable amount of parameter variation trade offs to optimise performance.

III,5,3,2 Technical Tradeoffs

The PLL tradeoffs have been examined in considerable depth elsewhere in this study. This section highlights certain aspects of the development phase activities.

i IC Phase Locked Loops

Currently available are complete phase locked loops on a single IC (e.g. RCA CD4046) priced at a few dollars and available as stock items. These PLL's are capable of operating up to several hundred kHz and contain phase detector, VCO and lock indicator circuitry. Loop filter elements are added externally to the chip.

Part of Phase III should be devoted to examining these PLL's to identify whether these devices exhibit any significant shortcomings e.g. phase noise, coupling problems, etc., at the relatively low operating frequencies (15 kHz) under consideration.

On the pessimistic assumption that the IC PLL will prove unsuitable it will be necessary to realize the PLL components in discrete or separate function form.

ii Phase Detector

One promising technique of realising the phase detector is to use an

exclusive OR gate. This produces a linear phase vs voltage characteristic over the interval $+\pi$ to $-\pi$ i,e. a practical realisation of the sawtooth phase detector.

iii VCO

For the voltage controlled oscillator the major unknown as yet is the phase noise performance. This will be particularly important in the tracking mode with the narrow loop bandwidth employed.

Types of oscillator in order of improving phase noise performance are:

- relaxation oscillator - voltage tuned
- L-C oscillator - voltage (varactor) tuned
- crystal oscillator - voltage (varactor) tuned.

Hopefully, the phase noise performance of one of the first two types of oscillators is adequate. If a VCXO is required it will be necessary to generate the signal at a frequency of 100 kHz or more (typically a VCXO provides $\pm$ .1% deviation capability) and translate down to the loop VCO frequency.

This problem could clearly prove more troublesome for the sweeper receiver where a $\pm$ 6 kHz deviation is required.

A factor in favour of the stepper receiver is that VCO sweep is not required. This will result in significant reduction in circuit and control complexity compared with the sweeper.

iv Loop Filter

The compensated integrator and the requirement to switch bandwidths for the tracking and search modes is discussed elsewhere in this report.

v Lock Detector

Two levels of circuit complexity may be required in the evaluation of the lock detector.

a. The simple lock detector where lock is indicated by the d.c. term from a product detector whose input signals are the loop input signal, and a 90° shifted sample of the VCO signal.

b. The dual condition lock detector whereby lock is indicated both by (a) above and by suppression of noise at the phase detector output.

The additional development effort required for (b) should result in a higher integrity for the lock indicator.

III.5.3.3 Capital Costs

The capital cost for the PLL components is not expected to exceed $1000 since it contains only relatively simple elements.

III.5.3.4 Engineering Costs

The engineering development costs for the PLL will dominate the capital costs by a factor of around 7-10:1.

III.6 The Sweeper Receiver

III.6.1 Make or Buy

The sweeper receiver is again a clear case of 'make' for the reason that suitable devices are not commercially available.

III.6.2 Technical Tradeoffs

Many of the technical tradeoffs discussed for the PLL in the stepper receiver apply to the sweeper receiver i.e. phase detector, lock indicator and loop filter.

The key differences are seen as follows:

i There is a risk of loop instability due to the inclusion within the loop of the narrow band IF filter and its associated poles.

ii The VCO is required to operate over the full 12 kHz deviation range of the input signal band. This may require a more careful selection of VCO operating frequency than for the stepper PLL i.e. added risk.

iii A sweep voltage and associated control circuitry are required even for type A operation. This, although not particularly difficult to implement practically, will increase the developmer

effort required significantly because,

a. Examining the sweep rate vs acquisition characteristics will involve hardware changes to the sweep circuitry.

b. A further option must be critically examined i.e. termination of sweep by hardware (lock indicator) or by software.

c. Circuitry must be included for adjustment of sweep rate, and periodic calibration of the sweep rate.

III.6.3 Capital Costs

Capital costs for the PLL portion of both stepper and sweeper receivers are expected to be essentially similar - under $1000.

The capital cost (or development cost) of the programmable synthesizer is a significant cost disadvantage to the stepper receiver.

III.6.4 Engineering Costs

The engineering costs for the sweeper receiver will again dominate the capital costs by a factor of 10 or 12 to 1.

III.7 Conclusions on Stepper vs Sweeper

i The stepper receiver represents a significantly lower technical and schedule risk than the sweeper receiver.

ii The higher costs of the stepper receiver (around $3000 for a two channel receiver) are offset by its lower technical and schedule risk.

iii A commercially available synthesizer has significant advantages over a new development in terms of reduced performance and schedule risk and increased flexibility. Overall costs, are only marginally in favour of developing a synthesizer in-house.

iv The recommended approach is the stepper receiver utilising the commercially available programmable synthesizer.

III.8 The Frequency Counter

III.8.1 Make or Buy

A valid make or buy option exists for the frequency counter. Counters with a gate control capability are commercially available for $1000 - $1500. e.g. Fluke Model 1953A. They have the advantage of being able to double as test instruments during the development phase, but require extra engineering attention to design the counter/computer interface. On the other hand on-card counters using integrated circuits are quite simple to include and quite inexpensive (under $100 parts cost). The make-buy decision is thus probably in favour of making the counter. Both approaches appear to be low cost, and low risk.

III.8.2 Technical Tradeoffs

Two types of on-card counters will be considered

i The fixed period counter which counts zero crossings for a pre-determined time under computer control.

ii The A/D converter which measures the control voltage on the VCO, A to D converts and inputs this information to the computer. With a knowledge of the voltage to frequency characteristic the computer can derive the VCO frequency.

Fixed Period Counter

Assuming a 15 kHz VCO operating frequency and 250 ms measuring time the maximum count expected is

$$2 \times 15000 \times 0{,}25 = 7500$$

(due to doubling)

A 13 bit binary counter can provide a maximum count of 8192 and would thus be suitable. In practice two cascaded 7 bit counters e.g. (MC14024) giving a total count capability of 16,384 would probably be employed and incidentally give a 2:1 overflow protection.

A reduction in the number count bits required to interface with the computer can be achieved by taking advantage of the knowledge of the lowest expected count

e.g. if the lowest expected count is say $2 \times 14900 \times .25 = 7450$

The counter could be inhibited until the count reaches $2^{12} + 2^{11} + 2^{10} + 2^{8} = 7424$

and the maximum count required would thus be

$$7500 - 7424 = 76$$

which could be interfaced to the computer using 7 bits ($2^{7} = 128$) only.

A/D Converter

Assuming a linear voltage to frequency characteristic and a dynamic frequency range of Δf Hz the number of bits required to achieve a resolution of 1 Hz is n

where

$\Delta f = 2^n$

e.g. if Δf = 100 Hz 7 bits are required

Encoding times can be very fast (10 μS) for the DEC A811 10 bit A/D converter, and encoding accuracy quite high (0.1% of full scale).

The disadvantages of this type of scheme are

i Non linearity of the VCO - may require linearisation or look up tables

ii Change of characteristics with time e.g. voltage references, linearity.

It is felt that these disadvantages are serious enough that the approach is not attractive at this time.

III.8.3 Conclusions

i The counter represents a straight forward low cost, low risk element of the receiver.

ii The on-card counter is preferred to the commercial counter for reasons of system flexibility and lower cost.

iii The direct fixed period counter has significant advantages in terms of stability and reproducibility over the D/A type of counter.

III.9 Type 'A' vs Type 'B' Receiver

III.9.1 General

This section identifies some additional features required on the Type B receiver which may not be necessary on the Type A receiver. Generally these features are associated with the requirement to maintain tracking in the narrow band mode.

III.9.2 The Sweeper Receiver

Upon loss of lock for any reason (e.g. ELT fade or pulsed ELT drop-out) the receiver is required to attempt to extrapolate the ELT frequency and reacquire. In order to achieve the advantage of the type B mode of operation (i.e. rejection of interferers) it is essential to maintain the narrow band mode of operation during re-acquisition. Thus due to the limited pull in range of the loop ($\pm$ 3.75 Hz) the extrapolated frequency will be required to be very precise. For the sweeper two approaches which can be used are

a. Open Loop using
   - i ramp
   - ii D/A

b. Closed Loop

The open loop approach relies on controlling the VCO frequency by applying an external voltage either a ramp voltage whose slope is selected to approximate the ELT drift rate, or rapidly updated analog voltage applied from the computer via a D/A converter. Both approaches have the fundamental practical disadvantage of requiring time invariance of the VCO characteristic. In addition the ramp approach is limited practically by the finite number of ramp slopes which can be easily provided.

The closed loop approach requires a software controlled routine whereby the extrapolated VCO frequency is verified by a measurement at several instants during the exercise. This technique would appear more promising in terms of reproducibility.

III.9.3 Stepper Receiver

The stepper receiver is more amenable to controlled extrapolation as it is controllable in discrete steps. Note that if the suggested model 6010A synthesizer is used the step resolution can be reduced to as low as 0.1 Hz on command. The actual time/frequency profile of the stepper then is entirely under computer control and the designer can then perform the tradeoff between probability of re-acquisition vs processor time spent in controlling the extrapolation process.

III.9.4 Conclusion

The stepper and sweeper receiver both require an accurate frequency extrapolation capability for Type B operation.

For the sweeper type of receiver this capability would be complex to realise and should be considered outside the scope of the planned activities for Phase III.

For the stepper receiver accurate extrapolation appears quite feasible. Since it involves additional software development, and an addition to the scope of performance verification testing it is expected to overrun the available time. However it is suggested as an area for additional work after March 1977.

III.10 Overall Conclusions

i A frequency plan has been suggested for the SARSAT receiver.

ii The down converter will probably be of the double down conversion type unless the delivery of a suitable RF crystal filter can be improved from 10-12 weeks to say 5-6 weeks.

iii Deliveries of high stability oscillators are critical - up to 90 days. Work around plans using lower stability oscillators are probably inevitable.

iv The stepper receiver is recommended over the sweeper from the standpoints of less technical risk, less schedule risk and only marginal additional cost even if commercial synthesizers are procured.

v Significant technical and schedule benefits result if the commercial synthesizers are procured rather than developed in house

vi The fixed period counter can provide adequate performance at low cost and complexity and should be integrated with the receiver.

vii Accurate ELT frequency extrapolation in the narrow band mode appears feasible using a high resolution synthesizer for

example, It is suggested that this area be considered beyond the scope of the present receiver development activities because of the short and extremely busy program between now and March 1977.

IV DEFINITION OF PROPOSED RECEIVER

Miller Communications Systems Ltd. proposes the implementation of the Type AB receiver described in II.3.1.1 for the detection and measurement of up to 8 ELT signals. This receiver will be capable of working fully in the Type A mode and also in a limited Type B mode, but will only be fully demonstrated under the present contract in the Type A mode. We believe that the proposed receiver will meet the required performance specification while providing advantages of flexibility in a cost-effective manner.

IV.1 Receiver System Description

IV.1.1 Receiver System Hardware

The receiver signal processing hardware will consist of a down convertor subsystem and two "test instruments" independently controllable and capable of being stepped to any one of 256 47 Hz or 128 94 Hz sub-bands in the 12 kHz band, detecting and measuring the frequency of a sinusoid having a $C/N_o \geq 26$ dB/Hz and a rate of change of frequency ≤ 14 Hz/sec. With appropriate microprocessor control this receiver can be operated in either a Type A or limited Type B mode, and expansion to a full Type B receiver* can be accomplished by adding

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* The receiver would still not have the capability of being able to narrow band track pulsed ELT's. This feature requires the addition of an input from the computer to each device to command and possibly control an extrapolation of VCO input voltage during out of lock periods.

six more devices - the control interfaces will be designed to accommodate this addition. The input/output for each test instrument is rather simple, consisting of the incoming noise filtered signal at appropriate centre frequency, an outgoing frequency measurement, and four logical control variables, namely:

i lock indicator status

ii stepper (synthesizer) frequency

iii PLL loop filter bandwidth (2 states)

iv counter start/stop command

The critical timing parameters (sweep rate, allowed acquisition time, and measurement period), which can only be finalized experimentally, are under complete control of the computer and can easily be varied.

Since the signal-to-noise ratio required to achieve satisfactory performance trades off with the allowable sweep speed, and since neither can be quantified exactly at this time, the instrument will be initially developed to operate with either 47 Hz steps/50 Hz pre-detection bandwidth or 94 Hz steps/100 Hz pre-detection bandwidth. This requires only that two sets of band pass and PLL loop filters be designed and built.

While priority will be given to developing a working Type A receiver, to give maximum operational flexibility, Type B requirements will be considered in the detailed design of the test instrument.

IV.1.2 Receiver Operation

In concise words, the sequential operation of the proposed receiver will be as follows:

In Type A mode:

1. Both devices (staggered 6 kHz apart) will be stepped synchronously across the 12 kHz band in 47/94 Hz steps. The holding time in each step will be sufficient to ensure detection of a continuous ELT; this determines the total sweep time, expected to be about 20 seconds per device.

2. Upon detection (coherent) of an ELT by either or both devices, the regular stepping will be interrupted until an attempt has been made to measure its (their)frequency. This interruption is expected to be about .5 seconds.

3. The PLL loop filter will be narrowed.

4. If lock is re-established within an allowable maximum waiting period, a simple counter, starting and stopping on computer command,

will measure the ELT frequency over a 50/100 Hz range. A counting period of .25 seconds should give the required 1 Hz rms measurement accuracy. If lock is lost within the first 80-100% (to be determined) of the measurement period, the measurement will be aborted.

5. A measured frequency will be read and time tagged in the computer. The net ELT frequency, consisting of the current step address plus counter measurement will be computed and stored in the computer for sorting.

6. Stepping will resume upon receipt of a counter measurement or by time default. If the same ELT is expected to be redetected in the next (overlapping) frequency interval and a successful measurement was taken (based simply on whether the previously read counter frequency exceeded a given value), lock indicator status will be ignored on this step.

In Type B mode

1. The first device will start the searching process by stepping across the 12 kHz band in 47/94 Hz steps until it detects an ELT.

2. Once an ELT is detected, the first device start tracking while the computer assigns the second device to continue searching the band. (A new searching device will continue where the previous

searching device has left off, will skip steps currently occupied by tracking devices, and will not be assigned to track an ELT currently tracked but detected in an adjacent step).

3. The tracking process continues for as long as possible and measurements are taken as commanded. (When the tracking device is stepped, it is possible that with only minor impact on the hardware requirements the narrow PLL bandwidth can be maintained; otherwise the widen filter/redetect/narrow filter mode would have to be adopted).

4. Measurements are time tagged and stored in the computer for sorting.

It is evident that a Type B demonstration model based on the proposed hardware will be limited by the fact that a second detected ELT cannot be tracked while active searching continues. However, it can be envisaged that a model with eight identical devices can operate in Type B mode to the full extent.

IV.1.3 Computer Software and Computer Interfaces

The receiver software and computer interface will provide the control of the two devices so as to realize the operational sequence defined in IV.1.2. The program will provide flexibility, and accommodate easy selectability of the critical timing parameters which not only facilitates receiver development, but may prove useful during extended field trials under a variety of input conditions. Hardware and soft-

ware will be arranged so as to be easily expanded to handle 8 devices. For example 3 bits will be reserved for addressing a device even though only 1 bit is required to address 2 devices.

The programs will be written in PDP 11 assembler language. Modular, top down structured programming techniques will be utilized as much as possible to increase readability. The software will run under RT11 operating system but will interface to it as little as possible, but such things as the disk handler for RT 11 will be used. Other devices will be handled directly by the program using interrupts where possible with user written interrupt handlers.

The LSI 11 (PDP 11/03) asserts certain timing constraints based on instruction times. Because interrupts are not handled until the current instruction is finished, delay times from 3.15 μsec. (fastest instruction) to 21. μsec. (slowest instruction) can result. An external clock source (pulse generator) will be utilized due to the short term inaccuracy of the internal line frequency (60 cycle) closk. All control lines will be connected to one of the two interfaces. Each interface provides 16 input data lines, 16 output data lines, and 2 control lines for input and 2 for output with interrupt capabilities. Again, the lines will be assigned to accommodate up to 8 devices.

IV.2 Receiver Subsystems

The proposed receiver, as shown in Figure 10, is comprised of the following key subsystems:

1. Down Convertor

   - 70 MHz input frequency
   - 60 $\pm$ 6 kHz output frequency
   - stability < 2 X 10^{-9}/hr.
   - $\pm$ 7.5 kHz noise filtering

2. Programmable Frequency Synthesizer (Qty. 2)

   - 60 $\pm$ 6 kHz input frequency
   - Δf = 47/94 Hz
   - Δf precision << 1 Hz
   - digitally controlled by 8 bit address code

3. IF Filter and Limiter (Qty 2)

   - 50/100 Hz BPF
   - output signal hard limited

4. Phase Locked Loop (Qty 2)

   - 50/100 Hz input noise bandwidth and required pull-in range

- centre frequency to be determined
- switched resistor loop filter, automatically controlled
- coherent detector (lock indicator)

5a. Fixed Period Counter (Qty 2)

- rectified, digitized sine wave input from VCO
- start/stop externally controlled
- dynamic range > 100 Hz
- centre frequency and number of bits in measurement (> 8) to be determined

5b. High Precision A/D Convertor (Qty 2)
(alternate means of measuring frequency)

- linear
- > 8 bit
- requires highly linear and gain stable VCO

6. Microprocessor (Qty 1)

- PDP 11/03 (see section II.3.2)

Table 2 gives a detailed specification of the search/detect/measure device as a single subsystem. Note that the given system parameters are subject to experimental verification and may change during the receiver development.

TABLE 2

SPECIFICATION OF SEARCH/DETECT/MEASURING DEVICE

Number of devices in system	2
Synthesizer Step Size	47/94 (possibly computer controlled)
Number of Steps	256/128
Synthesizer Lock up time	to be determined
Pre-detection filter BW (Hz)	50/100
Wide Band PLL natural frequency (rad/sec)	16/25
PLL damping ratio	0.707
Wideband PLL pull in range (Hz)	$\pm$ 25/$\pm$ 50
Estimated Detection lock up time (msec)	80/40
Means of detection	coherent
Maximum time per step (msec) (variable under computer control)	80/160
Narrow Band PLL nat freq (rad/sec)	2.5
Narrow Band PLL Pull in range (Hz)	$\pm$3.75
Maximum Narrow Band PLL settling time (msec)	400

Table 2 Cont'd

Counting Period (if required) (msec)	250
Logical I/P from computer	synthesizer frequency, PLL loop filter state, counter start/stop command
Maximum rms frequency accuracy (Hz)	1.0
Doppler tracking range (Hz)	50/100
Minimum frequency separation for acquisition of two or more signals (Hz)	50/100
PLL modes	unlocked broad band locked narrow band locked
Input signal frequency	maximum deviation from centre frequency = 6 kHz, centre frequency to be determined
Minimum signal to noise ratio for specifications to be met	26 dB-Hz
Probability of failure to detect signal	small, to be determined
Probability of false detection	small, to be determined
Probability of spurious measurement (of noise)	negligible
Doppler rate tracking capability (minimum) (Hz/sec)	0 to -14
Allowable ELT signal modulation for undegraded performance	"chirp", sinusoidal or square wave with duty cycle from 1/3 to 1/2, maximum modulation 100%, sweep width 700 Hz in band 300 to 1600 Hz

Table 2 Cont'd

Effect of above ELT signal modulation on detection (wide band PLL)	may infrequently cause failure to acquire lock
Effect of above ELT signal modulation on PLL tracking (Narrow band PLL) and frequency measurement	none
Correction for length of time to make frequency measurement	time of measurement is taken to be the middle of the measurement period
Frequency measurement methods	fixed time counter at VCO output or A/D converter at VCO input
Minimum SNR at PLL input (before hard limiter) (dB)	9.0/6.0
PLL type	Loop filter: compensated
Strength of interfering signal to cause loss of lock of PLL in narrow band mode	At least 6 dB/octave more power outside tracking bandwidth; beyond bandwidth of IF filter add 12 dB per octave
O/P to computer	lock indicator state (interrupt) frequency reading

IV.3 Receiver Performance

Table 3 lists anticipated performance indices of the receiver operating in both the Type A and limited Type B modes with continuous "ideal" ELT signals. It is again noted that these are subject to experimental determination. Table 4 summarizes the degrading effects of carrier pulsing and incidental FM on receiver performance.

TABLE 3

ITEM	A	B
Number of devices searching	2	1
Range of search (kHz)	12	12
Operational Sequence	2 devices 6 kHz apart both stopping whenever ELT detected, resume stepping following measurement	a device searches till ELT detected, tracks & measures as instructed
Maximum time to detect new ELT (seconds)	10-14	10
Maximum number of ELT's which can be measured	8	2
Time between frequency measurements following initial detection (sec)	10-14	10
Measurement timing	asynchronous	synchronous or asynchronous
Doppler tracking range (kHz)	12	12
Maximum extrapolation time for estimated frequency readings before ELT signal is "lost" (seconds)	30	30

Table 3 Cont'd

ITEM	A	B
Minimum extrapolation time for estimated frequency readings before ELT signal is lost (seconds)	10 (when extrapolated regions of possible frequencies for 2 ELT's overlap)	0 (when 2 ELT's are extrapolated to fall within pull-in range of same PLL)
Types of frequency measurements provided	confirmed (i.e. lock maintained through measurement period) incomplete (i.e. lock lost in measurement period)	confirmed (i.e. lock maintained through measurement period) incomplete (i.e. lock lost in measurement period)
Identification of new ELT signal	at least 3 confirmed measurements	continuation of lock over a measurement interval
Procedure upon loss of lock	during measurement, that measurement is not confirmed	during measurement, that measurement is not confirmed. Switch to wide bandwidth mode; if not switched back to narrow band mode in 30 seconds, ELT is "lost"
Number of devices tracking	N/A	1
Effect, on an ELT being tracked, of other ELT's of strength greater than specified in part 1, Table 2	increased probability of failure to lock to weaker signal, loss of lock during measurement is possible	loss of lock during measurement is possible, eventual loss of lock assured

TABLE 4

ITEM	A	B
Pulsed ELT's	Increased probability of loss of lock during acquisition or measurement	periodic loss of narrow band lock
Incidental FM	More than 1 Hz maximum error in frequency reading if $\Delta f > 8$ Hz Loss of narrow band lock if $\Delta f > 10$ Hz approx. and sweep period is 1/4 sec.	More than 1 Hz maximum error in frequency reading if $\Delta f > 8$ Hz Loss of narrow band lock if $\Delta f > 10$ Hz approx. and sweep period is 1/4 sec.

IV,4 Data Stored in Computer for Transmission to Base

The ELT data record available for transmission to the Sarsat central processing station following a satellite pass will consist of the following:

TABLE 5

Maximum stored readings per ELT signal	120
Data associated with each measurement	a. frequency b. time of measurement c. "quality" of measurement
Quality of measurement	"Confirmed" (i.e. lock maintained through measurement period) or "estimated" (i.e. lock not maintained and measurement extrapolated from other data points)

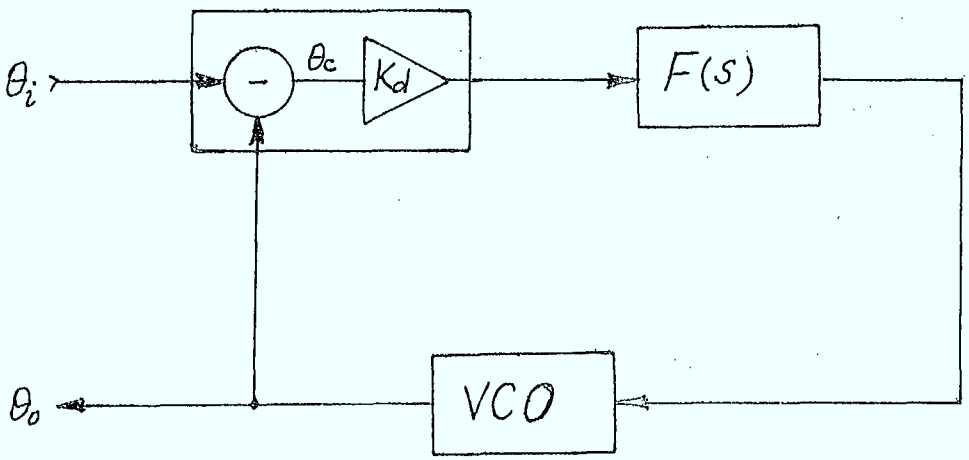
APPENDIX A

DESIGN OF PLL'S FOR SIGNAL ACQUISITION

A.1 Introduction

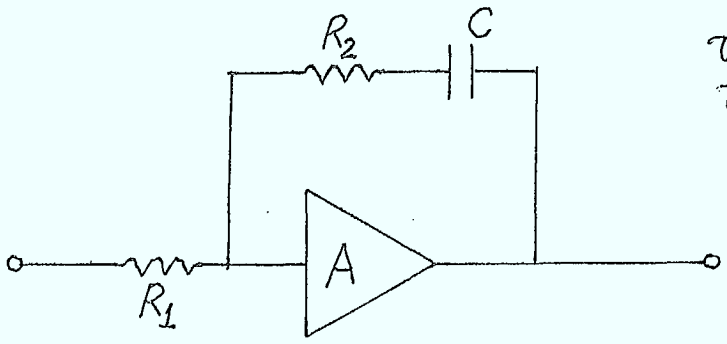
The purpose of this work is to describe the factors affecting the signal acquisition properties of the second order Phase Locked Loop (PLL). The PLL tracking performance will also be described.

The PLL consists of a phase detector (PD) of gain k_d volts out per radian of input phase difference, a loop filter/integrator of transfer function F(s) and a voltage controlled oscillator (VCO) of gain K_o rad/sec output per volt input.



Throughout this work F(s) will be assumed to take the form

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s}$$



$\tau_2 = CR_2$
$\tau_1 = CR_1$

ACTIVE LOOP FILTER

This type of loop filter gives a second order loop with the best signal tracking properties. The loop transfer function will be

$$\frac{\Theta_o(s)}{\Theta_i(s)} = H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \left(\frac{k_o k_d}{\tau_1}\right)^{1/2}$$

$$\zeta = \frac{\tau_2}{2}\left(\frac{k_o k_d}{\tau_1}\right)$$

where ζ and ω_n are the usual "control system" damping factor and natural frequency. For this case the loop noise bandwidth is

$$2B_L = \omega_n(\zeta + \frac{1}{4\zeta}) \qquad \text{(Gardner Eq. 3.12)}$$

This has a minimum value of $2B_L = \omega_n$ when $\zeta = 0.5$ (Note B_L in Hertz and ω_n in radians/second).

A.2 Phase Detection

The presence of noise affects the PD operation in two ways: firstly, it distorts the PD characteristic, lowering its amplitude and changing the shape to a sinusoid (if not already sinusoidal) as the C/N decreases, and secondly the PD output C/N is smaller than input C/N i.e. $\rho_o/\rho_i < 1$.

The characteristic changes are described by the parameter α, the relative PD output control signal and μ_p, the peak mean PD output. Thus the effective PD gain is αk_d and the normalized peak amplitude of the open loop PD beat note will be μ_p. These quantities are plotted in Figures 1 and 2 as functions of the PD input C/N ($=\rho_i$) and type.

The ratios ρ_o/ρ_i for various PD types are given in Figure 3. Also shown are the asymptotic values of the signal to noise spectral density ratios for small frequency offsets from the carrier. These are used to predict the final loop output signal to noise ratio (ρ_o).

A.3 PLL Operation

PLL operation is divided into Acquisition and Tracking modes. In general, solutions to problems of acquisition mode are empirical because the loop operation is highly non linear in this regime. However providing the signal to noise ratio is not too small, the linearized PLL model can be used to predict behaviour in the tracking mode to good accuracy.

A.3.1 Signal Acquisition

The time taken for natural (i.e. unassisted) frequency acquisition under noise free conditions is given by (approximately for $\Delta\omega > \omega_n$)

$$T_p = \frac{(\Delta\omega)^2}{2\zeta\omega_n^3}$$ where $\Delta\omega$ is the initial frequency offset (Gardner Eq. 4.31)

while for sweep frequency acquisition the time is

$$T_s = \frac{\Delta\omega}{R}$$ [Simply the angular frequency offset divided by the rate of (approach) sweep]

if $R = 0.5\ \omega_n^2$ (a typical figure only) and $\zeta = 1$ then these are equal for $\Delta\omega = 4\omega_n$. However T_p is for noise free conditions while T_s includes the effects of noise. Thus T_s is still likely to be smaller than T_p for $\Delta\omega < 4\omega_n$.

It has been found by an approximate analysis (Wakeman, 1976) that maximum sweep rate, R, to achieve a 90% lock up probability can be modelled by the relation

$$R = \frac{\omega_n^2 \left(1 - \sqrt{\frac{k}{\rho_L}}\right)\frac{\mu_p}{\alpha}}{1 + d} \quad \frac{\text{rad}}{\text{sec}^2}$$

(This formula follows the general form originally given by Frazier & Page)

In general experimental measurements show agreement to within 10%. The elements of the formula are,

1. ω_n the loop natural frequency

2. ρ_L the PLL output signal to noise ratio. This is related to the loop output rms phase noise σ by

$$\rho_L = \frac{1}{2\sigma^2}$$

3. μ_p/α is the ratio of the PD peak mean output μ_p, to the mean phase slope α. This ratio is unity for sinusoidal PD's under all conditions. The ratio for sawtooth and triangular PD's as a function of the input signal to noise ratio (ρ_{IF}) is given in Figure 2.

4. d is the peak overshoot in the transient response of the PLL to a frequency ramp input

$$d = \exp\left(-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}\right)$$

5. For 90% acquisition $k \cong 1$, for other acquisition probabilities k would change as in yet an undetermined manner

Curves of R vs ρ_L and PD type are given in Figure 4.

It should be noted that these curves are not directly comparable because the PLL using a sawtooth PD needs an approximately 2 dB better signal to noise ratio than the loop using a sinusoidal PD (see Figure 3) to achieve the same ρ_L value. Therefore R should be expressed in terms of C/N_o at the PD input and not in terms of ω_n^2. Using the relation between B_L and ω_n gives

$$\frac{R}{(C/N_o)^2} = \left\{\frac{\rho_o}{\rho_i} \cdot \frac{1}{\zeta + \frac{1}{4\zeta}}\right\}^2 \frac{1}{\rho_L^2} \left(1 - \frac{k}{\sqrt{\rho_L}}\right) \frac{\frac{\mu_p}{\alpha}}{1+d}$$

For sinusoidal PD's where $\mu_p/\alpha = 1$ the above has an optimum value at $\rho_L = \left(\frac{5k}{4}\right)^2$, if k=1 (for 90%) ρ_{Lopt} = 1.94 dB. $R/(C/N_o)^2$ is given in Figure 5 for some typical loop operating conditions.

Figure 4a shows experimental measurements of acquisition probability vs sweep rate for the sinusoidal PD. This information is given to show the reduction in sweep rate necessary to increase the probability of acquisition.

Since d also depends on ζ the loop damping ratio there will be an optimum ζ that maximizes R. ζ_{opt} depends on the C/N ratio however, and lies between 0,5 and 1. The value ζ = ,7 is nearly optimum from other considerations as well.

If sinusoidal PDs are used, the input bandwidth has little consequence on the operation of the PD. If triangular or sawtooth PDs are used, μ_p/α is great for the largest input C/N ratio. Therefore for best R the PD input C/N should be as high as possible, ie. the input bandwidth as small as possible. This can be achieved by placing the IF bandpass filter within the PLL structure. See comments on configuration .

μ_p/α for Costas and squaring loops is 0.5 and for this and other reasons these loop types have very poor signal acquisition properties. This is mentioned for the information of the reader only.

The effect of incidental phase modulation on R depends on the nature and magnitude of the modulation. For sinusoidal PM, R is multiplied by the factor $\left(1 - \phi_p/2.4\right)$ if the PM frequency is greater than ω_n.

Acquisition will be seriously affected if the signal is ON/OFF keyed at a rate $\lesssim T_p^{-1}$.

A substantial increase in the sweep rate is allowable if the VCO sweep is removed as soon as possible after the frequency difference has been brought to zero. This is because the sweep rate limit is set by conditions in the PLL <u>after</u> $\Delta\omega$ has been brought to zero.

No satisfactory model for this situation has been developed, although the process of lock detection or detection of frequency coincidence

is well understood. More details will be given in the section entitled 'lock detection'.

In summary then, optimum or near optimum acquisition times will occur for sinusoidal or triangular phase detectors with sweep removal and $\rho_L \doteq 2$ dB and $\zeta \doteq 0,7$.

A.3.2 Signal Tracking

A.3.2.1 Output Signal

The division between linear and non linear PLL operation occurs approximately when the VCO mean square phase noise $\sigma^2 = 0.25$. That is at a loop signal to noise ratio of $\rho_L = 2$ (3 dB).

The loop output C/N is found simply by treating the PLL as a band-pass filter at bandwidth 2 B_L

$$\sigma^2 = \frac{\omega_n(\zeta+\frac{1}{4\zeta})}{2\ C/N_o} \quad (\text{rad}^2) \qquad = \frac{1}{2\rho_L}$$

where C/N_o is the PD output carrier to noise spectral density ratio and is found from the input value with the aid of Figure 3

A.3.2.2 Tracking a Frequency Ramp

For an input signal frequency ramp of R (rad/sec^2), the steady state phase error also known as dynamic tracking error is easily calculated

to be

$$\phi_e = \frac{R}{\omega_n^2} \quad \text{for small values of R (Gardner 4.5)}$$

The maximum value of R that may be tracked is the same as the maximum allowable sweep rate for acquisition (when the sweep is not removed at lock-up).

A.3.2.4 Cycle Skipping

At large values of σ^2 the probability that the loop will jump out of lock on the noise peaks becomes significant. When this happens the loop will skip one or more cycles. If this occurs, on average, more often in one direction than the other, then a frequency error will exist between the signal and VCO. Graphs are given for the normalized time to unlock and the number of cycles skipped (Figure 5).

An empirical formula for the calculation of the probability P(T) that the VCO will skip during time T starting from zero phase error is:

$$P(T) = 1 - e^{-T/T_m} \qquad \text{where } T_m \text{ is the mean time to skip}$$

A.3.3 Effect of Signal Fades

With a PLL having the loop filter internal offset voltages cancelled and connected as a perfect integrator, when the input signal fades the loop VCO average frequency should not shift from its value at

signal fade. The second order loop is said to have frequency memory. If the signal has a frequency ramp (due to changing doppler etc.) of R rad/sec^2 and the fade lasts T seconds the signal-VCO frequency difference at return of the signal will be $\Delta\omega = RT$. If this frequency is less than about $2\zeta\omega_n$* then the PLL will reacquire the signal rapidly (possibly without skipping cycles) in a time of approximately $t = 5/\zeta\omega_n$† A third order loop has frequency rate memory which may be useful for longer signal fades.

A.3.4 Effect of Carrier Phase Noise

For proper operation of the PLL the PD error signal amplitude must be restricted. A satisfactory criterion might be ϕ_e (max) < 1 radian, or for gaussian signals $\sigma_e^2 < 0.25$. If the phase noise spectral density of the signal is given by $S_{\phi_i}(f)$ and the phase noise of the VCO is $S_{\phi_o}(f)$ then it can be shown the mean square phase error will be (Blanchard, 1976)

$$\sigma_e^2 = \int_{-\infty}^{\infty} [S_{\phi_i}(f) + S_{\phi_o}(f)] \left| 1 - H(j2\pi f) \right|^2 df$$

Since $|H(j2\pi f)|$, the PLL transfer function, is a low pass function, $|1-H(j\omega)|$ is a high pass function; then to a first approximation

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* Lock in range $\Delta\omega_L \simeq 2\zeta\omega_n$ rad/sec

† Pull in Time $T_p = \dfrac{(\Delta\omega)^3}{2\zeta\omega_n}$

$$\sigma_e^2 = 2 \int_{\frac{\omega_n}{2\pi}}^{B_{IF}/2} [S_{\phi i}(f) + S_{\phi o}(f)]\, df$$

[ω_n, the loop natural frequency, is the 1/2 power frequency of the function $|1-H(j\omega)|$ for $\zeta = .7071$]

This shows immediately that ω_n should be large to make σ_e^2 small.

A.3.5 Changing the Loop Bandwidth

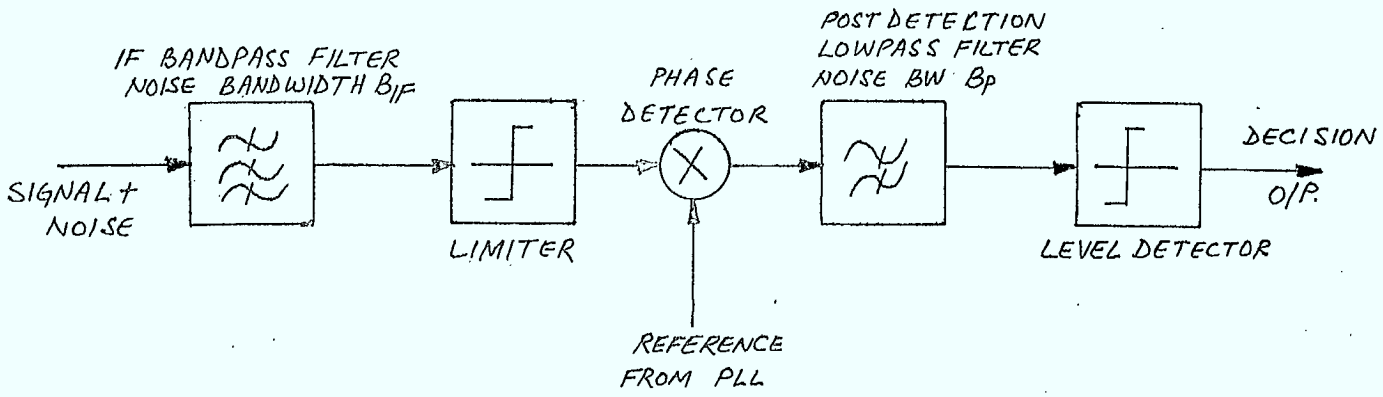
The optimum loop C/N for best acquisition occurs at a relatively low value and therefore to improve the tracking performance once lock is achieved, it will probably be necessary to reduce the PLL bandwidth.

A.3.6 Effect of Sweep Voltage on Loop Operation

The sweep voltage causes a large static phase error to appear between the VCO and signal. If a coherent detector is used for lock detection (next section) then the phase shift caused by the sweep voltage will have to be bucked out. Also if the lock indication output is still required after initial lock detection and sweep removal the excess phase shift introduced for the coherent detector will have to be removed.

A.4 Coherent Lock Detection

Block diagram for coherent detection:



Assuming the filter used in the lock detector to be narrow band with respect to the PLL bandwidth, then the phase of the (noisy) sinusoidal input will equal the phase of the (noisy) sinusoidal reference provided by the PLL.

At the same time, the signal amplitude from the limiter is constant, so the output with signal present is noiseless in the band of the lock detector filter. However, there will be some loss of signal amplitude from the no noise input case, due to a compression effect caused by the IF noise. As the signal power is decreased below the

typical 26 dB-Hz level, the d.c. level in the lock detector filter will fall from its value of $\frac{1}{2}$, but not rapidly. (The modifying factor is α, as in Figure 1). An additional small amplitude loss will be experienced due to the phase error in tracking.

When the loop is not locked, the noise output power is $\frac{1}{2}$, assuming unity amplitude levels, and is taken to be uniformly distributed over a frequency range $B_{IF}/2$, where B_{IF} is the double sided noise bandwidth of the IF filter. The spectral density is therefore equal to $\frac{1}{2}\left(\frac{2}{B_{IF}}\right)$. Taking the effective bandwidth of the integrating system to be small compared to B_{IF}, the noise power out of the integrator is

$$\overline{n^2} = \int \phi_I(\tau)\ \phi_n(\tau)\ d\tau$$
$$= \frac{1}{2}\ \frac{1}{B_{IF}}\ \phi_I(o)$$

where $\phi_I(\tau)$ is the auto-correlation function of the integrator, so that

$$\phi_I(o) = T$$

then

$$\overline{n^2} = \frac{1}{2}\ \frac{1}{B_{IF}}\ T$$

and the signal output from the integrator at that same time when the loop is locked is $\frac{T}{2}$. Compared to this level the relative noise

variance is $\frac{2}{B_{IF}} \frac{1}{T}$, and if the threshold level is set at $\beta \tilde{>} 1$, the false alarm probability is

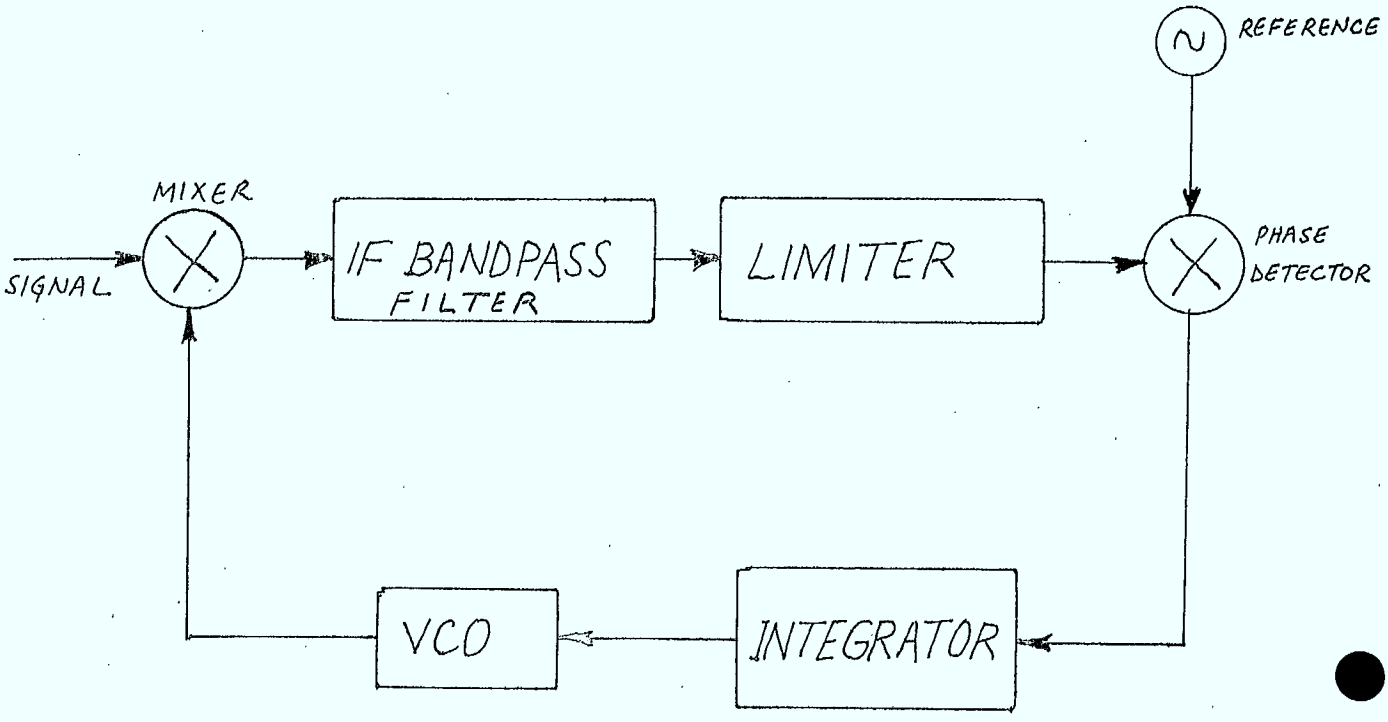
$$p = \frac{1}{2} \operatorname{erfc} \sqrt{\frac{B_{IF} T}{2}}$$

A.5 PLL Design

A.5.1 Configurations

a. Tracking filter PLL. Here the PLL is 'tacked on' at the output of the receiver IF. This is a simple minded approach to the use of the PLL having the advantage of simplicity only.

b. PLL with IF filter or heterodyne PLL



The advantages are

i The IF bandwidth can be much narrower than the input signal frequency uncertainty. This means the PD operates at a much better C/N than the tracking filter case.

ii During signal fades the VCO frequency stays put, while for the tracking filter connection the VCO drifts towards the center of the input noise band.

iii There is some flexibility in the choice of VCO and PD frequencies.

iv When the loop is locked the phase shift through the IF filter is constant and independent of the signal frequency. This point is mentioned for general information only.

Caution There are limits on the ratio B_{IF}/B_L and the number of equivalent resonators, N, in the IF filter due to stability reasons. Gardner gives a good discussion on these practical values which are approximately $B_{IF}/B_L > 4$ and $N < 3$. Most crystal filter units are not suitable for use in the above configuration as they contain typically 6 or more equivalent resonators.

A.5.2 The Phase Detector

Easily realizable PD's fall into 3 categories based on the characteristic shape.

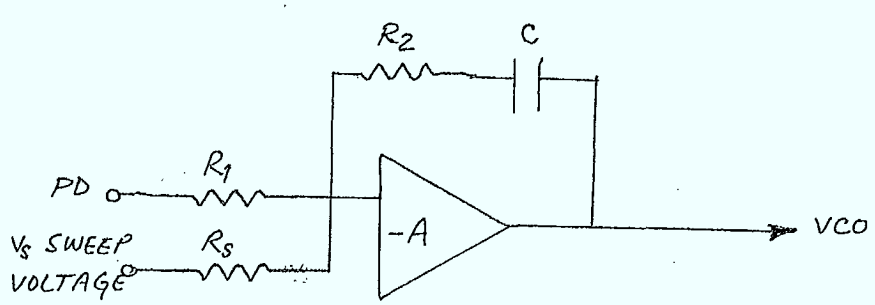
1. Sinusoidal. At low RF frequencies this may be the most difficult to realize, usually by transformers and diodes or active circuit analogue multiplier.

2. Triangular. This characteristic is generated by multiplying two square waves together i.e., simply an exclusive or logic function.

3. Sawtooth. An edge triggered set-ret flip-flop will generate this phase characteristic.

A.5.3 The Loop Filter and Sweep Circuitry

The best filter for a second order loop from a tracking and frequency memory viewpoint is the high gain integrator with high frequency break to set the damping ratio. The VCO ramp voltage for frequency sweep can also be generated by this integrator.



For most operational amplifiers $A > 10^5$ yielding an almost perfect second order integration loop,

Briefly the loop design equations are

$$R_1 = \frac{\alpha k_d k_o}{\omega_n^2 C} \quad , \quad R_2 = \frac{2\zeta}{\omega_n C} \quad , \quad R_s = \frac{k_o V_s}{\dot{\omega}_o C}$$

where

α = relative PD output signal (Figure 1)

k_d = PD no noise conversion gain (volts/rad.)

k_o = VCO gain (rad./sec./volt)

$\dot{\omega}_o$ = VCO output sweep rate (rad./sec^2)

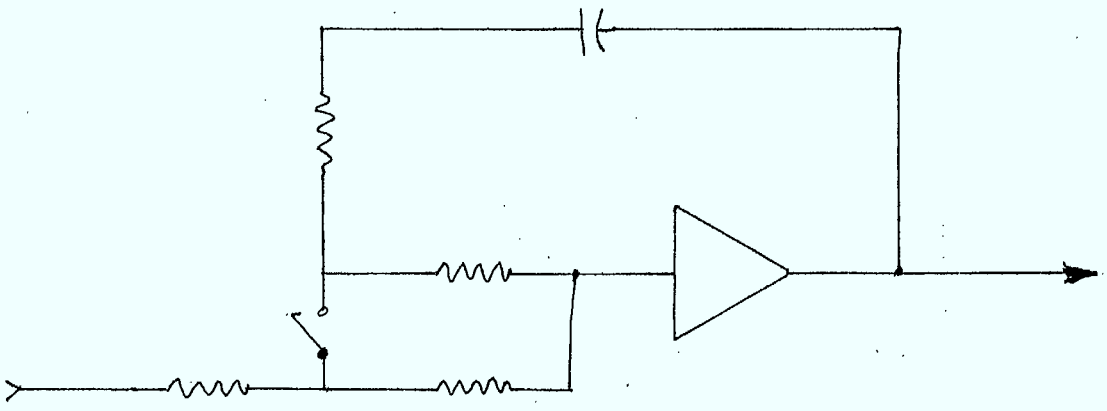
ζ = loop damping factor

ω_n = loop natural frequency

V_s = sweep voltage

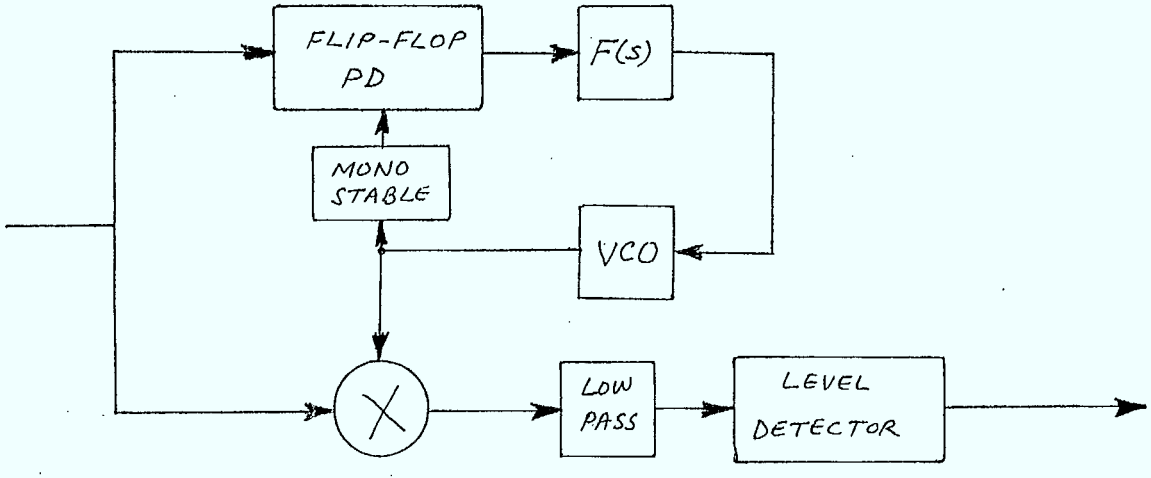
A.5.4 Changing the Loop Natural Frequency

Both R_1 and R_2 will have to be changed. Provided the loop integrator bias currents are insignificant (e.g. CMOS op-amp) then the following circuit will accomplish this



A.5.5 Phase Shift for the Coherent Detector

A sawtooth PD operates on positive transitions of the input waveforms, thus a phase involves only delaying the positive edges. This is easily accomplished by the use of a monostable. Phase shifters for triangular and sinusoidal PD's must preserve the waveshape and are therefore more complex.



A.5.6 Limiters

Use of triangular or sawtooth phase detectors automatically implies limiting to obtain the necessary waveforms for correct operation. The curves given for $(C/N_0)/(C/N_i)$ for these two PD's include the effect of limiting on the signal to noise ratio as this effect is not separable from the operation of the PD's.

For sinusoidal PD's the effect of limiting is to decrease C/N by a maximum of $\pi/4$ (-1.05 dB) and more typically by 0.95 to 0.86 (-.27 to -.66 dB)

If it is recognised that some form of amplitude control is required for the signal being applied to the PLL then there are three possible methods this may be accomplished.

1. Automatic Gain Control (on total of signal and noise applied to the PLL)
   - no signal to noise degradation
   - complex circuitry
   - slow acting (for stability reasons)

2. AGC derived from the coherent detector output
   - no signal suppression effects
   - complex

- non-operational till loop is locked
- total power applied to PD may vary over a wide range

3. Limiter
   - fast action
   - simple
   - high gain IC limiters readily available (e.g. CA3012)
   - slight C/N degradation.

A.5.7 Input Frequency Range

Factors

i Noise analysis of PLL assumes narrowband conditions i.e. $B_{IF}/f_{IF} << 1$. Measured and theoretical performance may diverge if B_{IF} is significant w.r.t. f_{IF}.

ii Range of the VCO frequency
RC oscillators - decade range
LC oscillators - octave range
XTAL oscillators - 0.5% range
Note that for the heterodyne loop the VCO frequency $\neq f_{IF}$.

iii Technology used to construct the IF bandpass filter. For example, if a 3rd order maximally flat filter of 1/2 power bandwidth = 500 Hz and f_o = 25 kHz is desired, the circuit Q's needed are

2 of 50 and 1 of 100 [Active filter gain bandwidth product needed is $f_o Q^2 = 250$ MHz],

iv Phase detector operating frequency. CMOS logic circuits have upper operating limit of approximately 250 kHz.

Taking the above factors into consideration there appears to be no objection to a PLL frequency of 25 to 40 kHz as is preferred.

A.5.8 Choice of VCO Type

The PLL cannot distinguish between $S_{\phi_i}(f)$ and $S_{\phi_o}(f)$, the VCO phase noise. Therefore care should be exercised in the choise of VCO type so that $S_{\phi_o}(f) << S_{\phi_i}(f)$. In general the order of VCO types from largest $S_{\phi_i}(f)$ are RC, LC and crystal oscillators.

A.6 REFERENCES

1. Frazier J.P. and Page J, "Phase Lock Loop Frequency Acquisition Study" IRE Trans. SET Sept. 1962, pp. 210-227.

2. Sweep Acquisition Study of PLL using Sinusoidal PD's and Limiters. There appears to be a mistake in the empirical sweep rate formula they give - mentioned by Gardner.

3. Gardner F.M. "Phase Lock Techniques" John Wiley & Son, 1966. A good basic PLL handbook. His treatment of limiters and signal suppression and signal to noise ratio after phase detection is a little misleading.

4. Gardner F.M. "Acquisition of Phase Lock" IEEE Communications Conference Philadelphia 1976. Some interesting comments on various acquisition techniques.

5. Blanchard A. "Phase Locked Loops" Wiley 1976. An excellent advanced level PLL handbook. A pity the graphs are not really suitable for design purposes.

6. Lindsey W.C. "Synchronization Systems in Communication and Control". This work is difficult to follow due to the use of obscure terminology and symbols

7. Wakeman P.E.D. "Sweep Frequency Acquisition Study" C.R.C. Report 1976, to be published.

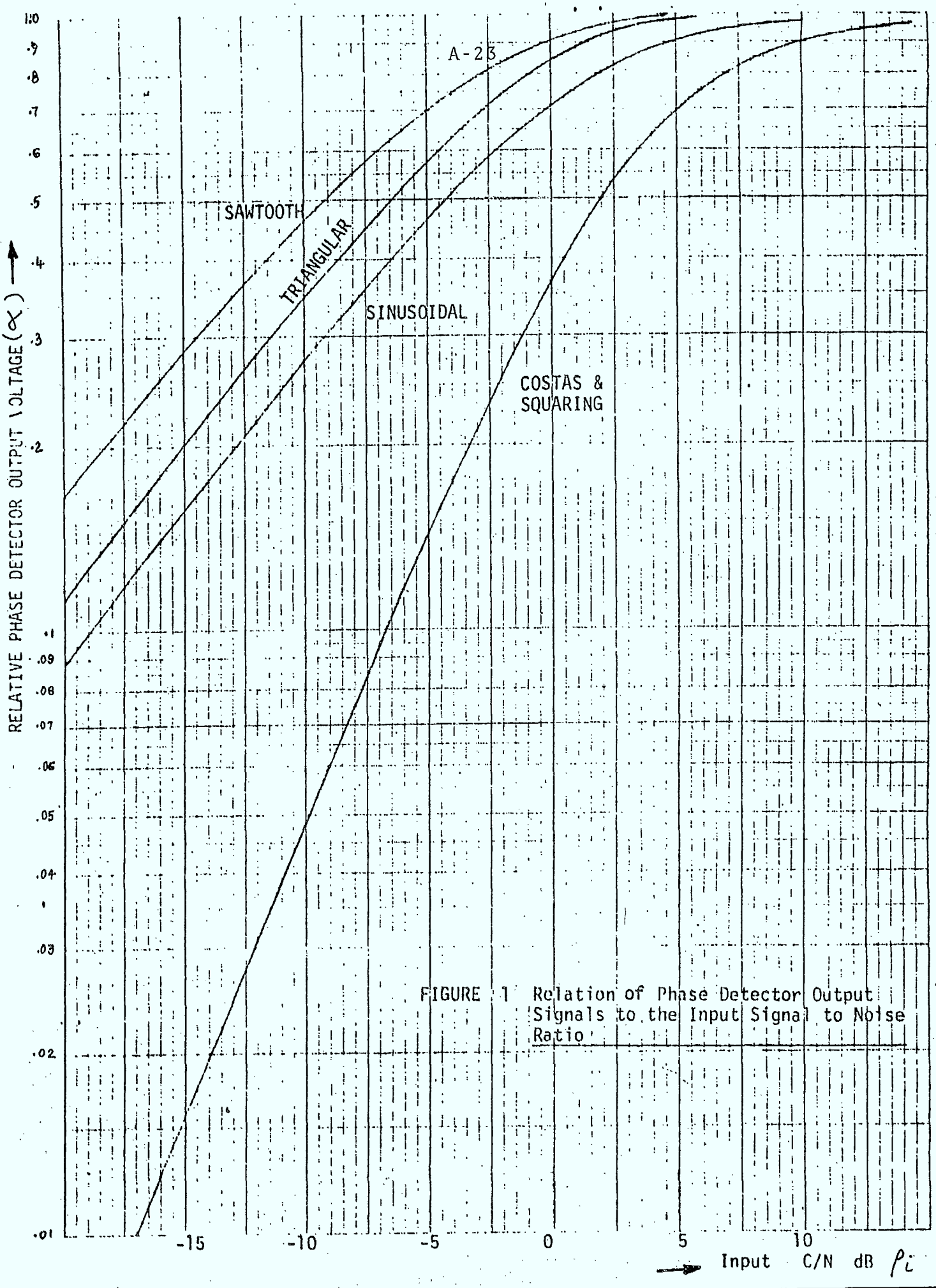
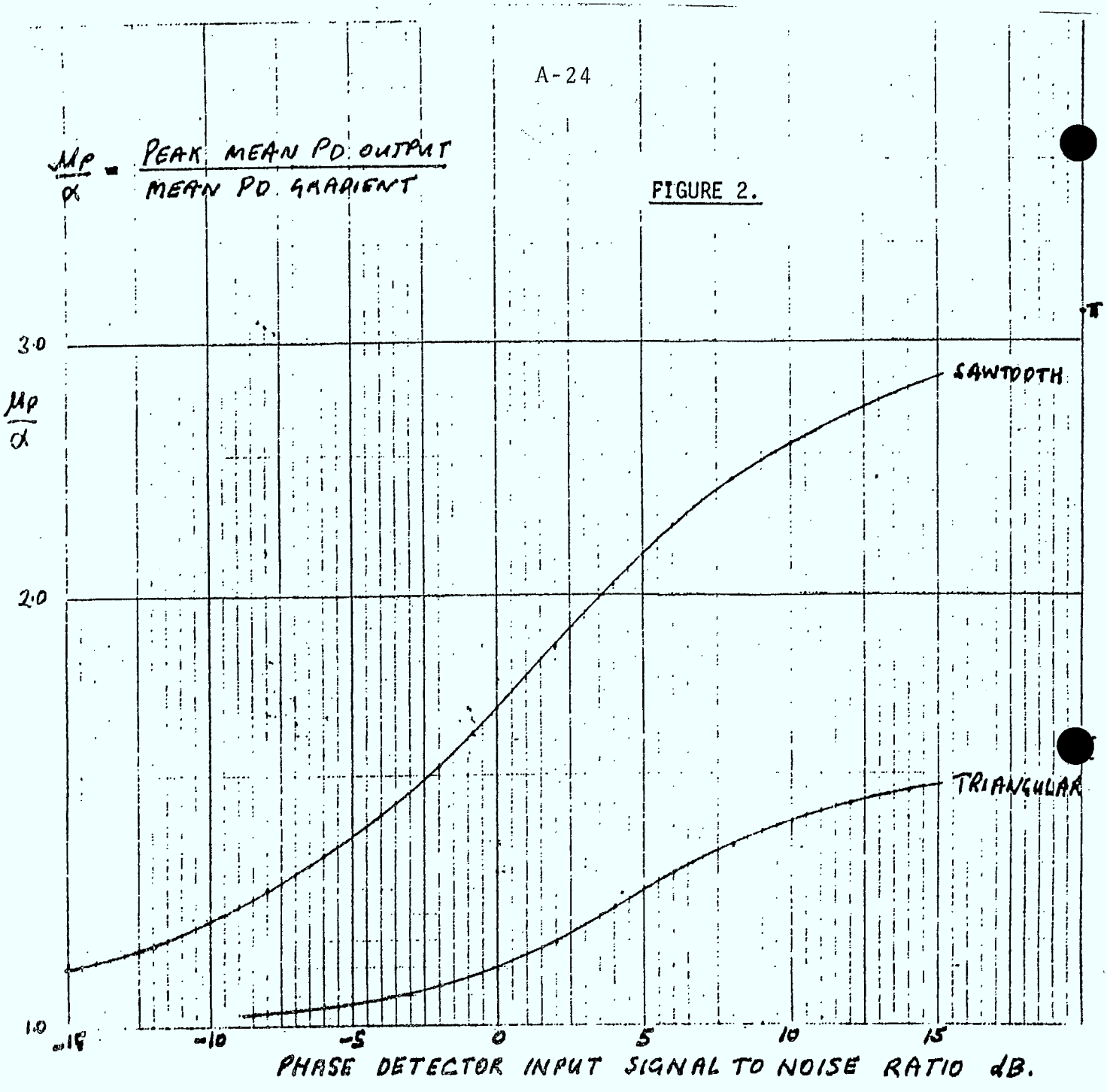


FIGURE 1 Relation of Phase Detector Output Signals to the Input Signal to Noise Ratio

$\frac{\mu_p}{\alpha}$ = PEAK MEAN PD OUTPUT / MEAN PD GRADIENT

FIGURE 2.



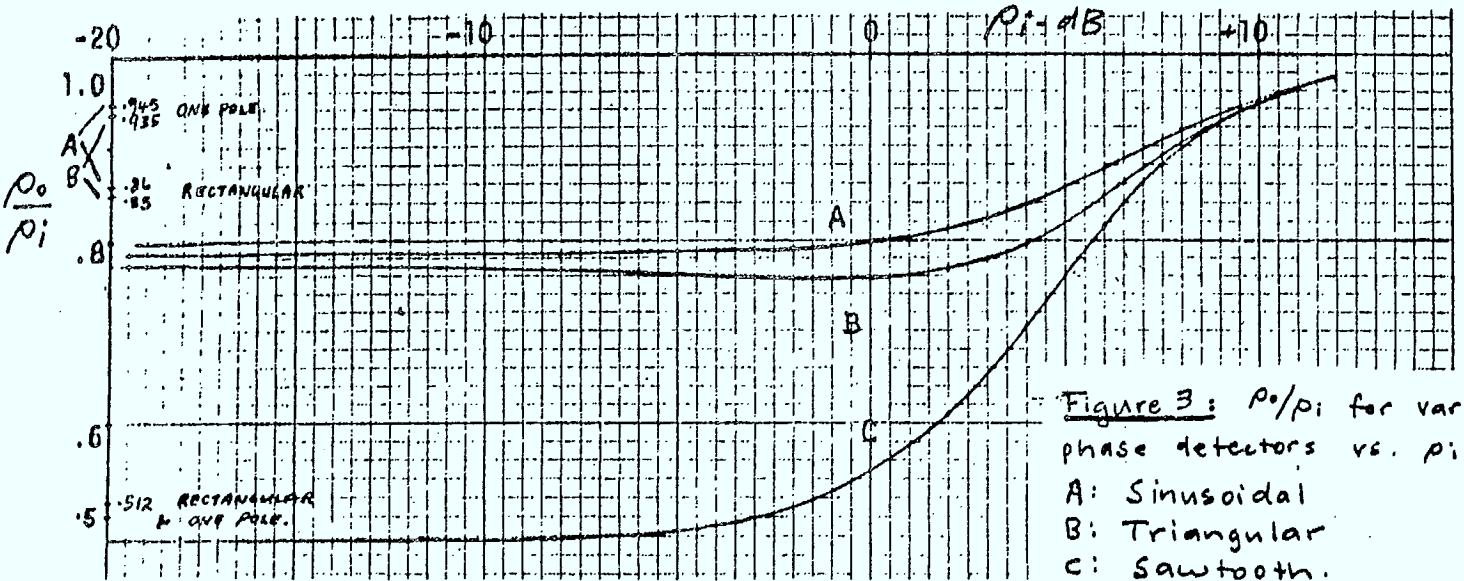
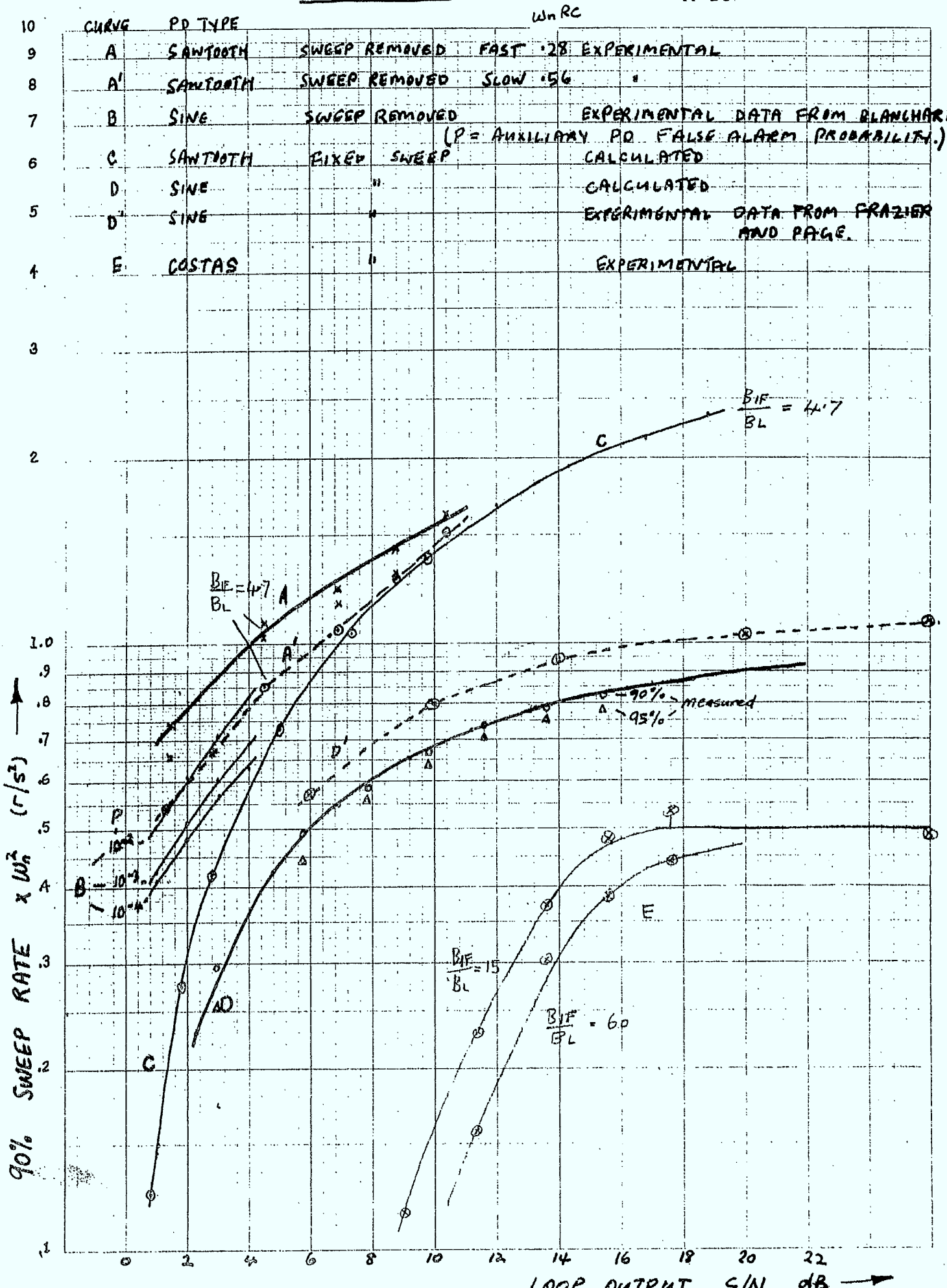


Figure 3: ρ_o/ρ_i for various phase detectors vs. ρ_i.

A: Sinusoidal
B: Triangular
C: Sawtooth.

FIGURE 4.


CURVE PD TYPE
A SAWTOOTH SWEEP REMOVED FAST .28 EXPERIMENTAL
A' SAWTOOTH SWEEP REMOVED SLOW .56 "
B SINE SWEEP REMOVED EXPERIMENTAL DATA FROM BLANCHARD
(P = AUXILIARY PD FALSE ALARM PROBABILITY.)
C SAWTOOTH FIXED SWEEP CALCULATED
D SINE " CALCULATED
D' SINE " EXPERIMENTAL DATA FROM FRAZIER AND PAGE.
E COSTAS " EXPERIMENTAL
ωn RC
90% SWEEP RATE x ωn² (r/s²)
LOOP OUTPUT C/N dB
BIF/BL = 4.7
BIF/BL = 15
BIF/BL = 6p
P
10⁻²
10⁻³
10⁻⁴
90% measured
95% measured
A
A'
B
C
D
D'
E

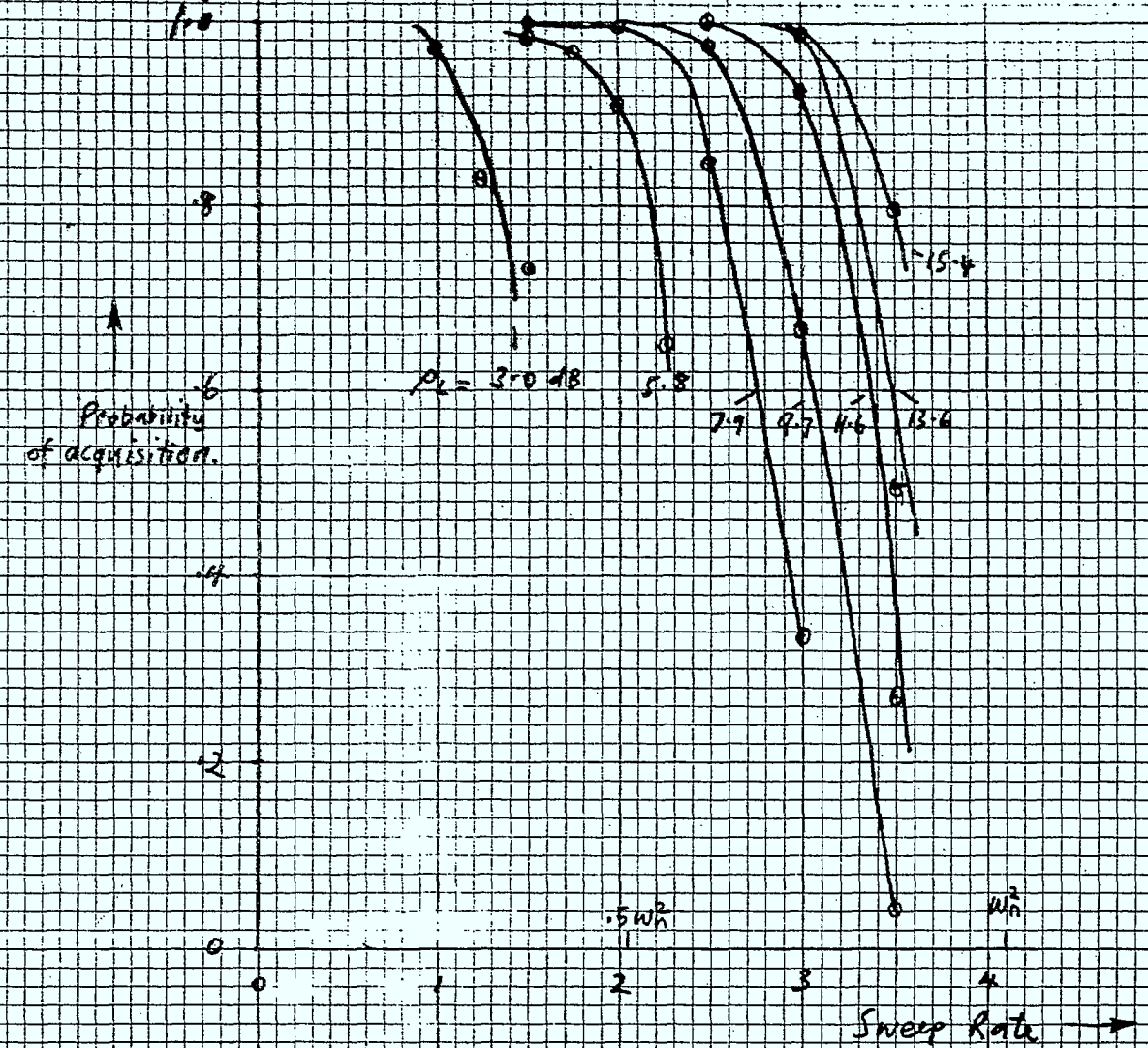


FIGURE 4.a

SINUSOIDAL PD

$\zeta = .7$

$\omega_n = 2\pi \times 200$ Hz

500 trials per point.

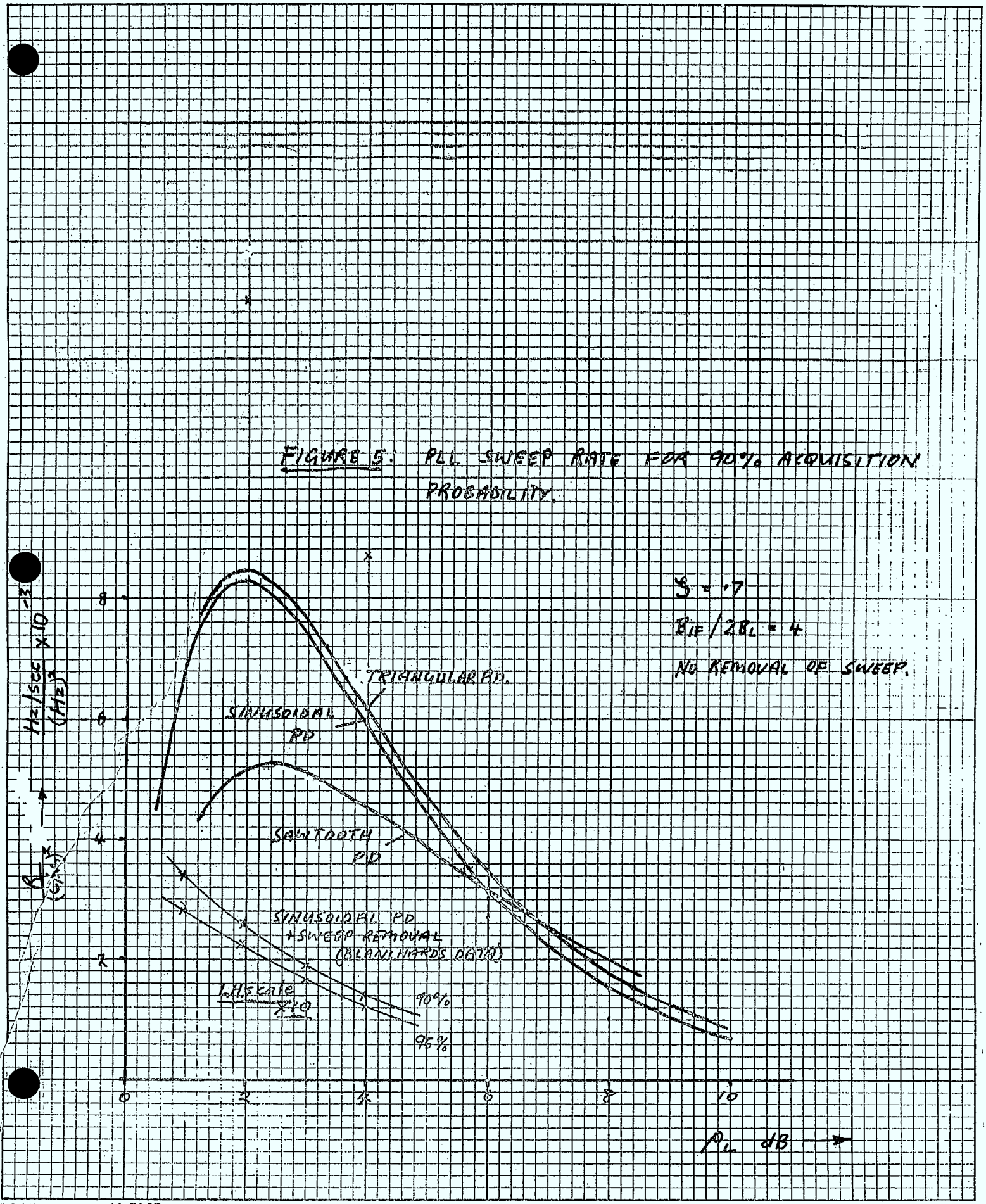


FIGURE 5: PLL SWEEP RATE FOR 90% ACQUISITION PROBABILITY.
ζ = .7
B_IF / 2B_L = 4
NO REMOVAL OF SWEEP.
TRIANGULAR PD.
SINUSOIDAL PD
SAWTOOTH PD
SINUSOIDAL PD + SWEEP REMOVAL (BLANCHARD DATA)
LHS CASE
90%
95%
Hz/sec x 10^-3
(Hz)^2
ρ_L dB
0
2
4
6
8
10

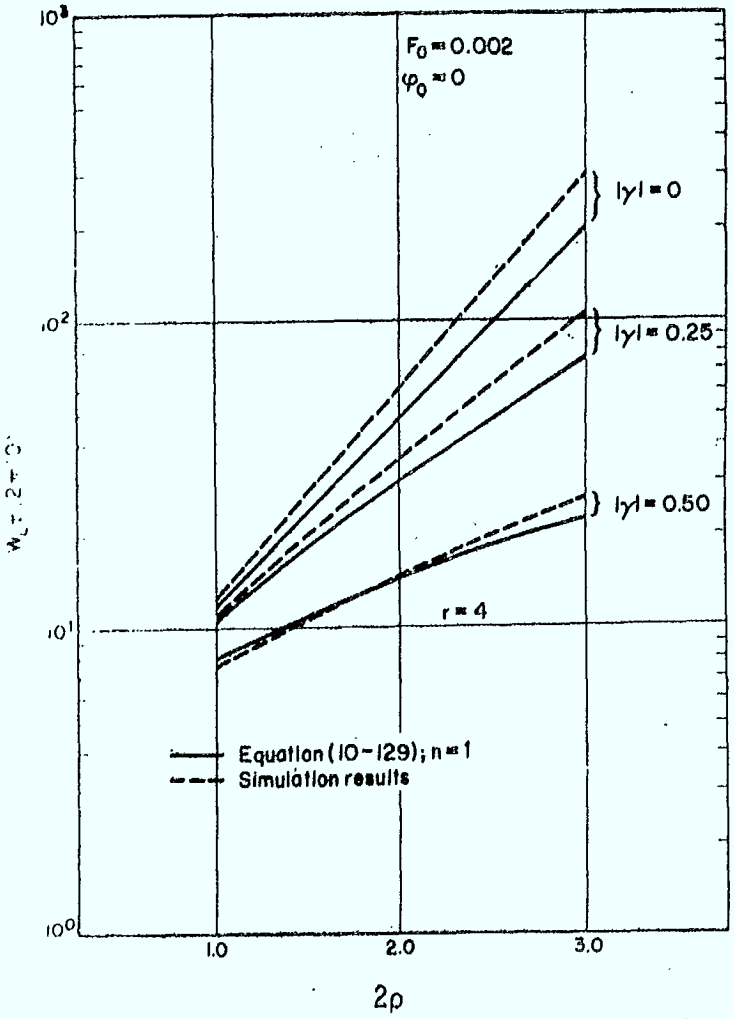


Fig. 6a Mean Time to First Slip versus ρ for Various Values of γ.

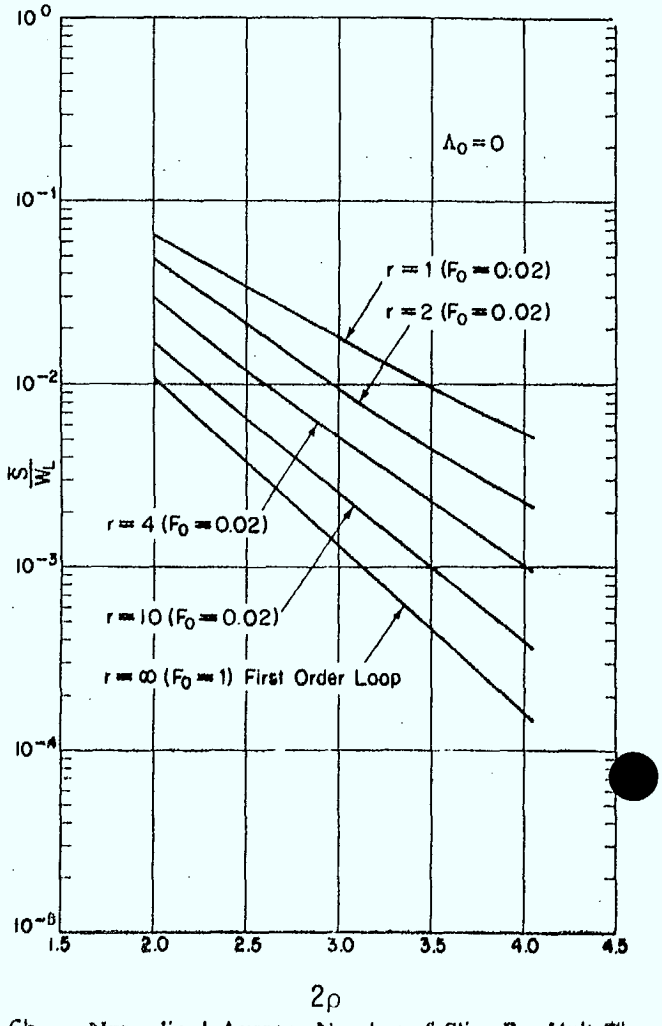
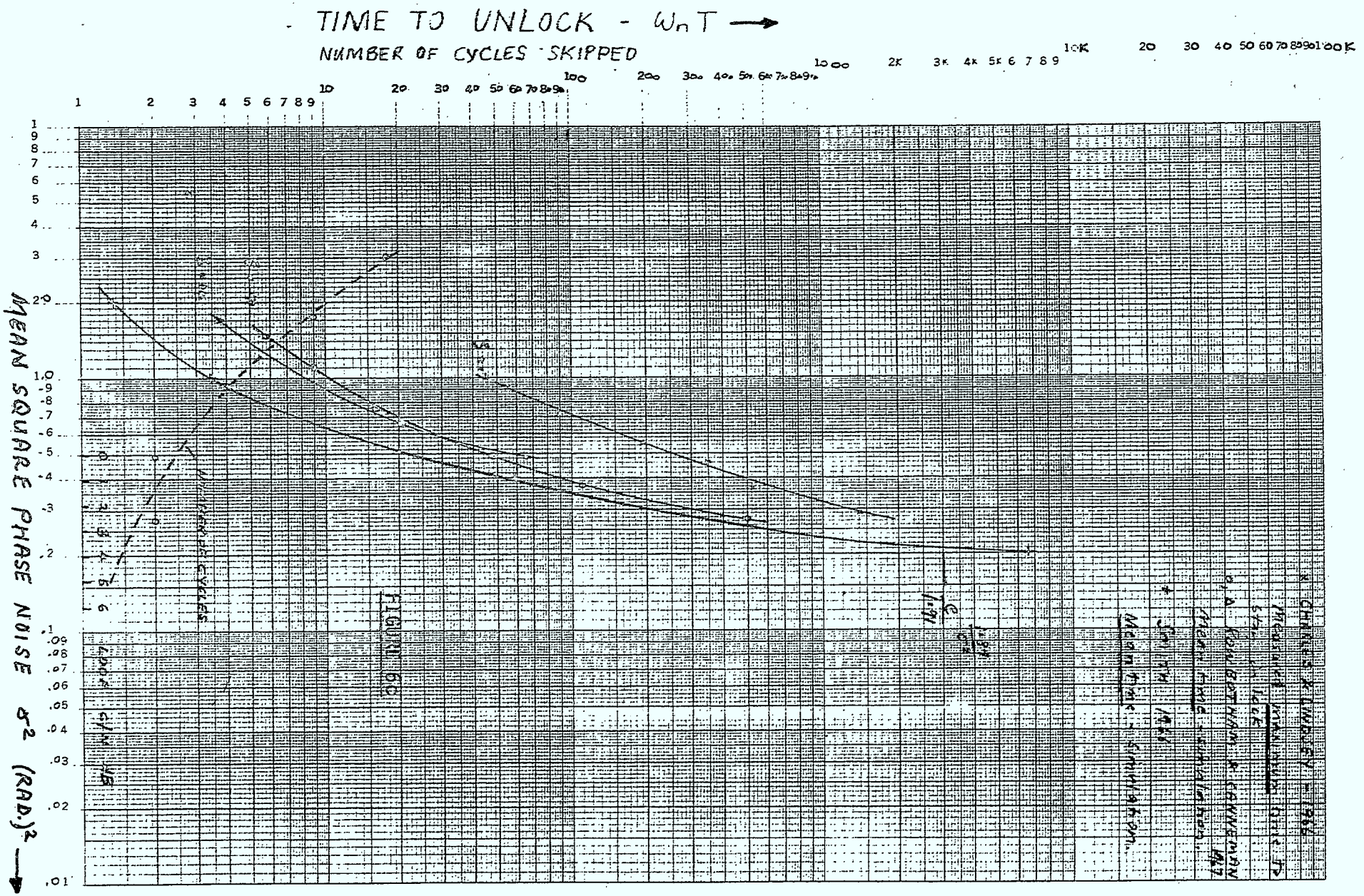


Fig. 6b Normalized Average Number of Slips Per Unit Time versus ρ for Various Values of r. (Courtesy of M. K. Simon)

$r = 4\zeta^2$ $\quad \sigma^2 = 1/2\rho$ $\quad \gamma = \Delta\omega / K_d K_0$


TIME TO UNLOCK - $\omega_n T$ →
NUMBER OF CYCLES SKIPPED
MEAN SQUARE PHASE NOISE σ^2 (RAD.)^2 →
FIGURE 6C

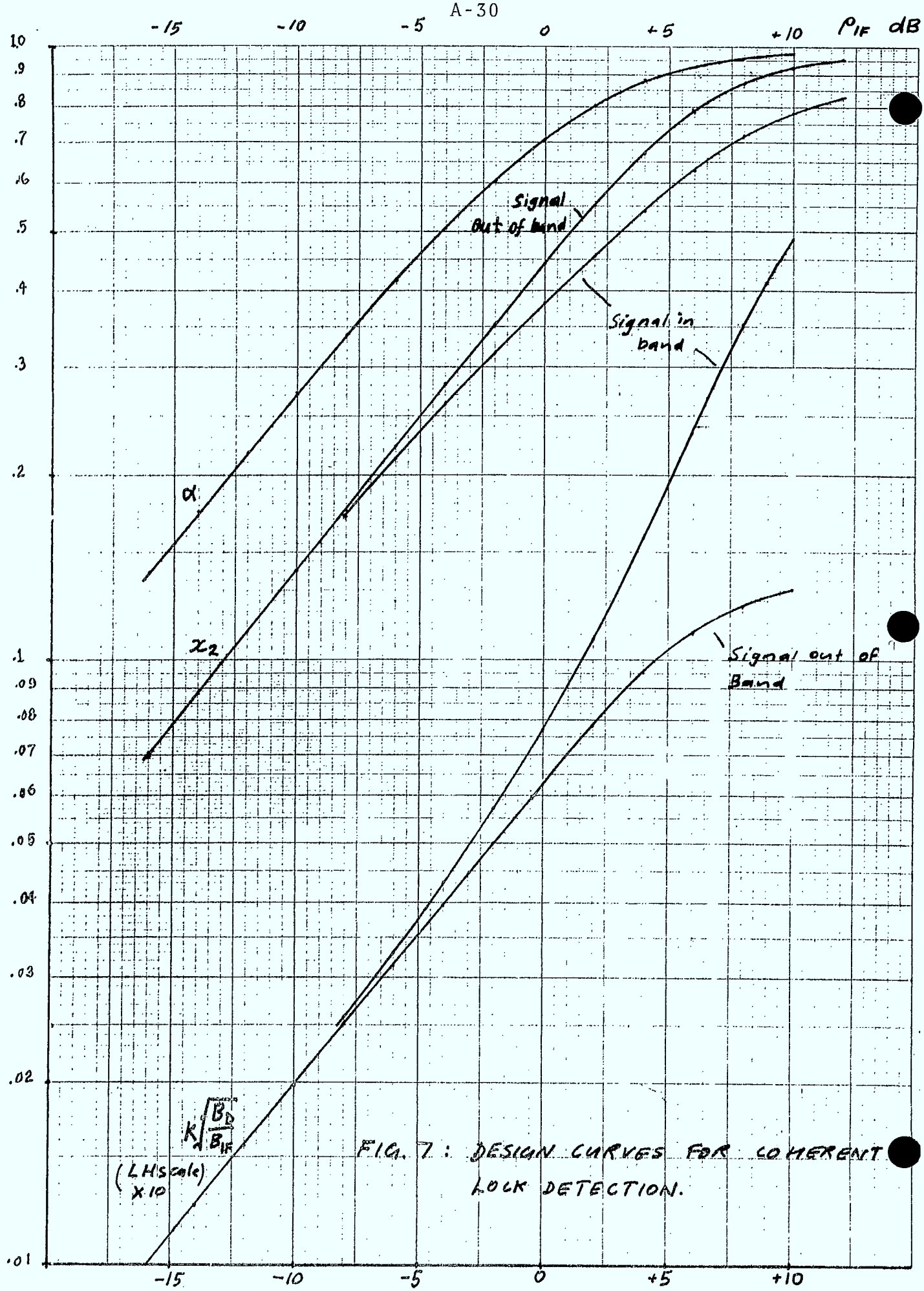


FIG. 7 : DESIGN CURVES FOR COHERENT LOCK DETECTION.

APPENDIX B

DIGITAL SIGNAL PROCESSING TECHNIQUES

ELT detection, tracking and frequency measurement can be performed using one or more of the following digital processing elements: Fast Fourier Transform (FFT), digital filter, and digital phase lock loop. These elements perform the same functions as their analog counterparts and exhibit similar performance characteristics; however, there are significant differences in implementation and additional sources of error due to the digitization of the signal. This memorandum reviews basic digital signal processing principles as a prelude to considering the application of digital processing in the Sarsat receiver.

B.1 The Discrete Fourier Transform (DFT)

The Fourier Series is used to determine the frequency content of a time varying signal. However, the Fourier series always requires a periodic time function. The Fourier Transform defined below overcomes this shortcoming

$$S(f) = \int_{-\infty}^{\infty} x(t)e^{-j2\pi ft}dt \qquad (1)$$

S(f) is called the Fourier Transform of x(t). It contains the amplitude and phase information at every frequency present in x(t) without demanding that x(t) be periodic.

In order to implement the Fourier Transform digitally, the continuous input signal is converted into a series of discrete data samples. The input waveform x(t) is sampled at Δt intervals of time. The sampling theorem states that these samples uniquely characterize the waveform providing

$$\Delta t \leq (2F_{max})^{-1}$$

where

$$S(f) = 0 \text{ for } f > F_{max}$$

The Fourier Transform can thus be calculated as follows:

$$S''(f) = \Delta t \sum_{n=-\infty}^{n=+\infty} x(n\Delta t) e^{-i2\pi fn\Delta t} \qquad (2)$$

where $x(n\Delta t)$ are exact measured values of input function. For non ideally band limited functions, the Fourier Transform calculated by equation (2) does not have the same magnitude and phase information as in equation (1). However, it approximately describes the spectrum of x(t) up to some maximum frequency

$$F_{max} = (2\Delta t)^{-1}$$

if energy beyond this frequency is small.

Practically speaking we cannot perform the summation in (2) up to infinity and therefore we truncate the equation and only observe the input signal from zero to T seconds. Then we have

$$\frac{T}{\Delta t} = N$$

where N is the number of samples, and T is the "time window".

As we no longer have an infinite number of time points, we cannot expect to calculate the magnitude and phase values at an infinite number of frequencies between zero Hz and F_{max}. Equivalently the truncated version of (2) does not produce a continuous spectrum. This is called the discrete finite transform (DFT) and is given below:

$$S'(m\Delta f) = \Delta t \sum_{n=0}^{n-1} x(n\Delta t) e^{-i2\pi m\Delta f n\Delta t} \qquad (3)$$

Note that for baseband sampling there are N points of a real valued function in the time series. However, to fully describe the spectrum of the signal both magnitude and phase (or real and imaginary components) must be calculated. As a result N points in the time domain define $\frac{N}{2}$ complex quantities in frequency domain and conversely. Alternatively, with bandpass sampling, N complex time samples, whose real and imaginary parts are quadrature components of a signal centred on f_c, generate N complex frequency samples from $f_c - F_{max}$ to $f_c + F_{max}$.

The quadrature samples are derived by mixing the incoming bandpass signal with $\cos(2\pi f_c t)$ and $\sin(2\pi f_c t)$ followed by low pass filtering and coherent sampling.

If F_{max} is the maximum frequency present in the spectrum, then

$$\frac{F_{max}}{N/2} = \Delta f$$

$$\text{or} \quad \Delta f = \frac{2F_{max}}{N}$$

where Δf is the separation of frequencies (referred to as resolution) in the frequency domain.

The value of the Fast Fourier Transform is in the reduction of computer time in evaluating the discrete Fourier Transform. An N-point transformation by the direct method requires a time proportional to N^2 where the FFT requires a time proportional to $N \log_2 N$. The approximate ratio of FFT to direct computing time is given by

$$\frac{N \log_2 N}{N^2} = \frac{\log_2 N}{N} = \frac{\gamma}{N}$$

where $N = 2^{\gamma}$.

For example, if $N=2^{10}$, the FFT requires less than 1/100 of the normal computing time.

B.2 DFT On Staggered Blocks

In staggered blocks two successive blocks A^{j-1} and A^{j} are said to be staggered of M elements, in the sense that the last N-M elements of A^{j-1} coincide with the first N-M elements of A^{j}. As an example we show the following eight element blocks staggered by two

$$\overbrace{\ldots, f_{2j-2}, f_{2j-1}, f_{2j}, \ldots\ldots, f_{2j+5}}^{A^{j-1}}, \underbrace{f_{2j+6}, f_{2j+7}}_{A^{j}}$$

Three procedures will be examined for solving the DFT problem. The first procedure is based on a kind of relation that can be established between A^{j} and A^{j-1}. This relation is obtained by observing that if the first M elements of the previous block A^{j-1} are removed and substituted by the last M elements of A^{j}, we obtain a new block representing a right circular shift of M positions.

A new DFT is therefore obtained in a recursive way, by modifying the old DFT by means of proper transforms on that data for which the two successive blocks differ.

In the other two procedures, the two dimensional in time decomposition rule is used with proper dimensions, so that successive blocks

staggered of M elements are fractured into successive matrices in which corresponding columns are successive blocks staggered of one element. In the second procedure, the DFT on a column of a matrix is obtained in a recursive way, by properly modifying the DFT on a corresponding column of the previous matrix. In the third procedure, the matrix column is obtained in non-recursive way by using the DFT's on proper subsets of the corresponding column of some preceding matrices.

The memory requirements of the first two procedures is the same, the third procedure needs more memory. The third procedure being non-recursive is also more accurate.

The three procedures can be implemented in the three structures which work on the hypothesis that:

1. samples arrive sequencially at uniformly spaced instants of time and

2. every time a new sample arrives each computational element (multiplier, adder) performs an operation (multiplication, addition).

As a DFT on N elements must be computed every M time intervals, a structure generates L=N/M DFT coefficients every step. From this it follows that two quantities X^j and $X^{j-\alpha}$, that represent the same

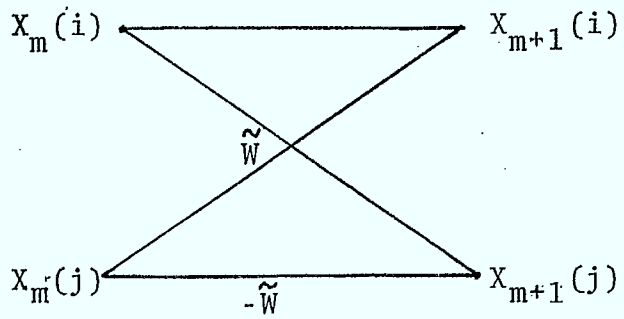
entity relative to the processing of two blocks A^j and $A^{j-\alpha}$, are spaced of αM time interval.

The three structures execute in real time the DFT on successive blocks of N elements staggered of M. Structure I and Structure II are both recursive although Structure I requires more multipliers and memory elements than Structure II. On the other hand, to implement Procedure III, we need more multipliers, less adders and memory elements. However, Structure III being non-recursive, gives more accurate results.

When samples are digitized to a finite word length, the quantized signal and the original signal differ from one another in a random manner. This difference or error may be viewed as noise due to the quantization process and is called quantization error. The magnitude and characteristics of these errors must be known if an FFT is to be designed with the minimum word lengths needed for acceptable performance.

The Fast Fourier Transform itself introduces further error due to round off in arithmetic.

Consider the FFT butterfly* shown below.



This can be specified in terms of previous definition e.g, going from mth to m+1 iteration of the data is computed as follows:

$$X_{m+1}(i) = X_m(i) + \tilde{W}\, X_m(j)$$

$$X_{m+1}(j) = X_m(i) - \tilde{W}\, X_m(j) \qquad (1)$$

where $X_m(i)$ and $X_m(j)$ represent a pair of numbers in mth array, and $\tilde{W}$ is some integer power of W, i.e.,

$$\tilde{W} = W^m = e^{-j2\pi m/N}$$

An error due to the rounding or truncation of the arithematic results will be introduced by each multiplication and addition in (1).

---

* Flow graph representation of sequence of parallel computations required on input data to complete an $N=2^{\gamma}$ point FFT.

Also, in general, the FFT butterfly operation is performed with rounded coefficients W^m rather than the exact FFT coefficient W^m; such errors are called FFT coefficient quantization errors. These are discussed in more detail later.

B.3 Low Pass DGTL Filters with Decimation

The process of sampling rate reduction is called decimation, Sampling rate conversion between any rational ratio of sampling frequencies can be efficiently implemented by a two stage process consisting of an integer sampling rate increase followed by an integer sampling rate decrease. That is, if a sampling rate conversion by a ratio L/M (where L and M are integers) is desired we can achieve this by first interpolating (sampling rate increase) by L and then decimating by M. However, to retain the desired frequency band in the final output, interpolation must precede decimation.

For implementing sampling rate change in the SARSAT signal, the choice of a low pass filter is extremely important. A finite impulse response (FIR) filter saves significantly in computations. The filter output v(n) is computed from the input w(n) by relation

$$v(n) = \sum_{m=1}^{N-1} h(m)\, w(n-m)$$

where h(m), m = 0,1,2,...,N-1, are filter coefficients and N is the duration of the unit sample response of the filter. The output in this relation depends only upon past and present values of w(n) and not upon past values of any internal filter variables. This is why FIR design is best suited as a low pass filter.

For large changes in sampling rate, however, it is generally more efficient to reduce the sampling rate with a series of decimation stages rather than making the entire rate reduction with one stage. In this way the sampling rate is reduced gradually resulting in much less severe filtering requirements on the low pass filters at each stage. Sampling rate can be reduced by any chosen ratio.

The overall sampling rate reduction is given by

$$D = f_{ro}/f_{rk}$$

$$= \prod_{i=1}^{k} D_i$$

where D_i = reduction at each stage

f_{ro} = initial sampling rate

f_{rk} = final sampling rate

From the sampling theorem, the highest frequency f_p in v(n) must satisfy

$$f_p \leq f_s = \frac{f_{rk}}{2}$$

However, due to filter realization constraints, the usable portion of the baseband will always be somewhat less than f_s. Each filter

should be reasonably flat over the desired passband (0 to f_p) in order to avoid distortions - in our case of "meandoring" sinusoids, amplitude ripple only alters relative signal levels and need not be severely constrained.

To ensure a cost-effective LPF design, appropriate constraints are imposed. A passband ripple constraint for each stage should be within $1+\delta_{pi}$ where $\delta_{pi} = \delta_p/k$.

δ_p = is the ripple tolerance of the incoming signal.

In the stopband ($f_p > f_s$) a rolloff constraint must be imposed on each of the individual low pass filters in order to suppress the effect of aliasing. Also to assure that no high frequency components are aliased into the baseband at stage i, the stopband cutoff frequency of low pass filter i can be chosen to be $f_{ri}-f_s$. At stage k, the final stage, it can be seen that this cutoff frequency is then equal to f_s as desired since $f_{rk}=2f_s$.

The SARSAT signal can also be processed by using a single very narrow band lowpass PLL loop filter. The following advantages can be realized using cascaded stages and decimation.

1. reduced multiplication rate

2. lower order filters required in implementing the design (for two or more stages)

3. linear phase

4. lower roundoff noise (for two or more stages of lower order filters)

5. lower coefficient sensitivity (for two or more stages)

It can also be realized that the lower the order, the lower the roundoff noise and coefficient sensitivity. However, unlike FIR, a narrow band LPF is not strictly time or shift invariant. But if aliasing can be neglected, then the system is effectively a linear phase, linear, time invariant system.

Time delay may or may not be of importance. In digital filtering it occurs in two locations. A/D conversion is not instantaneous and time taken depends on method of A/D taken. However it can be a source of significant delay. Digital computation time is the other source of delay. This depends on method employed and accuracy desired, as determined by no. of bits in each digital word.

Also the representation of pulses by a digital word with finite number of bits results in amplitude error. In A/D converters this is known as quantization error. It appears as a noise term added to the input of the digital filter. Errors which occur in the digital calculation due to finite word length are called round off errors. The effect of these errors is to introduce a noise term to the output signal which may increase with time in a recursive filter. Additional errors due to finite word length occur in the coefficients of the transfer function.

In case it is not possible to sample at the rated capability of digital filter, the filter can be time shared. One of the major advantages of digital filters is the flexibility with which the filter characteristics can be changed merely by changing the values of the stored filter coefficients. Also filter accuracy can be improved by merely extending bit lengths.

B.4 Digital Phase Lock Loops with Decimation

Generally a digital phase lock loop (DPLL) consists of sampling the received signal, quantizing these samples as binary words, and performing a set of digital computations on these words to estimate the phase of the received signal. A digital processor performs functions analogous to the phase detector, filter and VCO of an analog phase lock loop (APLL). As in the case of the FFT either low pass (real samples at rate twice the highest signal frequency) or bandpass (complex quadrature signal samples at rate equal to signal bandwidth) sampling may be employed, followed by real or complex arithmetic operations as appropriate.

The major advantage of a DPLL is a consequence of sampling being independent of the subsequent digital processing. The samples contain all the phase information of the received signal and can be stored. The parameters of the DPLL can easily be modified by simple selection of arithmetic constraints - this facilitates adaptive operation or optimization of the design. For example, the loop bandwidth can be narrowed following ELT detection in order to accurately estimate frequency.

The DPLL has two parts, the sampling circuit and the digital processor. For bandpass sampling, the sampling circuit obtains a sample pair relative to the local oscillator phase. The received signal is mixed with sin and cos components of the local oscillator, low

pass filtered, and A/D converted. The complex (I,Q) channel sample pairs are then fed to the digital processor. The general mathematical operation performed is by a digital filter in a feedback form. The input noisy phase samples are filtered to obtain phase estimates $\hat{\theta}$ of the ELT signal which is being tracked. This is achieved in a manner analogous to the analog PLL:

1. digital low pass filter with complex input/output

2. limiting, which is equivalent to retaining most significant bit only

3. integration, which is equivalent to summation, estimates $\hat{\theta}$

4. input complex samples multiplied by exp $(j(\hat{\theta}+\pi/2))$.

The last operation involves the accurate and rapid computation of sines and cosines, a simple function in the analog comain but difficult in the digital domain. In the search mode, the DPLL can be swept by varying the frequency of the local oscillator used to derive the I and Q channels, or, preferably, by superimposing $\alpha_i = 2\pi i^2(\frac{R}{2}\Delta t)$, i=1,2,....N (R = sweep rate), on $\hat{\theta}$; detection is achieved by multiplying the input samples by exp $(j(\hat{\theta}+\alpha_i))$, digital LPF and comparing the received word with a fixed threshold.

Thermal noise and truncation noise are present in DPLL. Thermal noise is approximately independent from sample to sample. The noise at the output of the phase detector can be considered as the input of the noise to the PLL and it can be characterized as independent zero mean noise.

5 Quantization Effects in FFTS and Digital Filters

When digital signal processing operations are implemented on a computer or special purpose hardware, errors and constraints due to finite word length are unavoidable. The main categories are errors due to A/D conversion, errors to roundoff in arithmetic, constraints on signal levels imposed by the need to prevent overflow, and quantization of system coefficients.

The effect of the finite word-length constraint manifests itself in several different ways. Finite word length requires that A/D conversion of the sampled waveform can produce only a finite number of values. The effect of the resulting quantization noise depends on the dynamic range of the incoming signal, the number of bits of quantization, and the desired signal bandwidth-to-sampling bandwidth. Accuract detection of a narrow band carrier in a high noise environment, as in our case, does not require fine quantization due to dithering or linearizing effect of the noise. The effect of finite word length also depends on factors such as fixed point or floating point number representation (the latter accomodates a much greater dynamic range, the former retains a fixed precision) and whether, for fixed point arithmetic, numbers were represented as fraction, integers or a mixture.

In fixed point arithmetic, a register represents a fixed point fraction. When two numbers are multiplied, the register length is maintained

by truncating or rounding off the least significant bits. While addition, truncation or roundoff is not required. Though adding may only cause overflow multiplication causes both underflow and overflow. In floating point arithmetic, dynamic range considerations are neglected due to the large range of representable numbers, but quantization is introduced for multiplication and for addition.

Inaccuracies in parameter values can be avoided by developing designs that are insensitive to parameter accuracies or specified so that they are consistent with limited register length.

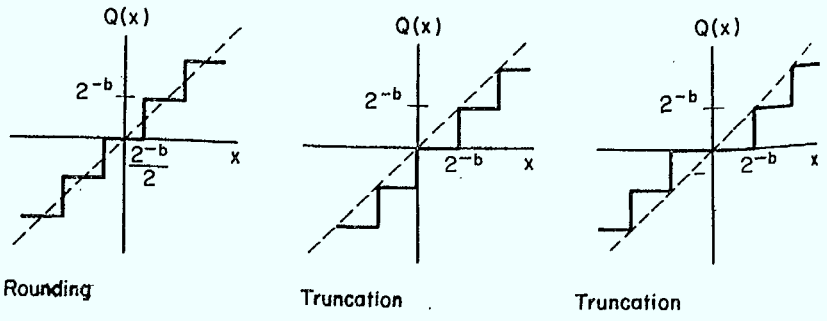
In a digital hardware system numbers are represented by a sequence of bits (0 and 1). Fractions or decimal points are also represented in binary digits with a binary point dividing the integer part and the fraction part. Thus if Δ denotes the location of the binary point, then a positive number can be represented as $1001_{\Delta}0110$ in bits having the decimal value $(1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0) + (0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4})$.

In a digital computer it is important to know the location of the binary point in the register. In fixed point arithmetic, the location is fixed. Additions will not depend on the location of binary point although for multiplication the location of binary point must be known. In general the product of two b-bit numbers will be 2 b bit long. In digital applications, the result of fraction multiplication is made to be b-bit long by truncating or rounding to the most significant bits. For example, $_{\Delta}00011010$ can be approximated by $_{\Delta}0001$ (truncation) or $_{\Delta}0010$ (rounding). This is not possible for integer multiplication.

In floating point representation a positive number F is represented as $F = 2^{c}M$ where M, the mantissa, is a fraction between 1/2 and 1, and e, the characteristic, can be either positive or negative. The product of floating point numbers is carried out by multiplying the mantissa as fixed point fractions and adding the characteristics. Since the product of mantissas will be between 1/4 and 1, a normalization of the mantissa and corresponding adjustment of the charactoristic may be necessary. The sum of two floating point numbers is carried out by scaling the mantissa as of the smaller number to the right until the charactoristics of the two numbers are equal and then adding the mantissas. Thus in general with floating point arithmetic, the mantissas can exceed the register length and must therefore be truncated or rounded for both addition and multiplication whereas this was only necessary for multiplication in the fixed point case. On the other hand even though floating point introduces error due to arithmetic round off, it provides much greater dynamic range than fixed point as a fixed point would overflow the register regardless of truncation or roundoff

Negative numbers are represented three ways. Firstly the leading binary digit represents 0 for positive and 1 for negative numbers (or vice versa). Two other methods are one's complement and two's complement. In two's complement a negative number is represented by 2.0 minus its magnitude. For one's complement, the negative number is represented by subtracting the magnitude from the largest number represented in the register.

It is found that in a fixed point case, the value after truncation minus the value before truncation is always negative for positive numbers, However, the magnitude of negative numbers increases or decreases after truncation for two's complement or one's complement respectively. The effect of rounding is same and is independent of how negative numbers are represented. The figures below show the characteristics for rounding and truncation.



In case of floating point, the error reflects only in the characteristic and is multiplicative rather than additive as in the case of fixed point cases.

B.5.1 Effects in Digital Filters

In digital filters represented by a difference equation of the form $y_n = \alpha y_{n-1} + xn$ the mathematics involved is multiplication by a constant and addition. For fixed-point arithmetic, roundoff is introduced only after multiplication. Because of possibility of overflow due to addition, there is a range limitation in fixed point filters. In contrast, floating point filter implementation has a much less severe dynamic range constraint, although arithmetic roundoff is introduced due to both multiplication and addition.

It is observed by introducing a uniformly distributed white noise source at filter input that the noise to signal ratio is proportional to $2^{-2b}/\delta$. Thus if δ is halved, then to maintain noise to signal ratio b must be increased by 1, i.e., one bit must be added to the register length. As δ approaches zero the frequency response of both first and second - order filter becomes more selective so that more and more of the input energy is out of band. For fixed point filters, it is found that the output noise is independent of the form and amplitude of the input signal. The above conclusions are drawn on the basis that overflow must be avoided.

The quantization noise to signal ratio is slightly larger in the floating-point arithmetic as compared with fixed-poing arithmetic with a sinusoidal input of known frequency, but a significantly smaller for floating point arithmetic as compared with a fixed point

arithmetic with a white noise input (due to its larger peak-to-rms ratio). Also if we decrease the signal level, the NSR will increase in the fixed point filter since the output noise variance is independent of input signal level. For floating point arithmetic, on the other hand, the output noise variance is proportional to the output signal variance and as the input level is scaled up or down so is the roundoff noise. However, we must also realize that implementing a floating point filter is much more complex than a fixed point filter.

A compromise in complexity is by using block floating point arithmetic. Here the input and filter states (i.e. input to delay registers) are jointly normalized before the multiplications and additions are performed in fixed point arithmetic. The scale factor (or exponent) obtained during the normalization is then applied to the final output to obtain a fixed point output. The NSR in such a case was found to lie between that for fixed and floating point.

B.5.2 Effects in the FFT

As shown in equation (1) before, the computation is the FFT algorithm, referred to as a "butterfly" in

$$X_{m+1}(i) = X_m(i) + \tilde{W}X_m(j)$$

$$X_{m+1}(j) = X_m(i) - \tilde{W}X_m(j)$$

Where $X_m(i)$, $X_m(j)$ and $\tilde{W}$ are as before, For a decimation in frequency algorithm, the butterfly computation is

$$X_{m+1}(i) = X_m(i) + X_m(j)$$

$$X_{m+1}(j) = [X_m(i) - X_m(j)]\tilde{W}$$

The roundoff noise can be modelled by associating an independent white noise generator with each multiplier. It can then be evaluated that the variance of the output noise is proportional to N, the number of points transformed. The effect of doubling N, or adding another stage in the FFT is to double the output noise variance. The output noise is also white. In the FFT, the dominant factor causing the increase of NSR with N is the decrease in signal level (required by the overflow constraint) as we pass from stage to stage. In the final array, very little noise, just a least significant bit or two is present. However, the mean squared signal level has decreased by a factor of 1/N from its initial value, due to scaling. The output consists of 1/N times the input DFT.

Another approach to avoiding overflow is the use of block floating point. Here the original array is normalized to the far left of the computer word, and the computation proceeds in a fixed point manner, except that after every addition there is an overflow test; if overflow test; if overflow is detected, the entire array is shifted right 1 bit and the computation continues. The number of necessary shifts

are counted to determine a scale factor or exponent for the entire final array. The output noise-to-signal ratio depends strongly on how many overflows occur, and at what stages of the FFT they occur. The positions and timing of overflows are determined by the signal being transformed, and thus, in order to analyze noise-to-signal ratio in block floating FFT, one needs to know the signal statistics. This is in contrast to the fixed point analysis above, where it was not necessary to assume specific signal statistics.

In Fig. 1 experimentally measured values of output noise-to-signal ratio are presented for block floating FFT's of white inputs using rounded arithmetic. The quantity plotted is the rms noise-to-signal ratio. For comparison, a theoretical curve representing fixed point noise-to-signal ratio (for rounded arithmetic) is also shown. We see that for white input block floating point provides some advantages over fixed point, especially for the larger transforms. For N=2048, the rms noise-to-signal ratio for block floating point is about 1/8 that of fixed point, representing a 3-bit improvement.

Noise-to-signal ratios are generally a bit or two worse by using truncation than for rounding. The rate of increase of noise-to-signal ratio with N seems to be about the same as for rounding.

In floating-point arithmetic noise is introduced due to each butterfly computation. Second-order error terms are neglected so that noise

sources are introduced after each multiplication and addition that are assumed to be white but for which the variance is proportional to the variance of the signal at that node. Here we consider a white input signal, where the signal at any array in the FFT is also white, with constant variance across the array.

The relation $(\sigma E^2/\sigma x^2\sigma\varepsilon^2)$ bits = 1/2 $\log_2$ (2v) is used to represent the number of bits by which the rms noise-to-signal ratio increases in passing through a floating point FFT. For example, for v=8 this represents 2 bits and for v=11 it represents 2.23 bits. The number of bits of rms noise-to-signal ratio increases as $\log_2$ ($\log_2$ N), so that doubling the number of points in the FFT produces a very mild increase in output noise, significantly less than the half-bit-per-stage increase for fixed-point computation. In fact, to obtain a half-bit increase in the result above, we would have to double v, or square N.

A consequence of the analysis is that the output noise is white. This follows from the fact that each array of noise sources is white. The reduced noise source variance for $\tilde{W}$=1 and j implies that for some arrays there will be a variation of noise source variance over the array. This implies a slight variation of output noise variance over the output array, and thus the modified noise analysis will only predict an average noise variance over the output array.

As with the implementation of digital filters, the implementation of the FFT algorithm requires the use of quantized coefficients.

Although the nature of coefficient quantization is inherently non-statistical. This statistical analysis corresponds to introducing random jitter in the coefficients and determining the output noise-to-signal ratio due to this noise. While the detailed effect due to coefficient error due to quantization is different than that due to jitter, it is expected that in a gross sense the magnitude of the errors is comparable.

The key result of quantization is that the error-to-signal ratio increases very mildly with N, being proportion to $v=\log_2 N$, so that doubling N produces only a slight increase in the error-to-signal ratio.

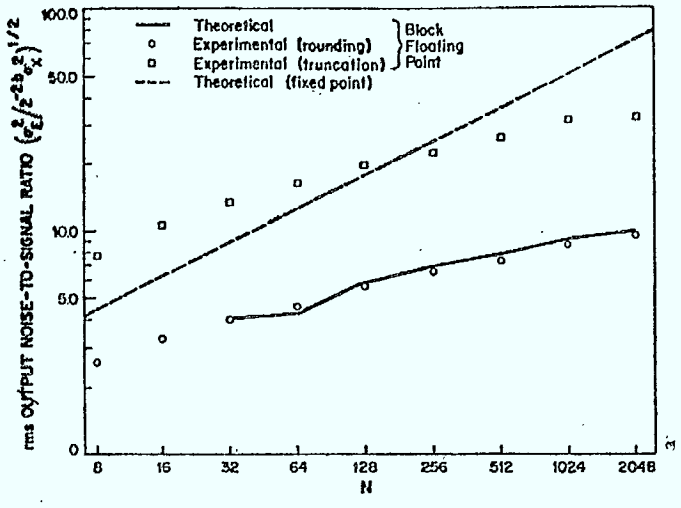


FIG 1 Experimental and theoretical noise-to-signal ratios for block floating-point FFT.

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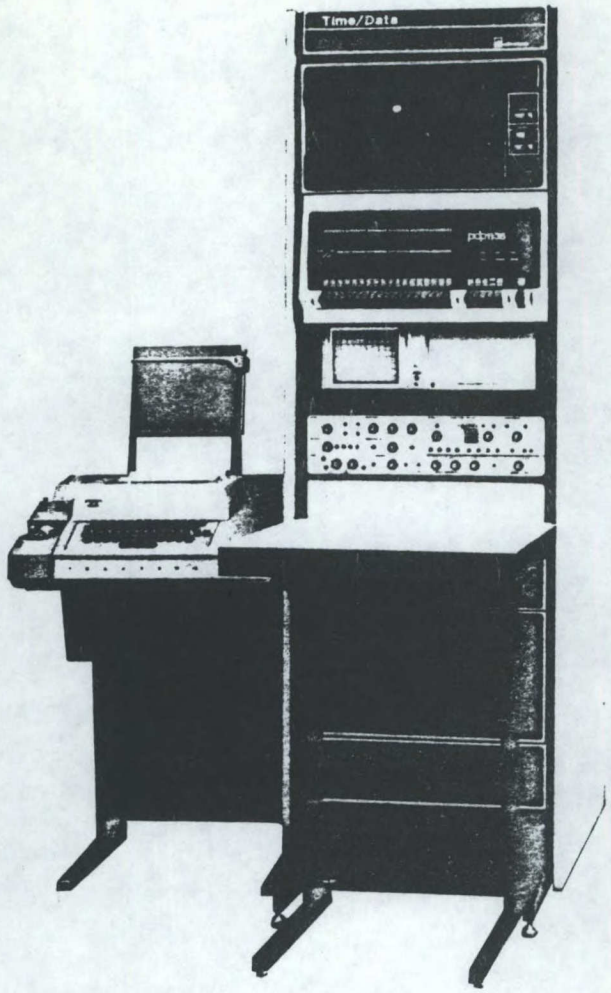

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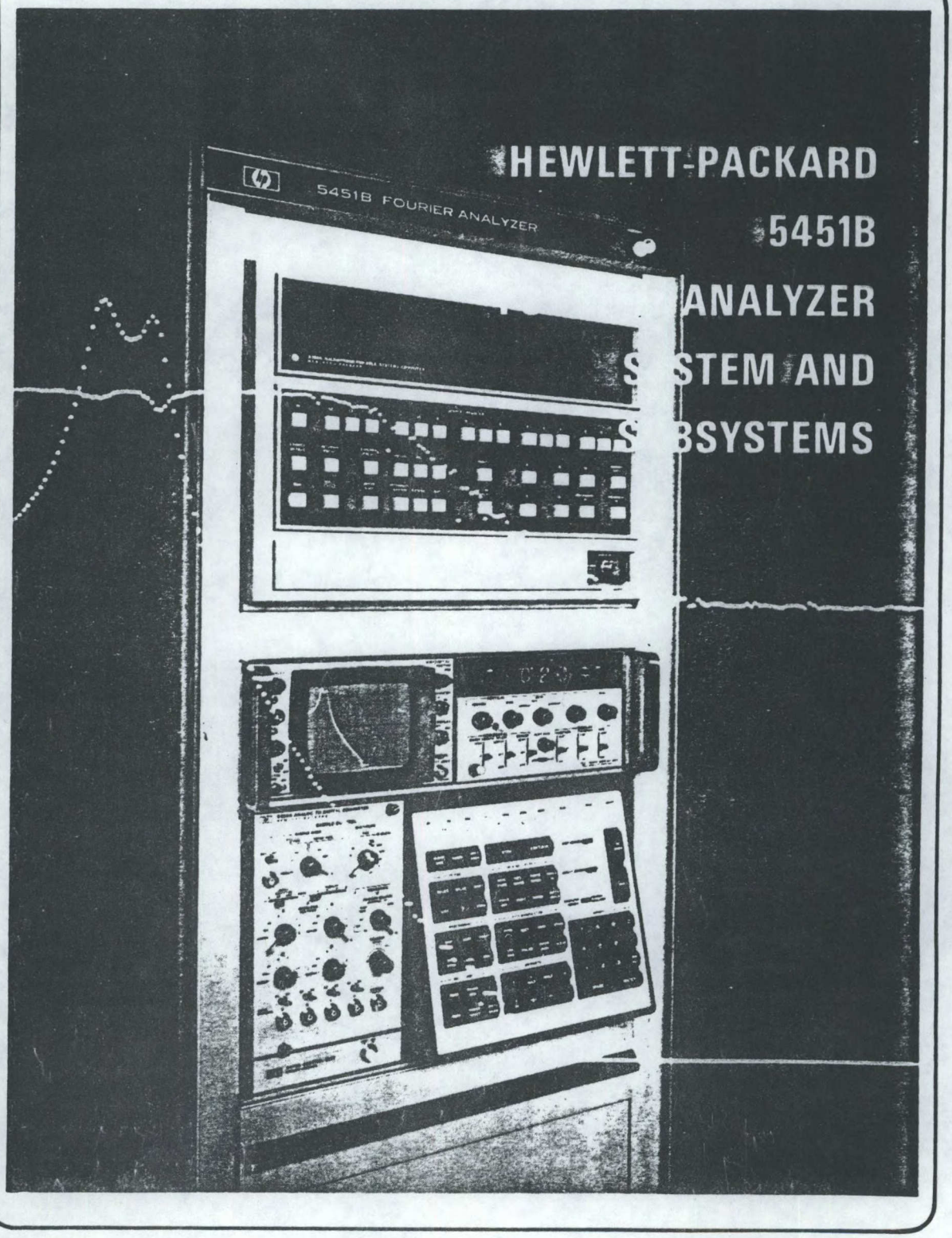

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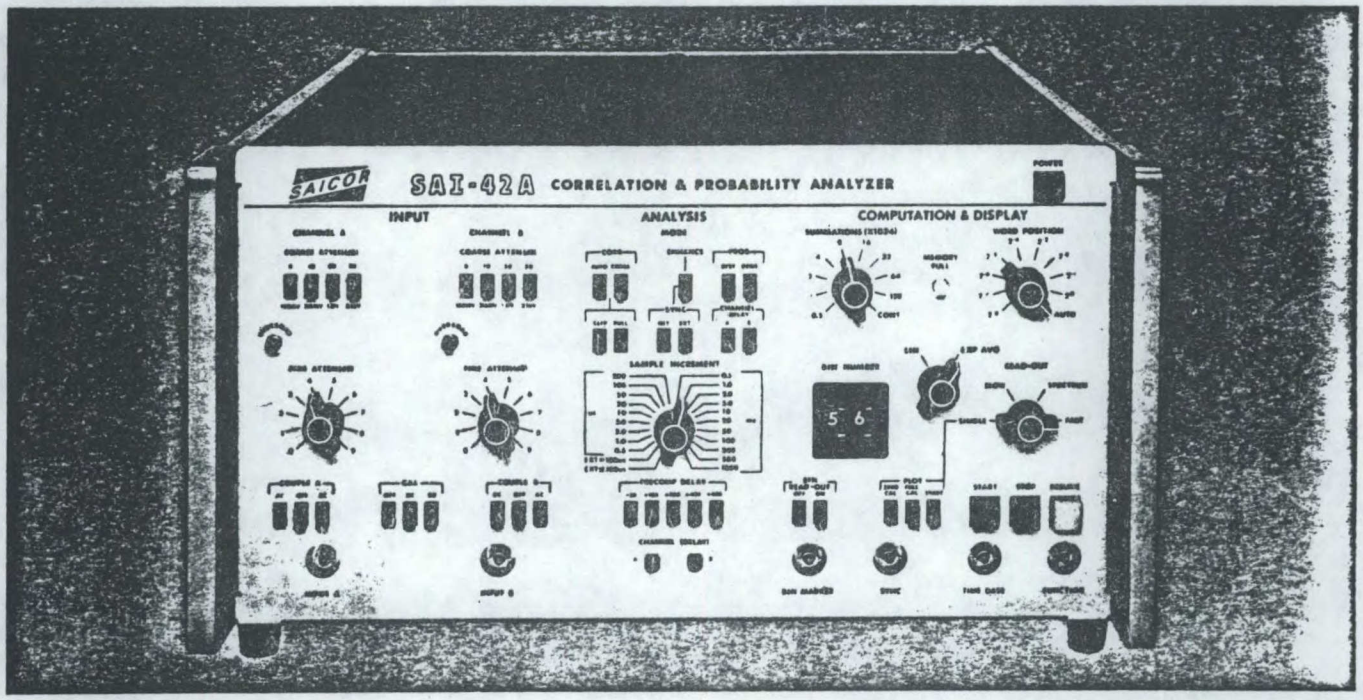
Signal Analysis Products

CORRELATION & PROBABILITY ANALYZER MODEL SAI 42A

PRODUCT INFORMATION

All digital, high speed processing instrument for on-line, real time Correlation, Enhancement and Probability computation



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Correlation is particularly useful for a) measurement of time delays in a signal transmission path, b) recovery of periodic signals buried in noise, c) establishing the relationship between random signals and d) system response identification problems. Enhancement or Signal Averaging is extremely important in applications where it is desired to study the actual signal which is buried in noise. The coherent pattern of the signal is re-inforced at each repetition but any noise present in the signal averages to zero. The Probability modes are important to applications in which the signals' amplitude characteristics are vital The SAI-42A is the economical member of the SAICOR family of Correlation & Probability Analyzers. It performs most of the functions of the more sophisticated SAI-43A which has a higher sampling rate and 400 point analysis Detailed descriptions of correlation, enhancement (signal averaging) and probability operating principles are found in the 8-page SAI-43A bulletin. The same bulletin contains applications, standard and optional features and a photo calling out all controls and indicators.

Output options include tape punch interfaces, digital printer outputs, teletype machine interface and code converter. Photon counting or direct digital inputs for correlating laser light scattered pulses is easily accomplished by adding the appropriate input interface option. Consult the factory for details.

Also, the new Fourier Transform Analyzer, Model SAI-472, is now available. This instrument is a unique add-on unit which complements and extends the SAI-42A capability by Fourier transforming any time display and presenting its equivalent frequency information. The Model SAI-472 performs Real and or Complex (Real and Imaginary — Magnitude and Phase) transformation of auto or cross correlation functions to produce Power Spectrums. The Fourier Transform of time averaged data can be computed as well as the Characteristic Function resulting from the transform of the Probability Density data.

Complete specifications for the SAI-42A Correlator & Probability Analyzer are on the reverse side.

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High-speed FFT chip set under development

Fast Fourier Transform (FFT) analyzers that sell for several thousand dollars may soon have some stiff competition from an FFT chip set under development at TRW.

The ICs, being produced under contract for the Air Force, can perform a multiplication and three addition operations on a 12-bit parallel word—in only 240 ns. When used to perform a Fourier Transform, the set can complete the task on 1024 points in only 2.5 ms. More sample points or higher speed can be achieved by cascading devices and adding a larger external memory.

The three chips in the set are fabricated with a triple-diffusion process that permits very-large-scale integration, according to James Buie, an engineer working on the project at TRW's Redondo Beach, CA facility. The main IC of the set is the signal-processing arithmetic unit (SPAU), which contains 15,000 devices on a 350 by 310-mil chip—the equivalent of roughly 3000 gates.

The SPAU replaces about 55 conventional TTL/MSI ICs, Buie says. Among other things, the architecture of the SPAU provides for register transfers, parallel multiplication and simultaneous addition.

The second chip in the set is the signal-processing address-control chip (SPAC). This device controls accessing of the memory that stores the FFT data points. It also controls the accessing of SIN and COS look-up-table ROMs.

SPAC chips may be cascaded to extend the total number of FFT sample points that can be handled. One SPAC can provide 32 points, two will accommodate 1024 points, and with three SPACs up to 32,768 points may be sampled.

The final chip in the set is called a signal-processing delay line or SPDL for short. It is basically a shift register composed of 60 D-type flip-flops plus input/output control circuitry. The SPDL can accept digital words that are 12-bits wide and 5 bits long and is used to make data available to the processor when they are needed.

In addition to being used as a Fast Fourier Transform analyzer, the SPAU can also be used to filter and digitize all types of complex signals, Buie reports. Specific frequency components of a given signal can be filtered with greater speed and accuracy by FFT techniques than with other filtering methods.

The chip is not yet available, but should be on the market by the first quarter of next year, Buie notes. And although there is no firm pricing available yet, Buie estimates that the 3-chip set will probably sell for about $300. Considering that the 55 military-grade MSI devices the SPAU alone replaces cost about $750, that's a bargain.

Another benefit of the new FFT chip set is a significant savings in the cost of assembly. Much smaller PC boards—with a five-to-one reduction in the total number of interconnections—can be used.

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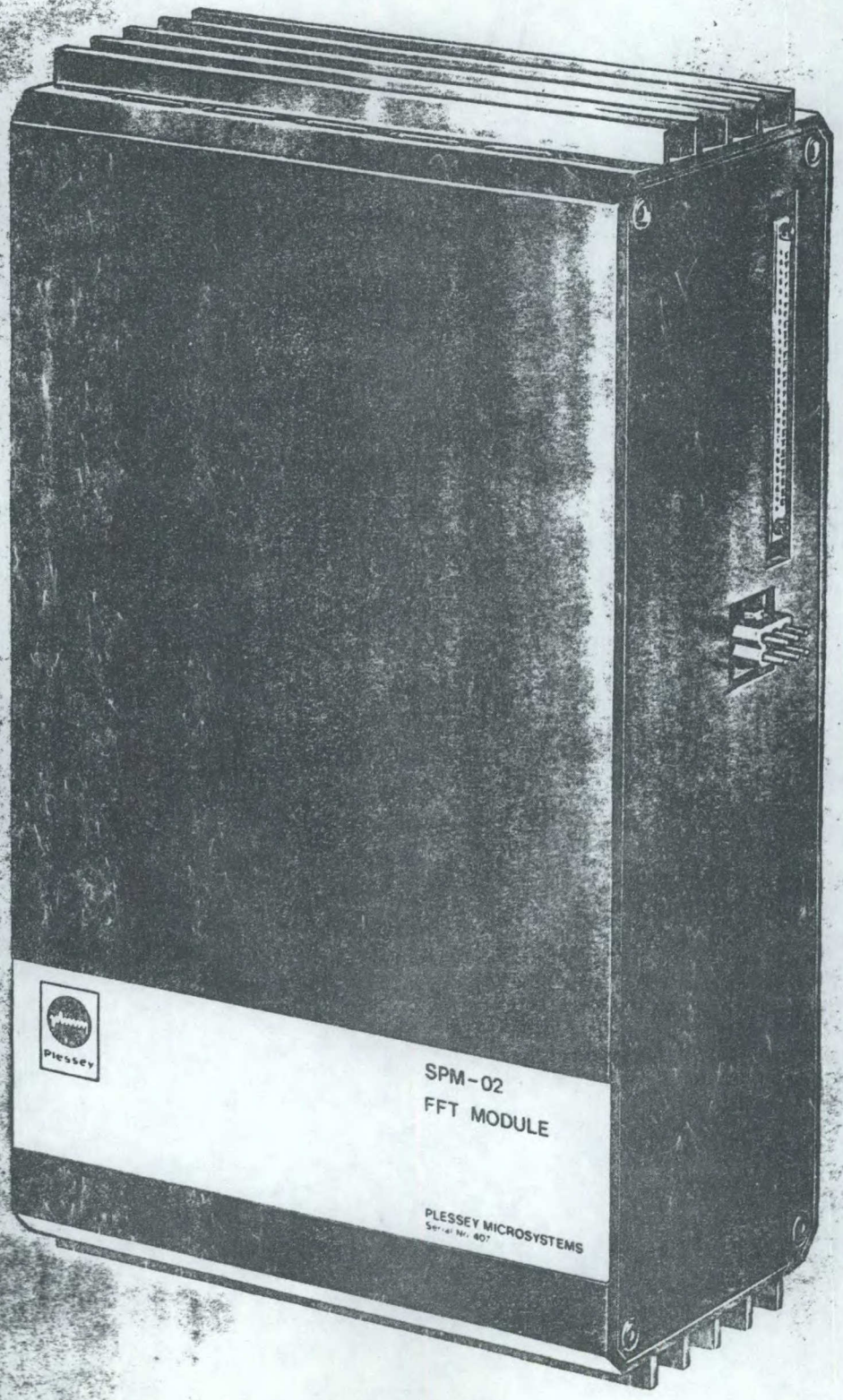

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Model SAI-470

12 OCT 1976

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All digital Fourier Transform Analyzer used in conjunction with SAICOR Correlators

Outstanding Features

- Complete digital analysis for repeatable and accurate results — no adjustment or re-calibration.
- Variable marker for digital display and readout of co-ordinate information.
- Simultaneous display of both input data and computed Fourier components.
- Digital log scaling for dB presentation.
- Real, imaginary, magnitude and phase calculation for versatile display.
- Compatible for analysis of external digital data.
- 1000 point interpolated display. 0-2.5 MHz analysis — SAI-43; 0-1 MHz analysis — SAI-42.
- Directly compatible with SAI-42 and SAI-43 100 and 400 point Correlators.
- Four (4) block processing for improved resolution of 100 point Correlator.
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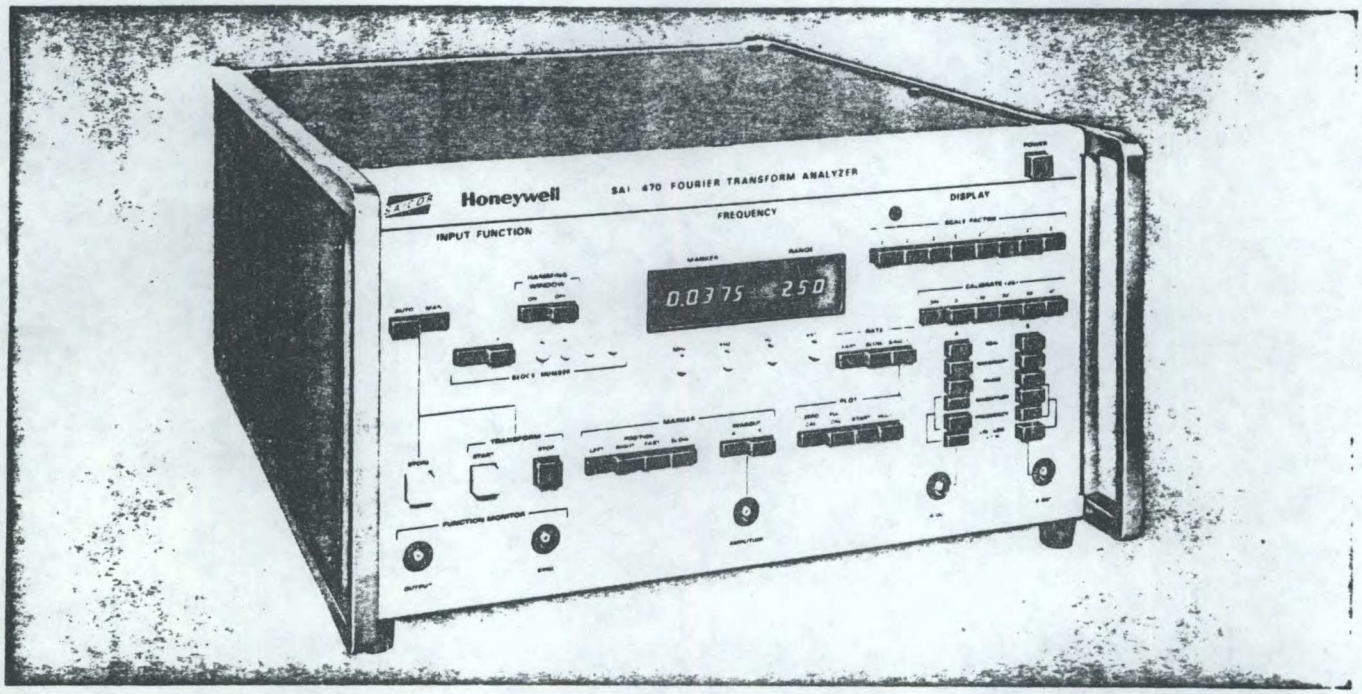

General Concepts

Fourier series analysis is basically the representation of a periodic function by an infinite series of weighted sines and cosines. The frequency components are at multiples of the reciprocal of the period of the data. The extension of Fourier analysis to non-periodic data results in Fourier Transform theory and the resultant integral analysis. This analysis yields a continuous frequency analysis instead of the discrete or line spectrum which arises from periodic data.

The link between the above concepts lies in the fact that in the real world, only a finite length segment of data is available for analysis. Moreover, discrete or digital Fourier Analysis is used when the data to be transformed is available only at discrete or sampled values.

Principles of Operation

I. FTA Processing

The SAI-470 Fourier Transform Analyzer (FTA) is a fully digital instrument which performs a Fourier analysis of any function computed by either the SAI-42 or SAI-43 100 and 400 point Correlation and Probability Analyzers (External digital input data can also be applied to the FTA for transformation.) The basic computation of the FTA is given by:

$$\text{Real} = a_n = \sum_k x_k \cos\left(\frac{2\pi kn}{N}\right)$$

and

$$\text{Imaginary} = b_n = -\sum_k x_k \sin\left(\frac{2\pi kn}{N}\right)$$

The "data" values X_k are the computed values at the Correlator output. For example, if the SAI-42 Correlation and Probability Analyzer is performing a cross-correlation analysis, then the X_k are the 100 values of $R_{1,2}(k\tau)$ — the cross-correlation function of the two original signals 1 and 2. The index k therefore runs from 0 to 99 for a total of 100 data points.

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