Digital Code Conversion between Delta Modulation and PCM

Final Report
March 31, 1982

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Government of Canada
DSS Contract #05V80-00023

EP

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COMPANY: Spar Aerospace Ltd.

TITLE: M-SAT Canadian demonstration spacecraft : report and baseline : performance document SEE OVER

DOC CR NO: DOC-CR-SP-81-047

DSS CONTRACT NO: 36100-0-0768

DOC SC. AUTH.: H. Raine

REPORT DATE: 1981 (1 set)

ONE SET CATALOGUED AS: P 91 C654 M73 1981 (filed in document filing cabinet)

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COMPANY: Spar Aerospace Ltd.

TITLE: M-SAT phase A extension : Canadian demonstration spacecraft : report and baseline performance : document addendum. 3v. (SEE OVER)

DOC CR NO: DOC-CR-SP-82-004

DSS CONTRACT NO: 36001-1-3040

DOC SC. AUTH.: H.R. Raine

REPORT DATE: 1982

ONE SET CATALOGUED AS: P 91 C655 M84 1982

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DOC-CR-SP-82-079

ORIGINAL DOCUMENT: REVIEW AND PUBLICATION RECORD

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6. SCIENTIFIC AUTHORITY D. Wholberg (S.O.S.) contact director	7. LOCATION DSS/CRC	8. TEL. NO.

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Appendix

1. Introduction

The objective of this research is to develop an interface between "telephone standard" PCM systems and Delta modulation systems. Although PCM is a well characterized standard and low cost PCM codecs are now available, Delta modulation is often used where the available bit rate is low or when a noisy channel introduces frequent bit errors. Both coding formats are used in existing systems.

When different communication systems are interconnected, code conversion is customarily achieved by decoding to the analog signal and then re-coding. The general case of CVSD, EVSD and CPCM interfacing at non-synchronous bit rates is discussed in the report. The special case of 64 KBPS CPCM interfaced to 32 KBPS EVSD has been thoroughly researched in this study and a digital code conversion system has been constructed for evaluation. The report includes a comparative evaluation against the normal technique of decoding to an analog signal.

In order to digitally convert between coding formats such as CVSD, EVSD and CPCM and possibly DPCM and ADPCM, it was first necessary to select a suitable standard interface format. High sample rate 16 bit linear pulse code modulation (LPCM) was considered as a model of the analog signal used in existing converters. Further investigation revealed that 10 bit DPCM could also be used as the exchange format and some saving in hardware would result [Ref. 6]. For example the conversion of delta code to PCM requires an accumulation of the delta code to produce 16 bit LPCM, then a 3.4 kHz sub sampler and a LPCM to LPCM compression circuit. By reversing the order of filtering and accumulation the filter processes 10 bit DPCM and the required filter word length is reduced. DPCM is also a convenient format for interfacing EVSD and CVSD as it can be easily generated from either codec.

Figure 1 illustrates possible code conversion combinations. Shaded portions are interfacing circuits required to produce the high sampling rate DPCM.

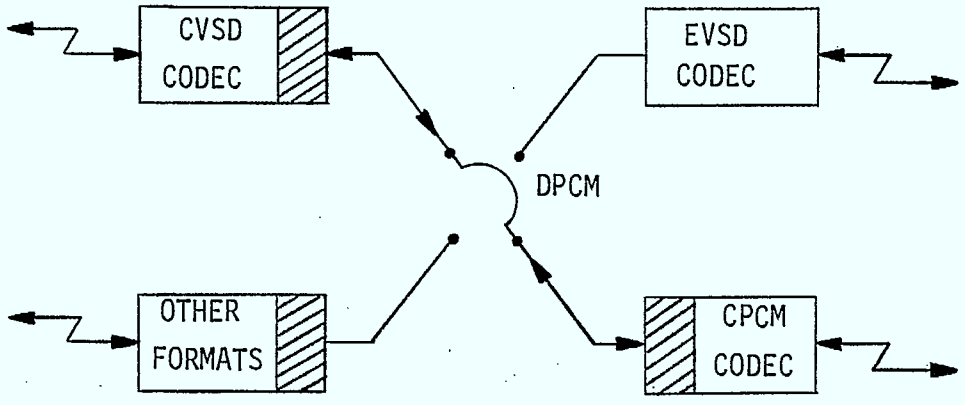


Fig. 1 Block diagram illustrating conversion between any two codes.

2. Interfacing CVSD and EVSD

2.1 Comparison of EVSD and CVSD

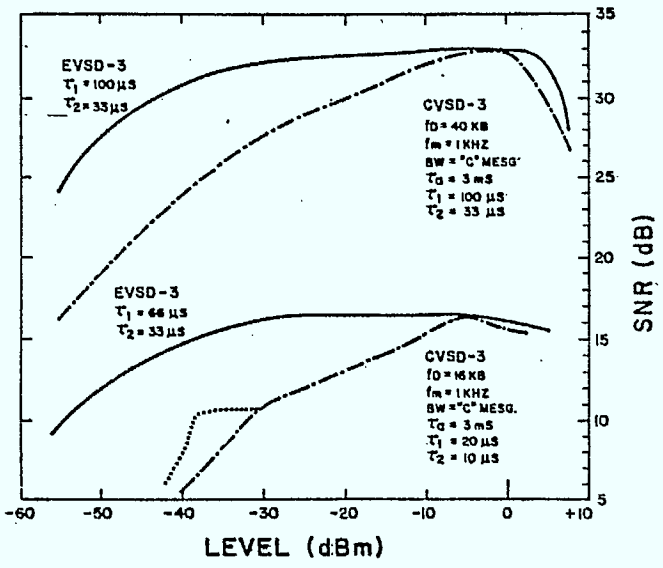


Fig. 2 EVSD and CVSD Performance

Continuously variable slope delta modulation (CVSD) and exponentially variable slope delta modulation (EVSD) are different only in the algorithm which adapts the step size to an approximation of the optimal value. CVSD adaption is definitely sub-optimal and substantial degradation occurs in the SNR performance. A lengthy discussion of the adaption techniques may be found in references 27 and 29. Existing systems mainly use the older CVSD technique but EVSD is finding application in newer systems. Interoperability is now a matter of interest.

2.2 Direct Connection between CVSD and EVSD

An EVSD decoder may be used directly with CVSD data (or vice versa) to give intelligible decoded voice. The decoded waveform is not significantly distorted as both types of decoder reconstruct the waveform in the same manner. Using the incorrect decoder, however, results in unexpected adaption of the decoded signal amplitude.

With EVSD coding, the probability of sequential identical bits changes only slightly from 50%. The largest and most rapid decrease in identical sequential bits occurrs as signals decrease below -30 dBm. A CVSD decoder has an output amplitude directly proportional to the probability of three identical bits and therefore the output amplitude remains nearly constant until the EVSD input becomes less than -30 dBm. A graph of amplitude ratio is shown below for an EVSD encoder with EVSD, CVSD-3, and CVSD-4 decoders. Improperly decoded voice signals have audible transients at the beginning of each word. The decoded voice is very loud but is clear and intelligible.

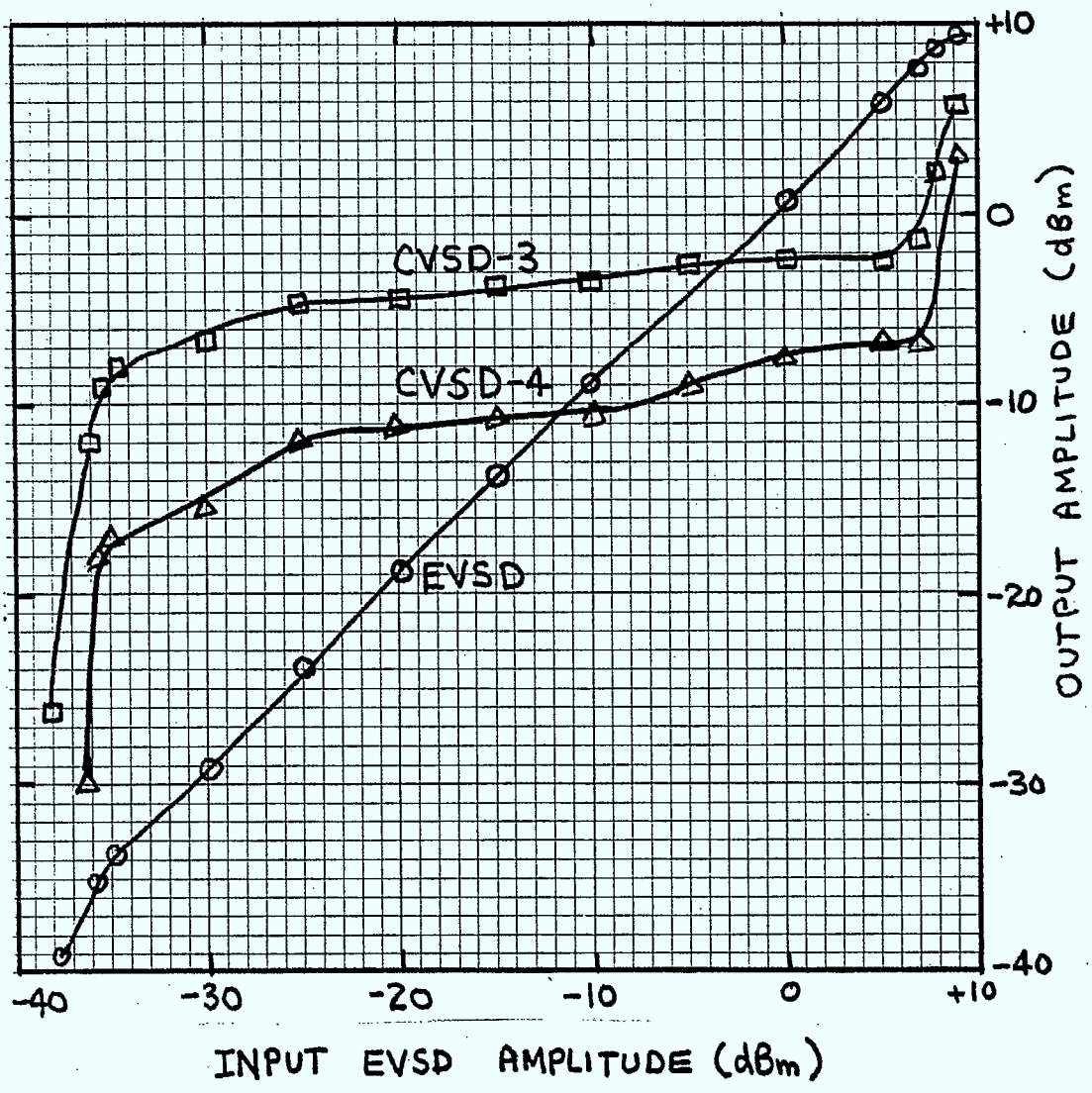


Fig. 3 Improperly Decoded EVSD Signals

With CVSD coding, the probability of sequential identical bits changes rapidly as the input signal is decreased in amplitude. When the probability falls below 50% the EVSD decoder changes abruptly from the maximum decoded amplitude to a small decoded amplitude. It then decreases more and more slowly to the minimum decoded amplitude. A graph of decoded output level versus input level is shown below. The voice quality from the incorrect decoder is quite poor. It resembles an audio amplifier with a loose connection. The decoded voice is moderately intelligible but has loud bursts during louder input passages or during the "S" sounds. If a low input level is used the output is even lower but the voice quality sounds almost normal.

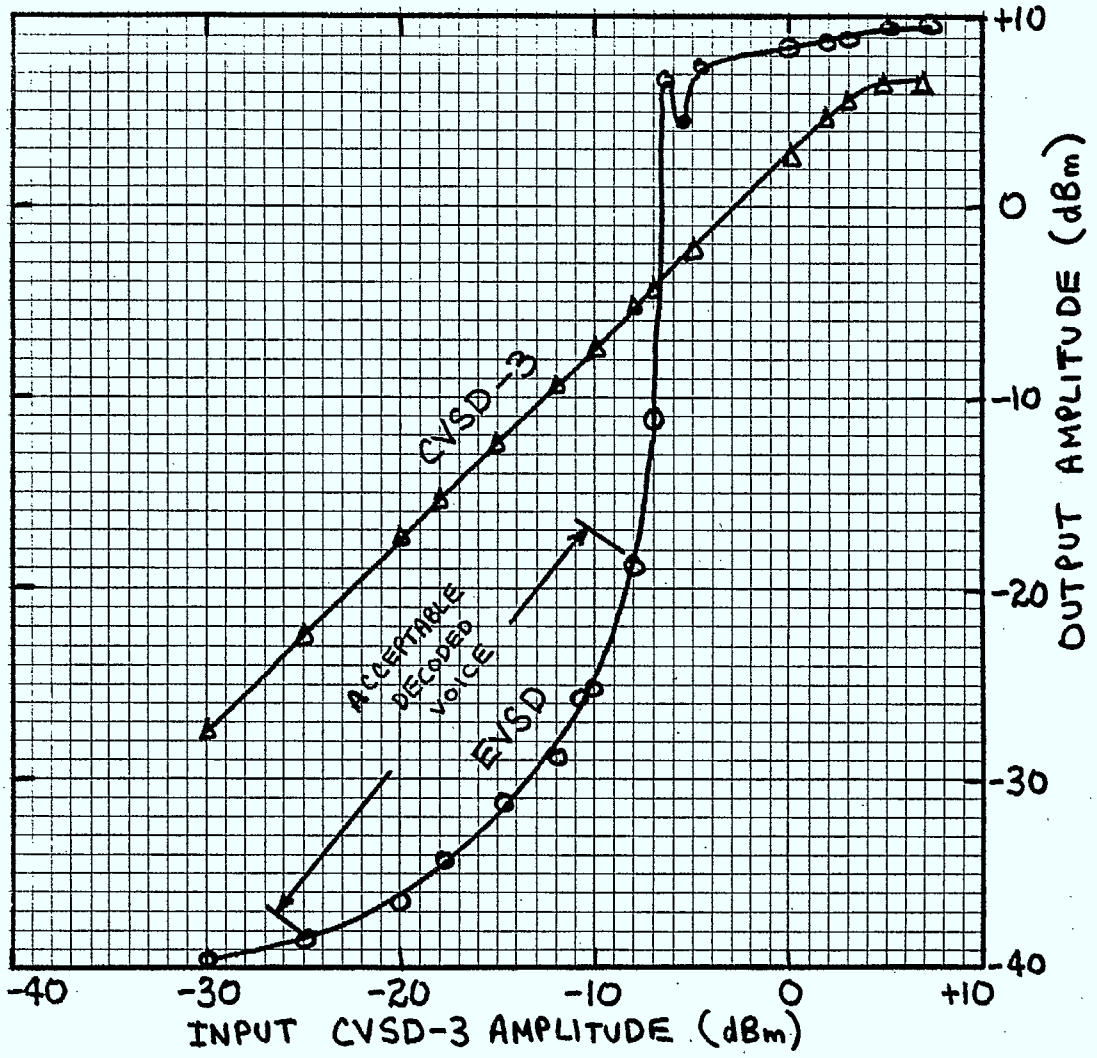


Fig. 4 Improperly Decoded EVSD Signals

2.3 Interfacing with DPCM Format

More accurate code conversion requires processing of the incoming EVSD bit stream to form an outgoing CVSD bit stream. This can be done by decoding to an analog signal then recoding in the other format. It is also possible to use an accumulator creating a numeric equivalent of the analog signal. The digital CVSD encoder would then use a numeric comparator and a numeric approximate signal in the feedback loop. The proposed scheme simplifies the latter hardware by replacing the incoming accumulator, the feedback accumulator and the digital comparator with a single accumulator. Incoming increments are added, feedback increments are subtracted and the resulting sign becomes the outgoing CVSD bit. This simplification is illustrated in Figure 18.

When converting between CVSD and EVSD it is desirable to create equal step sizes on the encoding and decoding capacitors where an approximation to the input signal is formed. A digital equivalent of the analog step size is

obtained from both the EVSD and CVSD codecs. A digital accumulator is then used to add incoming step sizes and subtract outgoing step sizes. If the contents of the accumulator remain nearly zero, the decoder approximate signal will closely match the encoder approximate signal. A proposed accumulator uses serial adders. As shown in section 3, this method has been used to interface DPCM to EVSD.

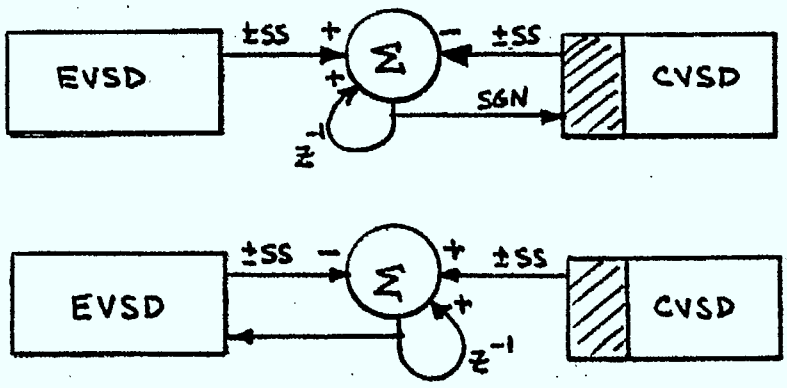
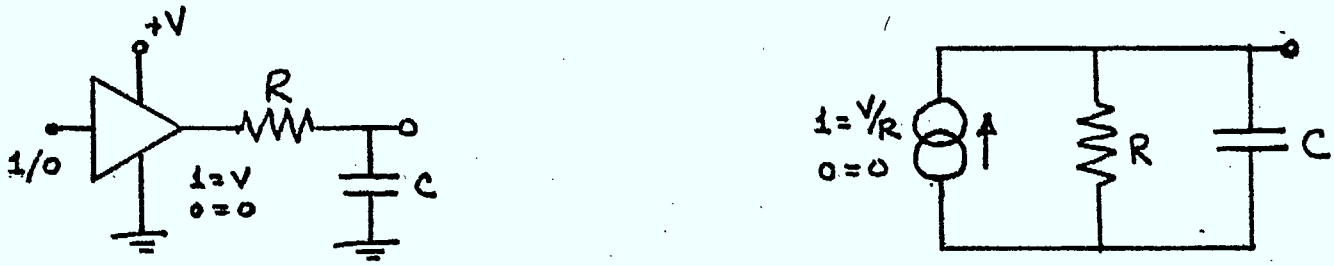


Fig. 5 Signal flow diagram of EVSD - CVSD conversion.

DPCM or signed step magnitude numbers can be generated by a simple digital filter which models the adaption circuit of a CVSD codec. The operation of the digital filter may be represented by the Norton equivalent of the RC adaption circuit.



(a) Actual Circuit (b) Norton equivalent circuit

Fig. 6 Representation of CVSD adaption circuit

The digital filter will have a transfer function of the form: $H(z) = \frac{1}{1 - aZ^{-1}}$

A detailed development may be found in example A1 of Appendix A.

f_s	a	τ
32 KB	1-1/64	2mS
32 KB	1-1/128	4mS

The time constant, τ, of the digital filter will vary directly with the sampling period. Some examles are given in the table. The digital filter may be implemented with serial adders. A signal flow diagram is illustrated in Figure 7.

Quantization error will become significant at small step sizes and this will be a source of noise. CVSD performance is quite poor at low signal levels and this quantization will cause a small amount of further degradation. The dynamic range of CVSD coding is approximately 35 dB (Ref. 29) and would require a step size range of 6 bits (36 dB). It is proposed to use a 9 bit register for step size which means a 3 bit (12%) accuracy for quantizing the smallest CVSD step size.

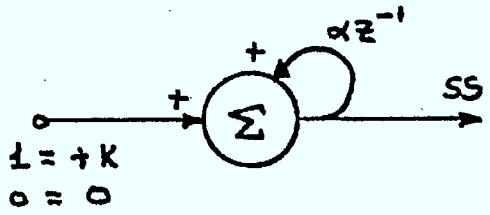


Fig. 7. Signal flow diagram of CVSD adaptive step size.

3. Digital Code conversion between EVSD and CPCM

3.1 Block Diagram

Conversion to standard companded PCM requires (1) accumulation (2) filtering (3) subsampling (decimation) and (4) companding. The reverse process requres (5) expansion (6) interpolation (7) filtering and (8) differentiation. As discussed in section 2.1, a more efficient implementation may be achieved by reversing parts (1) and (2) and also parts (6) and (8). The functions of the two filters will be discussed separately. It should be added that these filters should be approximately flat in frequency response. There should be little change in channel response when code conversion is not used. An illustration of DPCM/CPCM code and sample rate conversion is shown below. The components are discussed in following subsections.

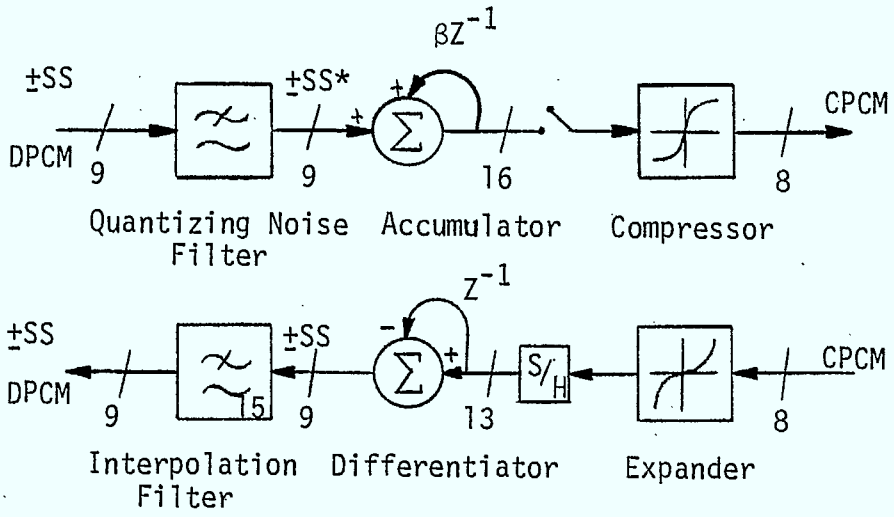


Fig. 8 Signal flow diagram of CPCM conversion

3.2 Filtering

3.2.1 Quantizing and Interpolation Filters

This digital filter is used prior to the accumulation and decimation of the DM-PCM conversion. Samples are filtered at the delta coding rate (32 KB). Prior to filtering, the equivalent accumulated signal spectrum has voice spectral power below 3 KHz, quantizing noise at intermediate frequencies followed by voice spectral power centered about the sampling frequency. The quantizing noise power at intermediate frequencies must be reduced before it is aliased into the voice band during the decimation process. Without this filter, voice band noise would be quadrupled (increased by 6 dB) for 32 KB DM if the quantizing noise has a white spectrum. If the filter stopband is merely 10 dB, the inband quantizing noise will increase by only 1 dB for 32 KB DM. An illustration of the filtering, decimation and noise aliasing has been adapted from reference 28. The quantizing noise filter and the interpolation filter have been constructed identically. The filter structure and coeficients are described in section 3.2.2.

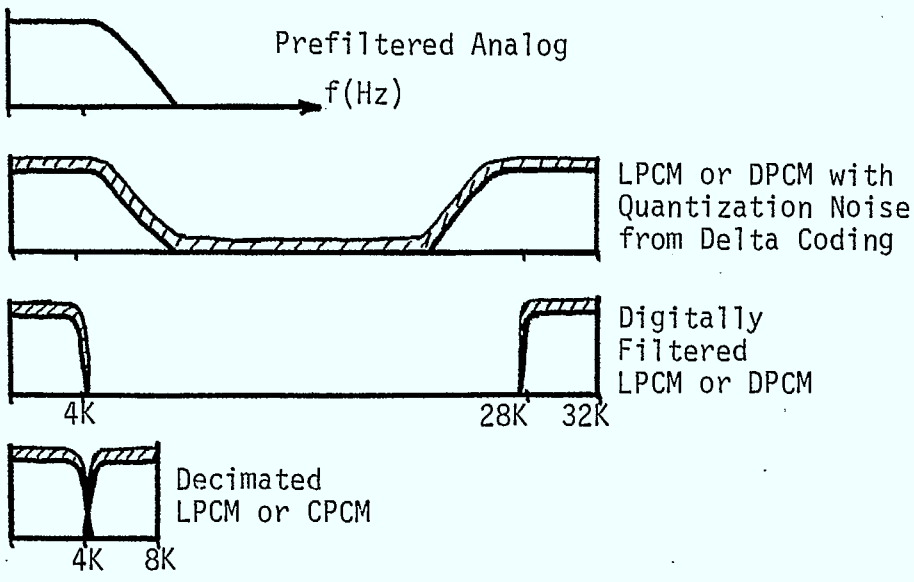


Fig. 9

In the conversion from CPCM the samples are first expanded to LPCM then differentiated to obtain DPCM. The DPCM samples occur at an 8 KHz rate. Images of the voice spectrum are centered about 0, 8, 16, 24 KHz (etc.). The interpolation filter provides intermediate samples at a 32 KHz rate as required by the delta modulation decoder. The interpolation filter attenuates signals above 3.4 KHz and reduces the image components which would "worry" the delta codec making its step size larger than need be. The delta codec's frequency characteristics make it especially sensitive to these images. An attenuation exceeding 30 dB is recommended for frequencies 6 KHz and higher. Figure 10 illustrates the function of the interpolation filter.

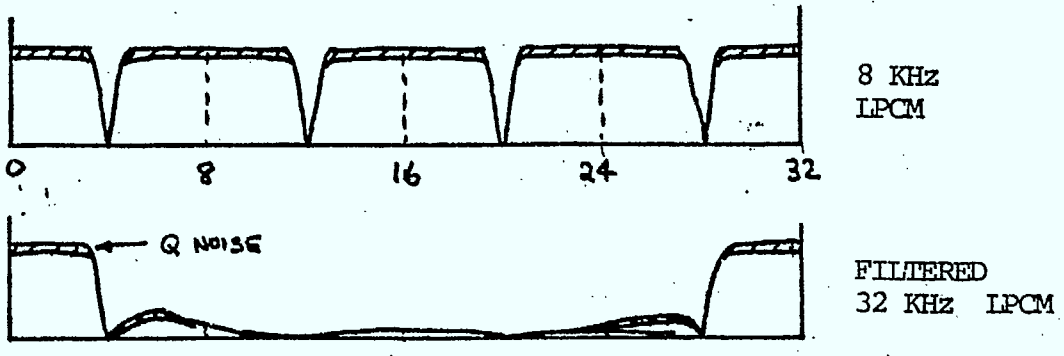


Fig. 10 Signal and Noise spectrum during conversion from CPCM

3.2.2 Filter Structure

The digital filter constructed for this research project consists of 25 CMOS SSI and MSI packages. Consideration was given to recursive and non-recursive structures, serial, parallel and ROM based processing techniques. With the possibility of eventual LSI fabrication, the equivalent gate count was considered for each case. The selected technique was a recursive filter (to minimize sample storage) with serial computation (to reduce interconnection wires). The speed of parallel processing was not required and a multiplexed ALU would complicate the wiring. The serial processing circuits (CD4015, CD 4032, etc.) could operate 5-10 times faster than required in this project. A modern 16 bit processor (8086) was calculated to be approximately 10 times too slow in performing the filter function. The 4 pole, 4 zero elliptic filter was optimized for 5 bit coeficients by using computerized response plotting with a trial and error procedure. The filter structure is illustrated below.

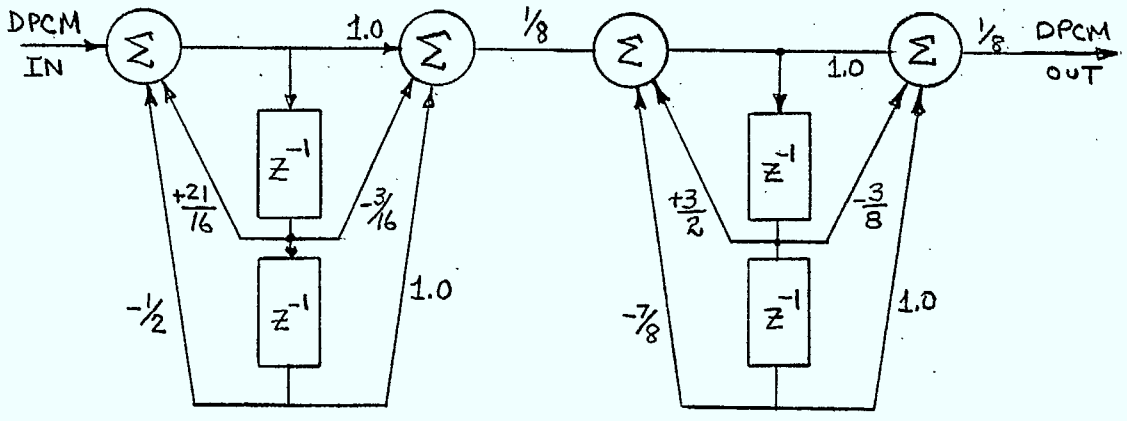


Figure 11 Elliptic Filter Structure

3.2.3 Coefficient Selection and Calculated Response

To limit the amount of circuitry used in the digital filter, the multiplying coefficient word length has been limited to 5 bits. The illustration below is a partial map of the z plane with grid lines spaced in proportion to the coefficient resolution. Possible pole or zero locations occur where the grid lines intersect. A relationship between the tap coefficients and the pole locations is found in Appendix A2 examples 3 and 4. Pole and zero locations used in the actual filter are shown on the grid below.

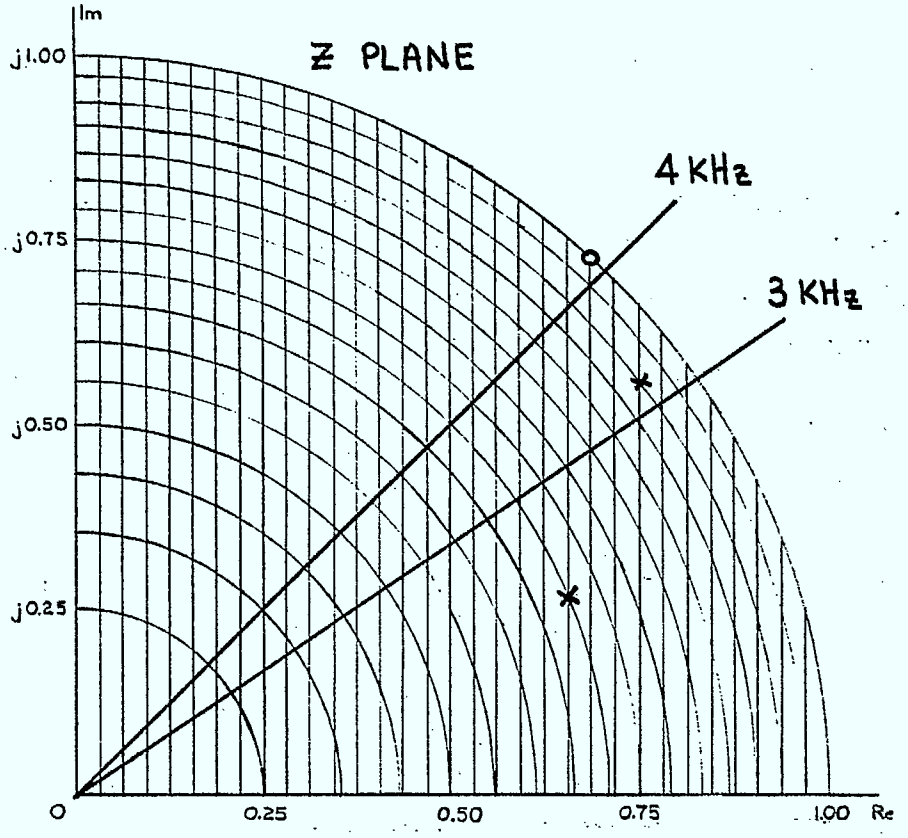


Fig. 12 Digital Filter Pole Locations

Pole and zero locations were chosen by trial and error to get equal ripple in the passband, equal ripple in the stop band and a transition region between 3.4 and 4.0 KHz. With the 4 pole 4 zero elliptic filter the achievable stop band attenuation was 25dB. Calculated gain versus frequency characteristics are shown on the following pages.

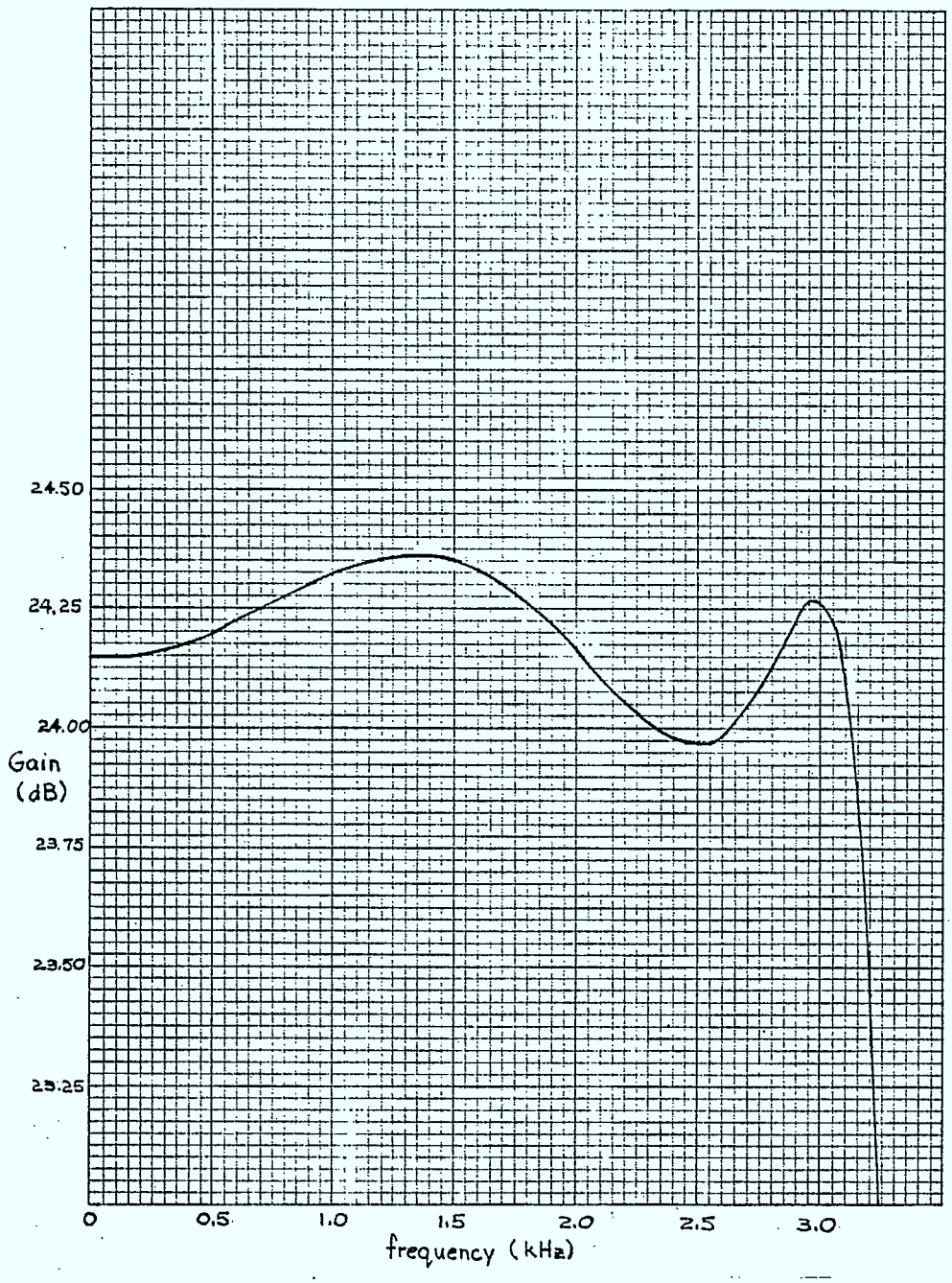


Fig. 13 Digital Filter Passband Response

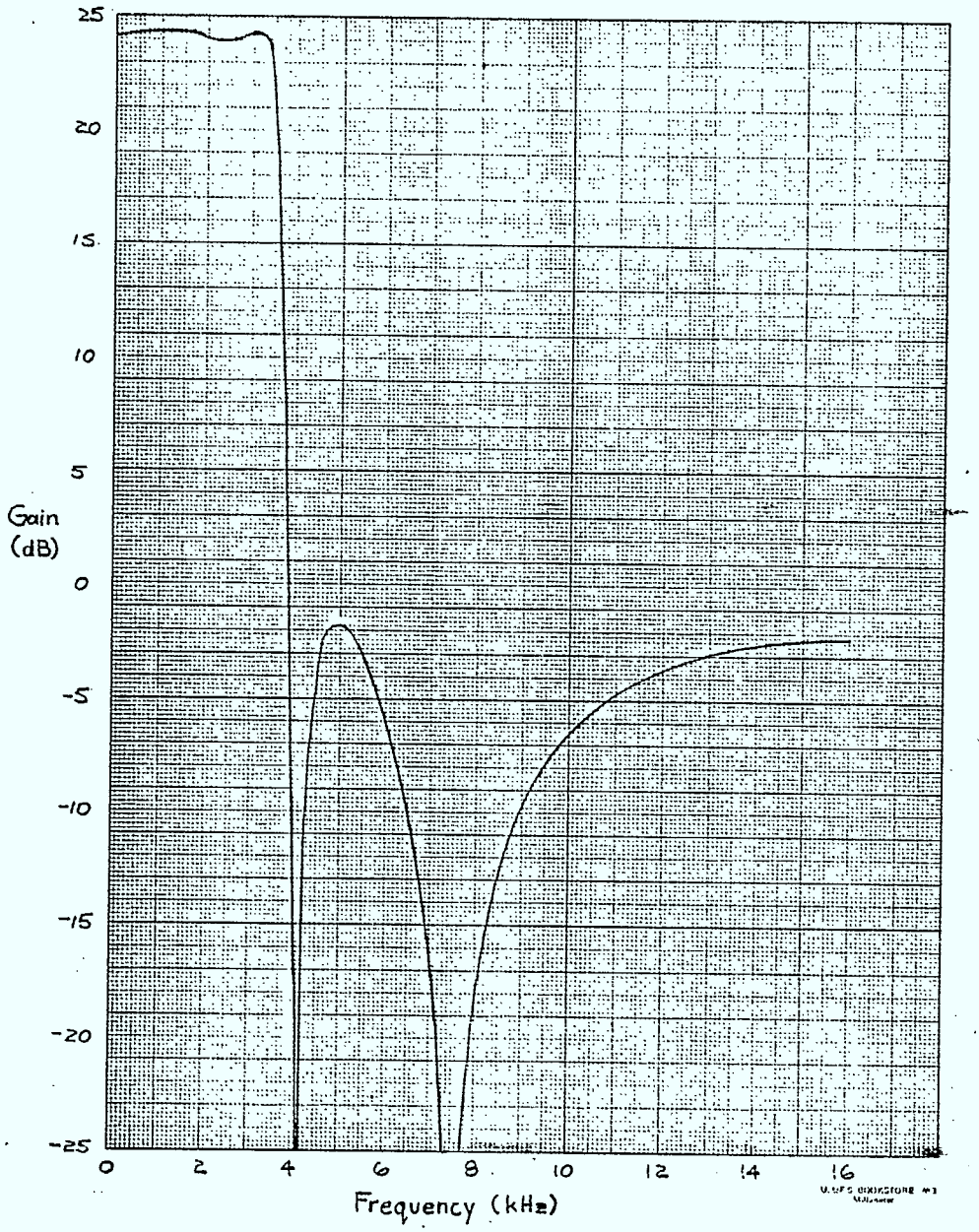


Fig. 14 Digital Filter Stopband Response

The photographs below illustrate the performance of the filter on a time waveform composed of two linearly added sinusoids. The input analog waveform is shown in the lowest trace. The middle trace shows the waveform after delta coding. The upper trace shows the delta coded signal after digital filtering and conversion to analog.

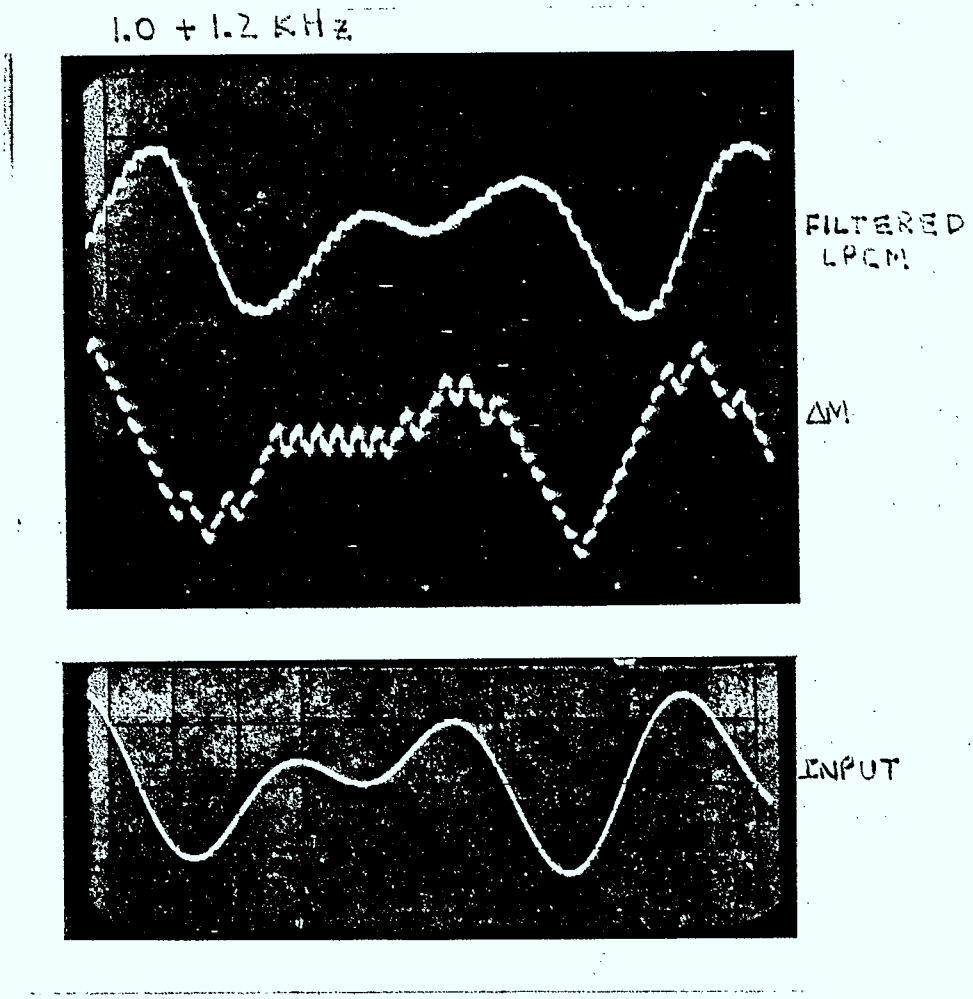
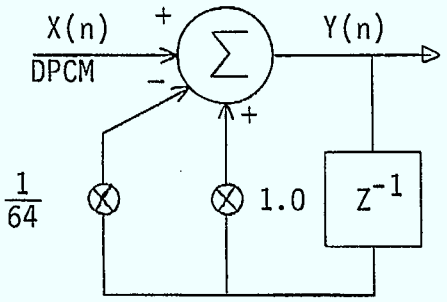
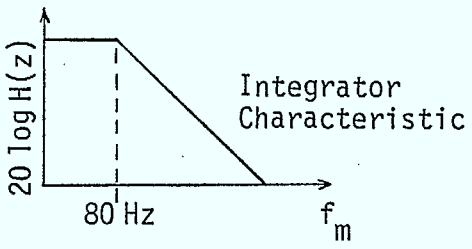


Fig. 15 Waveforms in the Digital Filter

3.3 Accumulator and Compressor

Filtered DPCM samples are accumulated in a 16 bit register to form LPCM samples at a 32 KHz rate. A small "leakage" has been included with the accumulator to force the resulting LPCM values toward the center of the register's numeric range. A block diagram of the accumulator is shown below. A detailed circuit diagram can be found in the appendix.





$$Y(n) = X(n) + a\,Y(n-1)$$

$$H(z) = \frac{1}{1-az^{-1}} = \frac{1}{1-.984z^{-1}}$$

$$\omega_c = \frac{1-a}{T} = \frac{1/64}{1/32\ ms}$$

$$f_c = \omega_c/_{2\pi} = 80\ Hz$$

Fig. 16 Accumulator Block Diagram

The leakage in the numeric integrator is required to accommodate asymmetry in the current sources of the delta encoder. If the positive current source is smaller than the negative source, the number of logic 1 code bits must exceed the number of logic 0 bits. This condition is required to maintain a constant average value in the feedback approximate signal. Differential PCM samples generated from the delta codec will have positive average value.

Given the above DPCM samples, a pure integrator (accumulator) would steadily increase in numeric value until the register overflowed to the most negative number. Following overflow the register value would increase steadily until overflow occured once more. With the "leaky" accumulator, the LPCM maintains a positive average value and the average leakage then compensates for the non zero average of the DPCM samples. The system gain versus frequency response can be maintained at low frequencies if the encoder uses a leaky analog integrator with a corner frequency equal to the leaky numeric integrator.

After accumulation to LPCM with a slight offset, the signal enters the companding process. The compressor first converts LPCM samples to sign magnitude format and transfers the sign bit to the CPCM output register. The sample magnitude is then increased by 16.5 by a serial adder. The enlarged magnitude is then passed through a register which counts trailing or most significant zeros in the bianry number. A preset down counter is used to subtract the number of leading zeros from 7 which gives the desired exponent value for the CPCM output. The 4 bits adjacent to the most significant 1 of the magnitude are shifted into place then transferred to the mantissa of the

CPCM output. An overflow detector is used to set the CPCM output to maximum value when the sample magnitude exceeds 12 bits. The CPCM sample is then serialized most significant bit first - sign, exponent then mantissa. The output serial code is inverted to interface directly with a CPCM decoder (MC 14407).

$$\text{Encoding threshold magnitude} = (M + 16.5).2^{E} - 16.0$$

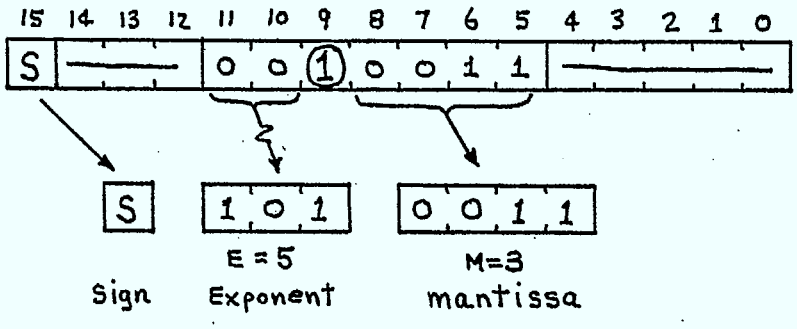


Fig. 17 Illustration of Compression Algorithm

3.4 Expander and Differentiator

Serial samples from a standard CPCM system are inverted then stored in a shift register in sign - exponent - mantissa form. The mantissa is added to the number 16.5 and the resulting 6 bits are stored in a second shift register (B1). The exponent is loaded into a down counter which will prefix up to 7 least significant zeros to the enlarged 6 bit mantissa which is shifted out after the down counter reaches zero. A serial adder is used to add the negative number - 16.5 to obtain the sample magnitude. A second serial adder is used to incorporate the sign bit resulting in serial LPCM samples. the equation of the decoder is as follows:

$$\text{LPCM magnitude} = (M + 16.5).2^{E} - 16.5$$

The previous LPCM sample is stored in a shift register and subtracted from the current LPCM sample to obtain DPCM samples at an 8 KHz rate. These samples are passed to the interpolation filter which operates at 32 KBPS. A schematic diagram is shown in the appendix.

3.5 Accumulator/Comparator

The accumulator compressor is used to generate ADM from a DPCM input. In a conceptual implementation shown in the first part of the diagram below, DPCM is accumulated to form LPCM. A digital leakage would be required to prevent numeric overflow in this accumulator. Conventional delta codec topology is shown in the remainder of the circuit where the step size is accumulated to form an approximate LPCM signal. This approximate signal is compared to the input CPCM signal to determine the sign of the next bit. An existing EVSD decoder circuit is used to develop the adapted step size.

The second part of the diagrm below shows the actual implementation which results in simplified hardware. The subtraction operation has been placed prior to the accumulation. Only one simple accumulator is required which will not overflow (it is located inside the feedback loop). The sign of the accumulator is obtained by simply inverting the most significant bit. A detailed schematic diagram is available in the appendix.

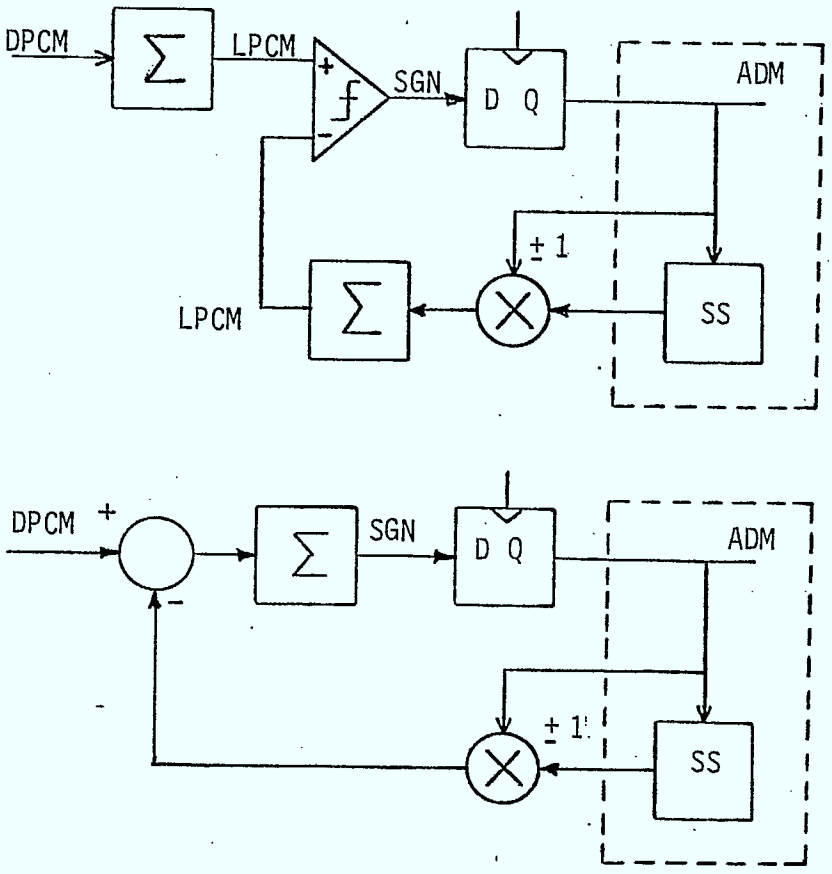


Fig. 18 Alternate Implementations of the Accumulator/Comparator

3.6 Serial D/A Converter

This circuit is not an integral part of the code conversion equipment but serves as an auxillary diagnostic tool. Serial data samples (2's complement form) are clocked into a shift register and then presented in parallel to a D/A converter. The DAC output may be connected to an oscilloscope to display the sample magnitudes. Linear PCM and DPCM signal waveforms may be observed at several points in accumulation, differentiator and digital filters. The magnitude of the delta modulator step size may also be monitored. Points may be tested using a single wire just as an oscilloscope probe would be used in an analog circuit.

The serial DAC has a "x16" gain switch which effectively performs a 4 bit left shift on the sample data. The 12 bit DAC is normally connected to decode the most significant bits while ignoring the least significant four bits. In the high gain position, the most significant 4 bits are ignored and all others including the LSB of the data sample are decoded. The high gain position is useful for small signals but results in "wrap around" if the signal is too large. A block diagram of the serial DAC is shown below. A detailed schematic may be found in the appendix.

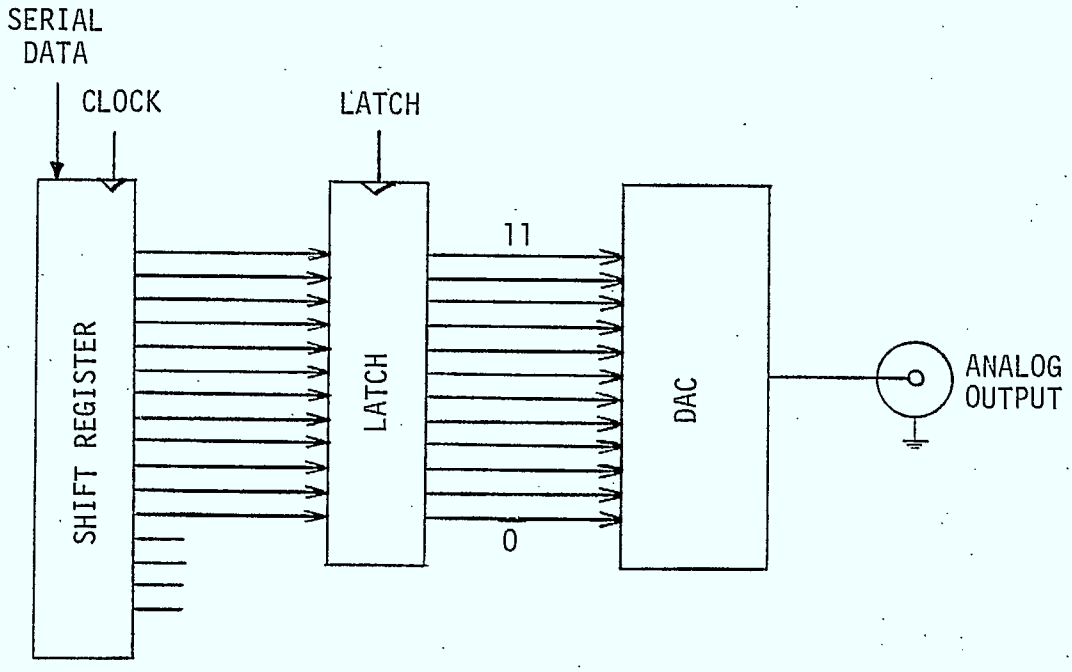


Fig. 19 Block Diagram of Serial DAC

3.7 Performance of the EVSD/CPCM Digital Code Converter

The performance of the code converter was evaluated for SNR vs amplitude, gain vs amplitude and gain vs frequency. The major interest lies with SNR performance which was measured at the standard modulation test frequency of 1 KHz and also at 300 Hz. The latter frequency allowed better evaluation of the noise added by code conversion.

3.7.1 Conversion to CPCM

The conversion from adaptive delta modulation (ADM) to companded PCM (CPCM) was studied by applying a sinusoidal signal to the EVSD codec. The output bit stream was then digitally processed to form linear pulse code modulation (LPCM) and CPCM. As shown in the block diagram, the ADM, LPCM and CPCM digital signals were decoded to analog form and the SNR of each output was evaluated.

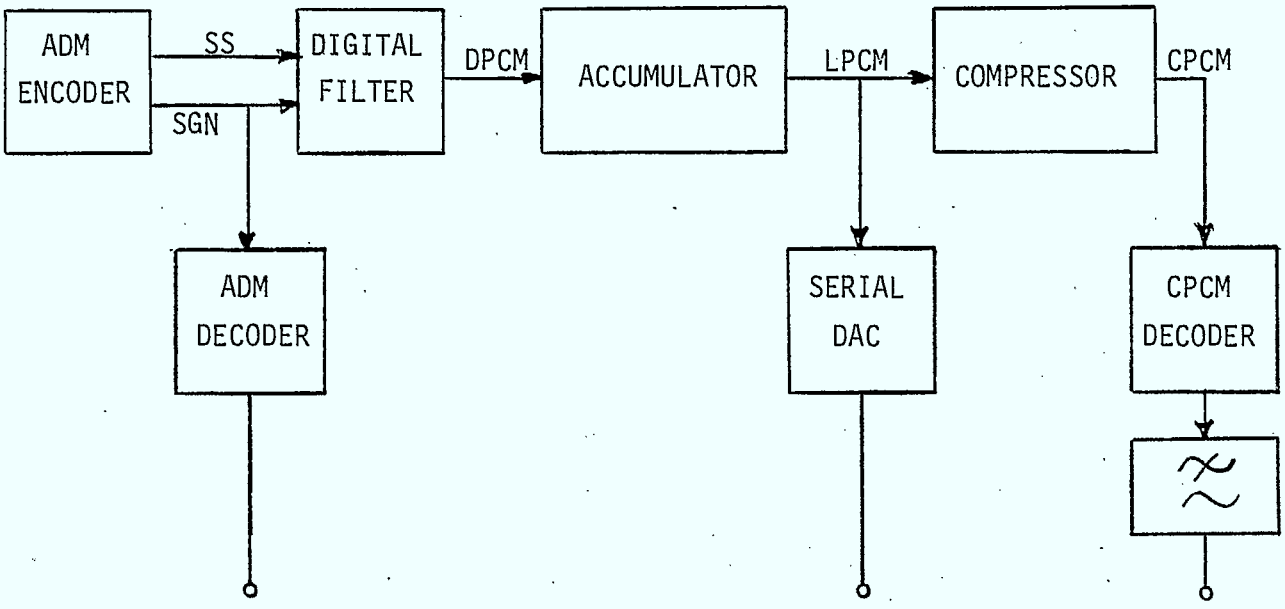


Fig. 20 Code conversion to CPCM

At 1 KHz test frequency, the 32 KBPS delta codec decoder had SNR approximately 26.5 dB when measured with 3 KHz flat noise weighting. Measurement of the LPCM output showed a 0.5 dB improvement due to the sharp cut off of the digital filter which slightly reduced the noise bandwidth. At lower amplitudes, truncation errors in the digital filter became the dominant source of noise and the SNR was substantially reduced.

Digital code conversion to CPCM and subsequent decoding introduced relatively little extra noise and the SNR was reduced to 26.0 dB in the region between overload and truncation noise. The measurement data is shown in the graph below.

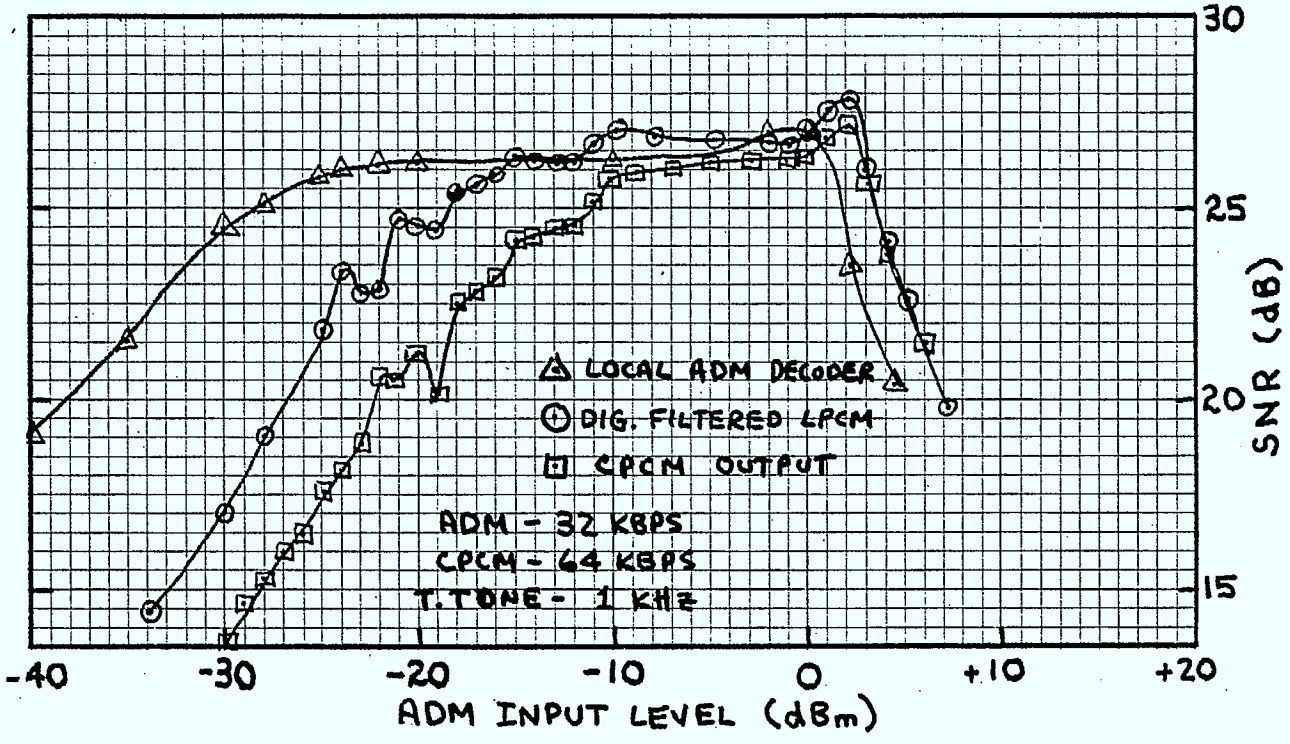


Fig. 21 EVSD - CPCM converter performance at 1 KHz

The effects of truncation in the filter and subsampling may be seen in several graphs. The filter has two sections each of which generate truncation noise. The noise at the output has noise components up to 32KHz originating from the second section. Noise contributed from the first section, however, is band limited by the second portion of the filter. Subsampling by a factor of 4 will fold over the noise which originates from the second filter section. The fold over noise will add on a power basis in the voice band. The resulting total noise will have one part from the first section and 4 parts from the second section. If each section generates an equal amount of truncation noise, subsampling will increase the noise to singal ratio by the factor 5/2. This represents a SNR decrease of 4 dB which can be observed between LPCM and CPCM at low amplitudes.

At 300 Hz test frequency, the SNR of the 32 KBPS delta codec was approximately 37.0 dB when measured with 3 KHz flat noise weighting. The LPCM output showed a 1.0 dB improvement again due to the reduced bandwidth of the digital filter. Truncation errors reduced the SNR of the LPCM output at lower amplitudes. The CPCM decoder output showed a 3.5 dB reduction in SNR when compared to the LPCM signal. This clearly shows the effect of the additional quantization. Measurement data is shown in the graph below.

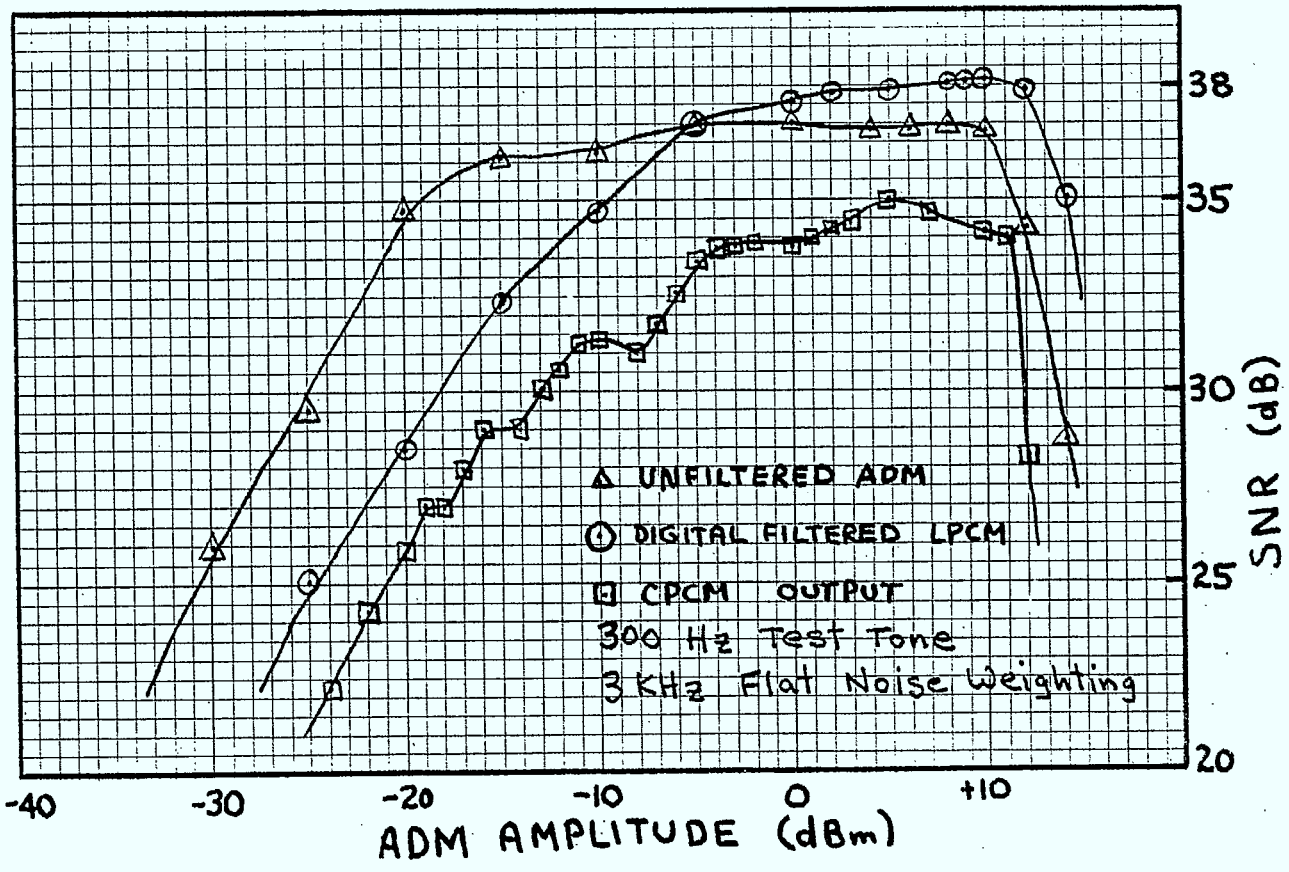


Fig. 22 EVSD - CPCM digital converter performance at 300 Hz

From previous measurements, the CPCM encoder-decoder SNR is approximately 40 dB when measured with a "C message" noise weighting filter. This corresponds to 38 dB when measured with a 3 KHz flat filter. Assuming that the noise from CPCM coding is not correlated with the noise from EVSD coding, the total noise may be calculated by taking the power sum of the two quantizing noises. A graph illustrating power addition is shown below. If the noise added in delta coding yeilds a 38 dB SNR and the noise added in CPCM coding also yeilds a 38 dB SNR then the cascade of both coders should result in a 35 dB SNR. This calculation is confirmed in the previous measurements.

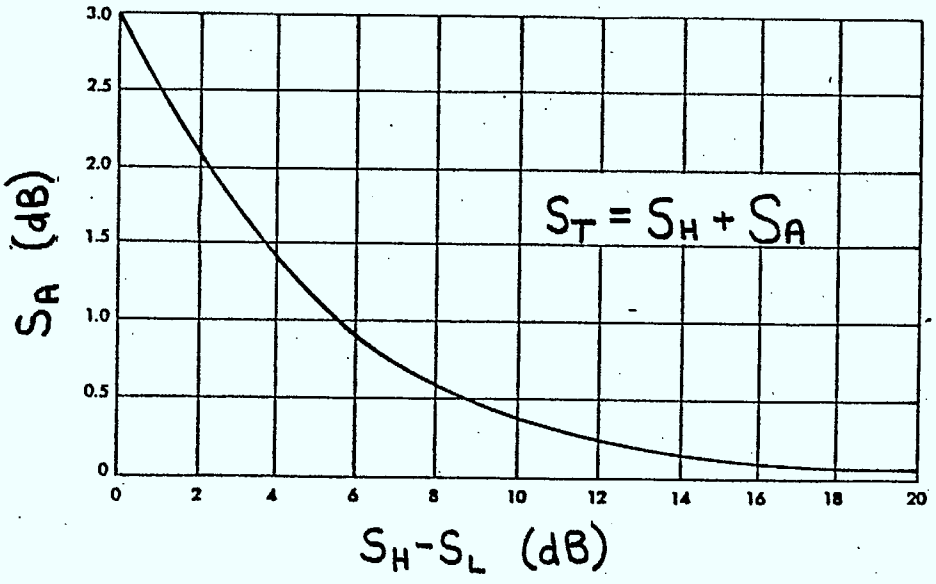


Fig. 23 Power sum of orthogonal signals

Gain vs amplitude measurements indicate a 1.5 - 2.0 dB gain in the conversion to LPCM and a 1.0 dB loss in the conversion from ADM to CPCM. These gain factors were nearly constant over the range +10 dBm to -30 dBm. for these measurements the digital filter was set with 18 dB (1/8) attenuation to compensate for its 24 dB processing gain.

Gain vs frequency measurements for the conversion to CPCM show the minor ripples in the digital filter response. At low frequencies the reduced gain is attributed to a slight difference in the leakage factors of the (feedback) analog integrator and the digital accumulator. Output response at frequencies above 4 KHz was due to excessive delta codec quantizing noise which had voice band energy.

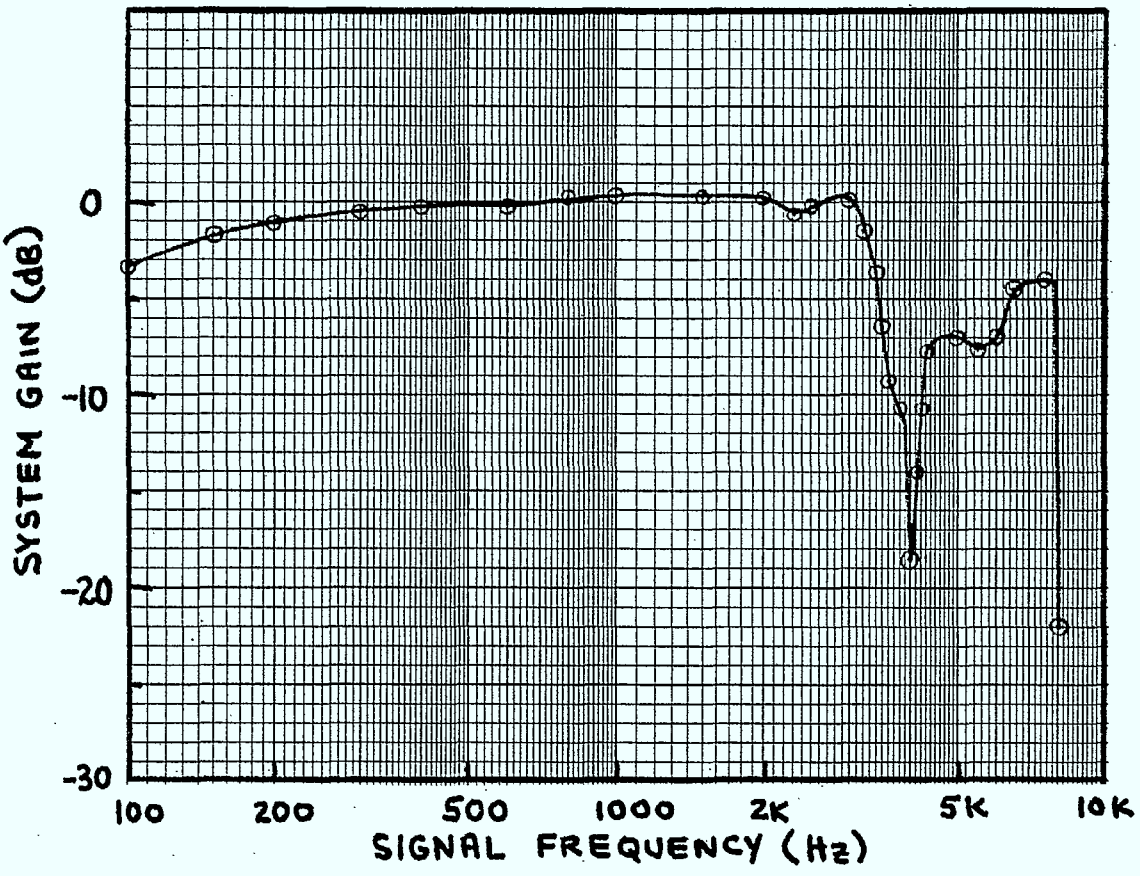


Fig. 24 CPCM Output versus Test Tone Frequency

3.7.2 Conversion to EVSD

The conversion from companded PCM to adaptive delta modulation (ADM) was studied by applying a sinusoidal signal to the CPCM codec. The output samples were processed to form ADM digital signals. For the purpose of comparative study, the DPCM signal from the digital filter was connected to the accumulator/compressor discussed in the previous section. The resulting block diagram is shown below.

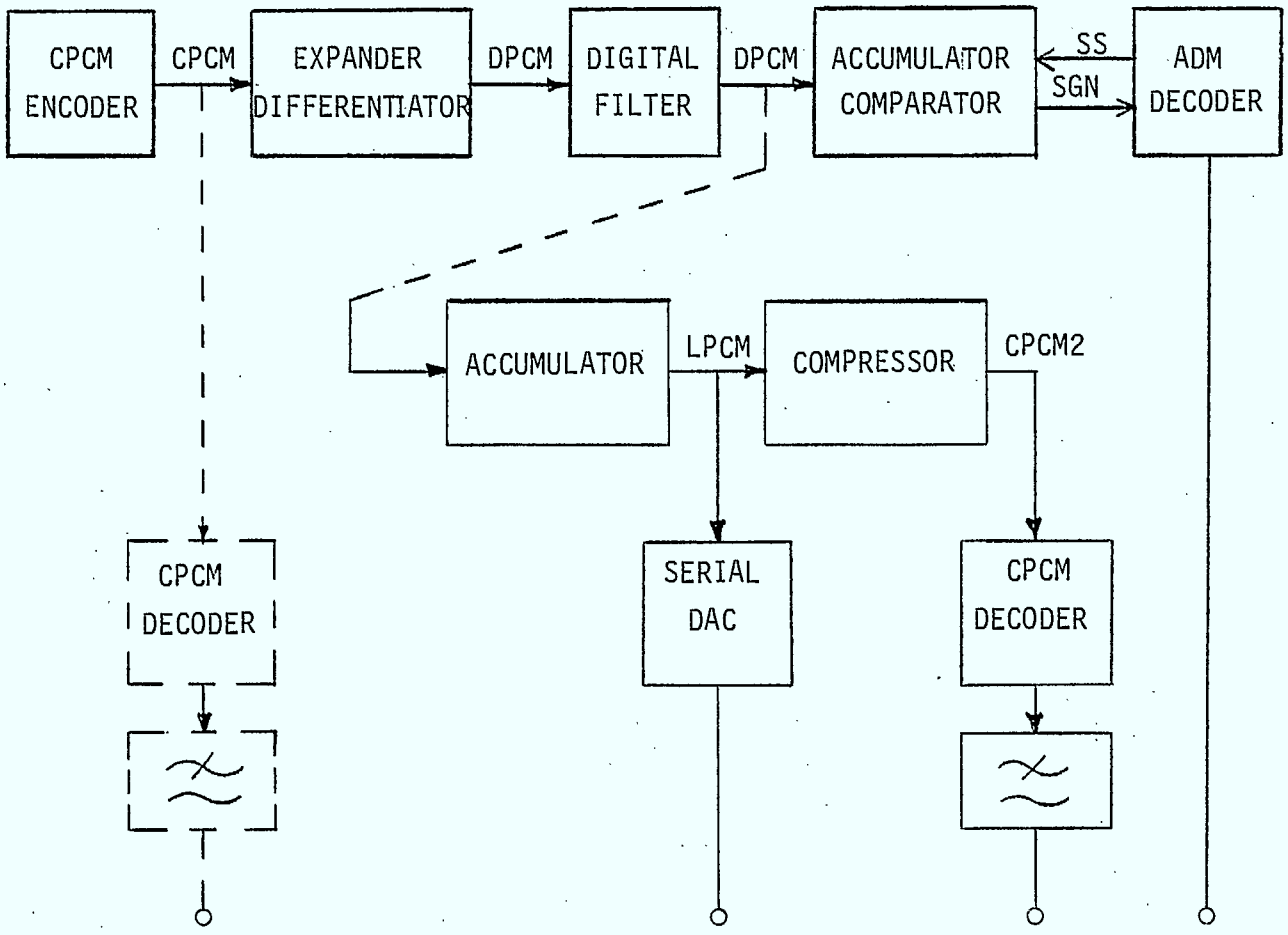


Fig. 25 Code Conversion to EVSD

At 1 KHz test frequency, the directly decoded CPCM had SNR approximately 40 dB when measured with "C message" noise weighting. A SNR of 38 dB would result if 3 KHz flat weighting were used. Measurement of the LPCM output shows a 39 dB SNR which reuslts from a slightly reduced noise bandwidth caused by the sharp cut off of the digital filter. The effects of truncation are evident at lower amplitudes.

Recoding to CPCM introduced the expected 3 to 4 dB additional noise resulting in a SNR of 35.5 dB. Recoding to EVSD delta modulation results in large quantizing noise and SNR approximately 26 dB. This compares closely with simply delta coding an analog signal. Measurement data is shown in the graph below.

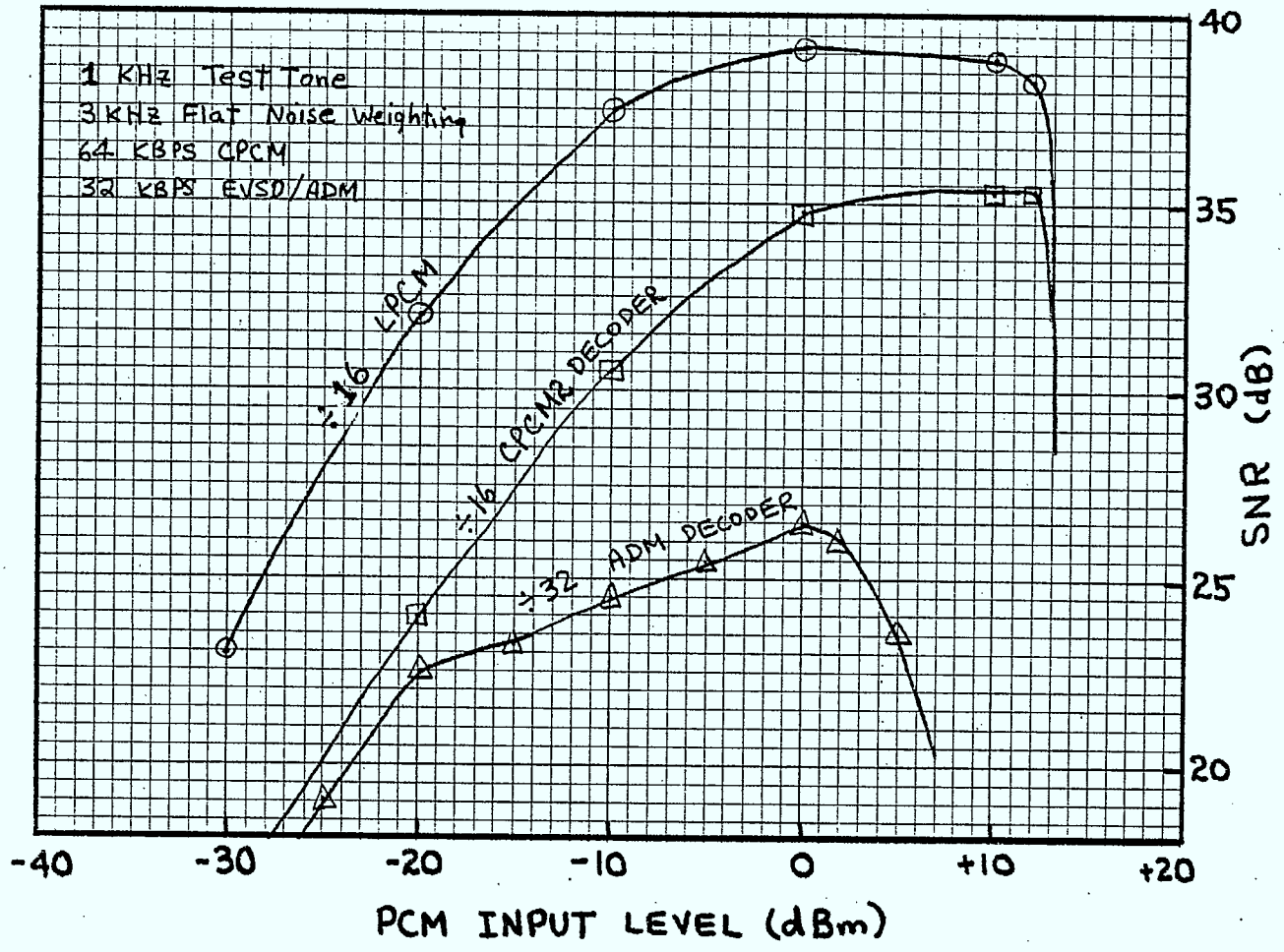


Fig. 26 CPCM - EVSD performance at 1 KHz

At 300 Hz test frequency, the direct CPCM decoded output has SNR approximately 39 dB. Measurement of the LPCm output shows a 39.5 dB SNR again attributed to the slightly reduced noise bandwidth. Digitally recoding to CPCM introduces an unexpectantly high loss of 5 dB in SNR. This compares with 3.5 dB loss in SNR between LPCM and CPCM which was observed in section 3.7.1. A possible explanation stems from the discussion in section 3.2.1. New PCM samples are given to the digital filter at every fourth sample of the filter. A spectral representation shows a signal components around 0Hz, 8KHz, 16KHz and 24 KHz. Noise components are centered about the same frequencies. Subsampling at 8 KHz folds over these image components which make no change in SNR if the filter has constant gain. If the filter is rectangular with cut off at 4 KHz and constant gain in the stop band (-25dB and in the passband (0dB) there is still no change in SNR. With the filter under study, the -25 dB signal components at 8 KHz and 24 KHz are effectively removed while the noise is relatively unchanged in the stop band. The correlated signal components must be subtracted on a voltage basis as follows.

$$\text{change in signal} = 20 \log[10^{0} - 10^{-25/20} - 10^{-25/20}] = -1 \text{ dB}$$

The SNR after subsampling is thus reduced by 1 dB.

The desired output of ADM shows a SNR of 35.5 dB which compares rather closely with the reverse sequence shown in section 3.7.1. Subsampling does not occur when the signal is recoded to ADM. Measured results are shown in the graph below.

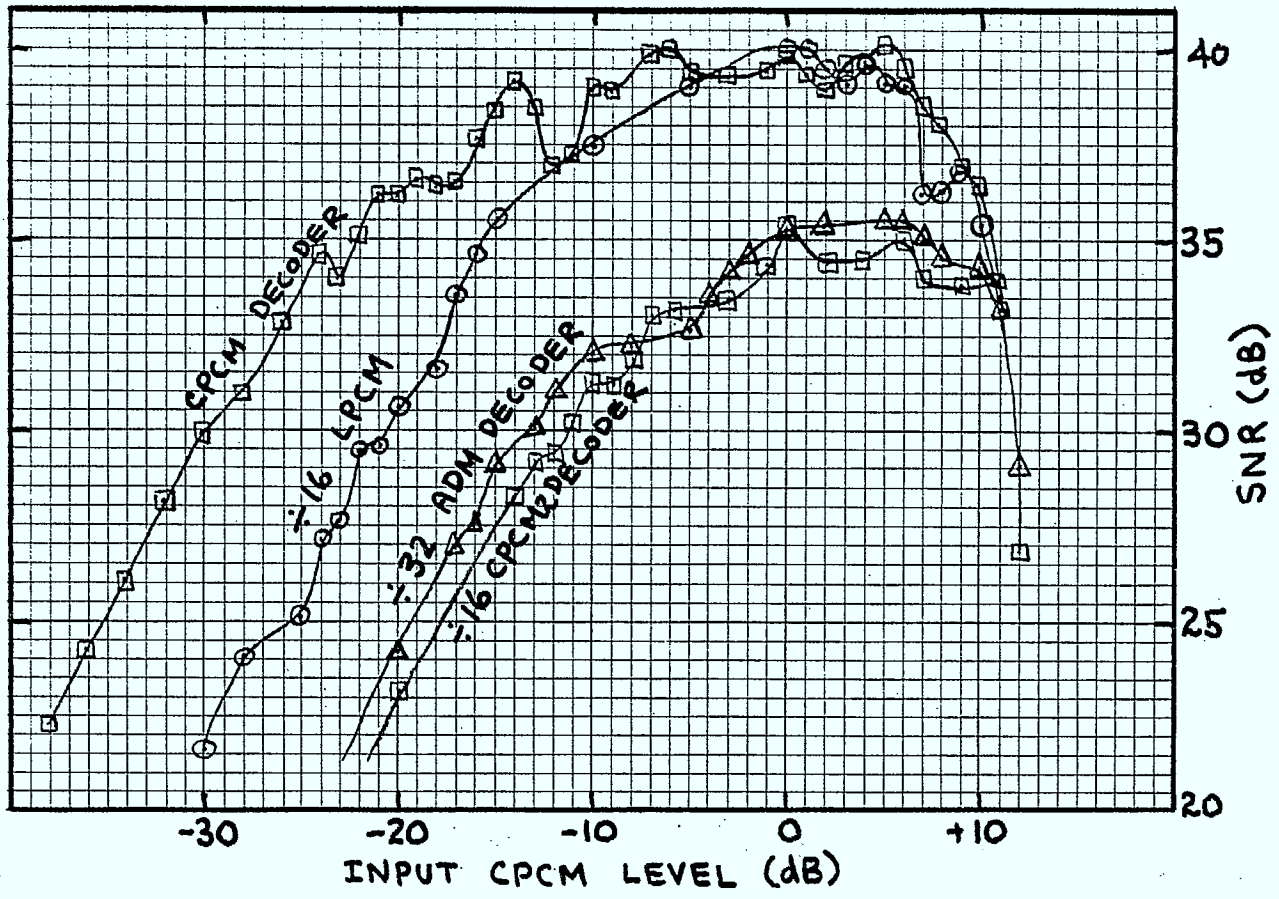


Fig. 27 CPCM - EVSD performance at 300 Hz

Gain vs amplitude measurements showed a 1.2 dB loss in the conversion from CPCM to ADM when the net filter gain was set at -6 dB (24 dB processing gain with 30 dB attenuation). The net filter gain was adjusted to 0 dB to get comparative measurements of LPCM and CPCM. The resulting gain factor was 0.8 dB for LPCM and -2.2 dB for CPCM. These gain factors were constant over the signal amplitude range of +10 dBm to -30 dBm.

Gain vs frequency measurements for the conversion to EVSD shows the ripples in the digital filter response. The cut off frequency is 3.4 KHz and the attenuation of 4 KHz is nearly 30 dB. The PCM coder has no input filter therefore aliasing occurs when the input frequency exceeds 4 KHz. A reverse image of the filter response occurs for input signals between 4 KHz and 8 KHz. the characteristic is shown below.

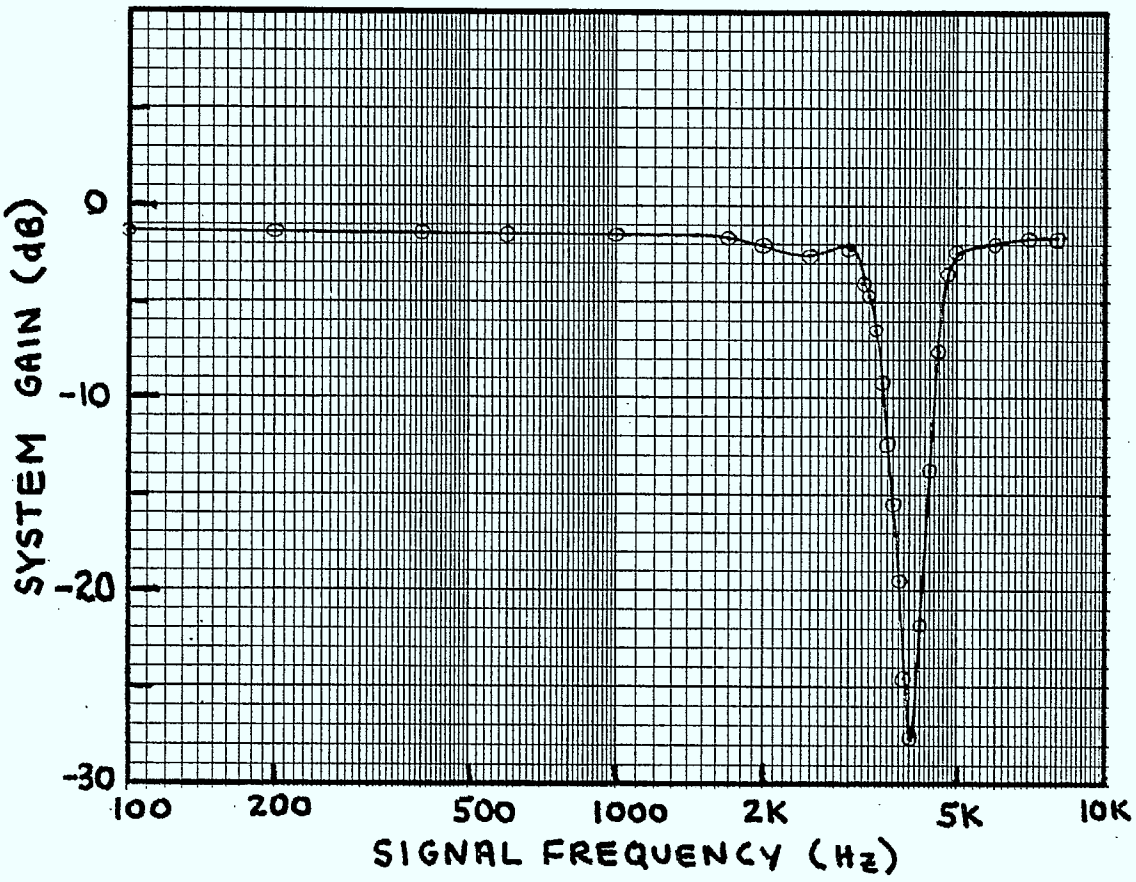


Fig. 28 EVSD output amplitude verses CPCM input frequency

4. Analog Interfacing of EVSD and CPCM

4.1 Analog Conversion to CPCM

Code conversion from ADM to CPCM may be conveniently acheived by decoding to analog and recoding in the CPCM format. A block diagram of the code conversion is shown below. It should be noted that, accurate, sharp cutoff analog filters are required for both the CPCM encoder and decoder.

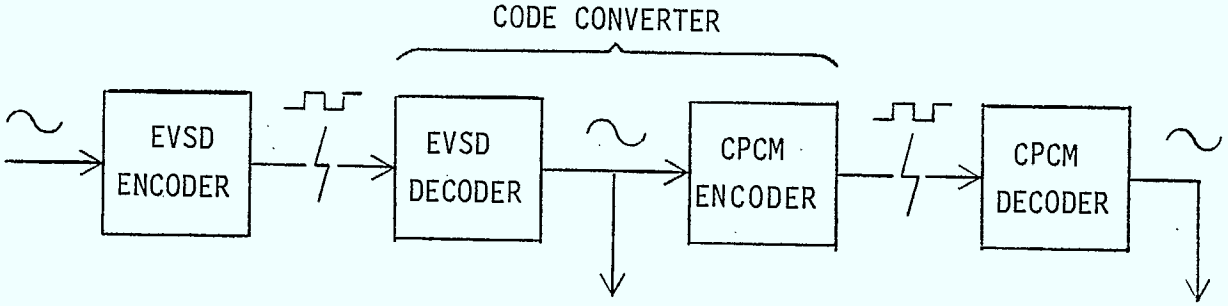


Fig. 29 Block Diagram of Analog Code Converter

Measurement data is shown graphically below. The results from the unfiltered ADM output illustrate that the 3 KHz flat noise weighting filter does not have sharp cut off in frequency. This has been shown in other measurements as well. If both codecs generate an equal amount of uncorrelated quantizing noise the total added noise would be 3dB larger than the individual contributions. In this case the added noise is 1dB larger for ADM. The cascade of the two codecs should result in total noise 2.5dB greater than simple ADM coding. This result is observable in the following graphs.

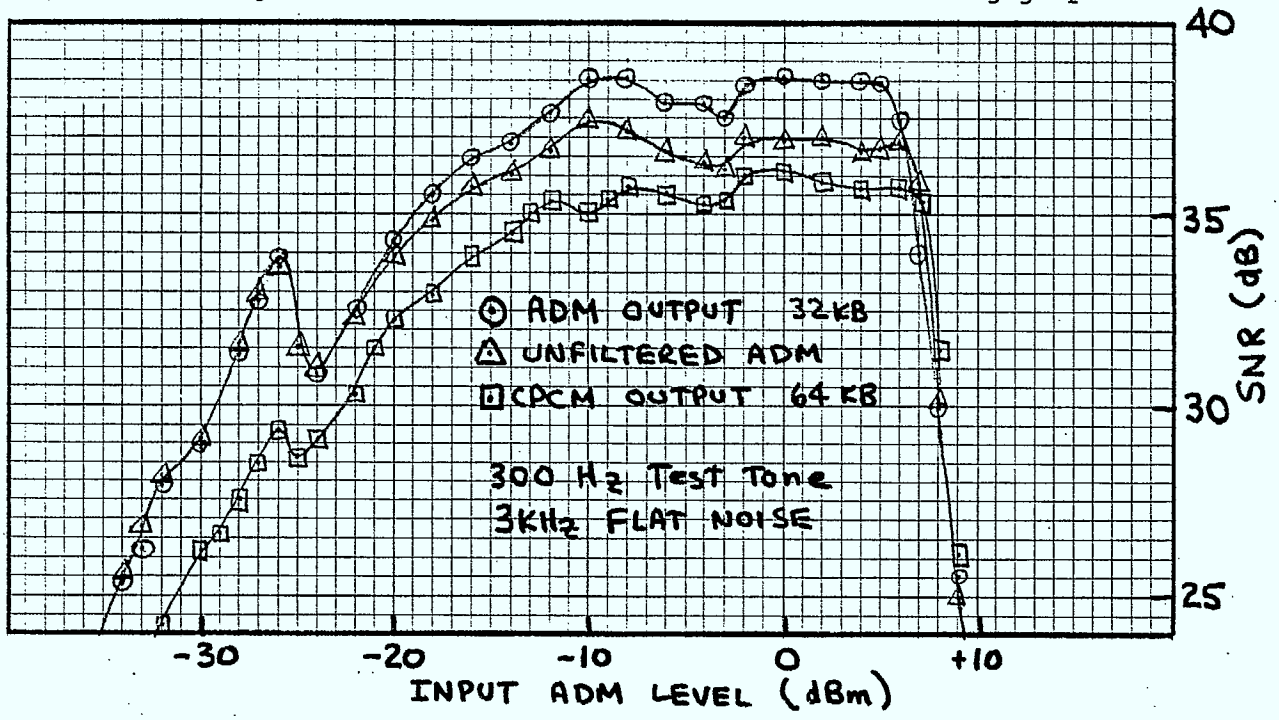


Fig. 30 EVSD - CPCM Conversion Performance with Analog Interfacing

4.2 Analog Conversion to EVSD

Code conversion from CPCM to ADM (EVSD) can also be achieved by decoding to analog then recoding in ADM. Measurements data is shown graphically below. As expected the product of 39dB SNR coding and 38dB SNR coding yeilds system SNR of 35.5 dB.

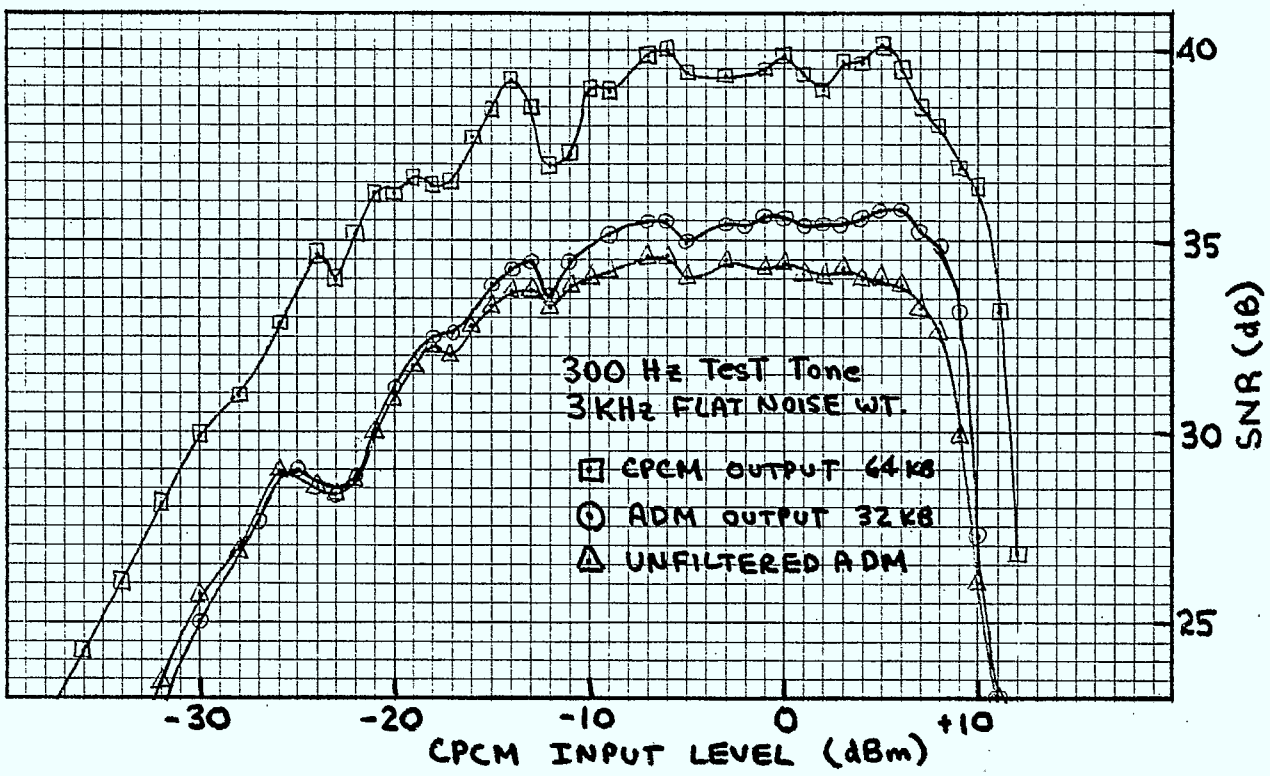


Fig. 31 CPCM - EVSD Conversion Performance with analog interfacing

5. Conclusion

As evidenced by the references, there has been substantial effort applied to digital code conversion at research establishments throughout the world. The major object of this work is to avoid the second quantization which occurs if the signal is decoded to analog. Other objectives may include the maintenance of digital format to avoid wire tapping and the possible economy of a single digital integrated circuit. The measured performance of the code converter described in this report exceeds that of similar systems listed in the references and approximates the performance of the technique using an analog interface. Although effort was made to reduce equivalent gate count by using serial processing and recursive filters, the bidirectional code converter requires approximately 3000 equivalent gates which is not practical at this time for a single custom LSI chip.

It can be seen in the digital implementation that 13 bit LPCM is reduced by the compressor to 8 bit CPCM. This necessitates truncation and introduces quantizing noise in the same manner as the analog input CPCM encoder. No advantage is gained by presenting a digital signal to the CPCM encoding process. Digital signal processing has the additional disadvantage of truncation noise (sample length = 16 bits) and fold over of noise components during subsampling. These latter effects have been kept to a minimum and the measured performance is nearly equal to that of the analog converter. In the conversion to EVSD, a numeric comparator is used to generate the binary ADM signal. This process introduces quantizing noise in the same manner as the analog input EVSD coder. No advantage is gained by maintaining the signal in digital format. The performances of analog and digital code conversion are similar.

In summary, the best and most simple method of code conversion between 8 KHz PCM and adaptive delta modulation is the analog technique where the signal is decoded and then recoded in the other format.

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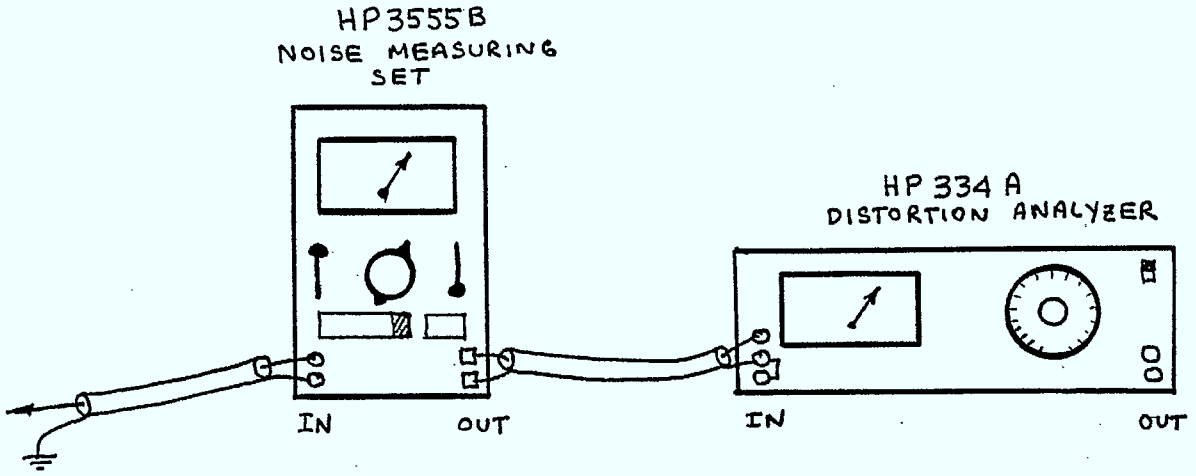
Papers of greatest relevance have been noted with *.

Appendix A1

Measurement Equipment

The following equipment arrangement was used to make SNR measurements.



Settings	Settings
Noise measurement 3 KHz Flat Noise Weighting 600Ω reference impedance	30 KHz low pass filter ON

Notes - The noise measuring set introduces a small amount of harmonic distortion prarticularly on the C message and Program weightings. The small distortion was not significant for the signals in this report.

- The power cord of the noise measuring set introduced considerable noise if the source impedance was high. This was a problem when the noise set followed the distortion meter. The input impedance of the noise measuring set is approximately 10K.
- The auto balance on the Distortion was more effective when the input signal was pre-filtered.
- the gain on the Noise Measuring Set was used to keep the output nearly constant. This simplified the operation of the Distortion Meter.

Appendix A2

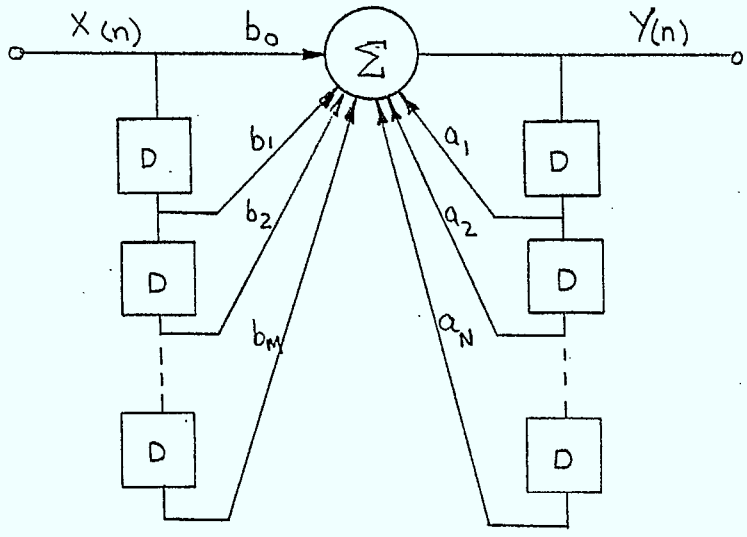
Digital Filter Fundamentals

Appendix A2

Digital Filter Theory

Discrete time filters combine delay elements with signal summation to create a network response which varies with the frequency of the input signal. Although delay elements for continuous signals (transmission lines or surface acoustic wave devices) may be used, it is most common to use sampling and clocked delay circuits (charge coupled devices) to delay the analog signal. If the signal is both sampled and quantized, digital logic circuits may then be used for the delay and numeric summation. Parallel or serial arithmetic units may be used depending on the application. It should be added that each delayed signal is added to the output with a different weighting. For analog signals this can be accomplished with different resistances in a summing network. Quantized numeric signals, however, require a relatively complex digital multiplier for each delayed signal.

All the above implementations may be represented by the block diagram below. The blocks marked D indicate a unit delay. For sampled signals the unit delay is typically one sample period. Delayed samples of the input are added with multiplying coefficients b_0, b_1 ... b_M. At some frequencies the added signals will cancel and the output will remain at zero. The delayed input signals contribute zeros to the transfer function. Delayed samples of the output are fed back and summed to form a new output signal. At certain frequencies, the delayed output signals add in phase resulting in positive feedback and output which is larger than the input. Delayed output signals contribute poles to the transfer function.



$$Y_{(n)} = \sum_{k=1}^{N} a_k Y_{(n-k)} + \sum_{k=0}^{M} b_k X_{(n-k)}$$

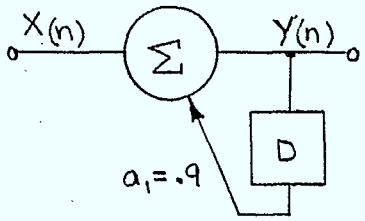
We can determine the following transfer function using the Z transforms shown below.

$$H_{(Z)} = \frac{Y_{(Z)}}{X_{(Z)}} = \frac{\sum_{k=0}^{M} b_k Z^{-k}}{1 - \sum_{k=1}^{N} a_k Z^{-k}}$$

$$Y_{(n)} \longrightarrow Y_{(Z)}$$

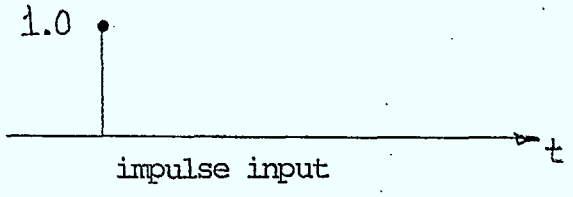
$$Y_{(n-k)} \longrightarrow Y_{(Z)} \cdot Z^{-k}$$

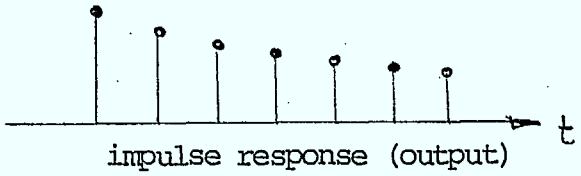
Example 1 In this example the output signal is fed back after one unit delay. A fraction of this signal is used to form the next output sample.



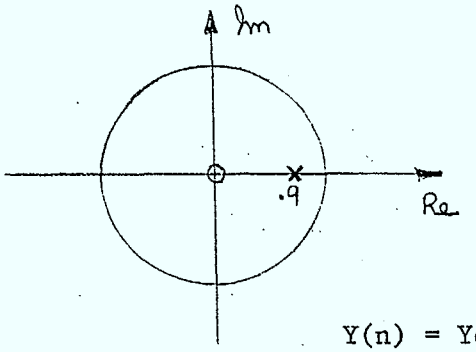
$$Y_{(n)} = X_{(n)} + a_1 Y_{(n-1)}$$

$$H_{(Z)} = \frac{1}{1 - a_1 Z^{-1}}$$



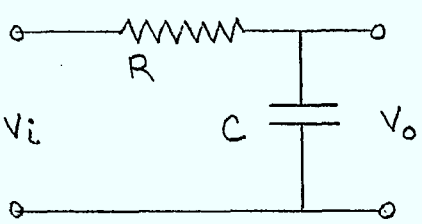


The transfer function, $H_{(Z)}$, becomes infinite when the digital frequency variable $Z = a_1$



$$Y(n) = Yo\ e^{-nT/a_1}$$

An equivalent circuit for continuous signals is a simple RC network.

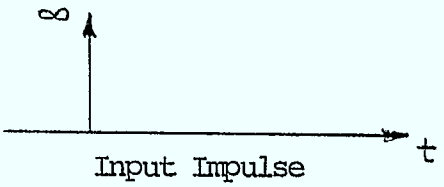


$$V_o = \frac{1}{C}\int i\,dt = \frac{1}{C}\int \frac{V_o - V_{in}}{R}\,dt$$

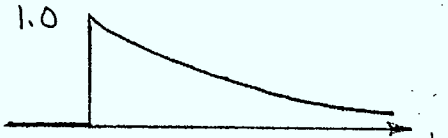
$$H_{(s)} = \frac{V_o(s)}{V_{in}(s)} = \frac{1/sC}{R+1/sC} = \frac{1}{sCR+1}$$

Transfer function $H_{(s)}$ becomes infinite when frequency variable $S = -1/RC$

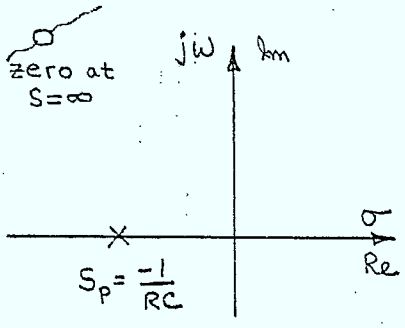
$$H_{(S)} = \frac{Sp}{S+Sp} \quad \text{when } Sp = \frac{1}{RC}$$



Input Impulse



Impulse response (output)



We can compare the discrete time and continuous time filters as follows

Digital $\quad Y_n = Y_o\, a_1^n$

Analog $\quad Y_{nT} = Y_o\, e^{S_p nT}$

$\Big\}\quad a_1 = e^{S_p T}$

The analog decay time constant $\tau = RC = \frac{-1}{\sigma} = \frac{-1}{S_p}$

The time constant of the digital filter may be developed as follows

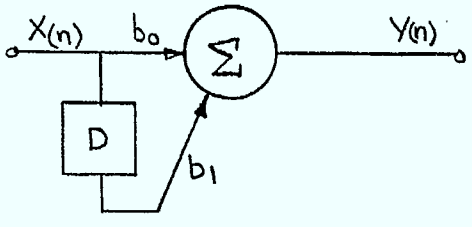
$$S_p = \frac{1}{T} \ln a_1$$

$$\tau = \frac{-1}{S_p} = \frac{-T}{\ln a_1}$$

$$\tau \simeq \frac{T}{1-a_1} \quad \text{if } a_1 \longrightarrow 1 \qquad \text{i.e.: for } a_1 = .9$$

$$\ln a_1 = -.105$$

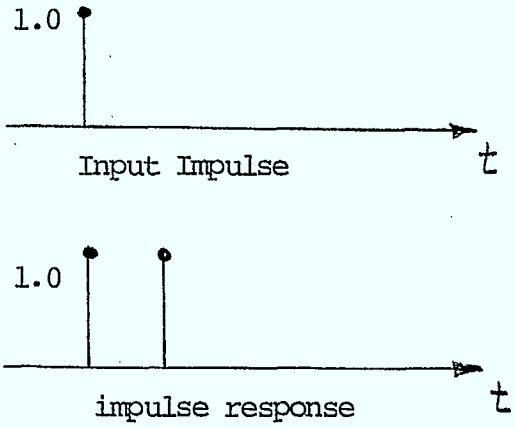
Example 2 The input signal is delayed and added with the new input to form an output.

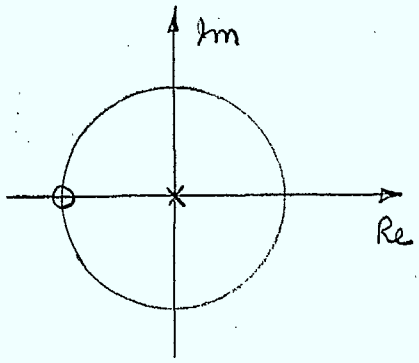


$$y_{(n)} = b_o x_n + b_1 x_{(n-1)}$$

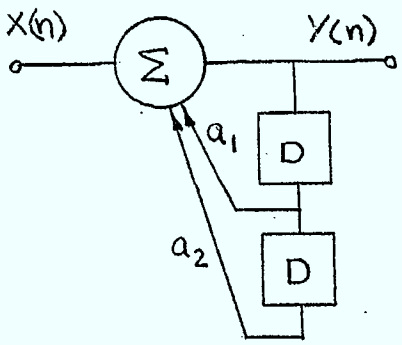
$$H_{(Z)} = b_o + b_1 Z^{-1}$$

The transfer function $H_{(Z)}$ becomes zero when the digital frequency variable $Z = -1$. There is a pole at $Z = 0$. This assumes that $b_o = 1$ and $b_1 = 1$





Example 3 Complex poles may be created by using two delays in the output signal.



$$Y_{(n)} = x_n + a_1 Y_{(n-1)} + a_2 Y_{(n-2)}$$

$$X_{(n)} = Y_{(n)} - a_1 Y_{(n-1)} - a_2 Y_{(n-2)}$$

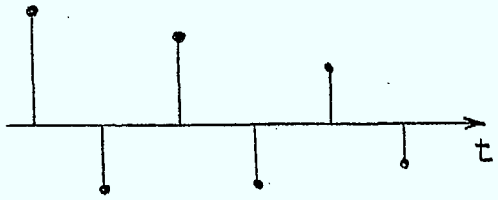
$$X_{(Z)} = Y_{(Z)} \left(1 - a_1 Z^{-1} - a_2 Z^{-2}\right)$$

$$H_{(Z)} = \frac{1}{1 - a_1 Z^{-1} - a_2 Z^{-2}}$$

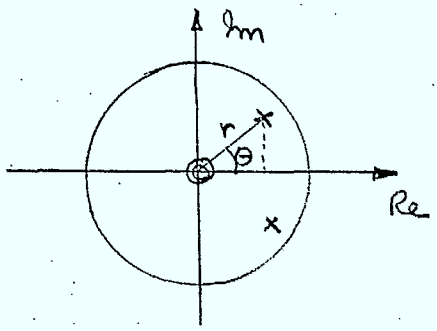
Denominator is zero for poles

i.e. $Z = \frac{+a_1}{2} + \frac{1}{-2}\sqrt{a_1^2 + 4a_2}$

For complex poles a_2 negative and $|a_2| > \left(\frac{a_1}{2}\right)^2$



Impulse Response



pole at r/θ

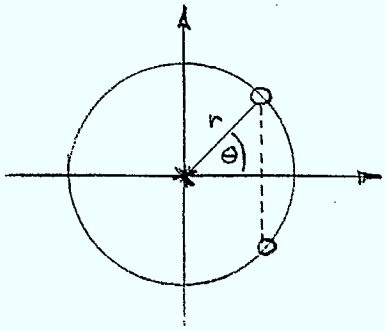
where $a_2 = -r^2$

see page 169 oppenheim

$$a_1 = 2r \cos\theta$$

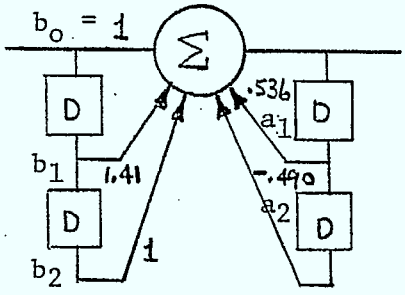
NOTE Complex zeros may be generated by delaying the input then summing.

$$H_{(Z)} = b_o + b_1 Z^{-1} + b_2 Z^{-2}$$



$$\text{If } b_o = 1 \quad \begin{cases} b_2 = r^2 \\ \text{Then} \quad b_1 = -2r\,\text{Cos}\theta \end{cases}$$

Example 4 The following section may be used to generate 2 poles and 2 zeros.



Design zeros at 6 KH_Z on the unit circle $\theta = 180^o \pm 45^o$

$r = 1$

zero locations at $-.707 \pm .707$

$b_2 = r^2 = 1$

$b_1 = -2r\text{Cos}\theta = +1.41$

Design poles at 3KH_Z and assume 16 KH_Z sampling $\theta = \frac{3}{16} \times 360^o = 67.5^o$

Let radius vector to pole be .7 to give a pole with moderate Q.

Pole locations, design values are $.268 \pm j.646$

$a_2 = -r^2 = -.49$

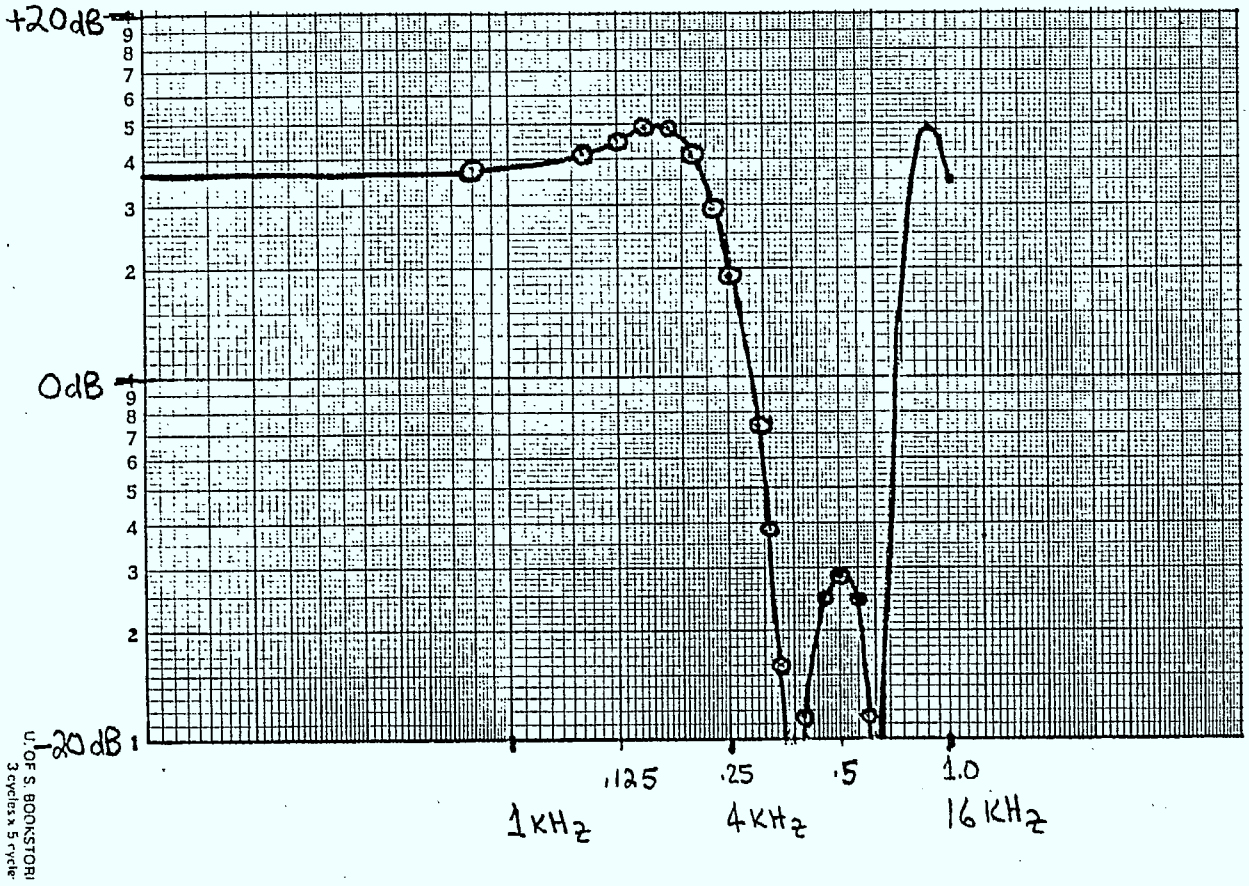
$a_1 = 2r\text{Cos}\theta = (1.4)(.382) = .536$

Computation of Filter Response

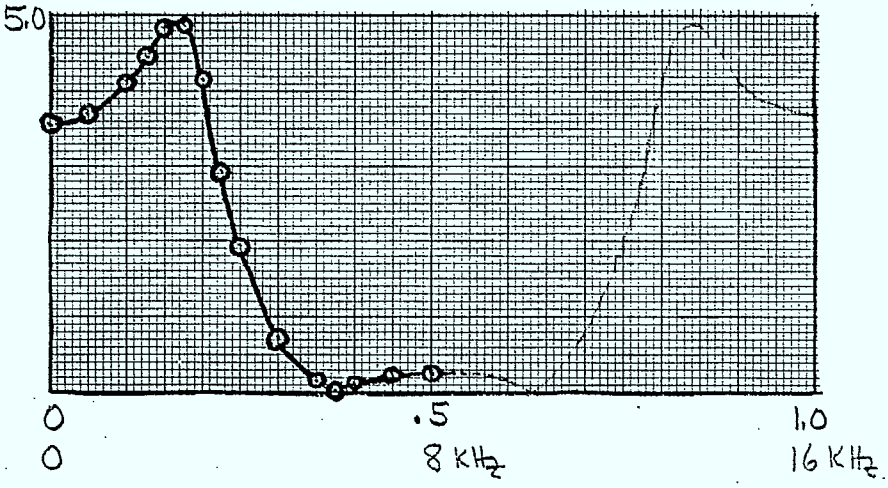
The following BASIC program has been written to calculate the response of digital filters. The response in Example A4 has been calculated and graphs have been prepared.

POLE2

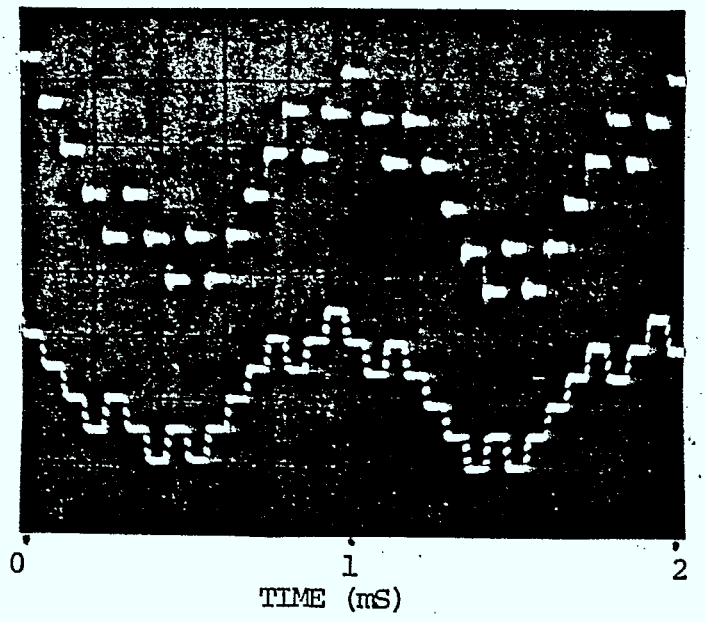
```
5 PRINT "ENTER TWO POLES"
10 INPUT P1,P2
25 PRINT "ENTER TWO ZEROS"
30 INPUT Z1,Z2
42 FOR N=1 TO 5
45 PRINT "ENTER NORMALIZED FREQUENCY"
50 INPUT F
60 F1=COS(F*2*π)
70 F2=SIN(F*2*π)
80 PRINT "RE=";F1,"IM=;F2
82 V1=1
84 V2=0
90 A1=P1
95 A2=P2
100 GOSUB 1000
140 A2=-P2
150 GOSUB 1000
160 A1=Z1
170 A2=Z2
180 GOSUB 1100
200 A2=-Z2
210 GOSUB 1100
220 PRINT V1,V2
230 NEXT N
240 END
1000 V1=V1/((F1=A1)↑2+(F2-A2)↑2)↑.5
1010 V2=V2-ATN((F2-A2)/(F1-A1))
1020 RETURN
1100 V1=V1*((F1-A1)↑2+(F2-A2)↑2)↑.5
1110 V2=V2+ATN((V2-A2)/(F1-A1))
1120 RETURN
```

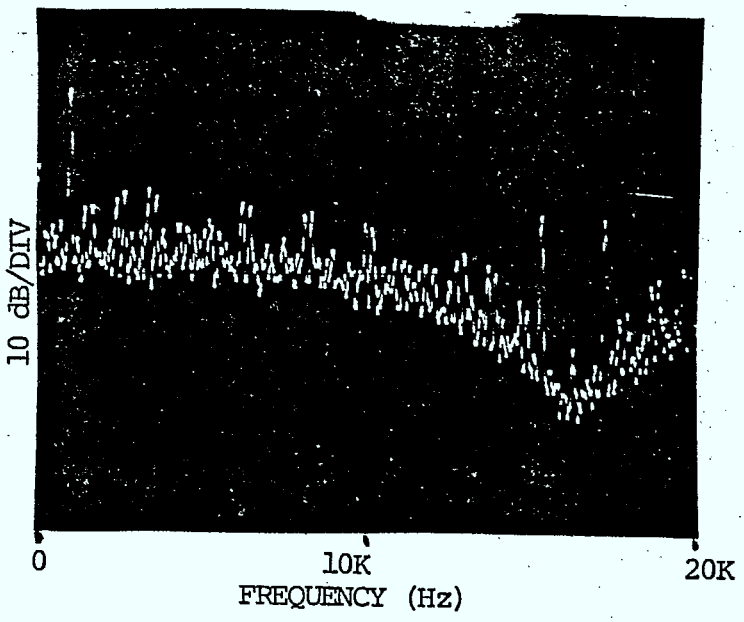


U. OF S. BOOKSTORE
3 cycles x 5 cycle



The two following photographs illustrate the unfiltered accumulator output signal with 16 KB sampling and a 1 KHz modulation signal x(t). The lower waveform shows the analog approximate signal $\hat{x}(t)$. The frequency spectrum shows the 1 KHz component at -15 dB and an approximately flat noise spectrum which has a null at the sampling rate of 16 KHz.



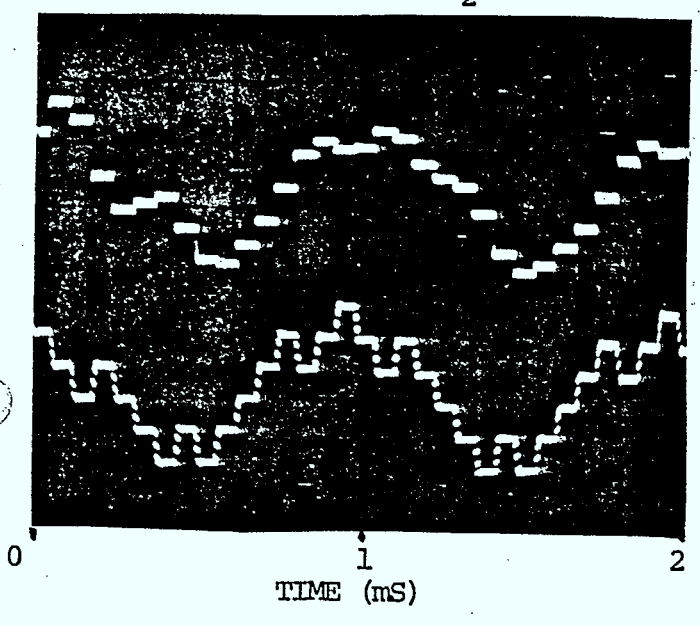


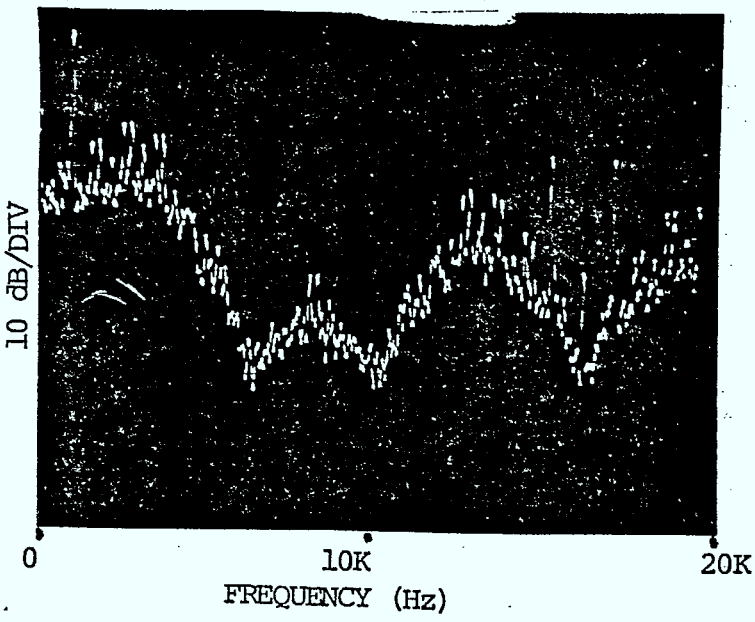
The two photographs below illustrate the accumulator output with digital filtering. The modulation signal and the sampling rate remain at 1 KHz and 16 KHz respectively. The filter has a pole frequency at 6 KHz. The pole has a radius of .707 in the Z plane. The frequency spectrum shows the 1 KHz component at -4 dB, peaking in the noise spectrum at approximately 3 KHz and a null in the noise spectrum at 6 KHz. The filler coefficients are as follows:

$a_1 = +.5$ $\quad b_0 = 1.0$

$a_2 = -.5$ $\quad b_1 = 1.5$

$\quad\quad\quad\quad b_2 = 1.0$



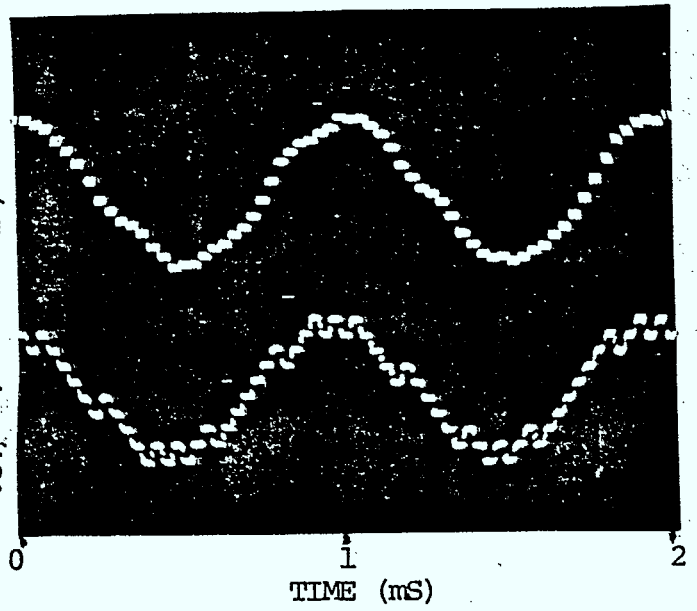


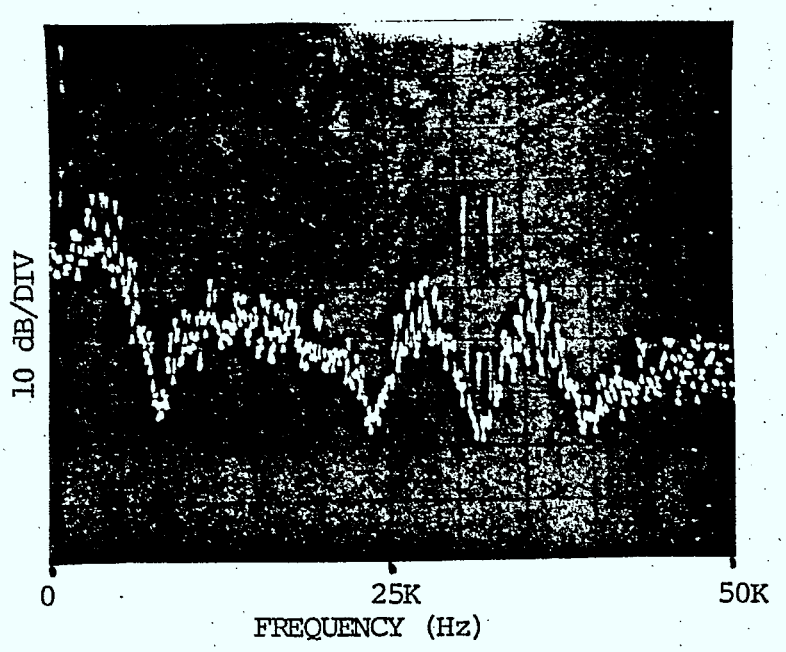
The digital filter was operated at 32 KB and the tap coefficients were changed to provide a pole at 4 KHz and a zero at 8 KHz. Waveforms and output frequency spectrum are shown below. Note the frequency scale has been changed to 5 KHz/division. The filter coefficients are as follows:

$a_1 = 1.0$ $\quad b_0 = 1.0$

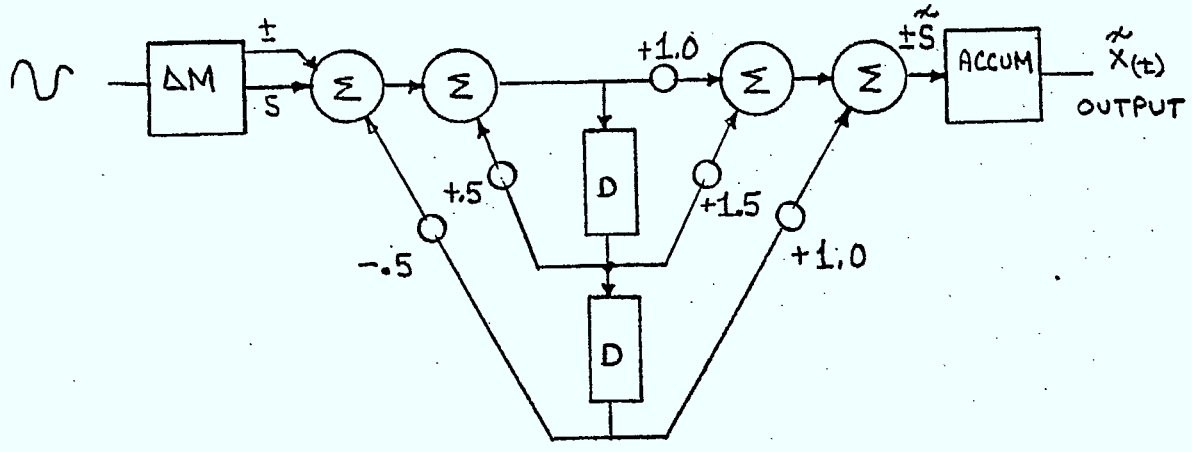
$a_2 = .5$ $\quad b_1 = 0$

$\quad\quad\quad\quad\quad\quad\quad\quad b_2 = 1.0$

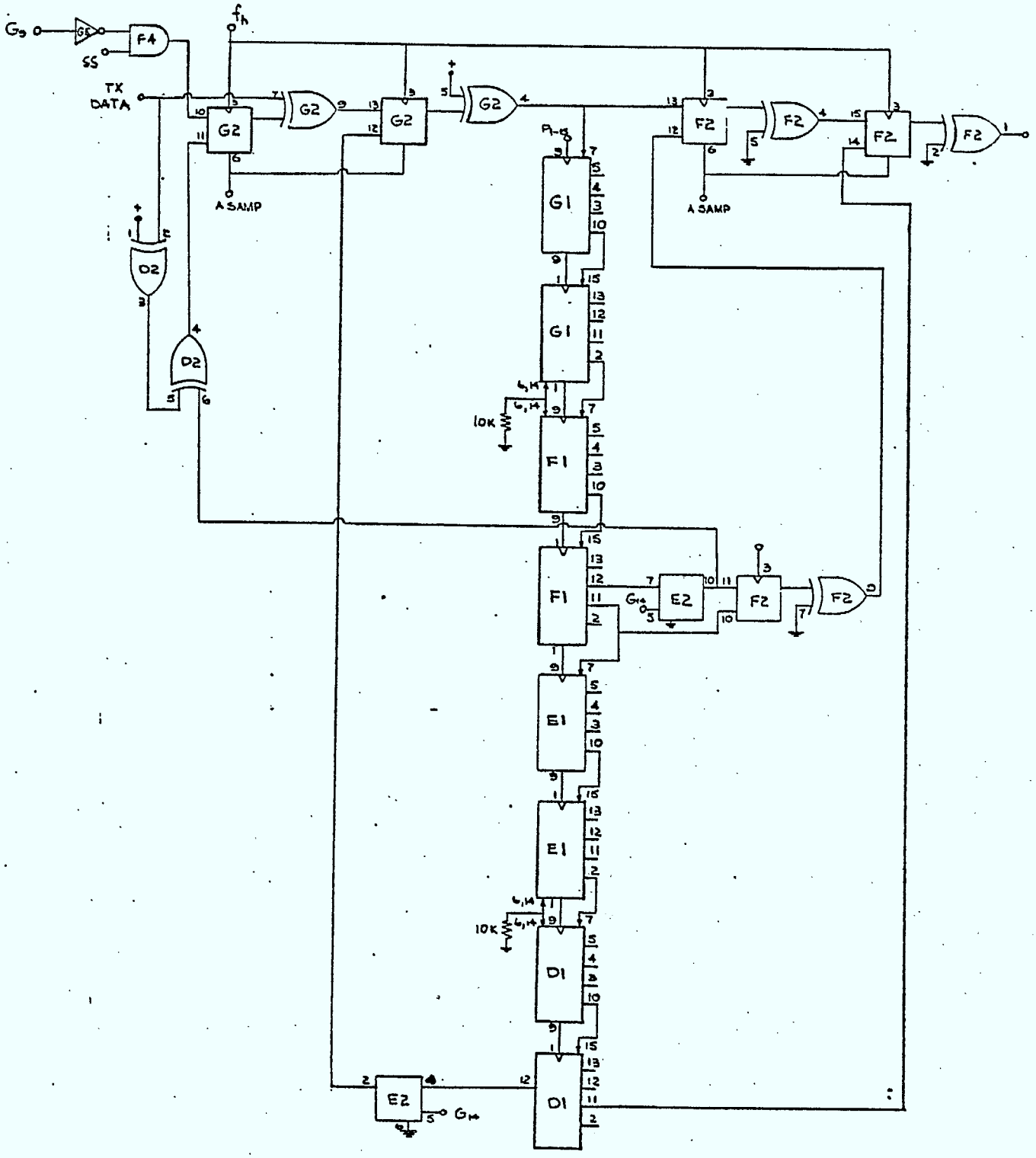




A block diagram of the filter structure is shown below followed by a logic diagram of the filter.



Logic Diagram of Single Filter Section.



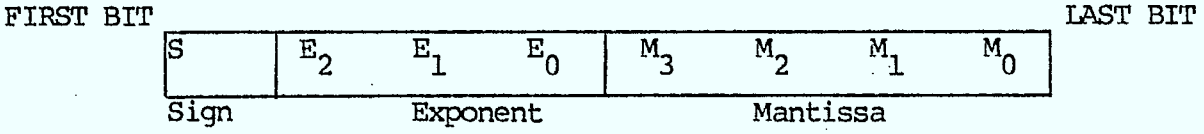
Appendix A3

Compressed Coding for PCM Transmission

Compressed Coding for PCM samples

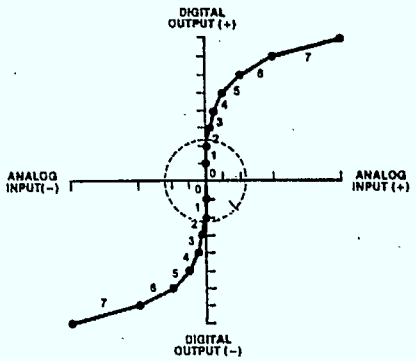
Preceived signal quality can be maintained for both large and small signals if the quantizer step size is reduced for small signals. As discussed in the following section, quantizer resolution can be adapted with time, based on the recent signal history. If the signal amplitude is small all step sizes in the quantizer are slowly decreased. Alternately, a time invariant, non-uniform quantizer can offer fine resolution for small signals and coarse resolution for large signals. This latter approach is used in companded PCM coding.

In digital computing, a wide range of numeric values can be represented in a fixed binary word length by using floating point (scientific) format. The binary word is separated in two parts to represent a signed binary mantissa and a signed binary exponent. In this case, the mantissa is not in logaritmic form; the represented number is obtained by multiplying the mantissa times 2 to the power of the exponent. Analog voice samples are represented with 8 binary bits for PCM transmission. One bit represents sign, 3 bits represent positive exponent and 4 bits are used to represent mantissa. Bits are transmitted serially, sign bit first, as they would be generated by a successive approximation A/D converter.

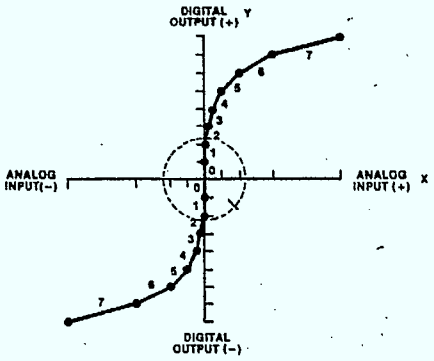


If the mantissa were to represent the values 0 through 15, the sample value of zero could be represented by several codewords, each with a different exponent. A similar situation exists for other small sample values. In practice, the mantissa is used to represent values between 16 and 31 which results in an unique codeword for each sample value. The mantissa may be considered to have a fifth bit M_4 which is always 1 and need not be transmitted. This representation, however, does not have codewords to represent sample values between 0 and 15.

Two coding schemes "A law" and "Mμ law" have been developed to allow representation of signals near zero. The "A law" coding modifies the E = 0 segment to have the same slope as the E = 1 segment thus including input values near zero. In "Mμ law" coding, an offset is subtracted from the floating point value so that samples near zero may be represented. When both positive and negative transfer characteristics are plotted, the segments on both sides of zero become co-linear. This results in 15 segment "Mμ law" and 13 segment "A law" characteristics. These points are illustrated in the following graphs and tables.

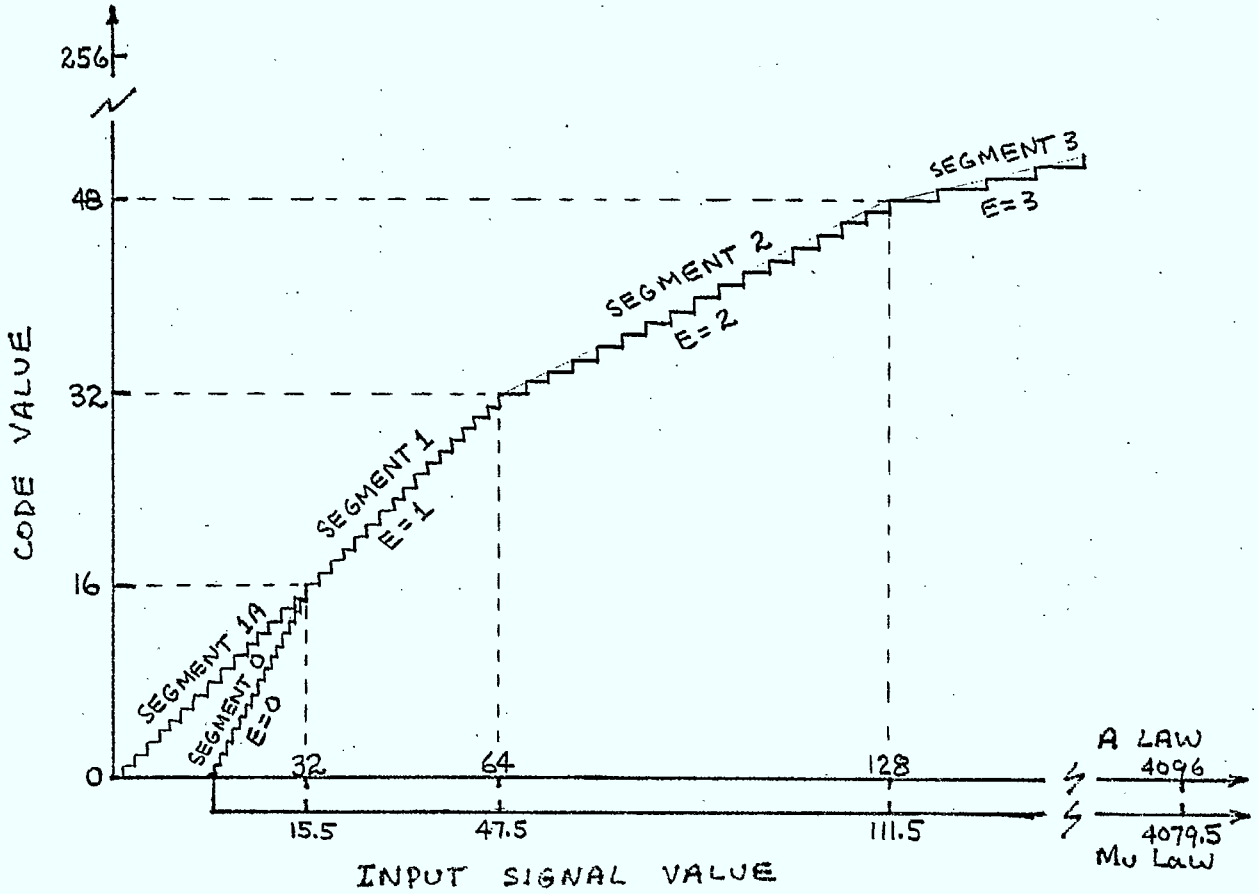


A-Law Transfer Function



μ-Law Transfer Function

PMI



The tables which follow illustrate encoding and decoding levels. Voltages in each quantizing range are converted to a single codeword. The best approximation to the input is acheived at the decoder by generating the mid value of the input quantizing range. In the tables below, each input unit is approximately equal to 0.4 millivolt. In A law coding, for example, input voltages between 0 and .8 mV will be decoded at .4 mV. Input voltages between .8 and 1.6 mV will be decoded as 1.2 mV.

CODE VALUE - MANTISSA	Code Value - EXPONENT 0	1	2	----	7
15	32 } 31 30 }	64 } 63 62 }	128 } 126 124 }	---- ----	4096 } 4032 3968 }
-	- -	-	- -		
-	- -	-	- -		
-	- -	-	- -		
-	- -	-	- -		
2	6 } 5 4 }	38 } 37 36 }	76 } 74 72 }	---- ----	2432 } 2368 2304 }
1	4 } 3 2 }	36 } 35 34 }	72 } 70 68 }	---- ----	2304 } 2240 2176 }
0	2 } 1 0 }	34 } 33 32 }	68 } 66 64 }	---- ----	2176 } 2112 2048 }
Quantizer bin size	2	2	4	----	128

+4096 ⇒ 3.14 dBmO
-4096

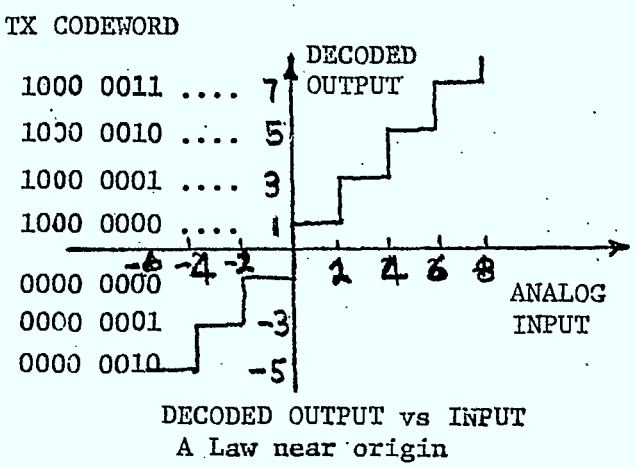
INPUT/OUTPUT LEVELS verses CODE Values
(13 segment, A law)

CODE VALUE - MANTISSA	Code Value - EXPONENT 0	1	2	---	7
15	15.5 } 15 14.5 }	47.5 } 46.5 45.5 }	111.5 } 109.5 117.5 }	---	4079.5 } 4015.5 3951.5 }
-	-	-	-		
-	-	-	-		
-	-	-	-		
-	-	-	-		
-	-	-	-		
-	-	-	-		
2	2.5 } 2 1.5 }	21.5 } 20.5 19.5 }	59.5 } 57.5 55.5 }	--- ---	2415.5 } 2351.5 2287.5 }
1	1.5 } 1 0.5 }	19.5 } 18.5 17.5 }	55.5 } 53.5 51.5 }	--- ---	2287.5 } 2223.5 2159.5 }
0	0.5 } 0 -0.5 }	17.5 } 16.5 15.5 }	51.5 } 49.5 47.5 }	--- ---	2159.5 } 2095.5 2031.5 }
Quantizer bin size	1	2	4	---	128

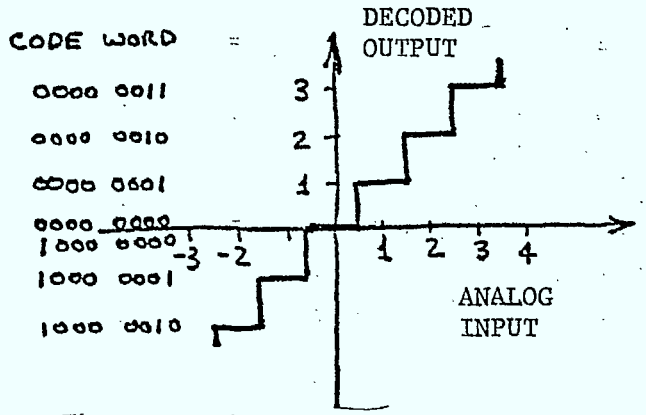
+4079 ⇒ 3.17 dBmO
-4079

INPUT/OUTPUT LEVELS verses CODE VALUES
(15 segment, Mμ law)

Modern PCM coding equipment uses direct digital coding. The segmented characteristic is implemented either through multiplying D/A conversion techniques or by high accuracy linear conversion followed by digital companding. To produce Mμ law code, the linear codec would require 13 bits to have a minimum step size of 1 and a maximum range of ± 4080. The CCITT recommendation G.711 as recorded in Orange Book Vol. III specifies the segmented format for Mμ law with a Mid Tread characteristic specified either by code value +0 or code value -0. The mid tread quantizer avoids idle noise at the output when the input is less than one LSB peak to peak. In digital transmission systems, it is often difficult to meet the idle channel specifications for telephone circuits. This 15 segment characteristic is attained by subtracting 16.5 from the floating point representation previously discussed. The smallest decoded level is then at zero and the lowest encoding bin extends from -0.5 to +0.5. The mid tread encoding characteristic and the decoding equations are given below for both A law and Mμ law coding.



DECODED OUTPUT vs INPUT
A Law near origin



DECODED OUTPUT vs INPUT
μ LAW NEAR ORIGIN

Encoding Threshold (A Law)

$= 2^E \times (M + 16)$ E=0

$= 2 \times (M)$ E=0

Encoding Threshold (Mu Law)

$= 2^E (M + 16) - 16.5$

Decoded Output Value (A Law)

$= 2^E \times (M + 16.5)$ $E \neq 0$

$= 2 \times (M + .5)$ $E = 0$

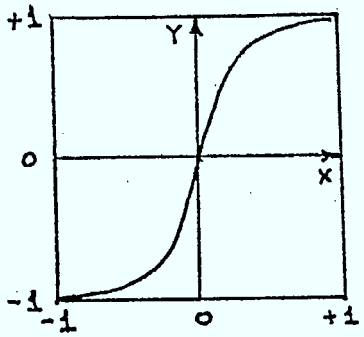
Decoded output (Mμ Law)

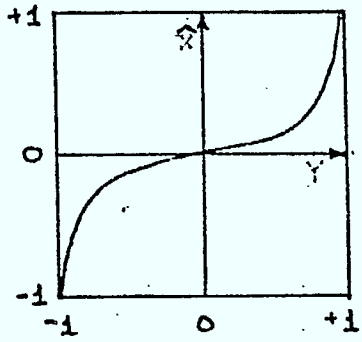
$= 2^E \times (M + 16.5) - 16.5$

In Mu law, the binary digits shown are always inverted for transmission to maximize the number of binary 1's which are sent when the circuit is idle or one party is listening and not talking. Frequent logic 1's are required by the clock recovery circuits in transmission line repeaters.

Analog Companding

When PCM equipment was first introduced, companded coding was achieved by using a nonlinear compressor followed by a linear A/D converter. The input compression characteristic was approximately logarithmic and was matched by a complimentary exponential expander following the decoder. The compressor characteristic given in the equation and graph below was first implemented with $\mu = 100$ followed by 7 bit coding. More recent equipment uses 8 bit coding and $\mu = 255$ compression. The word companded is a contraction of the words compressed and expanded.





$$y = \frac{\ln(1 + \mu x)}{\ln(1 + \mu)} \qquad x \leq 1 \qquad y \leq 1$$

$$y = 0.180 \ln(1 + 255x) \qquad \hat{x} = \frac{(1 + \mu)^{y} - 1}{\mu}$$

Although A law is not implemented with analog circuitry, continuously variable equations have been written which closely approximate the 13 segment characteristic. The variables X and Y have been normalized to the range $0 \leq X \leq 1$ and $0 \leq Y \leq 1$ resulting in the equation:

$$Y = \frac{1 + \ln(Ax)}{1 + \ln(A)} \qquad 1 \leq Ax \leq A \qquad y = 0.183[1 + \ln(87.6x)]$$

$$Y = \frac{Ax}{1 + \ln(A)} \qquad Ax < 1 \qquad y = 0.183(87.6x)$$

Mu Law versus A Law

Examining the digital line signal for each format reveals that the sign bit = 1 for positive values in both cases. For zero input signal, the exponent and mantissa bits are all 0 for A Law and all 1 for Mμ Law. Digital line repeaters require frequent 1's to maintain accurate bit timing for transmission. The 'inverted' coding in Mμ law is ideally suited for this constraint. In A law transmission systems, a bipolar violation channel coding technique, known as high density binary three (HDB3), is used to prevent the transmission of more than 3 consecutive zeros.

Although the number of transmitted bits is the same in each code, the Mμ law coding reuslts in almost 6dB wider dynamic range. As a trade off, M law coding results in slightly reduced SNR quality at lower signal levels. This will be illustrated in the graphs which follow. The mid-riser characteristic of A law coding limits the idle channel noise to -70 dB relative to a full load sinusoid. [Ref. Koneko] The mid-treaad characteristic of Mμ law can result in zero decoded idle noise.

Transmission systems are frequently measured using sinusoidal test signals. Signal to quantizing noise ratio for companded coding may be calculated by considering the time spent in each segment together with the quantizing noise in each segment. An example calculation is shown for a full load sinusoid with Mμ law coding.

$$\text{Average Noise Power} = \sum_{E=0}^{7} \frac{(\text{bin size}_E)^2}{12} \times \text{Probability of being in segment E}$$

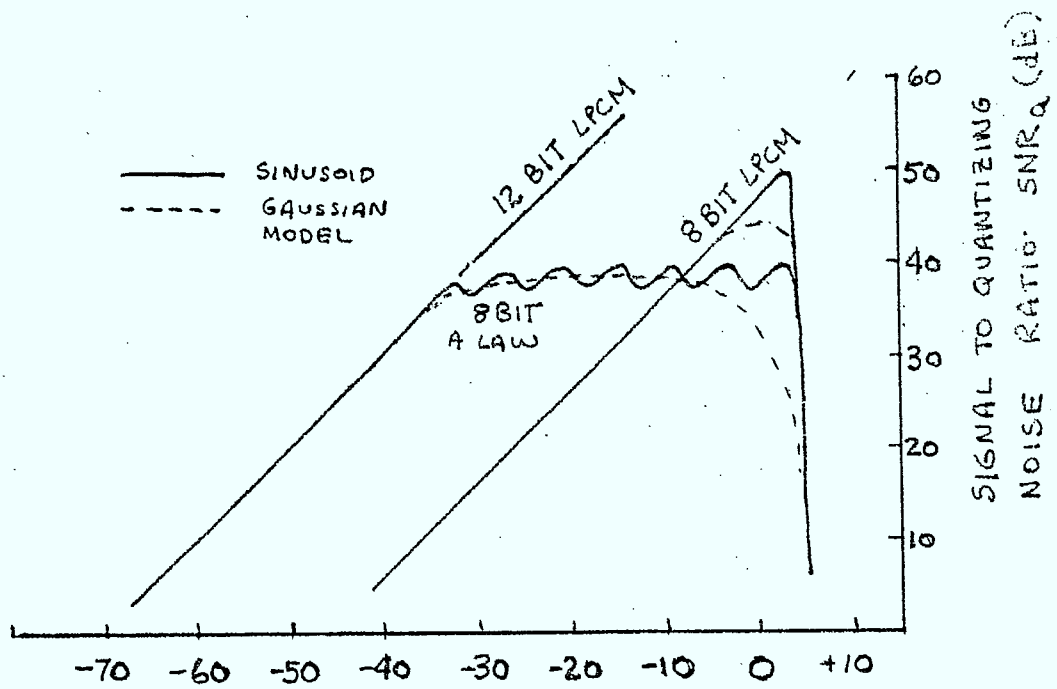
$$\overline{e^2} = \sum_{E=0}^{7} \frac{(S_E)^2}{12} \cdot P_E$$

$$\overline{e^2} \simeq \frac{(128)^2}{12} \cdot \frac{2}{3} + \frac{(64)^2}{12} \cdot \frac{1}{6} + \frac{(32)^2}{12} \cdot \frac{1}{12} + \ldots \simeq 974$$

$$\text{SNR} = \text{Ave } x^2 / \text{Ave } e^2 = \frac{1}{2} (4079)^2 / 974$$

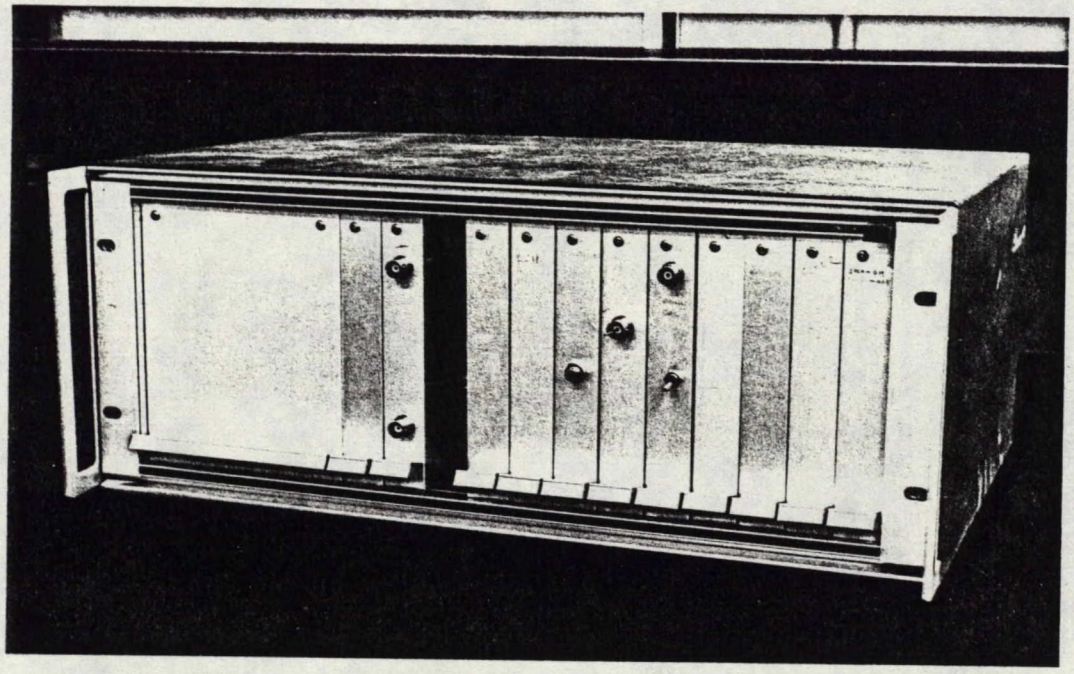
SNR = 39.3 dB

If the sinusoid peak value is reduced to middle of the highest segment (3/4 full load) the SNR decreases to 37 dB. As the sinusoid level is further decreased, less time is spent in the upper segment, noise decreases substantially and the SNR begins to increase. This is illustrated in the graphs which follow. The graphs also indicate SNR for speech like signals. This is represented by a Laplacian (negative exponential) amplitude distribution. Signal and noise have a bandwidth equal to half the sampling rate. Speech signal distortion may be approximated by averaging sinewave SNR in the region near the speech amplitude level.

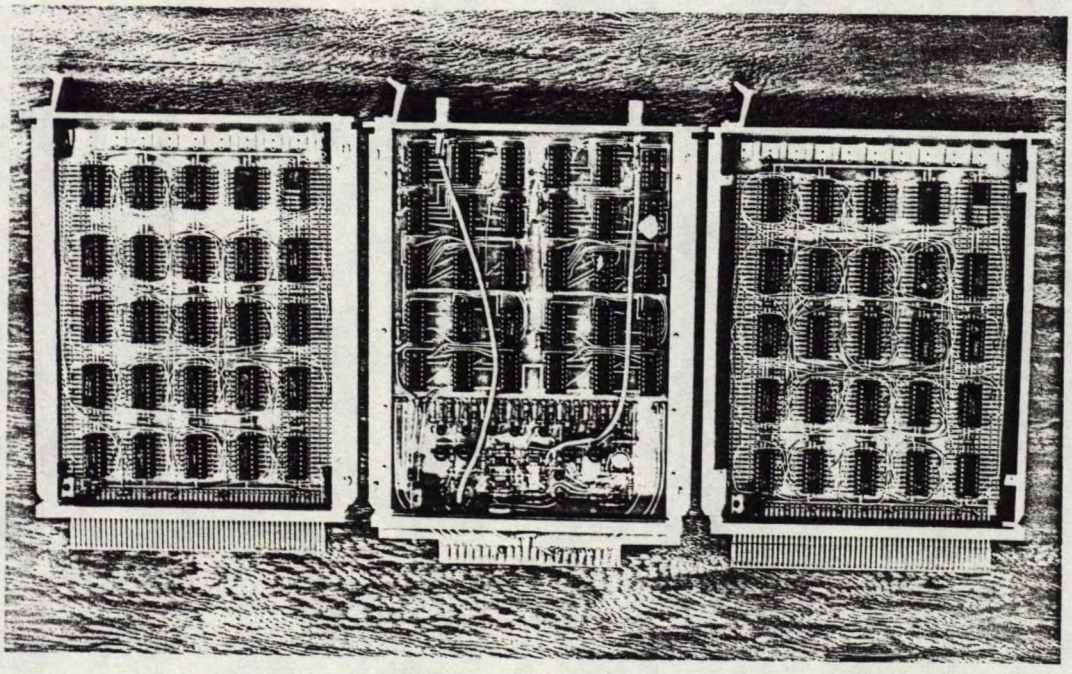


Appendix A4

Schematic Diagrams for CPCM to EVSD Conversion



Complete Bidirectional Code Conversion System



Digital Filter and Delta Codec Circuits

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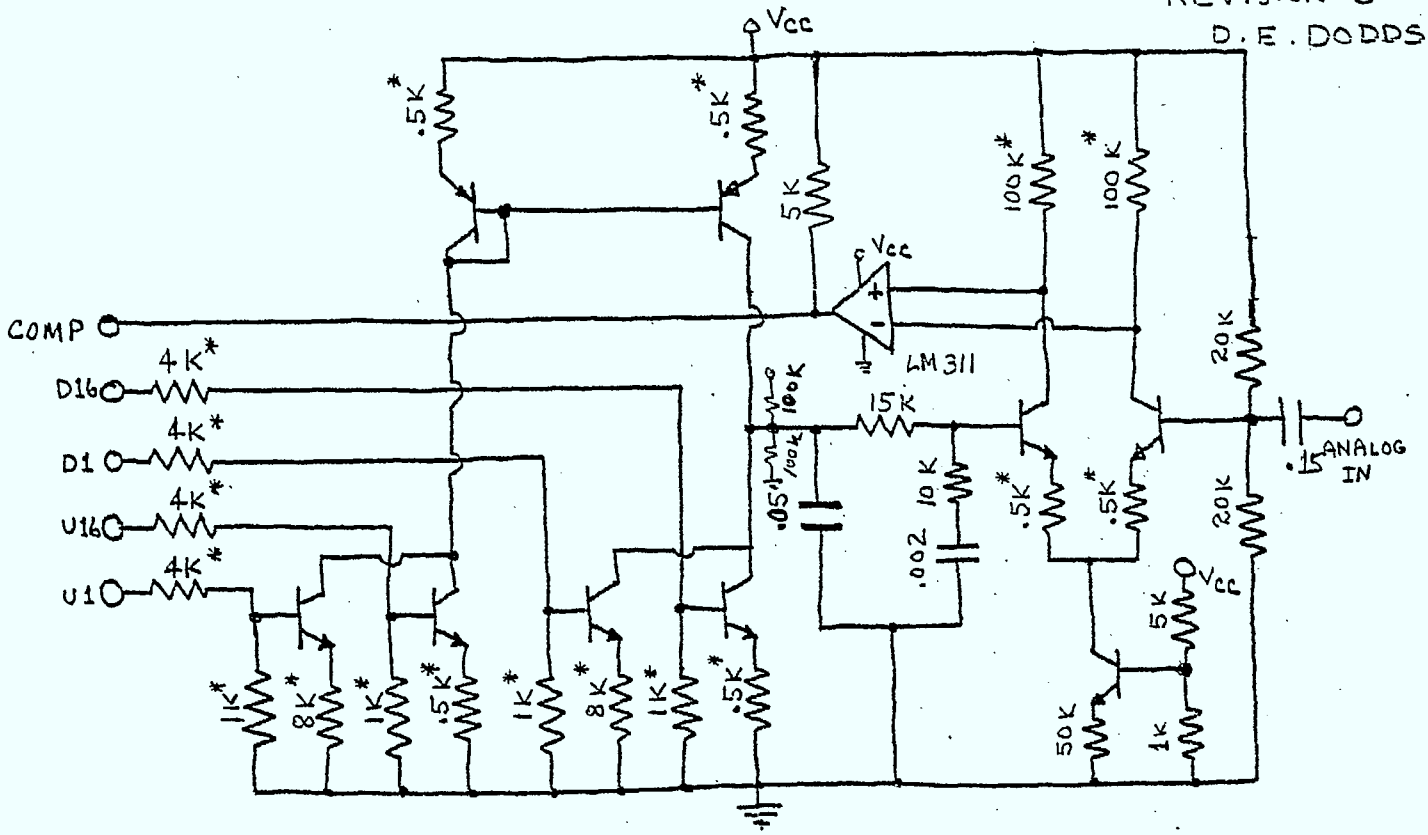
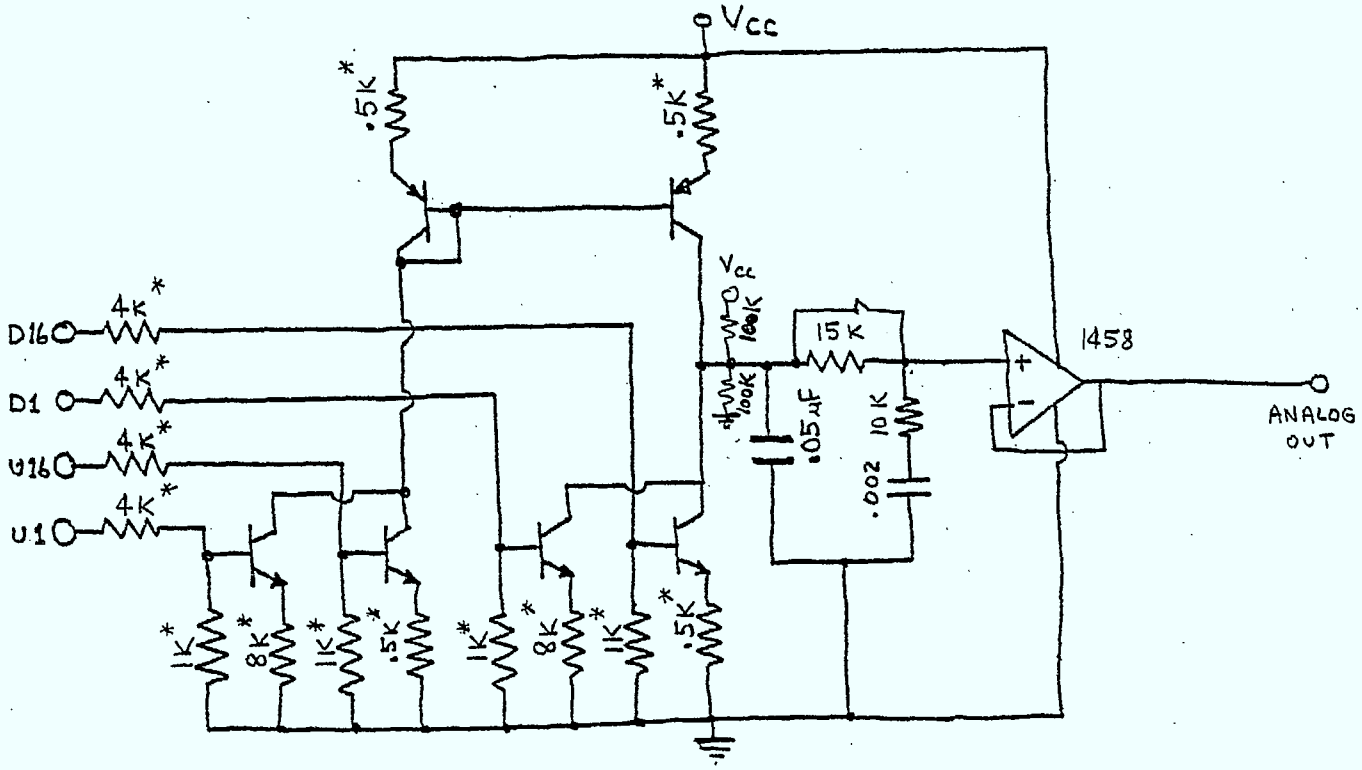
D.E. DODDS





DELTA MODULATOR ANALOG CIRCUITS

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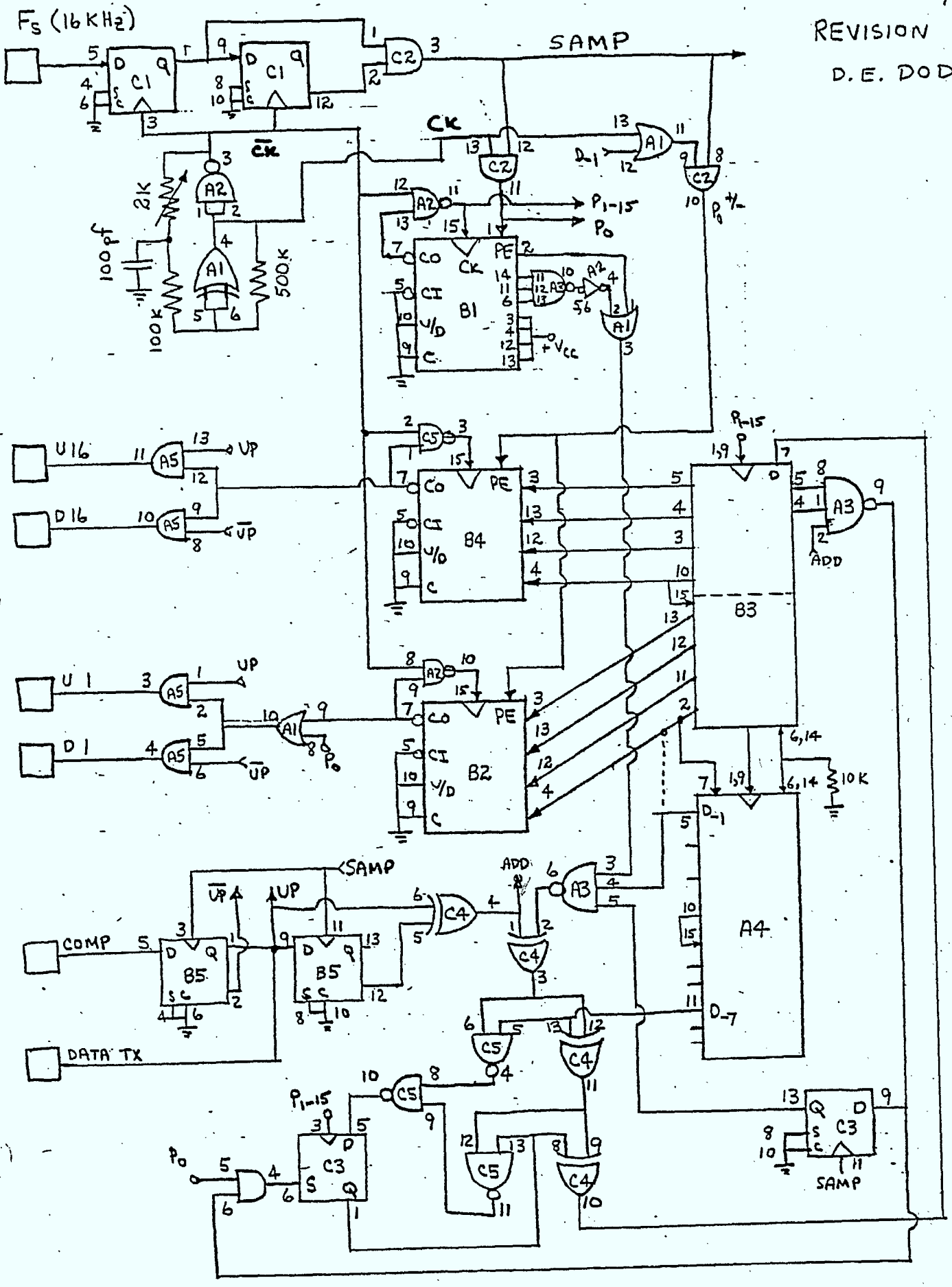
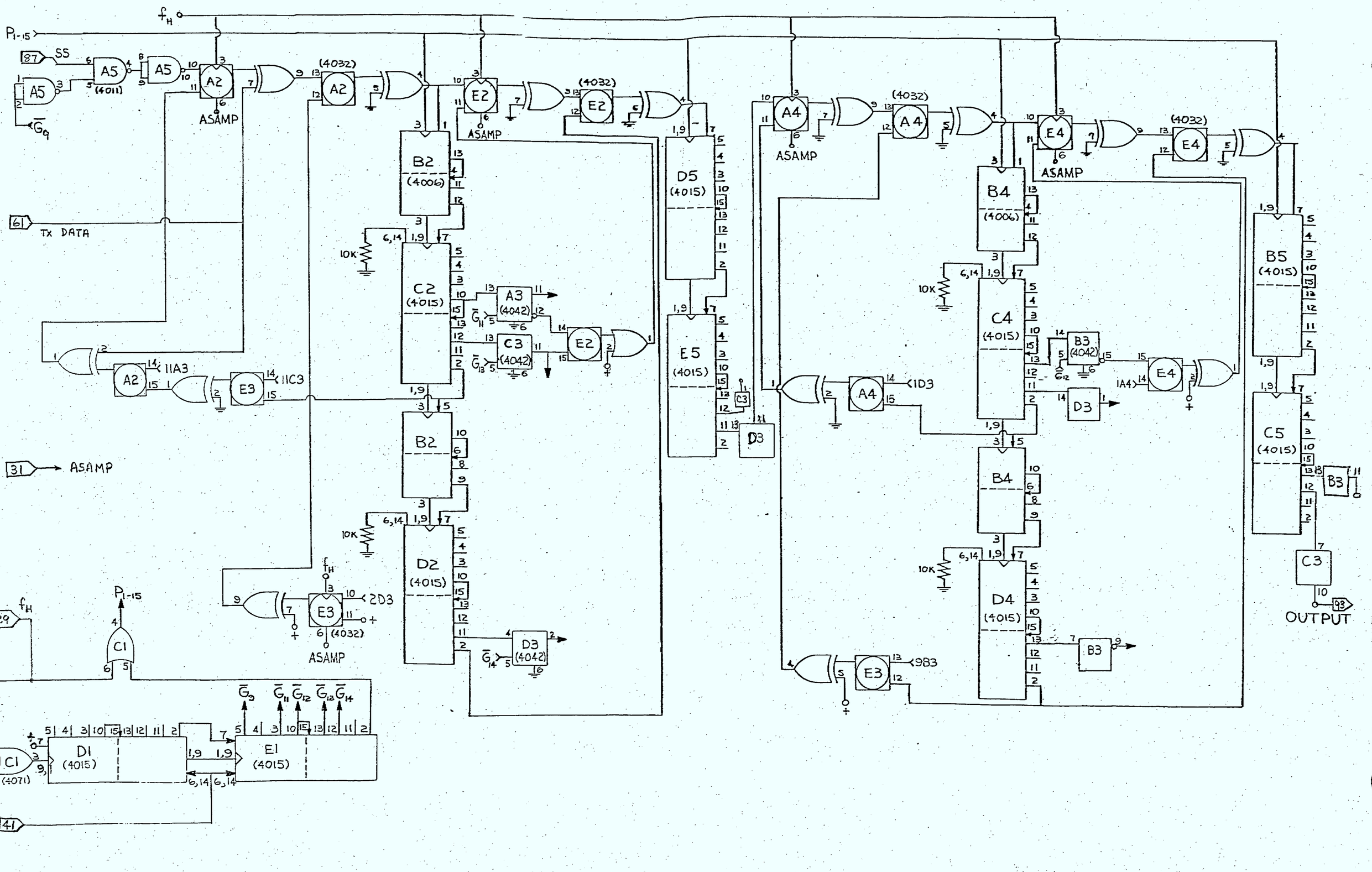
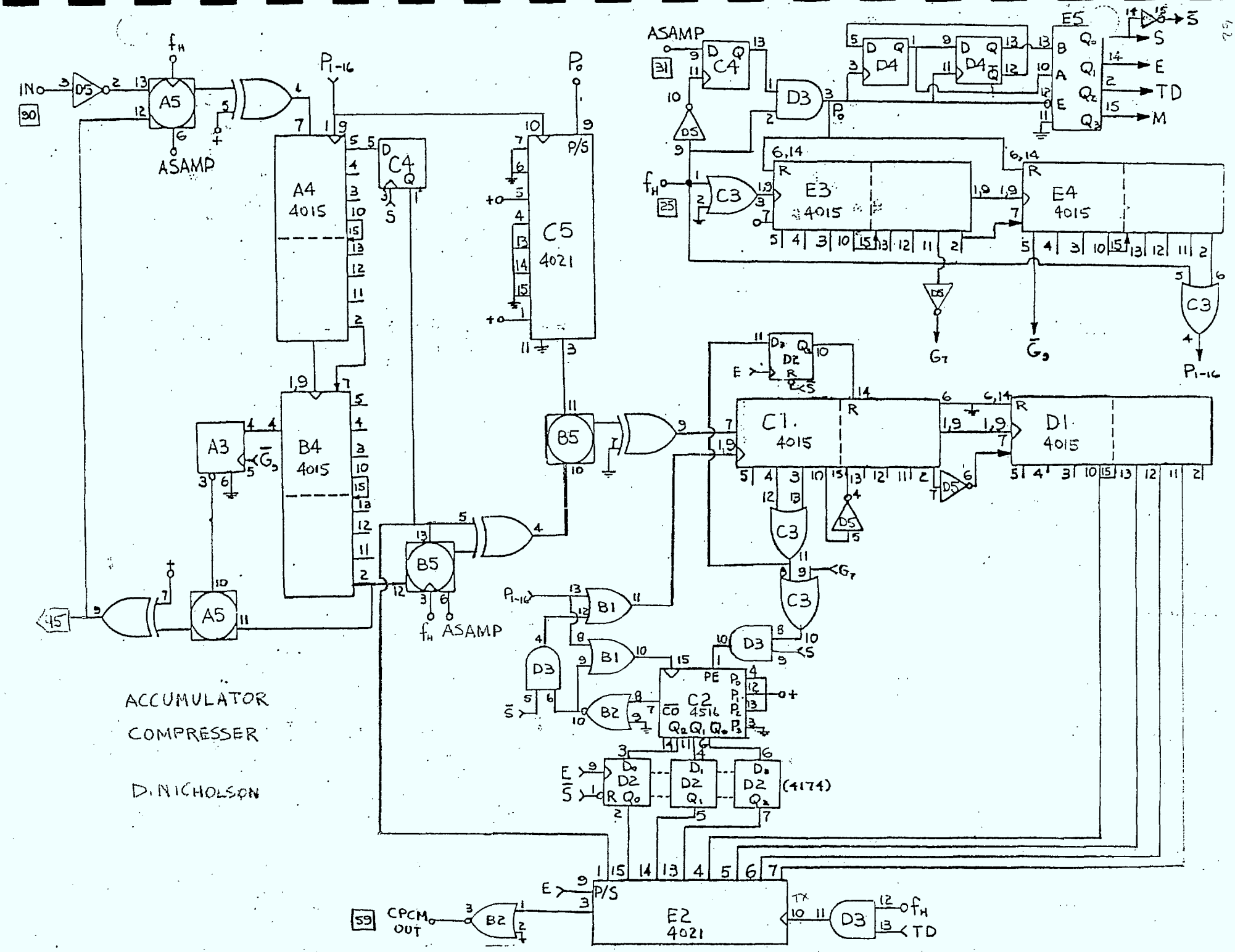
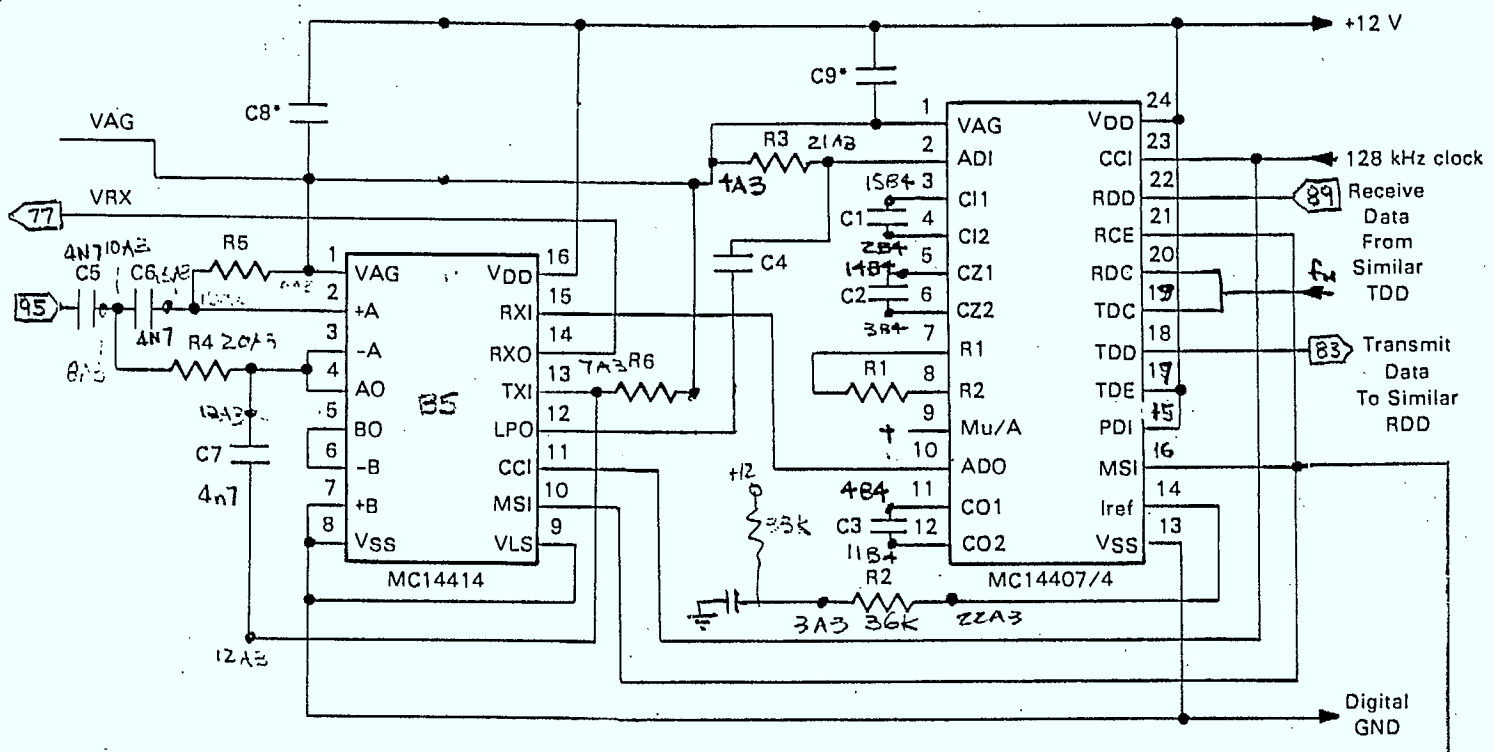
REVISION 16A
D. E. DODDS




f_H
P_{1-15}
87
SS
A5
(4011)
$\overline{G}_9$
ASAMP
A2
(4032)
B2
(4006)
C2
(4015)
10K
6,14
1,9
A3
(4042)
$\overline{G}_{11}$
C3
$\overline{G}_{13}$
E2
D5
(4015)
E5
(4015)
D3
(4042)
$\overline{G}_{14}$
61
TX DATA
A2
11A3
E3
11C3
B2
D2
(4015)
2D3
31
ASAMP
29
C1
(4071)
D1
(4015)
E1
(4015)
$\overline{G}_9$ $\overline{G}_{11}$ $\overline{G}_{12}$ $\overline{G}_{13}$ $\overline{G}_{14}$
41
A4
(4032)
B4
(4006)
C4
(4015)
D4
(4015)
B3
(4042)
$\overline{G}_{12}$
1A4
1D3
D3
983
E4
B5
(4015)
C5
(4015)
B3
C3
93
OUTPUT

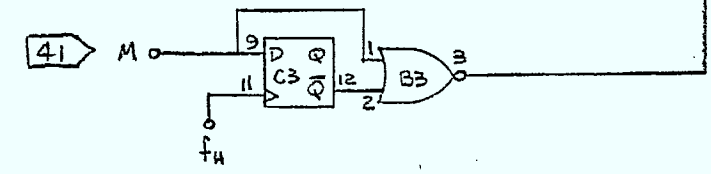

ACCUMULATOR
COMPRESSER
D. NICHOLSON
IN
ASAMP
A5
A4 4015
A3
B4 4015
B5
C4
C5 4021
P/S
A5
B5
ASAMP
C4
D3
D4
E5
E3 4015
E4 4015
C3
D5
C1. 4015
D1 4015
D2
B1
B2
C2 4516
E2 4021
CPCM OUT
TD
(4174)

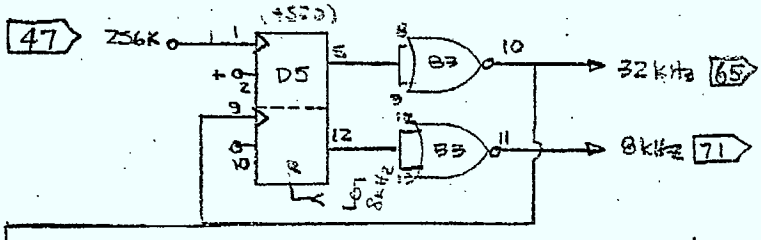
PCM DECODER & TIMING

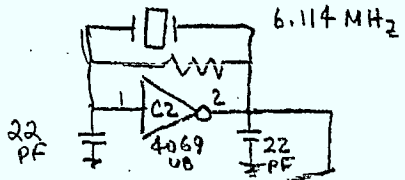


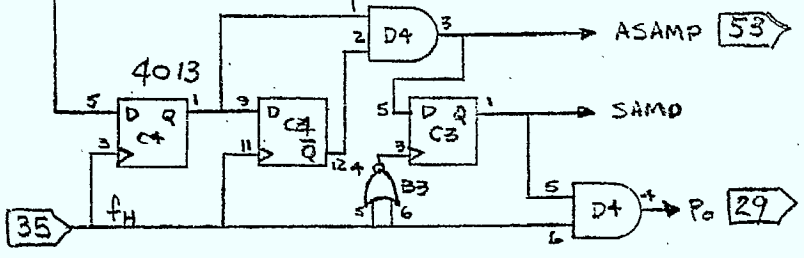
C1, C2	2000 pF	-20/+80% X7R
C3	3900 pF	-20/+80% X7R
C4	.2 μF	-20/+80% X7R
C5, C6, C7	4700 pF	±1% NPO
C8, C9*	.1 μF	-20/+80% X7R
R1	3.0 k	1%
R2	30 k	1%
R3	24 k	10%
R4	112 k	1%
R5	620 k	1%
R6	223 k	1%

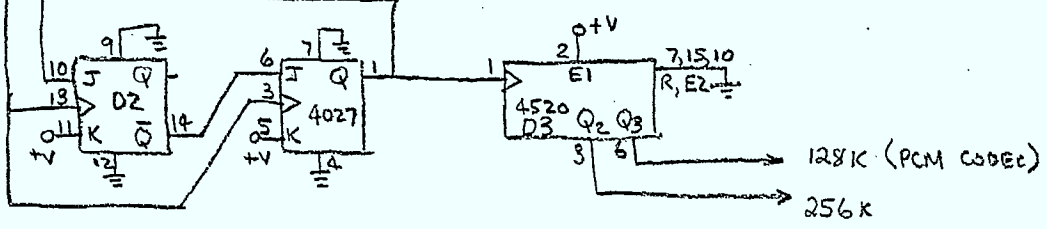
*C8 and C9 should be physically close to the MC14414 and MC14407/4 respectively.

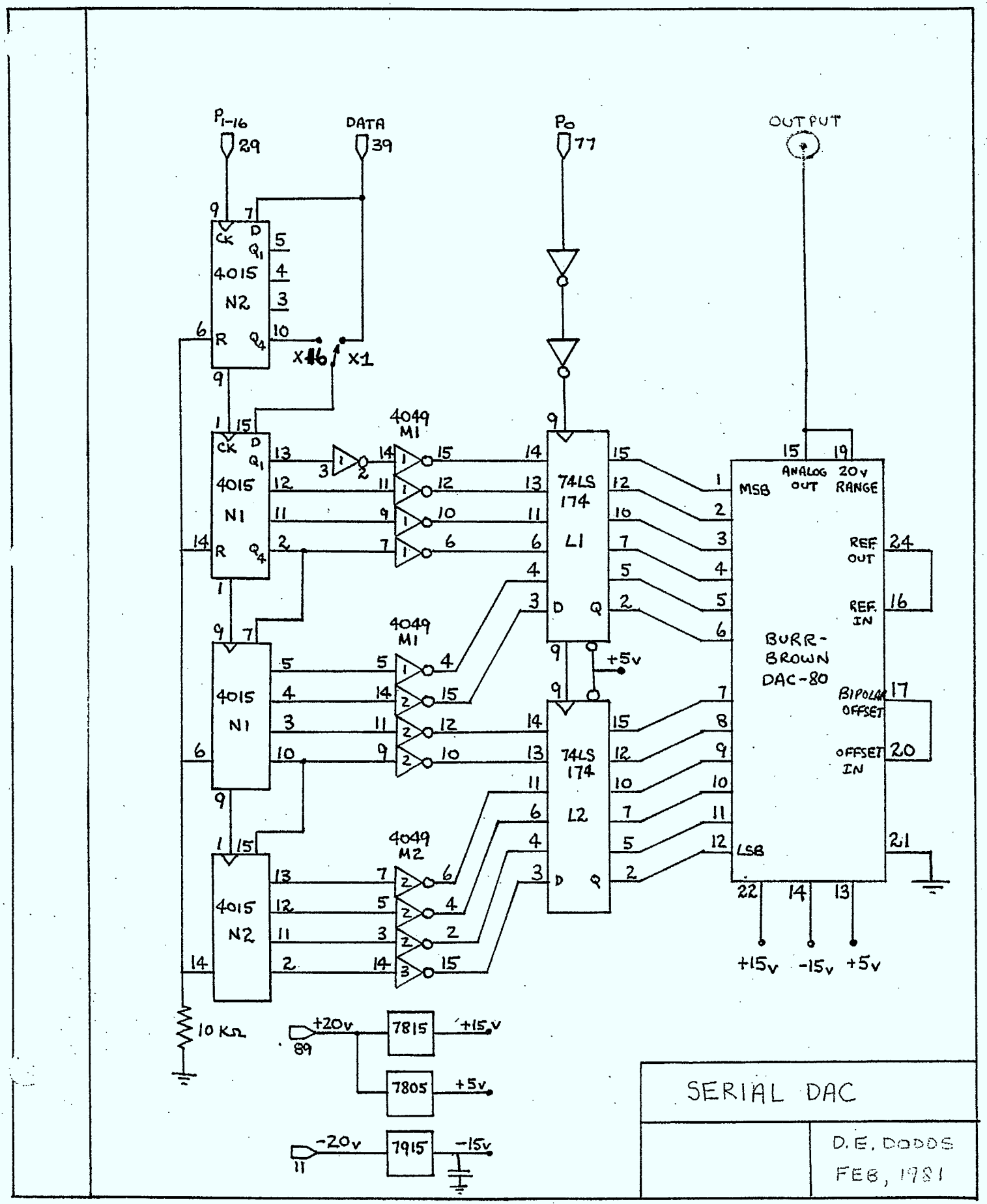








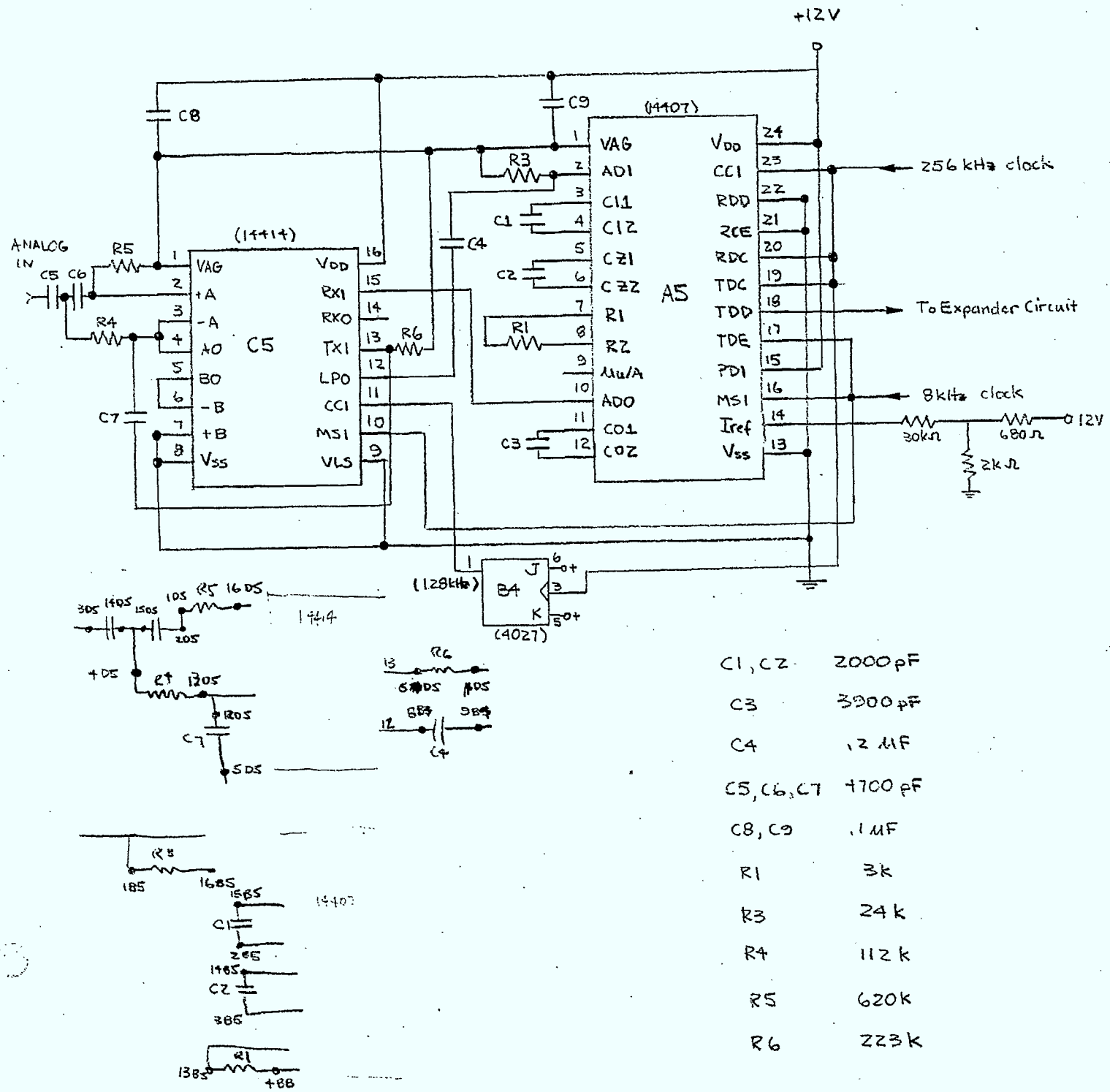




SERIAL DAC

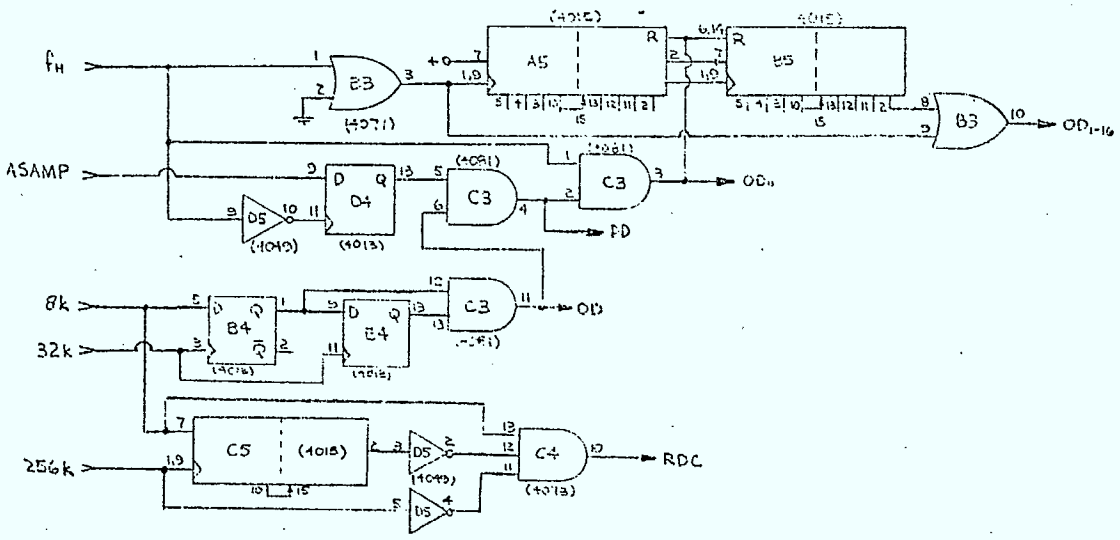
D. E. DODDS
FEB, 1981

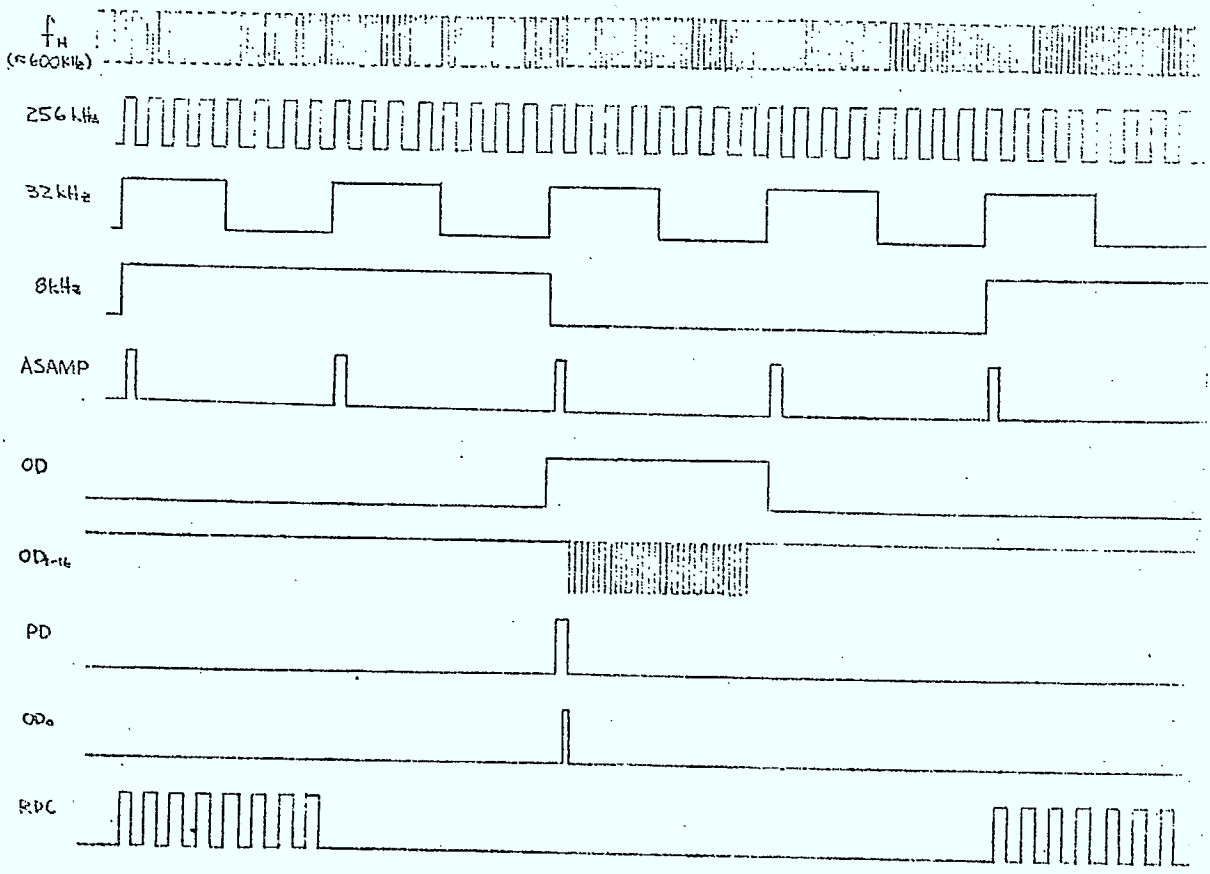
PCM ENCODER

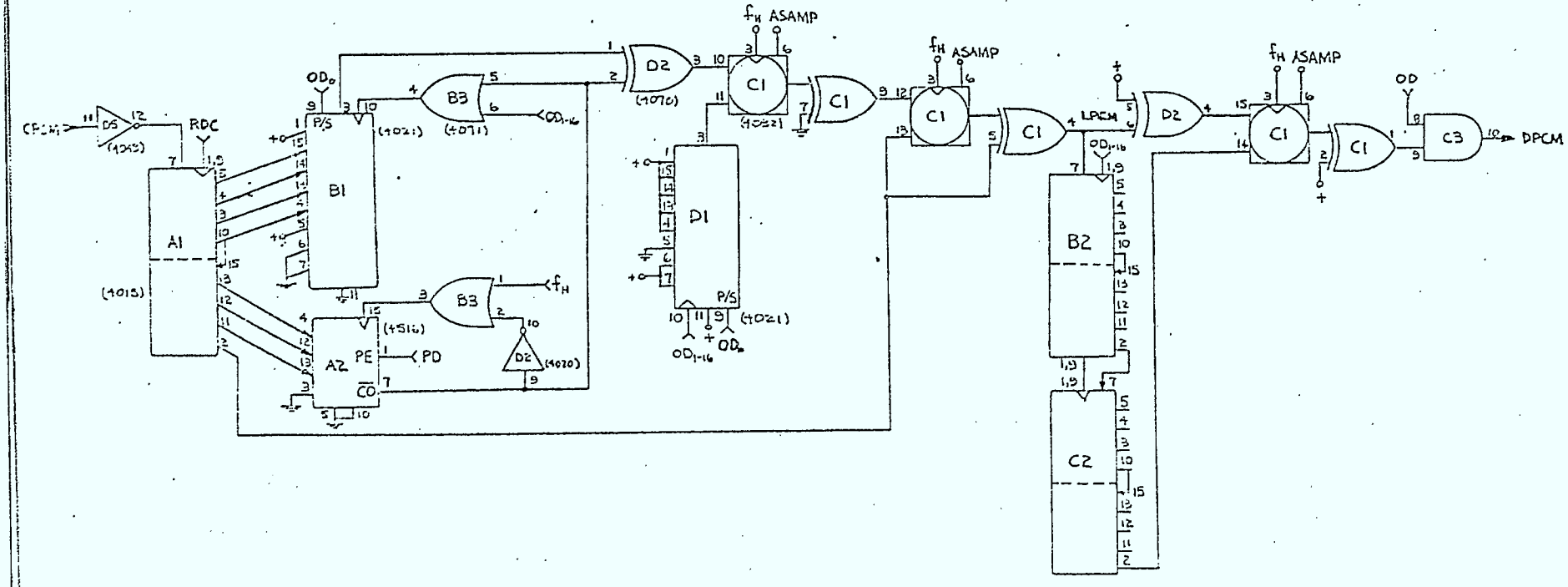


C1, C2	2000 pF
C3	3900 pF
C4	.2 μF
C5, C6, C7	4700 pF
C8, C9	.1 μF
R1	3k
R3	24 k
R4	112 k
R5	620k
R6	223k

EXPANDER TIMING AND CONTROL



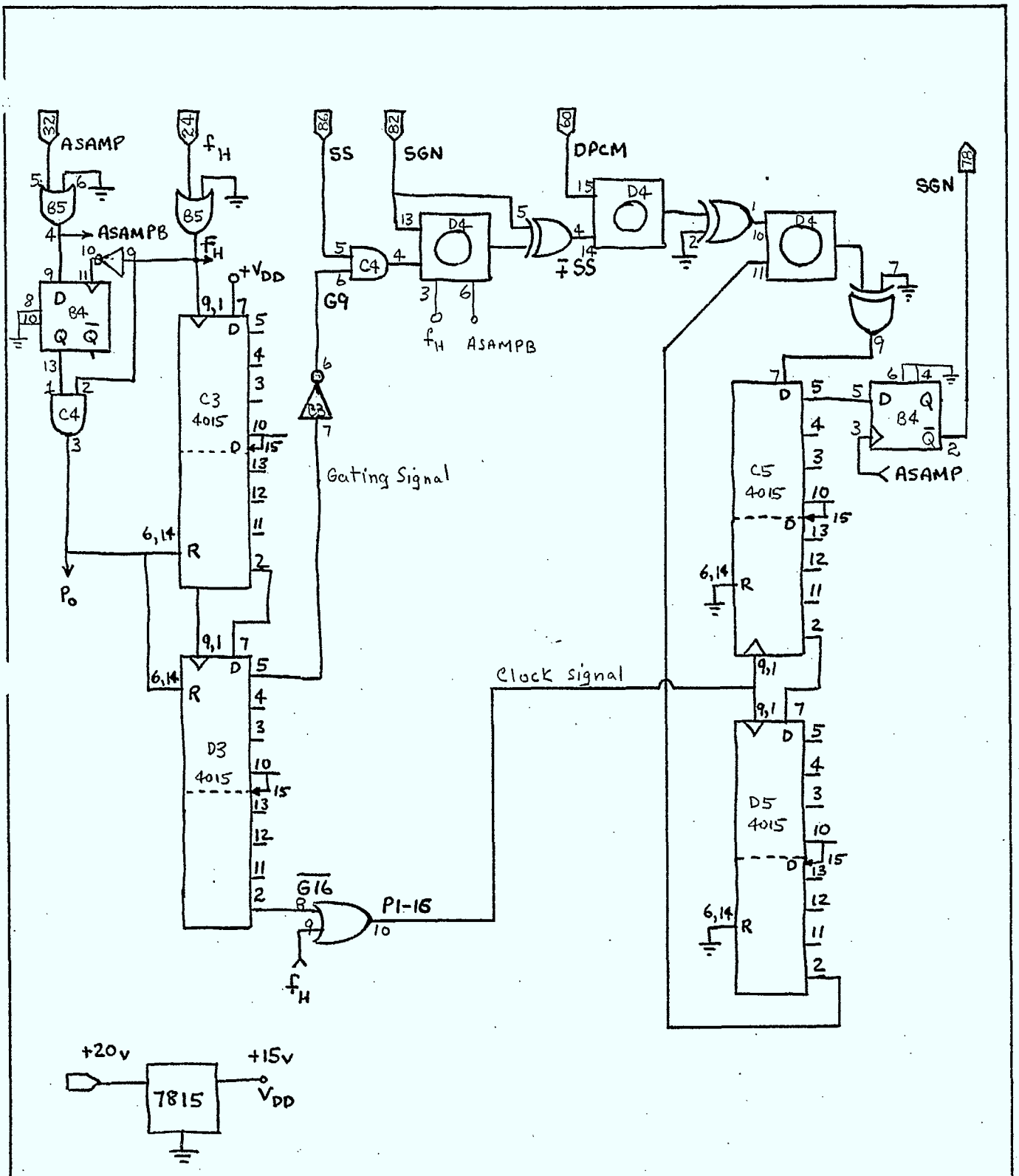




EXPANDER / DIFFERENTIATOR

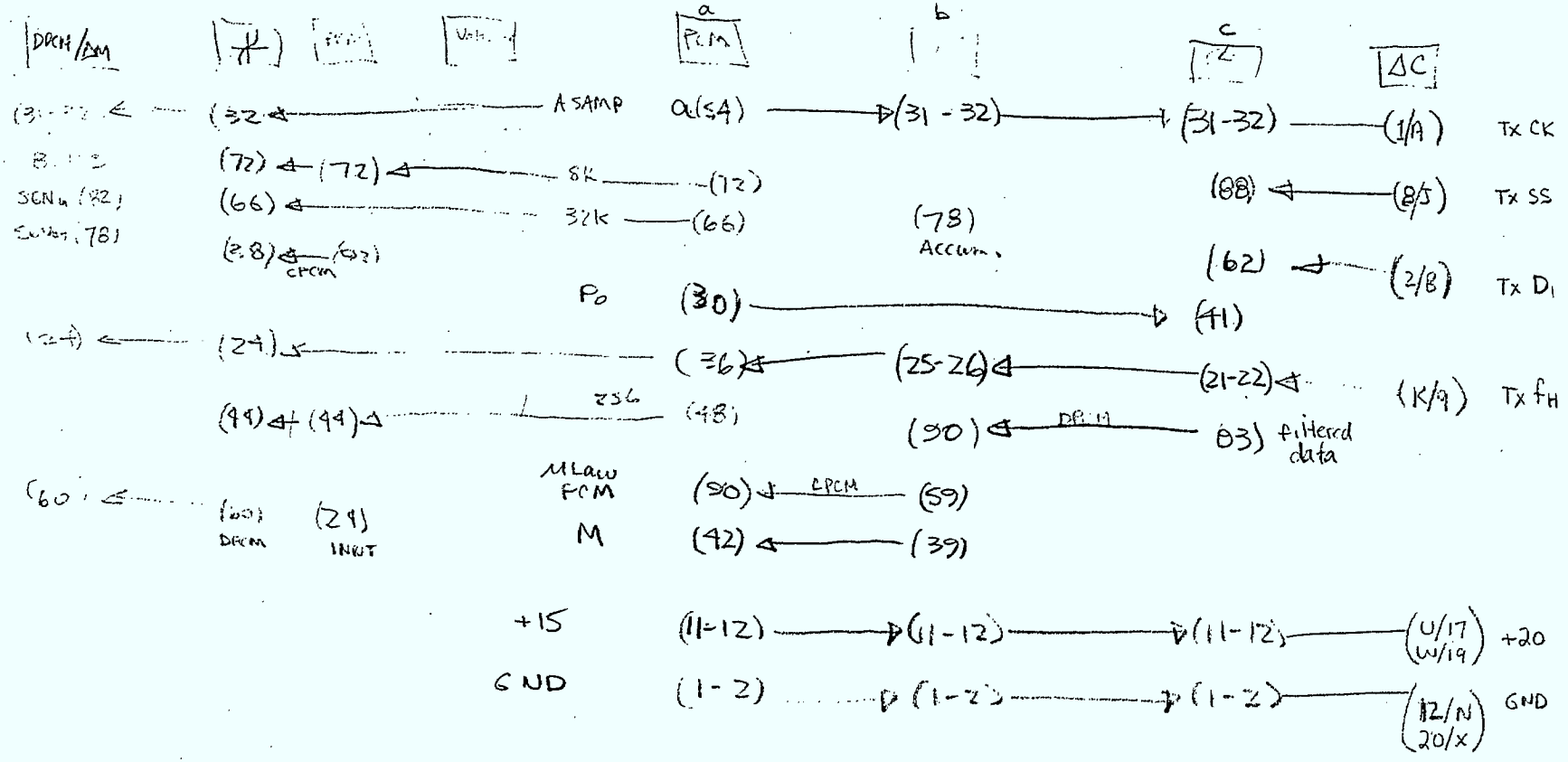
D. NICHOLSON

APRIL / 81



ΔM / DPCM
DIFFERENCE ACCUMULATOR

D.E. DODDS
JULY, 1981



BACK PLANE WIRING	
	D. NICHOLSON MAR. 81