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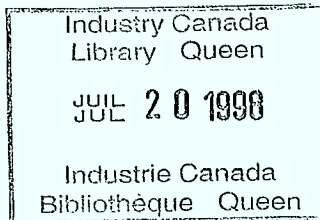
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EXECUTIVE SUMMARY

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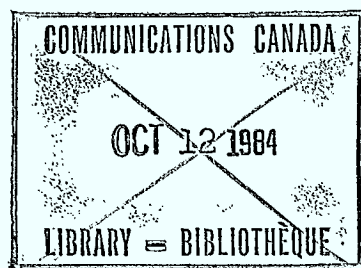
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EXECUTIVE SUMMARY



Computer Aided Engineering Tools for
Spacecraft Multiprocessor Systems
(Contract # OER 82-05067)



AUTHOR: Dr. C. Laferriere
APPROVED BY: Dr. S.A. Mahmoud

INTELLITECH CANADA LIMITED

352 MacLaren Street
Ottawa, Ontario
K2P 0M6

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Government
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Gouvernement
du Canada

Department of Communications

DOC CONTRACTOR REPORT

DOC-CR-SP -83-061

DEPARTMENT OF COMMUNICATIONS - OTTAWA - CANADA

SPACE PROGRAM

TITLE: EXECUTIVE SUMMARY - Computer Aided Engineering Tools for
Spacecraft Multiprocessor Systems

AUTHOR(S): Dr. C. Laferriere

ISSUED BY CONTRACTOR AS REPORT NO: INT-83-55

PREPARED BY: Intellitech Canada Ltd.
352 MacLaren St.
Ottawa, Ontario
K2P 0M6

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DATE: September 1983

FOREWORD

This executive summary reports on work done for the Federal Department of Communications, Communications Research Centre, Shirley Bay, Ottawa, Ontario, under contract # OER 82-05067.

The summary highlights the salient points of the following reports which were contract deliverables:

1. "CAE Tools for Spacecraft Multiprocessor Design: Progress Report for June-July 1982", (Including Trade Off Study), Intellitech Canada Limited, August 1982.
2. "CAE Tools for Spacecraft Multiprocessor Design: Progress Report for August 1982", Intellitech Canada Limited, September 1982.
3. "N.mPc and its Utility for Spacecraft Applications", Technical Report, Intellitech Canada Limited, Ottawa, Canada, January 1983.
4. "N.mPc and its Utility for Spacecraft Applications: N.mPc Simulation Listings", Technical Report, Intellitech Canada Limited, Ottawa, Canada, January 1983.
5. "Spacecraft Multiprocessor Design Methodology: Specification and Hardware/Software Partitioning", Technical Report, Intellitech Canada Limited, Ottawa, Canada, July 1983.

1.0 INTRODUCTION

In recent years, computer systems have seen their performance increase considerably. Faster circuits and devices, miniaturization, and better design techniques were major factors in bringing about this enhancement in computing power. This, in turn, has made possible the use of computers in applications which had hitherto been too complex to be cost effective. The control of a spacecraft by an on-board computer is such an application.

Given the power of today's microprocessors and the complexity of the tasks to be performed, it appears that a multiple processor architecture has to be employed if the performance criteria of the control system are to be met. However, the design of multiple processor systems, especially of a general purpose nature, is not well understood and can introduce a considerable overhead in the design activity.

In view of these facts, a research project was initiated to develop a design methodology for multiple processor systems for spacecraft applications and to specify a set of computer aided engineering tools to be used in conjunction with that methodology. The elaboration of the methodology was carried out in a previous contract; several areas worth further investigation were isolated.

- 1) the specification of desired multiprocessor system characteristics;
- 2) the mapping of functional specification into hardware/software components;
- 3) the hardware components development;
- 4) the software components development;
- 5) the system integration and testing.

Within the framework of the present contract, items 1,2 and 4 were treated in [5] and items 3 and 5 were covered in [1,2,3,4].

2.0 THE DESIGN METHODOLOGY

The design methodology is the basis for all work carried out under the present contract and therefore deserves some explanations. The purpose of the methodology is to guide the designers from the specification stage all the way to a practical implementation of the system. Figures 1 and 2 depicts the upper and lower levels of the methodology and, although not always evident from those diagrams, looping back to an earlier stage to modify some design choices is the way to handle some inadequacies whenever they are found.

In the upper levels of the methodology, as shown in Figure 1, a functional model of the planned system is obtained by specifying the system requirements, and translating those requirements into functions which are to be decomposed using data flow and hierarchical methods successively. Once a detailed functional model is available, two courses of action are possible:

1. A data flow analysis which tries to produce processing power requirements for each functions. This estimation is done analytically.
2. A functional simulation whose goals are similar to the data flow analysis stage but which uses simulation with estimations of processing power requirements.

The processing power requirements together with all the physical constraints affecting the eventual implementation are inputs to the hardware/software partitioning stage. The purpose of that stage is to take a functional view of the system and produce a set of software modules executing on some support hardware with, possibly, some hardware implemented functions. This is in fact the starting point of the implementation of the system.

Figure 2 depicts the lower levels of the design methodology, or in other words, the stages following the hardware/software partitioning stage. Figure 2 also shows some design choices (e.g. Ada simulation blocks, N.mPc, etc.) which will be covered later. Two streams of activity result from the partitioning stage:

1. The hardware development activity is concerned with designing and implementing the general purpose processors required to run the software and also the special purpose hardware components that may be required. It is essential that this activity be independent from actual hardware building yet, at the same time, be close enough to reality to allow for quick prototyping when the design is finalized and satisfactory. N.mPc was chosen as the computer aided engineering tool most suited for the task. Reference [1] describes the reasons why N.mPc was deemed to be the best alternative at the time. Those reasons were N.mPc's capabilities to define any hardware structure in software, to support code development (in assembler) and to provide for the integration of emulated hardware and target software for testing purposes. A complete description of the N.mPc system as received by Intellitech is to be found in [2]. References [3,4] established the viability of N.mPc as a design tool for multiprocessor systems for spacecraft. Several multiprocessor architectures were implemented and simulated successfully. Simulation listings are in [4].
2. The software development activity is concerned with developing the functional description of the system into a proper set of software modules. To help make this activity more efficient, it was suggested that Ada (*) should be used both to specify the system requirements (upper level) and to develop the code for the application (lower level). Reference [5] covers these topics; in particular, it describes the special constructs necessary to express high level functions in Ada and it describes how these functions can be easily developed into Ada code.

(*) Ada is a trademark of the U.S. Department of Defence.

Following the hardware and software development activities, the hardware/software integration stage takes the emulated hardware and the target software and prepares a simulation module. N.mPc is used to create the simulation and to provide the user interface for the control of the simulation execution. In this fashion, thorough testing can be achieved and any design and/or implementation inadequacies can be uncovered readily. These topics were also covered in reference [5].

3.0 SUMMARY

The major aspects of the design methodology for multiprocessor systems which had been developed during a previous phase of this work have been covered. The higher levels of the methodology as well as the practicalities of the lower levels were covered in [5]. The other reports [1,2,3,4] covered the use of the computer aided engineering tool N.mPc.

The use of the methodology as well as the computer aided engineering tools promise to improve considerably the design of multiprocessor systems. This improvement is achieved partly through the logic of the methodology and partly through the use of the CAE tools which allow quicker design turn-around times.

Several areas of investigation remain before a complete design environment can be put together. Foremost among these, is the study of reliability and recovery techniques and how they affect the design of multiprocessor systems. Reliability and robustness are, of course, extremely important in satellite work and thus justify the proposed investigation.

Finally, the work described herein was presented to the technical authority, Mr. R. Millar of CRC, at the Communications Research Centre, Shirley Bay, Ottawa on the 6th of May 1983 and on the 9th of August 1983. A selection of some of the slides shown on those occasions is included in Appendix A.

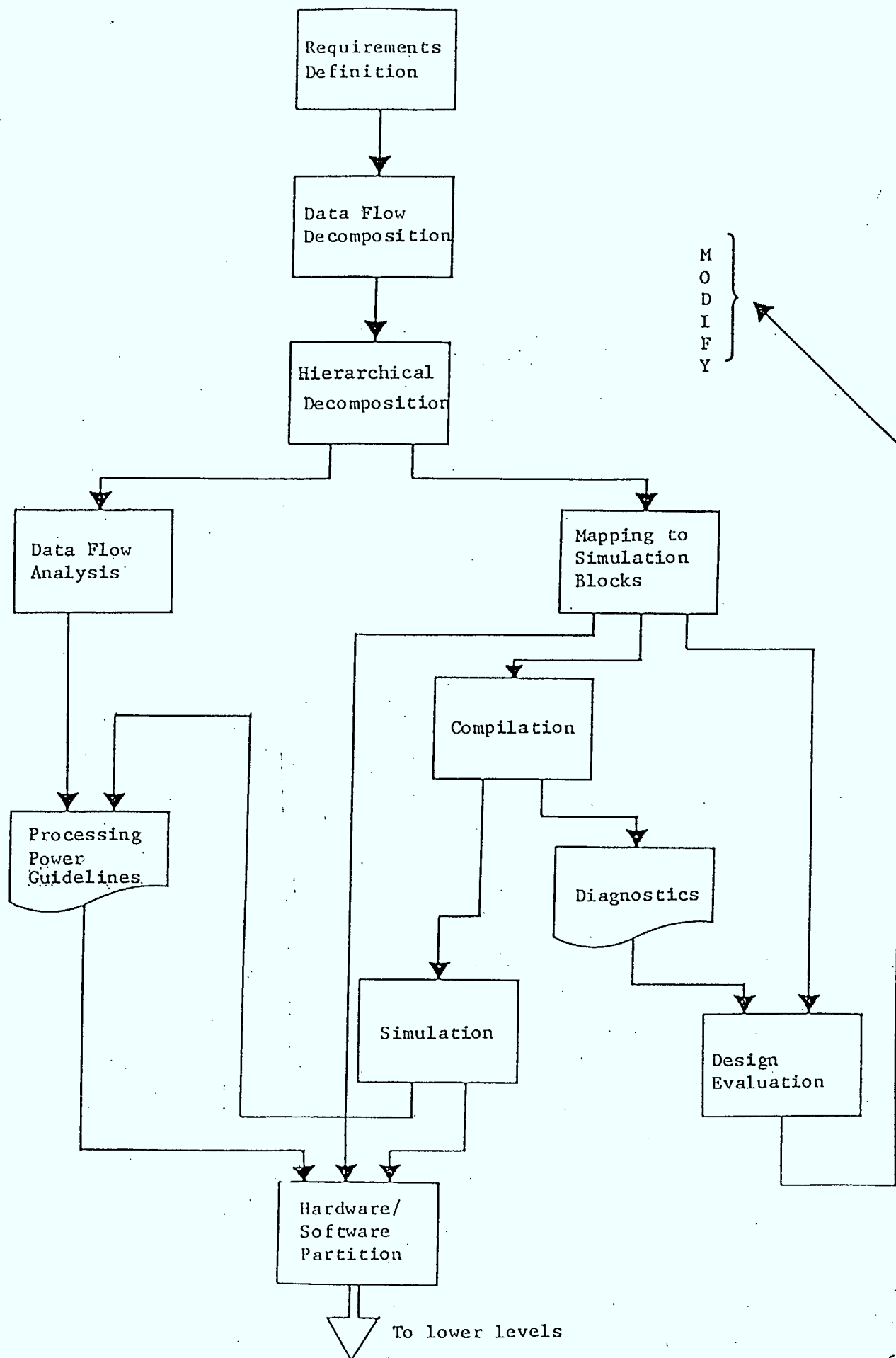


FIGURE 1 Upper Levels of the Design Methodology

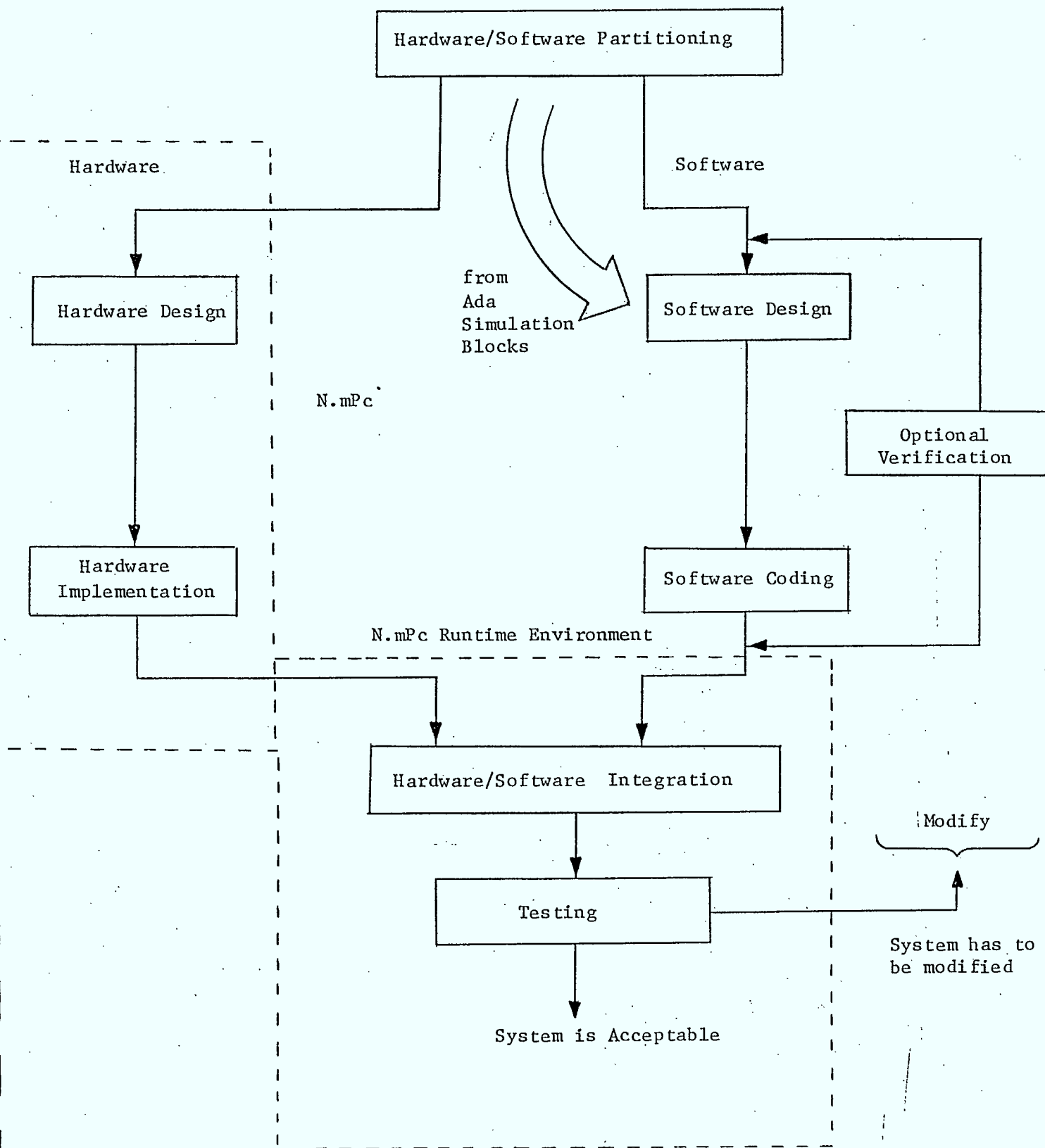


FIGURE 2 Lower Levels of the Design Methodology

REFERENCES

- [1] C. Laferriere and S.A. Mahmoud, "CAE Tools for Spacecraft Multiprocessor Design: Progress Report for June-July 1982 (including Trade-off Study)", Intellitech Canada Limited, Ottawa, Canada, August 1982.
- [2] S.A. Mahmoud and C. Laferriere, "CAE Tools for Spacecraft Multiprocessor Design: Progress Report for August 1982", Intellitech Canada Limited, Ottawa, Canada, September 1982.
- [3] C. Laferriere and A. Lam, "N.mPc and its Utility for Spacecraft Applications "Technical Report, Intellitech Canada Limited, Ottawa, Canada, January 1983.
- [4] C. Laferriere and A. Lam, "N.mPc and its Utility for Spacecraft Applications: N.mPc Simulation listings", Technical Report, Intellitech Canada Limited, Ottawa, Canada, January 1983.
- [5] "Spacecraft Multiprocessor Design Methodology: Specification and Hardware/Software Partitioning", Technical Report, Intellitech Canada Limited, Ottawa, Canada, July 1983.

APPENDIX A

This appendix contains a selection of slides
shown during two presentations at the Communications
Research Centre, on the 6th of May 1983 and the 9th of August 1983.

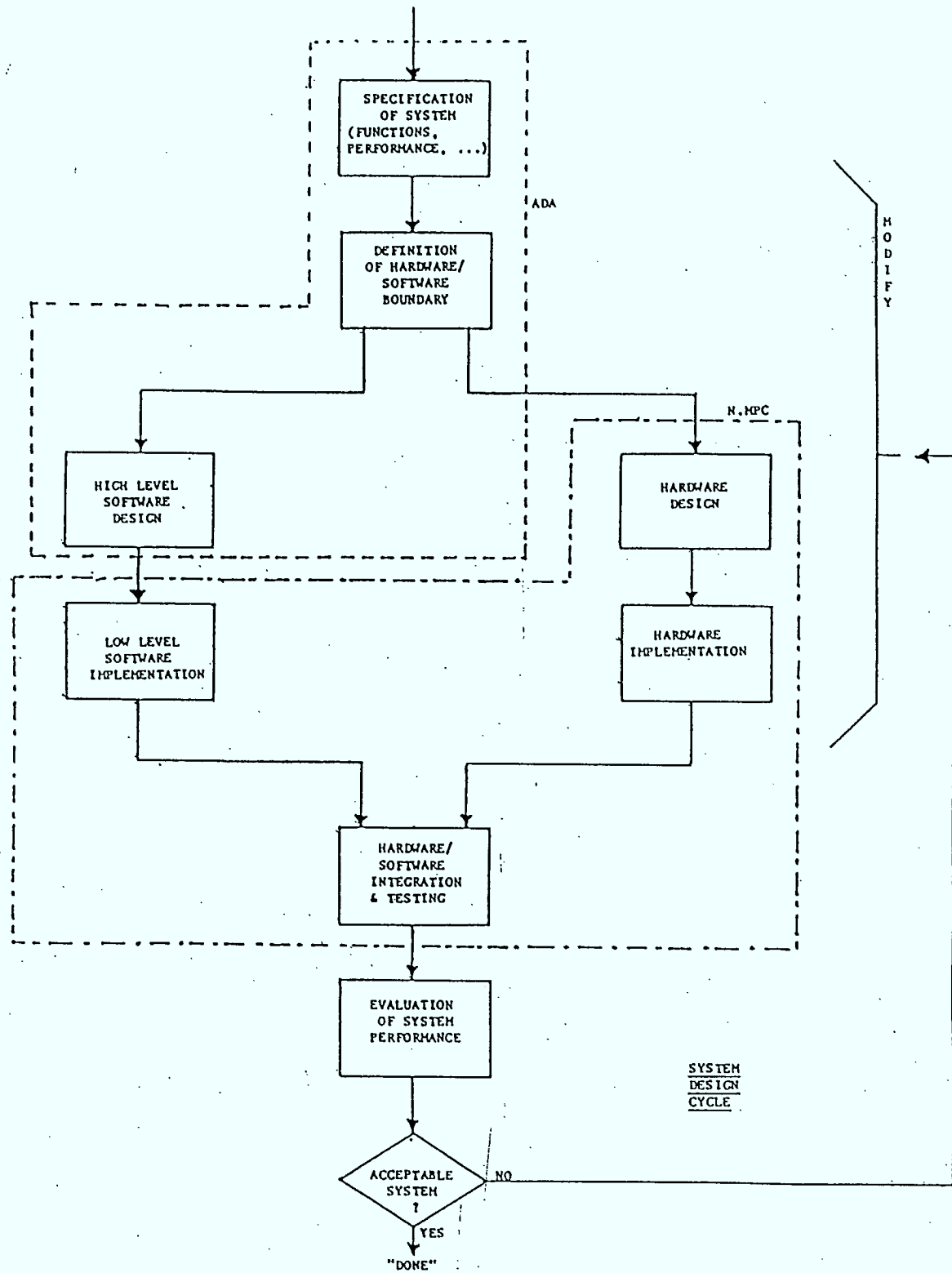
COMPUTER AIDED ENGINEERING TOOLS
AND THEIR APPLICATION TO THE DESIGN
OF SPACECRAFT MULTIPROCESSOR SYSTEMS

INTELLITECH CANADA LIMITED

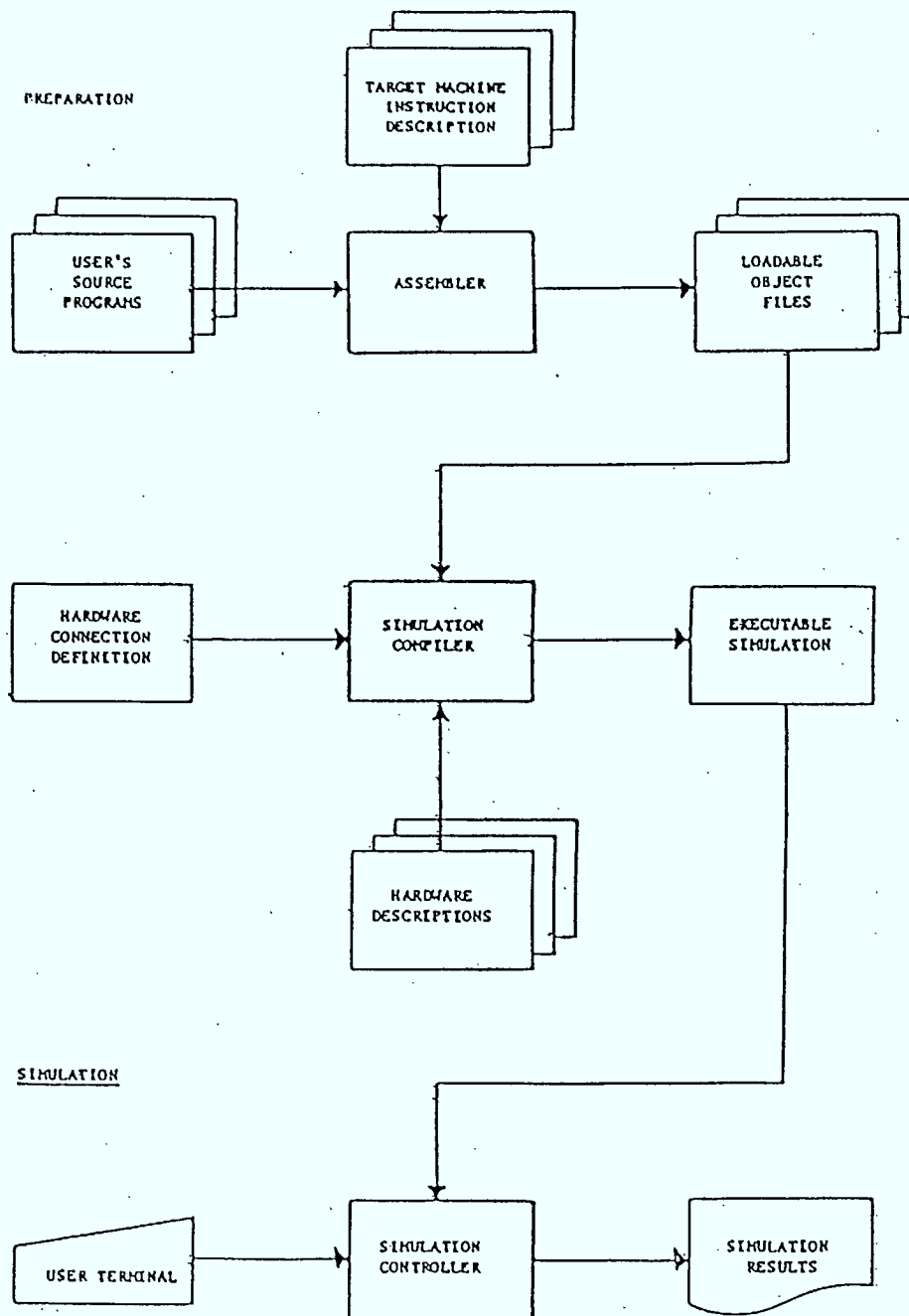
DR. S.A. MAHMOUD

DR. C. LAFERRIERE

MR. J. OUMET



N.HPC SIMULATION BLOCK DIAGRAM



N.MPC CAPABILITIES

1. PROVIDES FULL SOFTWARE DEVELOPMENT
ENVIRONMENT FOR MOST MICROPROCESSORS
2. PROVIDES HARDWARE FUNCTION SIMULATION
3. ACCOMODATES MULTIPROCESSOR ARCHITECTURE
EVALUATION
4. ENABLES SYSTEM PERFORMANCE EVALUATION

RECENT WORK WITH N.MPC

- IMPLEMENTATION OF FERRANTI F100-L AND SUPPORT CHIPS
- MULTIPROCESSOR SIMULATIONS USING F100-L's
- INVESTIGATION OF INTERPROCESSOR CO-ORDINATION
- EVALUATION OF F100-L ARCHITECTURE
- F100-L DEVELOPMENT SYSTEM

OBSERVATIONS ON N.MPC ON LSI 11/23 - UNIX

- SPEED
- OVERALL MEMORY
- SIMULATED MEMORY

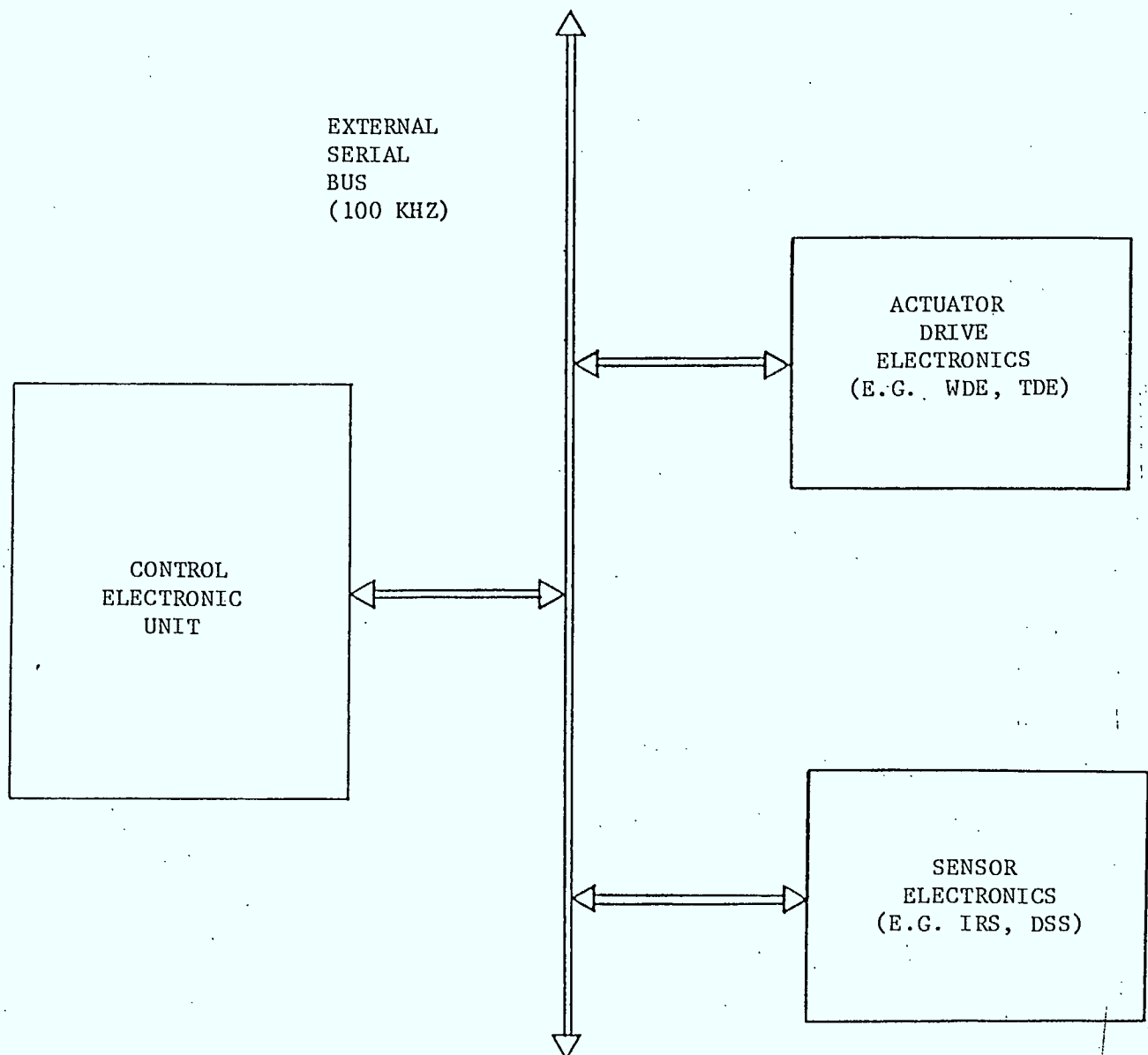
FAULT TOLERANT SYSTEMS

- OF EXTREME IMPORTANCE IN SPACECRAFT ON-BOARD PROCESSING SYSTEM.
- DEFINITION: FAULT TOLERANCE
RELIABILITY
- APPLIES TO WHOLE SYSTEM OR TO SETS OF COMPONENTS
- HAS TO BE BUILT INTO A DESIGN; HARDWARE & SOFTWARE
- SEVERAL CONFIGURATIONS MAY HAVE TO BE TESTED AND MODIFIED DURING DESIGN AND DEVELOPMENT
- RELIABILITY IS ALSO ASSESSED WHEN PRODUCT DESIGN IS FINALIZED

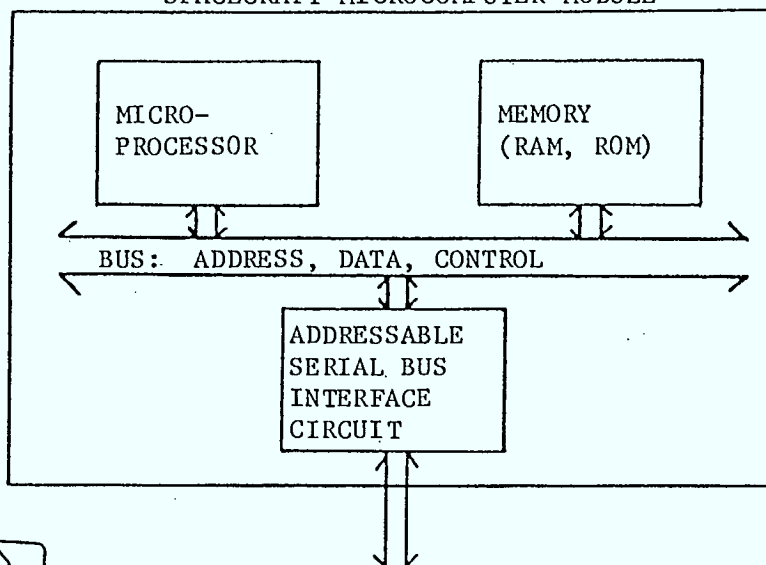
PROPOSED TECHNOLOGY DEVELOPMENT

- 1 - N.MPC/N.2 ON VAX/VMS
- 2 - FAULT TOLERANCE INVESTIGATION WITH N.MPC
- 3 - DESIGN, IMPLEMENTATION, SIMULATION OF MICROPROCESSOR BASED FAULT TOLERANT SYSTEMS WITH N.MPC
- 4 - USE OF CROSS DEVELOPMENT SOFTWARE AND INTEGRATION INTO N.MPC ENVIRONMENT
- 5 - SPECIFICATION AND DEVELOPMENT OF N.MPC GRAPHICS INTERFACES
- 6 - DEVELOPMENT OF HIGHER LEVEL SPECIFICATION TOOLS

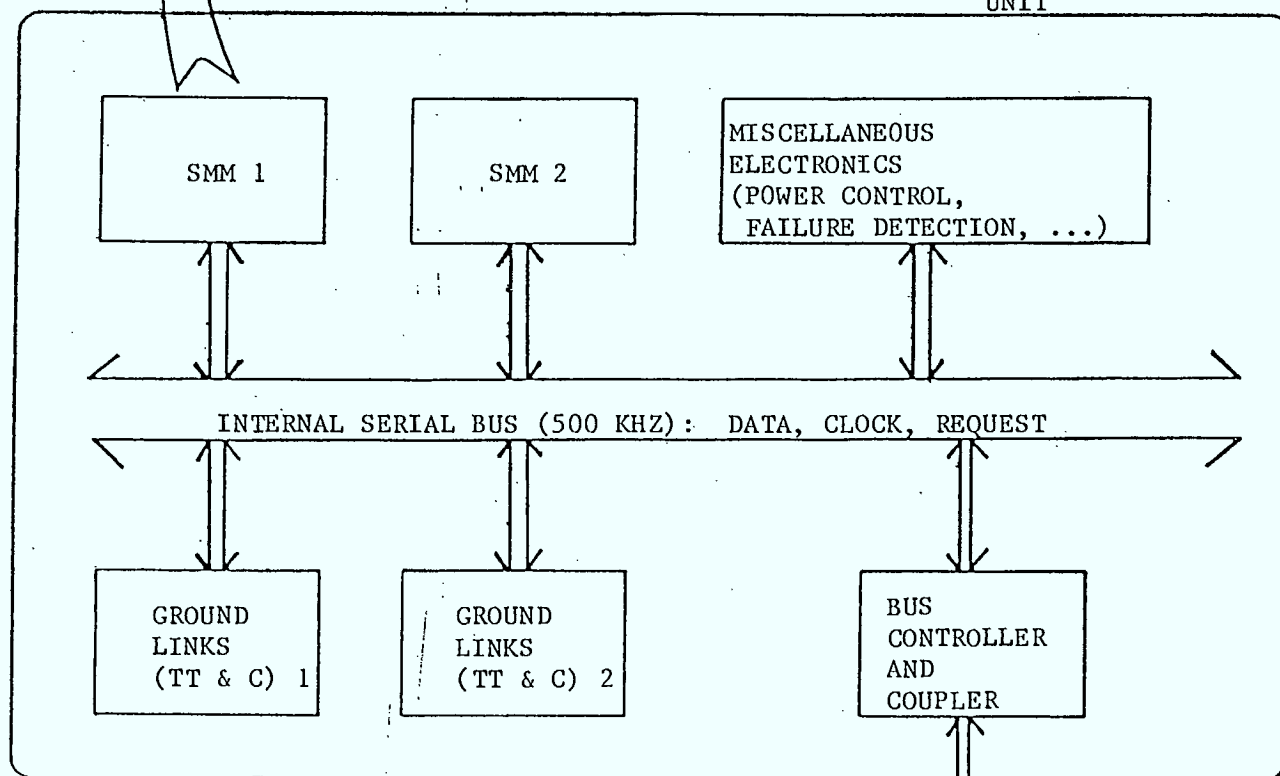
L-SAT ATTITUDE AND ORBIT CONTROL SYSTEM



SPACECRAFT MICROCOMPUTER MODULE



CONTROL
ELECTRONIC
UNIT



EXTERNAL
SERIAL
BUS (100KHZ)

PROPOSED M-SAT SUPPORT

- 1 - DEVELOPMENT OF MAJOR BUILDING BLOCKS OF M-SAT
ARCHITECTURE WITH N.M^PC
(E.G. TMS 9989)
- 2 - DEVELOPMENT OF HARDWARE DESCRIPTION OF M-SAT
ARCHITECTURE ON N.M^PC
(E.G. SMM, ASBIC, BUSCOT)
- 3 - PERFORMANCE & CORRECTNESS OF HARDWARE/SOFTWARE
BY EXERCISING THE HARDWARE WITH SKELETAL SOFTWARE
- 4 - COMPLETE SIMULATION OF HARDWARE/SOFTWARE SYSTEM
UNDER N.M^PC

INFORMATION REQUIRED

- 1 - DEFINITION OF MAJOR BUILDING BLOCKS
- 2 - HARDWARE CONFIGURATION: (E.G. INTERCONNECTION,
TIMING, DESCRIPTION OF SPECIAL PURPOSE CHIPS,...)
- 3 - ALGORITHMIC DESCRIPTION OF MAJOR SOFTWARE MODULES
- 4 - COMPLETE HARDWARE AND SOFTWARE DESCRIPTION

ADVANTAGES OF USING AN N.MPC SIMULATION

1. COMPARISON WITH SYSTEM TEST RESULTS
2. FAULT SIMULATION AND EVALUATION OF RECOVERY MECHANISMS
3. LEARNING ENVIRONMENT FOR UNDERSTANDING SYSTEM OPERATIONS
4. DEVELOPING SKILLS IN A MULTIPROCESSOR PROGRAMMING ENVIRONMENT
5. EVALUATION OF MODIFICATIONS
 - DESIGN PHASE (PRE LAUNCH)
 - OPERATIONAL SUPPORT PHASE (POST LAUNCH)

COST

I - HARDWARE - SOFTWARE

- N.MPc/N.2 ON MAX/VMS	\$ 45,000
- OPTIONAL C COMPILER	\$ 10,000
- MODEMS, TELEPHONE LINE, ETC.,	\$ 5,000
	<hr/>
	\$ 60,000

II - PROPOSED M-SAT SUPPORT

- TASKS 1 AND 2	\$ 45,000
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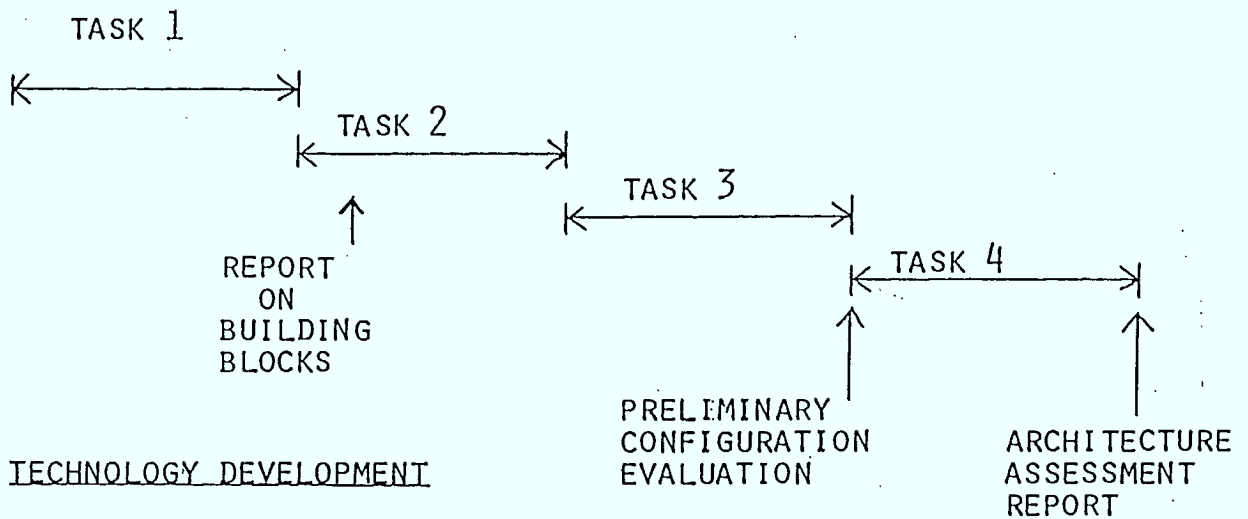
III - PROPOSED TECHNOLOGY DEVELOPMENT

- TASKS 1 & 4	\$ 12,000
- TASKS 2 & 3	\$ 82,000
- TASK 5	\$ 46,000
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	\$140,000

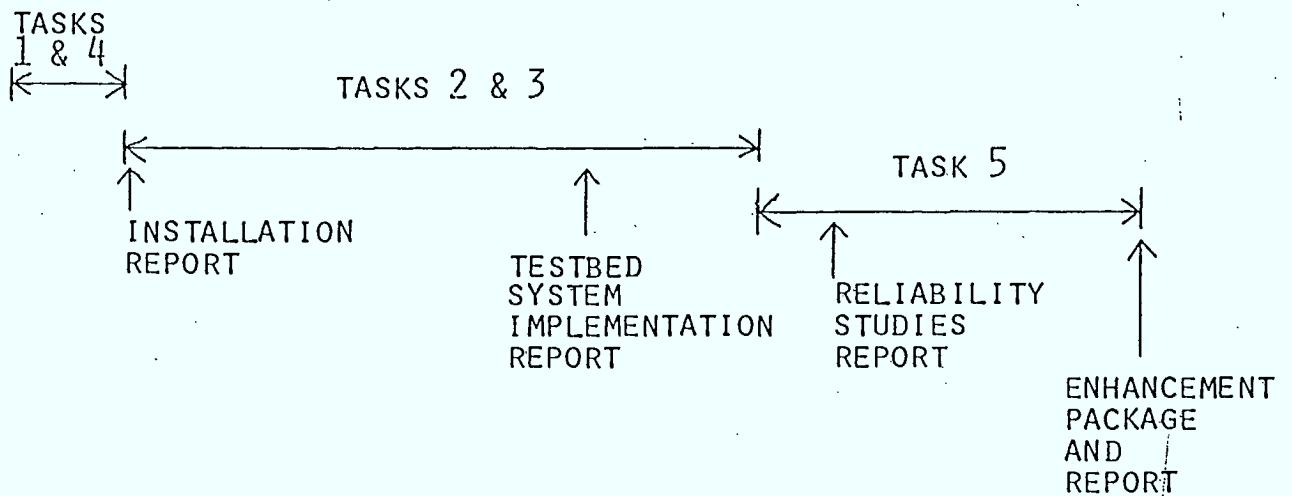
WORK SCHEDULE

JUL AUG SEP OCT NOV DEC JAN FEB MAR APR MAY JUN

M-SAT SUPPORT



TECHNOLOGY DEVELOPMENT



TMS 9900/TMS 9989

- TMS 9900 HARDWARE AND SOFTWARE MODELS
 - . ISP' DESCRIPTION
 - . META MICRO COMMAND FILE
 - . LINKING LOADER COMMAND FILE

- TMS 9989 HARDWARE AND SOFTWARE MODELS

IN PROGRESS

- TMS 9989 HARDWARE MODEL
 - . TIMING
 - . DEBUGGING
 - . FULL DOCUMENTATION

NEXT ACTIVITY

- TMS 9989 PERIPHERAL CHIPS
 - . INTERRUPT CONTROLLER
 - . INPUT/OUTPUT DEVICES
 - . BUS & MEMORY CONTROLLERS

TMS 9900 TMS 9989

	TMS 9900	TMS 9989
• PHYSICAL	4 ϕ CLOCK 64 KBYTES	1 ϕ CLOCK 128 KBYTES
	NEW PINS	MPEN INTERLOCK INTA EXTENDED INSTR.
• SOFTWARE	NEW INSTRUCTIONS	LOAD STATUS REG LOAD WP MUL (SIGNED) DIV (SIGNED)
• PERFORMANCE	1	2
• ANY OTHER CHARACTERISTICS ARE THE SAME		

M-SAT BUS SIMULATION

- INTERNAL ARCHITECTURE OF A SPACECRAFT MICROCOMPUTER MODULE.
 - . CHIPS
 - . WIRING DIAGRAMS
 - . FULL DESCRIPTION OF SPECIAL PURPOSE CHIPS SUCH AS PLA'S (E.G. ASBIC)
 - . TIMING DIAGRAMS WHENEVER DIFFERENT FROM MANUFACTURER'S OWN

- INTERNAL SERIAL BUS
 - . RESOLUTION OF ACCESS CONTENTION
 - . ANY PECULIARITY AFFECTING IMPLEMENTATION

M-SAT BUS SIMULATION (CONT'D)

- OTHER MODULES ON THE INTERNAL SERIAL BUS
 - . THEIR INTERFACE TO THE INTERNAL SERIAL BUS
 - . THEIR HARDWARE FUNCTIONALITY
 - . DESCRIPTION AND FUNCTIONALLITY OF BUSCOT
 - TIMINING DIAGRAMS
 - FSM (IF POSSIBLE)
 - . SPECIAL ATTENTION TO INTERFACING OF BUSCOT/
EXTERNAL SERIAL BUS WITH ASBIC/INTERNAL SERIAL BUS
- EXTERNAL SERIAL BUS
 - . RESOLUTION OF ACCESS CONTENTION
 - . ANY PECULIARITY AFFECTING IMPLEMENTATION
- OTHER MODULES ON EXTERNAL SERIAL BUS
 - . THEIR INTERFACE TO THE INTERNAL SERIAL BUS
 - . THEIR HARDWARE FUNCTIONALITY

intellitech

Intellitech Canada Ltd
352 MacLaren Street,
Ottawa, Ontario
K2P 0M6
(613) 235-5126