INVESTIGATION OF CIRCUIT FACTORS AFFECTING THE RELIABILITY OF GaAs FET MICROWAVE OSCILLATORS

(DSS CONTRACT NO. OSU77-00137)

Prepared by

Department of Electronics
Carleton University
Ottawa

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ABSTRACT

This report is based on a study under DSS contract No. OSU77-00137 of GaAs FET microwave oscillators and circuit related factors affecting the reliability of these components.

The S-parameters of a commercially available FET have been measured in the frequency range from 2 to 11 GHz at 1 GHz intervals. The calculated value of G_{max} extrapolates to a maximum frequency of oscillation of 25 GHz. A unilateral circuit model of the FET based on these measurements shows reasonable agreement with the measured results up to a frequency of 8 GHz.

An analysis of an FET common source oscillator was developed using the admittance matrix description of the transistor. The results showed that the feedback circuit must be designed to generate a negative conductance at the output of the oscillator and that the choice of the feedback elements controlls the small signal value of the output conductance. Design rules for achieving maximum output power from the oscillator are presented.

The analysis of oscillator behaviour presented above is applied to interpreting the results of testing FET's in a microstrip oscillator circuit at 10.8 GHz.

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1.0 INTRODUCTION

This report presents the results of an investigation carried out in the Electronics Department at Carleton University on the possible effects of circuit design on the reliability of microwave GaAs FET oscillators. This work was supported under a DSS contract number OSU77-00137. The motivation for this work was the observation of early failure in GaAs FET oscillators which was apparently not seen in amplifier designs. This led to speculation that there could be circuit-related conditions which imposed severe RF conditions upon the FET devices leading to early failure.

The investigation was divided into three phases which are reported in separate sections in this report. First, measurements were made of the two-port scattering parameters from 2 to 11 GHz. These measurements were used to develop a simple unilateral model of the FET which was useable to approximately 8 GHz. Second, the theory of oscillators was applied to a grounded source FET oscillator and some design principles regarding their use were determined. Thirdly, measurements of the characteristics of an X-band FET oscillator were made and interpreted with the results from part 2. A final fourth section presents conclusions and some recommendations for circuit design to avoid potentially troublesome areas.

2.0 S-PARAMETER MEASUREMENTS AND MODELLING

This section presents the results of S-parameter measurements and device modelling based on these measurements. The purpose of this

work was to characterize a typical device so that the interaction between the circuit and the device could be more clearly understood.

2.1 S-Parameter Measurements

The FET S-parameters were measured at 1 GHz intervals between 2 and 11 GHz using the HP Model 8410A network analyser and a special FET holder. A block diagram of the measurement assembly is shown in Figure 2.1. Since the parameters were measured on a point by point basis, the Model 8413A phase gain indicator with the meter display was used because of its more precise readings compared with the polar CRT display of the Model 8414A display unit.

The FET holder was a 50 Ω section of microstrip transmission line on alumina substrate. This was nearly identical to the circuit conditions encountered in a practical oscillator design. The substrate was mounted in an aluminum carrier and spring loaded dielectric posts were placed to hold the leads onto the 50 Ω line so that soldering of the FET's was not required. The lower cutoff frequency for waveguide modes propagating in the aluminum carrier was 11.8 GHz.

Calibration of the FET holder was accomplished by preparing "short" and "thru" dummy FET packages. The "short" package was used to calibrate S_{11} and S_{22} measurements and was machined from copper. The "thru" package for S_{12} and S_{21} calibrations was an empty package with a lead soldered across the ceramic, shorting the input and output leads to one another. TDR (time domain reflectometry) measurements of the impedance discontinuity of this package installed in the 50 Ω test circuit showed that, within the 12 GHz bandwidth of the TDR

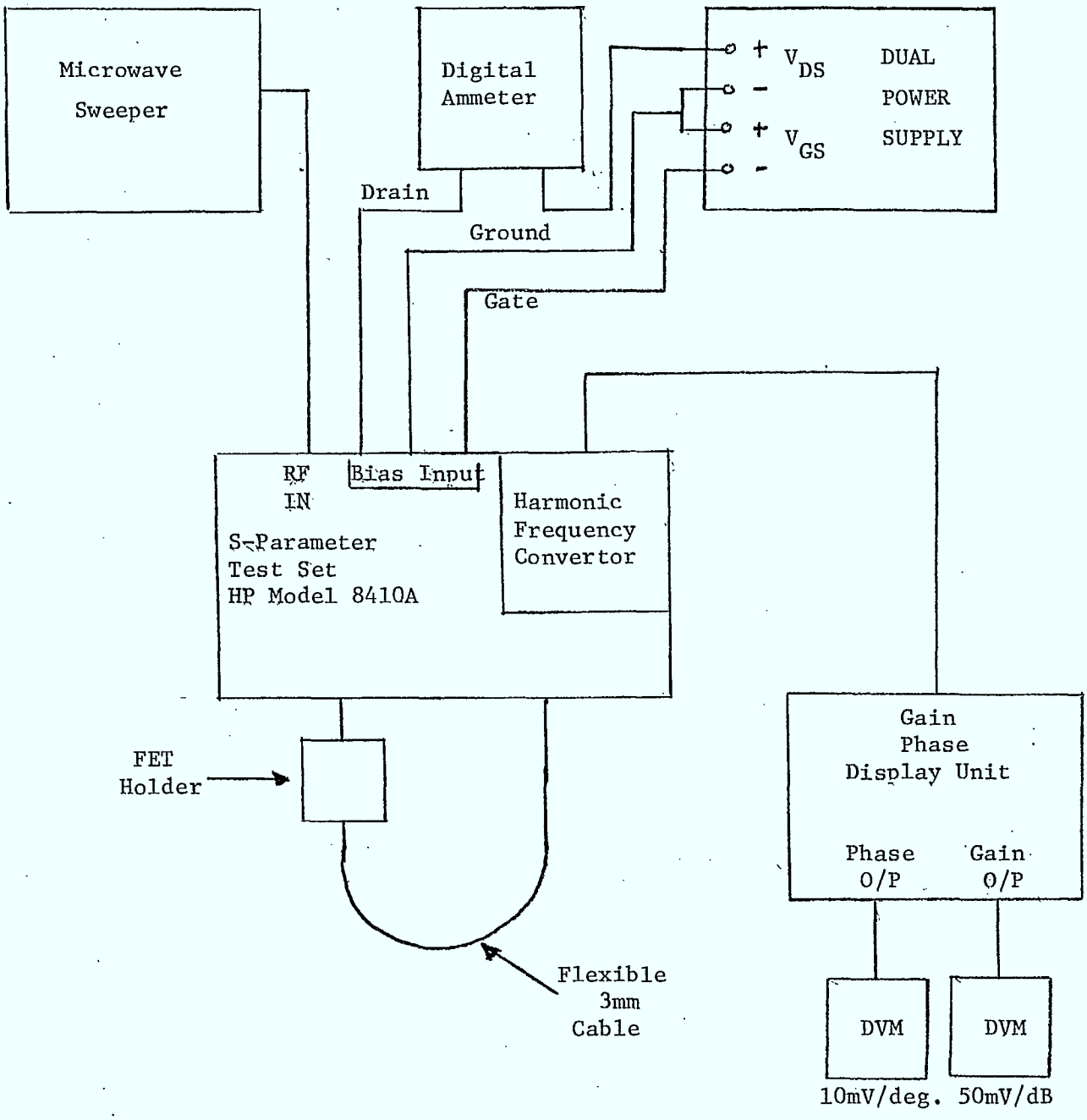

Figure 2.1 Block Diagram of FET S-Parameter Measurement System.

system, the reflections were less than 0.05 which corresponds to a return loss of 26 dB. Therefore, the "thru" package provided a known value of S_{12} and S_{21} of 1.00 at an angle of $\theta = 3.05f$ degrees where f is the measurement frequency in GHz.

Figure 2.2 shows the DC I-V characteristics of a Dexcel 501 FET, number 501-5. The low frequency transconductance is about .032 mho at low gate voltages and begins decreasing as $|V_{GS}|$ rises above 1 volt. The drain saturation current (I_{DSS}) is approximately 55 mA and the low current channel resistance is approximately 20 Ω.

The results of the S-parameter measurements of this FET are tabulated in Table 2.1. The right hand column gives the calculated value of the maximum unilateral gain

$$G_{max} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \qquad (2\text{-}1)$$

which assumes $|S_{11}| < 1$ and $|S_{22}| < 1$.

The extrapolated values of G_{max} vs. frequency, assuming a decrease of 6 dB/octave, leads to a maximum frequency of oscillation of approximately 25 GHz which agrees well with the manufacturers ratings.

The measured S-parameters were plotted on a Smith Chart and are presented in Figure 2.3 and Figure 2.4. The data for S_{11} looks well behaved with no abrupt jumps or indications of measurement error. The data for S_{22}, on the other hand, looks less reliable because of the discontinuous shift between 5 and 6 GHz. In the plots of S_{12} and S_{21},

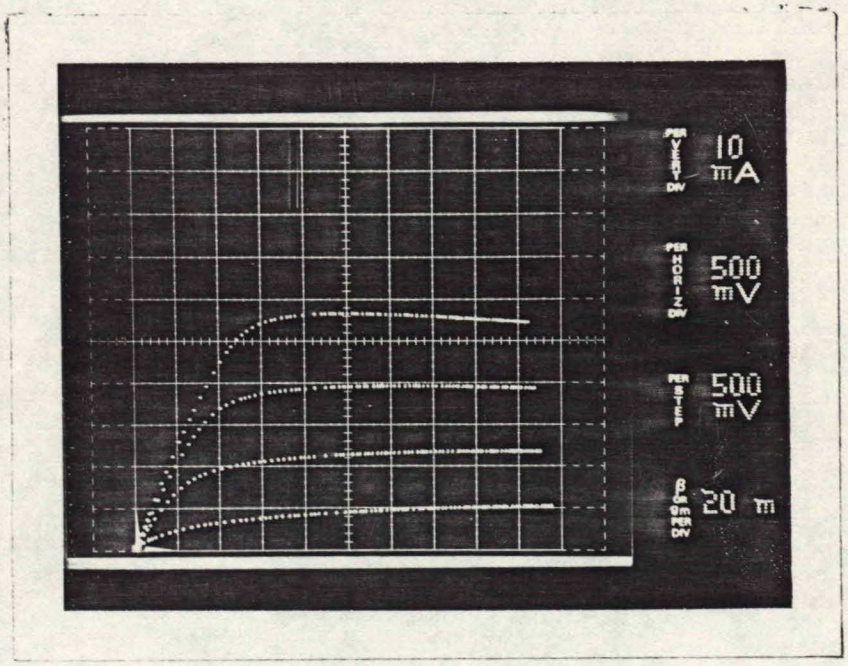

Figure 2.2 DC I-V Characteristics of Dexcel 501 FET, Unit #5.

Dexcel 501 #5

$I_D = 51.8$

$V_{DS} = 5$

$V_G = 0$

FREQ. (GHz)	S_{11} mag	S_{11} angle	S_{12} mag	S_{12} angle	S_{21} mag	S_{21} angle	S_{22} mag	S_{22} angle	G_{max} (dB)
2.0	.93	-52	.032	84	2.8	147	.84	-23	22.9
3.0	.82	-58	.039	83	2.7	139	.79	-26	17.7
4.0	.76	-90	.037	88	2.4	131	.75	-35	14.9
5.0	.73	-112	.037	115	2.4	132	.73	-33	14.2
6.0	.65	-134	.042	113	2.1	106	.86	-35	14.7
7.0	.68	-159	.047	113	1.9	88	.83	-65	13.3
8.0	.67	179	.051	112	1.8	85	.79	-57	11.9
9.0	.61	153	.056	113	1.8	81	.79	-64	11.4
10.0	.62	130	.037	104	1.4	70	.76	-77	8.8
11.0	.58	20	.048	170	1.2	66	.73	-102	6.7

Table 2.1 Measured S-Parameters and Calculated G_{max} vs. Frequency.

the behaviour of $|S_{21}|$ appears quite reasonable with a smooth decrease in amplitude. The phase of S_{21}, however, is poorly behaved with two occasions of frequencies crowding each other instead of being evenly spaced.

The data for S_{12} is highly irregular which we believe is due to the inherent presence of feedthrough between ports 1 and 2 in the mount itself. This feedthrough is the same order of magnitude as the S_{12} of the FET and could cause large errors in the measured values. The magnitude of the inherent feedthrough was 25 to 30 dB down from the incident signal level so the upper limit for the error in measuring the magnitude of S_{12} would be approximately .06.

The measured values of S_{11}, S_{21} and S_{22} are accurate enough to use in synthesizing a model of the packaged FET. It is not unreasonable to use some data smoothing in cases where the general trend is clear but the point by point details are not smooth. The probable sources of the errors in S_{11}, S_{21}, and S_{22} are: (1) the quality of the reference short circuit and through-line packages which were used in calibrating the FET holder and (2) the cumulative effects of poor cascaded VSWR on port 2 due to the flexible cable and connectors.

2.2 FET Modelling

A unilateral small signal model of an FET has been derived from the measured S-parameters presented Table 2.1. The model is valid for the packaged FET and includes lead inductance on the gate and drain leads but neglects the contact resistance and lead inductance of the source. The advantage of using such a simple model is that calculations using the model may be carried out with a hand calculator and reasonable

No. GC 19509

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SMITH CHART FORM 5301-7560-N	GENERAL RADIO COMPANY, WEST CONCORD, MASSACHUSETTS	DATE

IMPEDANCE OR ADMITTANCE COORDINATES

V_{DS} = 5 volts

I_D = 52 mA

⊙ S_{11} ⊡ S_{22}

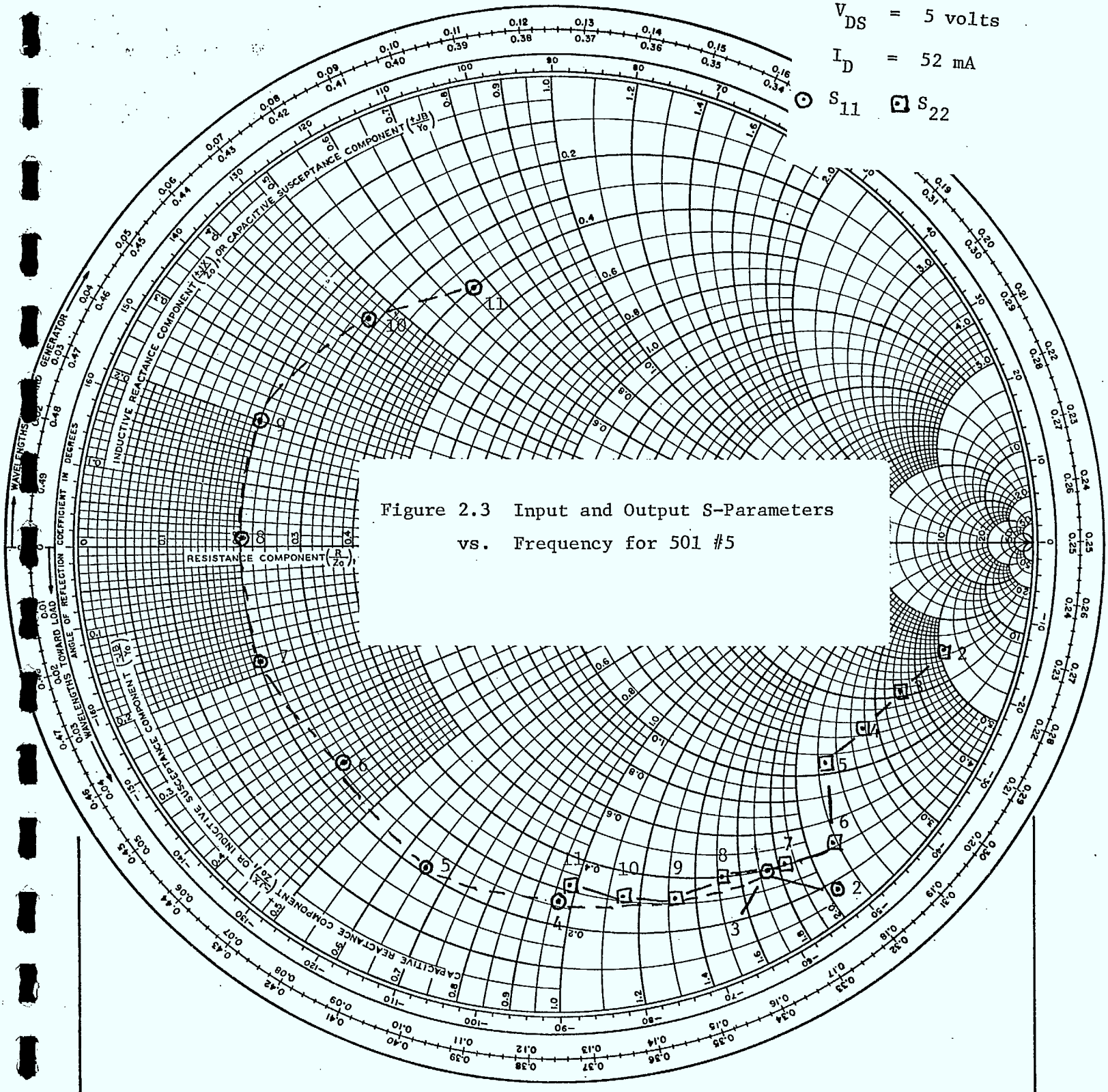
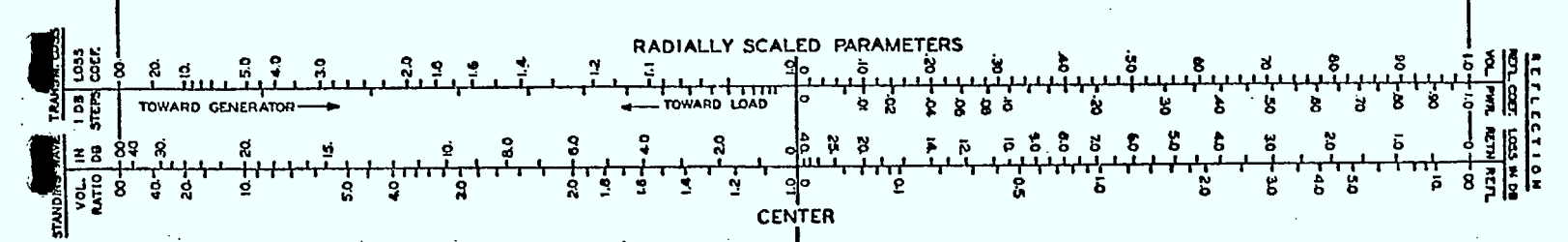
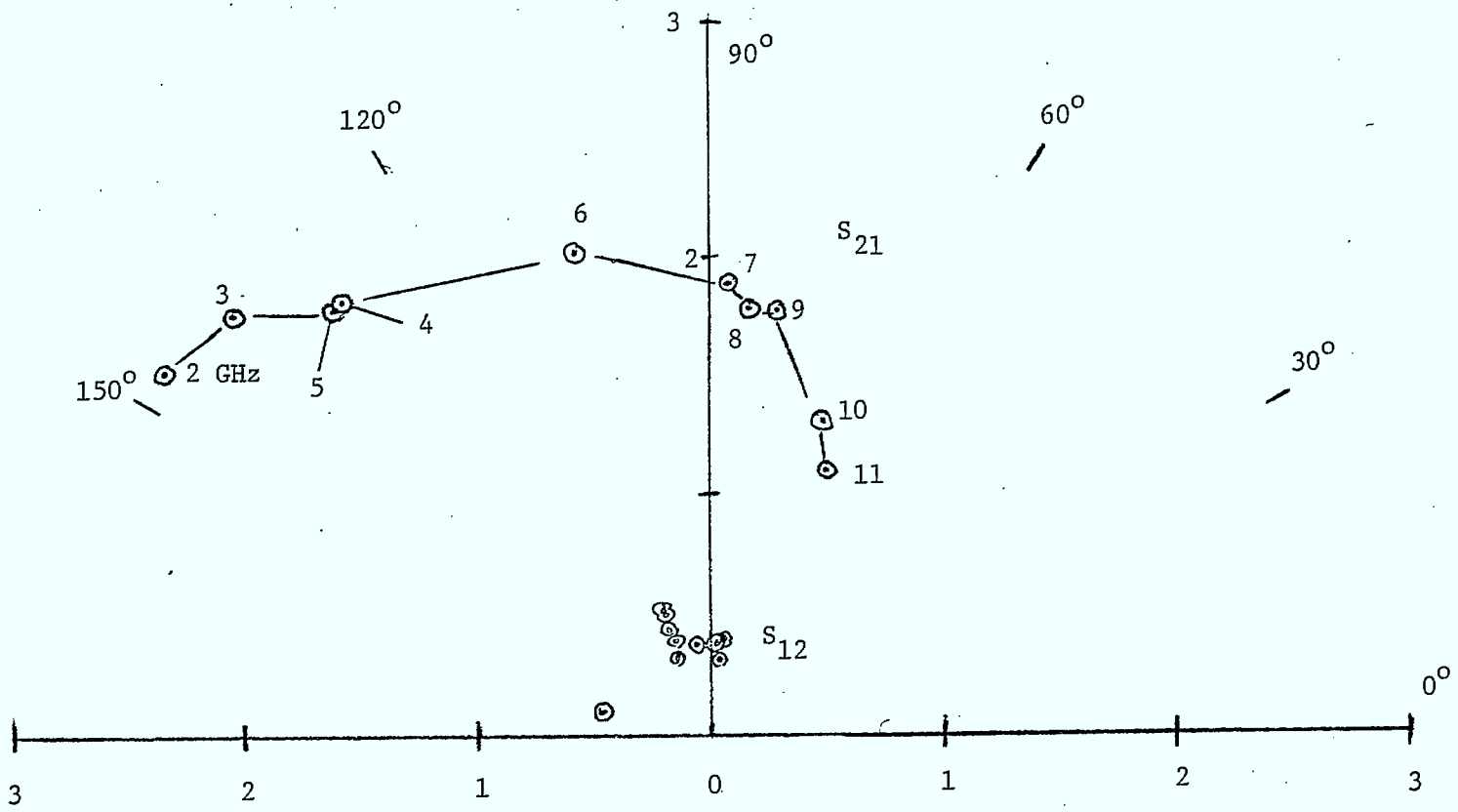


Figure 2.3 Input and Output S-Parameters vs. Frequency for 501 #5





V_{DS} = 5 volts

I_D = 52 mA

Figure 2.4 S_{21} and S_{12} vs. Frequency for Dexcel 501 #5

agreement with measurement is seen to about 8 GHz.

The model is adapted from a complete model [1] which accurately predicts FET small signal behaviour up to 12 GHz. Such models usually require computer aided optimization to select the element values [2] . The following equivalent circuit is an example of what can be accomplished with measured results and a hand calculator.

Figure 2.5 shows the complete unilateral model with the element values. The input and output RLC circuits were determined by matching the input and output impedances in the unilateral approximation, namely

$$Z_{in} = \frac{1+S_{11}}{1-S_{11}} \qquad (2\text{-}1)$$

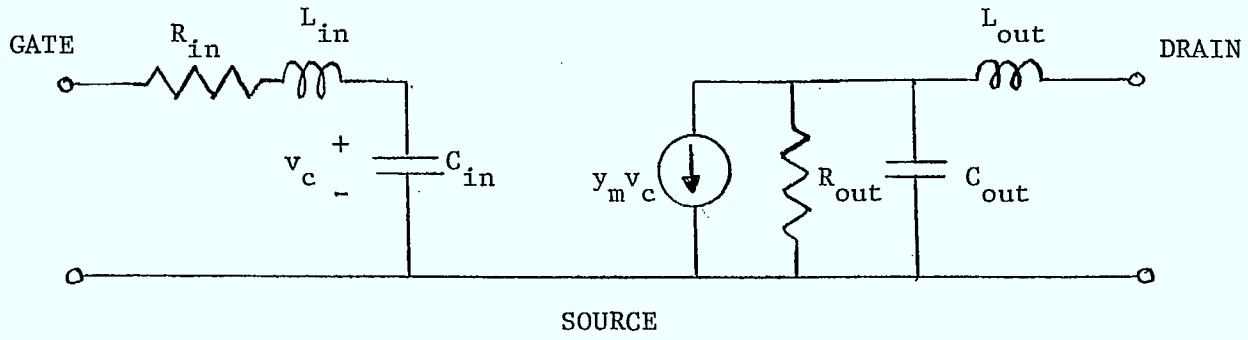
and

$$Z_{out} = \frac{1+S_{22}}{1-S_{22}} \qquad (2\text{-}2)$$

The DC value of y_m is denoted y_o and was found by extrapolating the measured value of S_{21} to DC and using the relationship between S-parameters and the impedance matrix elements, given by

$$S_{21} = \frac{2Z_{21}}{(Z_{11}+1)(Z_{22}+1)} \qquad (2\text{-}3)$$

where the Z_{ij}'s are all normalized to the Z_o of the S-parameters. Using the equivalent circuit of Figure 2.5, one can calculate the theoretical low frequency value of S_{21} and then solve for y_o.



R_{in} = 12Ω

L_{in} = .70nH

C_{in} = .57pF

R_{out} = 415Ω

C_{out} = .19pF

L_{out} = .36nH

$$y_m = y_o \exp(-j\omega\tau)$$

y_o = .0336 mho

τ = 5 psec.

Figure 2.5 Unilateral Equivalent Circuit for Dexcel 501 GaAs FET. V_{DS} = 5 volts, I_D = 52 mA.

The calculated S-parameters obtained from the equivalent circuit are compared to the measured values of S_{11}, S_{21}, and S_{22} in Figures 2.6 and 2.7 Good agreement is obtained for S_{11}, while the correlation between the measured and predicted values of S_{22} and S_{21} is not as close.

The value of the output resistor, R_o, is given by the extrapolation of the low frequency values of S_{22} to DC. Depending on the choice of how to extrapolate these values, the value of R_o could be taken higher, as high as 800 Ω in fact. But then it becomes difficult to match the S_{22} values above 7 GHz. The lower value was chosen as a reasonable compromise between fitting the data at low and high frequencies.

The worst aspect of the equivalent circuit is in the prediction of S_{21}. This is to be expected, however; because, once the S_{11} and S_{22} data have been matched, the only parameters left to fit to the S_{21} data are the DC trans-conductance, y_o, and the channel transit time τ. In the view of this fact, the degree of agreement between the measured and predicted behaviour of S_{21} which exists, validates the general usefulness of the model.

In section 3.0, the measured S-parameters at 8.0 GHz are used to analyse the general design rules for an FET oscillator.

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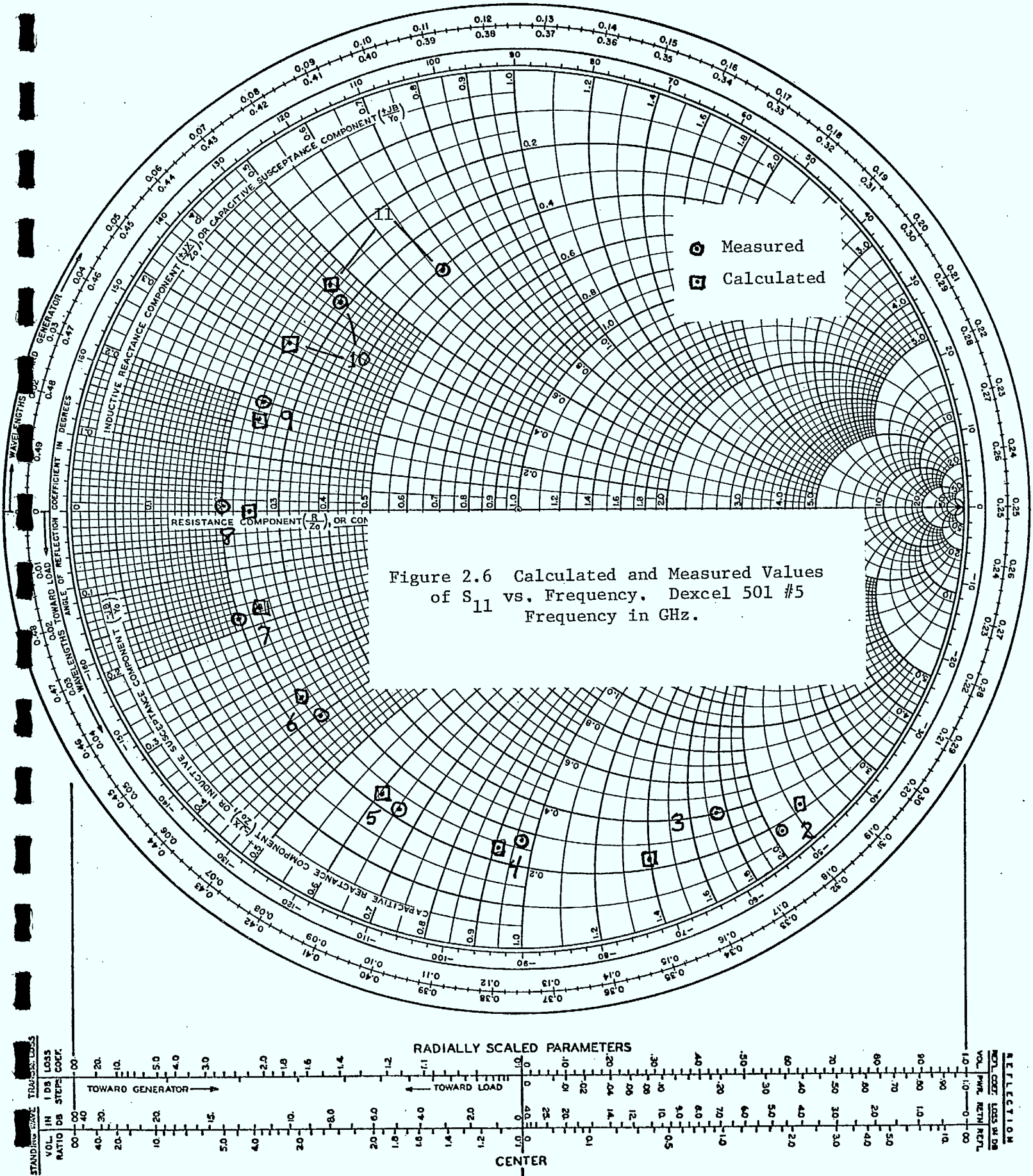

Figure 2.6 Calculated and Measured Values of S_{11} vs. Frequency. Dexcel 501 #5 Frequency in GHz.

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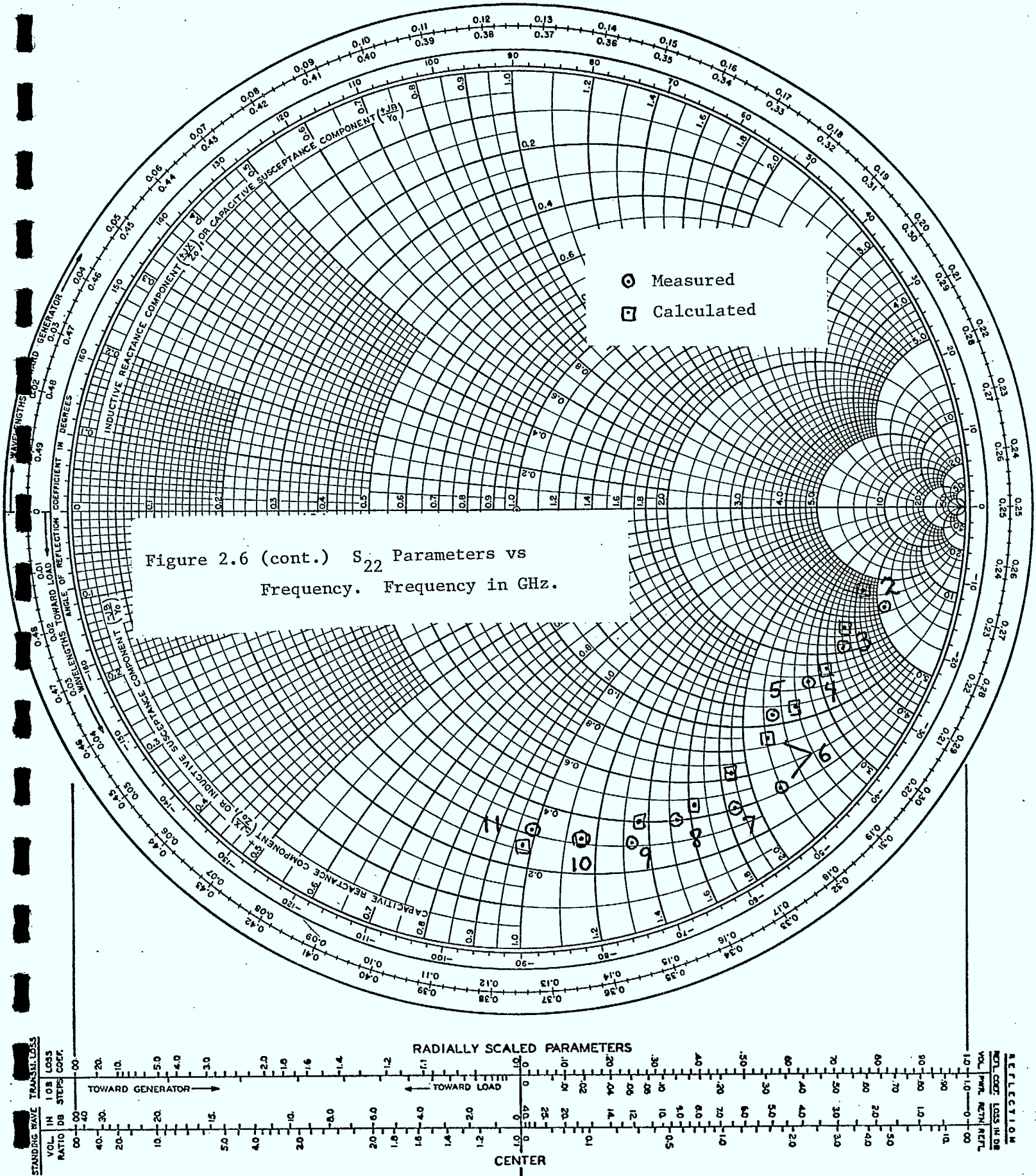


Figure 2.6 (cont.) S_{22} Parameters vs Frequency. Frequency in GHz.

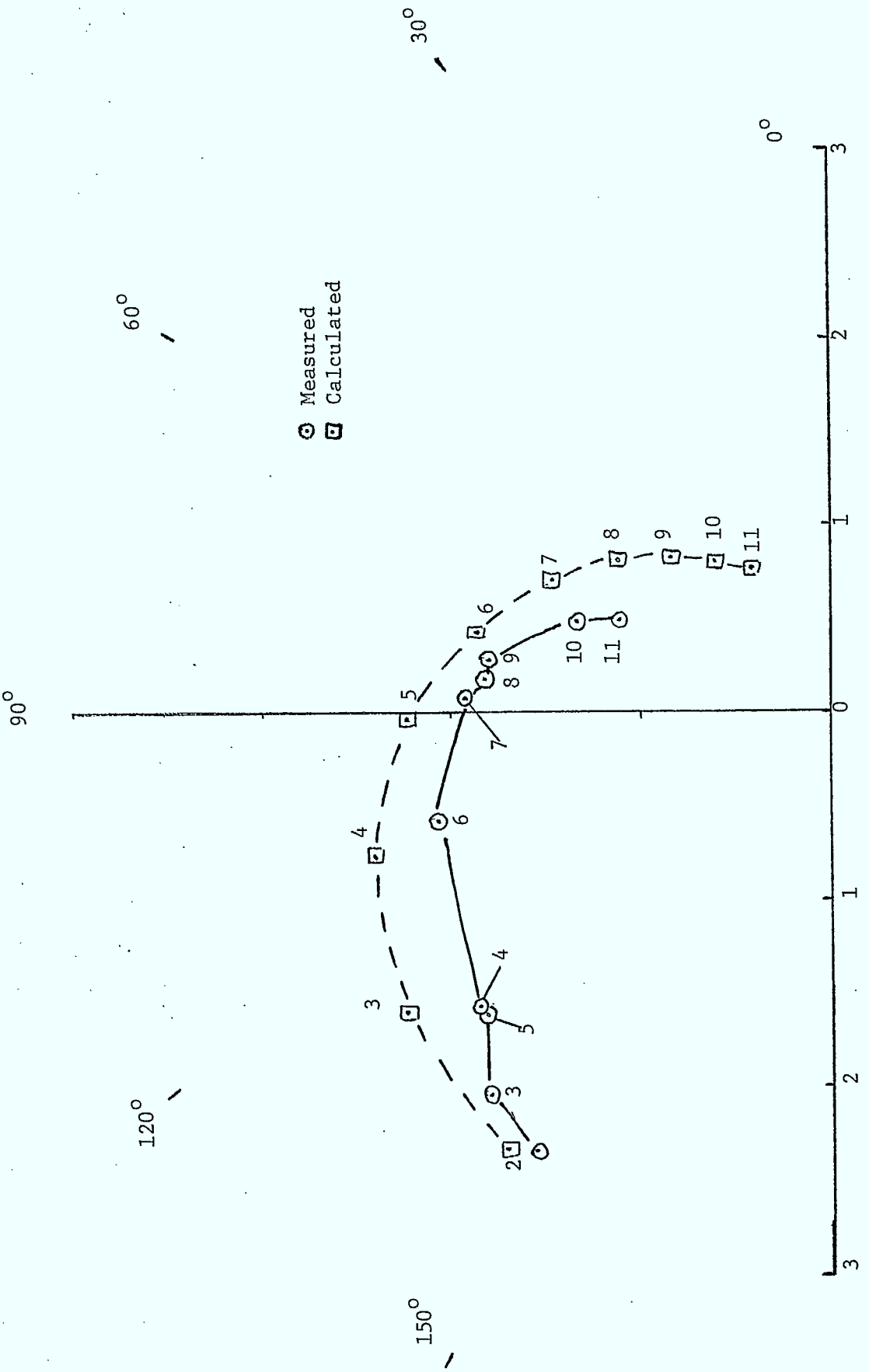


Figure 2.7 Calculated and Measured Values of S_{21} vs. Frequency. Dexcel 501 # 5. Frequency in GHz.

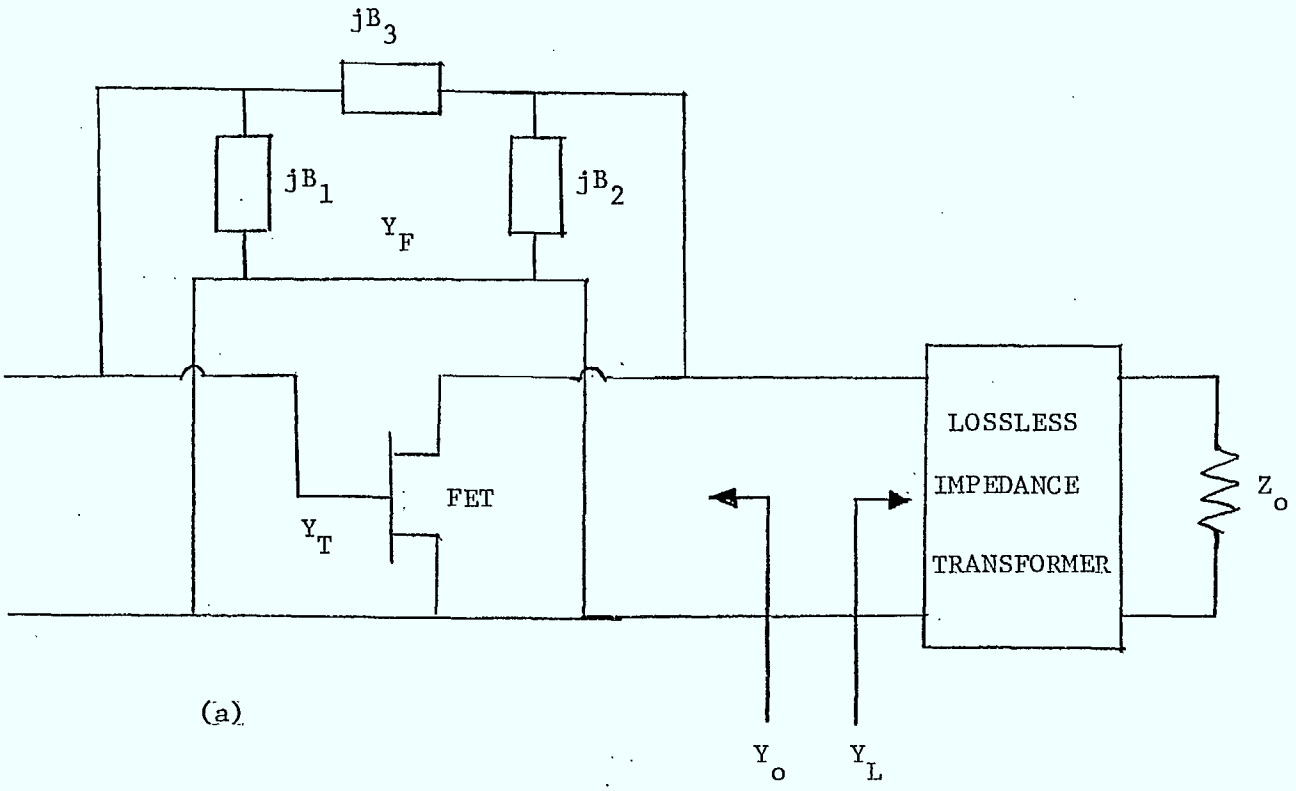
3.0 OSCILLATOR ANALYSIS AND DESIGN

To make an oscillator out of a two port device such as an FET, feedback is required to introduce a portion of the output signal into the input port. Steady oscillation is obtained when the closed loop gain is unity which, physically speaking, means that an applied voltage at the input to the FET produces a voltage at the output which in turn generates a voltage at the input which is equal in magnitude and phase to the original voltage.

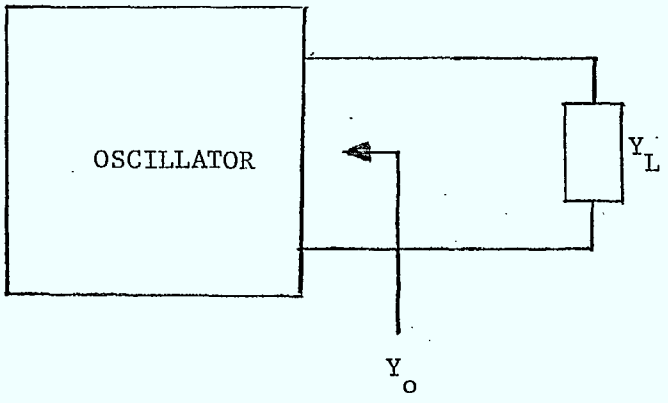
Oscillator analysis consists of determining the characteristics of the feedback network which will satisfy the above conditions. In the material to follow, the phenomenological description given above will be replaced by a more rigorous mathematical development. The theory will use the admittance matrix description of 2-port circuits connected in parallel to determine the general conditions for oscillation. Subsequently, methods of achieving the optimum behaviour from an oscillator will be discussed and an example using the measured S-parameters of a Dexcel 501 FET will be presented.

3.1 Two-Port Networks in Parallel

A generalized representation of an oscillator circuit is shown in Figure 3.1 (a). The two-port circuits are represented by their admittance matrices. The circuit Y_T represents the packaged FET together with any matching structures which are located close to the device. The feedback circuit Y_F may be a filter or an impedance transformer or any appropriate distributed microwave network. Such a network can be modelled by a 2-port lumped element pi-network with



(a)



(b)

Figure 3.1 (a) Equivalent Circuit of FET Oscillator with Feedback and Impedance Matching. (b) Black Box Representation.

lossless elements (since the feedback network is lossless), and that is what we shall use here.

The output admittance of the combined FET and feedback network, denoted Y_o in Figure 2.1, can be calculated by first combining the parallel networks Y_T and Y_F into a single network as shown in Figure 3.1 (b) with a new set of Y parameters given by

$$Y' = Y_T + Y_F \tag{3-1}$$

This addition of Y-parameters means that each element of Y' is given by the sum of the corresponding elements of Y_T and Y_F.

Denoting the elements of Y' by y'_{ij} we have,

$$Y_o = y'_{22} - \frac{y'_{12}y'_{21}}{y'_{11}} \tag{3-2}$$

Using the Y-parameter representation for the feedback network, and substituting Equation (3-1) into (3-2), we obtain an expression for the output admittance of the oscillator.

$$Y_o = y_{22} + j(B_2+B_3) - \frac{(y_{12}-jB_3)(y_{21}-jB_3)}{y_{11}+j(B_1+B_3)} \tag{3-3}$$

The parameters y_{ij} are the Y-matrix elements of the admittance matrix of the FET, Y_T.

Although the characteristics of GaAs FET's are almost universally specified by the measured S-parameters, simple transformations will convert the S_{ij} to the desired y_{ij} for Equation (3-3). These

relations are

$$y_{11} = \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$$

$$y_{12} = \frac{-2S_{12}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}} \qquad (3\text{-}4)$$

$$y_{21} = \frac{-2S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$$

$$y_{22} = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}$$

A particular feedback network will result in oscillation if the real part of the output admittance is negative. That is, if

$$\mathrm{Re}(Y_o) = G_o < 0 \qquad (2\text{-}5)$$

then the total circuit admittance, $Y_c = Y_o + Y_L$, can be made to vanish at a particular frequency and signal amplitude.

In order for the oscillation to grow from thermal noise, the total conductance $G_c = R_e(Y_c)$ must be negative in the small signal regime. This results in oscillation with the well known exponential amplitude growth which stabilizes when the magnitude of the output conductance decreases to equal the load conductance.

The task of designing a suitable feedback network for a

practical oscillator is to determine what load conductance is desired and then select the elements of the feedback network, B_1, B_2, and B_3 to yield the desired value of G_o. In the analysis to follow, one only has the small-signal transistor characteristics so one cannot accurately design the feedback circuit to produce a stable large-signal oscillation. It is possible, however, to use the fact that saturation will decrease the output conductance with signal level and select the small signal value of $|G_o|$ to be larger than the desired operating value.

The problem of determining an optimum value for G_o will be considered later, and we shall now address the problem of designing the feedback network assuming that the desired value of G_o is known.

Equation (3-3) which gives the output admittance of the entire oscillator must be expanded to determine the real and imaginary parts of Y_o. At this point we make an important simplifying assumption, namely that the FET is unilateral, or that y_{12} is negligible. In Equation (3-3), this implies that $|y_{12}| << |B_3|$ which means that the impedance of the series feedback element should not be too high. In practical FET oscillators operating in X-band, the maximum available forward gain of the FET will be in the neighbourhood of only 10 dB or less, so the amount of feedback needed in order to obtain a unity loop gain will have to be reasonably large. This rules against practical oscillator designs with a low value of B_3.

Returning to Equation (3-3), setting $y_{12} = 0$ and expanding, we obtain for the real part of the oscillator output admittance, denoted G_o,

$$R_e(Y_o) = G_o = g_{22} - \frac{g_{11}B_3(b_{21}-B_3) - g_{21}B_3(b_{11}+B_1+B_3)}{g_{11}^2 + (b_{11}+B_1+B_3)^2} \quad (3\text{-}6)$$

The feedback circuit elements B_1 and B_3 are present in this equation, but B_2 is absent. This is because B_2 appears directly in shunt with the oscillator output terminals and only affects the output susceptance without affecting the conductance.

Equation (3-6) may be treated as an equation in two variables, B_1 and B_3, which may be solved given a particular value of G_o. It is helpful to combine G_o with g_{22} and define a new parameter.

$$g'_{22} = g_{22} - G_o \quad (3\text{-}7)$$

before rearranging Equation (3-6). A complete derivation is given in Appendix A, and the final result is a quadratic equation in B_3 with coefficients which are functions of B_1.

$$a(B_1)B_3^2 + b(B_1)B_3 + c(B_1) = 0 \quad (3\text{-}8)$$

The coefficients are given by

$$a(B_1) = g'_{22} + g_{11} + g_{21} \quad (3\text{-}9a)$$

$$b(B_1) = 2g'_{22} + g_{21})B_1 + b_{11}(2g'_{22} + g_{21}) - g_{11}b_{21} \quad (3\text{-}9b)$$

$$c(B_1) = g'_{22}B_1^2 + 2\, g'_{22}b_{11}B_1 + g'_{22}(g_{11}^2 + b_{11}^2) \quad (3\text{-}9c)$$

Equation (3-8) may be solved given a particular value of G_o (hence g'_{22}) by picking successive values of B_1 and solving the quadratic equation

$$B_3 = \frac{-b(B_1) \pm b^2(B_1) - 4a(B_1)c(B_1)}{2a(B_1)} \qquad (3\text{-}10)$$

If the expression inside the radical sign is negative, then no solution is possible for real values of B_1 and B_3 (lossless feedback circuit).

The values of g_{ij} and b_{ij}, the FET y parameters, were calculated from the measured values of the S-parameters presented in section 2.0. A frequency of 8.0 GHz was chosen as it was the highest frequency for which the unilateral FET model was in reasonable agreement with the measurements. The calculated y parameters, normalized to .020 mho are

$$y_{11} = 5.44 - j.25$$

$$y_{12} = 0.32 - j.18$$

$$y_{21} = 2.12 - j6.58$$

$$y_{22} = 0.15 - j.53$$

The value of y_{12} has been included to estimate the validity of the unilateral assumption. It can be seen that the error caused by this assumption is not entirely negligible. If $|B_3| < 1.5$, then $|y_{12}|$ will be approximately 20% or greater of $|B_3|$ and the assumption that $y_{12} - jB_3 \simeq -jB_3$ will be highly questionable.

In spite of this objection, we have proceeded with the simplified analysis because we believe that the general nature of the results is more important at this stage than rigorous quantitative accuracy. The derivation in Appendix I provides the full expansion of Equation (3-6) of which the expressions in Equation (3-9) are

special cases for $y_{12} = 0$. It would be a straight-forward though time consuming task to solve for B_1 vs. B_3 including the effects of y_{12}.

After substituting the calculated y parameters as required into Equation (3-9), a series of curves of B_1 vs. B_3 were calculated for various values of G_o. The results are shown plotted in Figure 3.2. The values of B_1 and B_3 are normalized as is the value of G_o, to .020 mho. It can be seen immediately that a necessary condition for oscillation is that $B_3 < 0$. The condition $B_3 = 0$, corresponding to no external feedback cannot possibly result in oscillation which confirms our expectations for this unilateral device.

The region of maximum available small signal negative conductance is located within the closed contour labelled $G_o = -2.0$ and corresponds roughly to $B_1 = 5.5$ and $B_3 = -3.5$. For a given value of G_o, there are an infinite number of choices of the pair (B_1, B_3) which will give the desired result. The choice of which particular combination to use will be dictated by other factors such as the required value of the output susceptance and the ease of synthesizing the corresponding distributed circuit. There is, as well, the problem of frequency selectivity which requires that the oscillation condition, $Y_o = -Y_L$ be satisfied at only one frequency, and this could affect the choice of (B_1, B_3).

3.2 Oscillator Design

With these constraints in mind, we can use Figure 3. to design a feedback circuit to achieve an oscillator circuit with a given output conductance. The problem now is to choose the correct value of G_o.

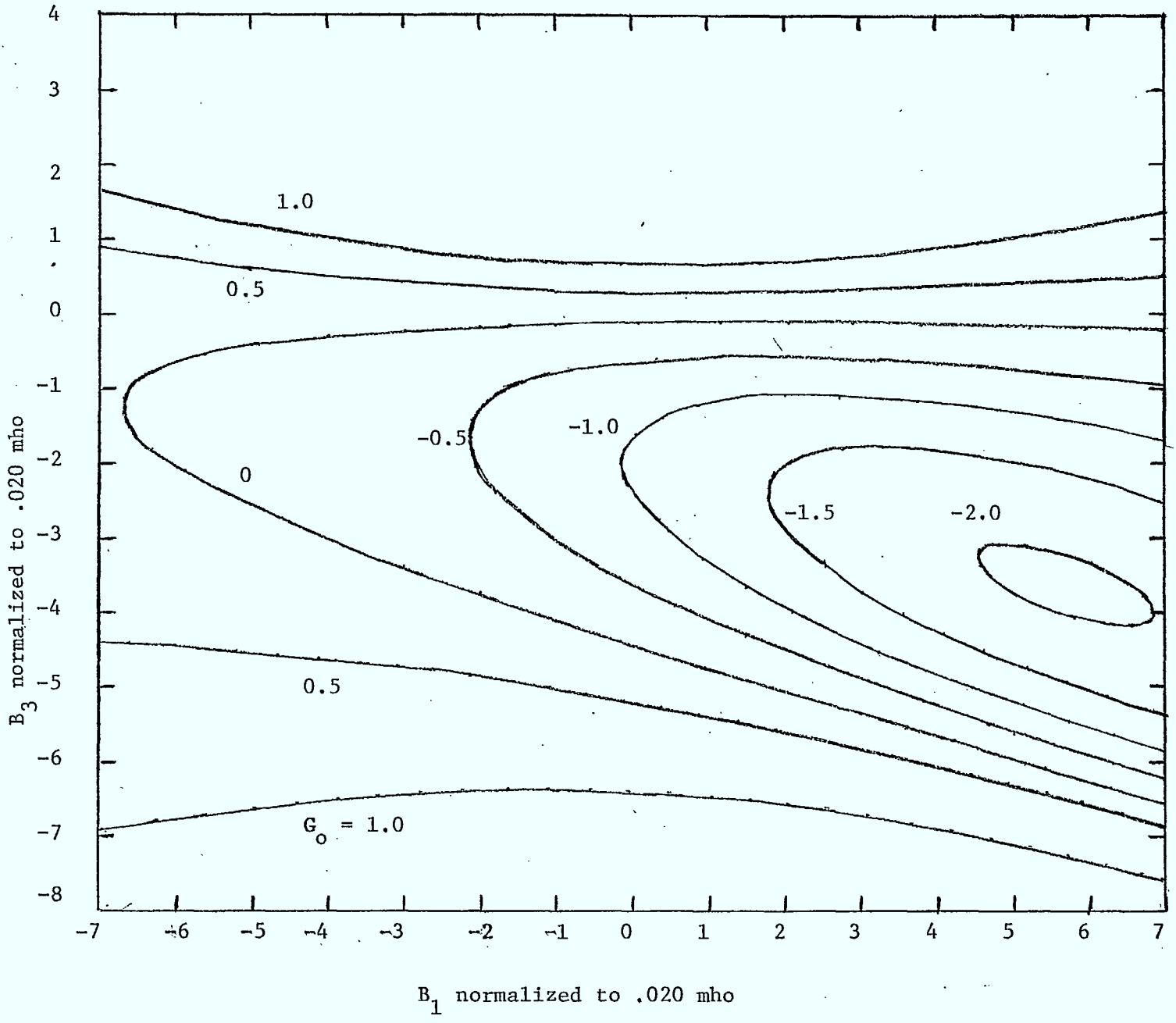


Figure 3.2 Contours of Constant G_o on B_3 vs. B_1 Plane

We shall assume that the primary design goal for an oscillator is to obtain maximum RF power at a given bias point. The factors which affect the oscillator output power are primarily the RF load line and the I_D vs. V_{DS} curve for $V_{GS} = 0$. This may be seen by referring to a plot of the transistor DC I-V characteristics. Figure 3.3 shows such a plot for a typical Dexcel FET. The bias point is assumed as $I_D = 40$ mA, $V_{DS} = 3.5$ volts. In steady oscillation, the instantaneous values of I_D and V_{DS} will move along the load line established by the load conductance, G_L. The excursions of the current and voltage will approximately be limited by the curve corresponding to $V_{GS} = 0$ in one direction and by the limit of $I_D = 0$ in the other direction. These limits correspond roughly to the familiar limits of saturation and cut-off respectively in bipolar transistors.

Three load lines, corresponding to $G_L = 0.5$, 1.0, and 2.0, have been drawn through the bias point and the limits to the voltage and current swings have been shown for the $G_L = 1.0$ case. The RF power generated is

$$P = \tfrac{1}{2}\left(\frac{\Delta I_D}{2}\right)\left(\frac{\Delta V_{DS}}{2}\right)$$

which has a value of 32 mW in this case. The RF power generated with the other two load lines would be less which indicates that $G_L = 1.0$ is roughly the optimum value. A detailed plot of the RF power vs. load conductance as derived from this type of calculation is shown in Figure 3.4. This indicates that the optimum value for the load line conductance occurs at approximately 17 mmho or 0.85 normalized to 20 mmho.

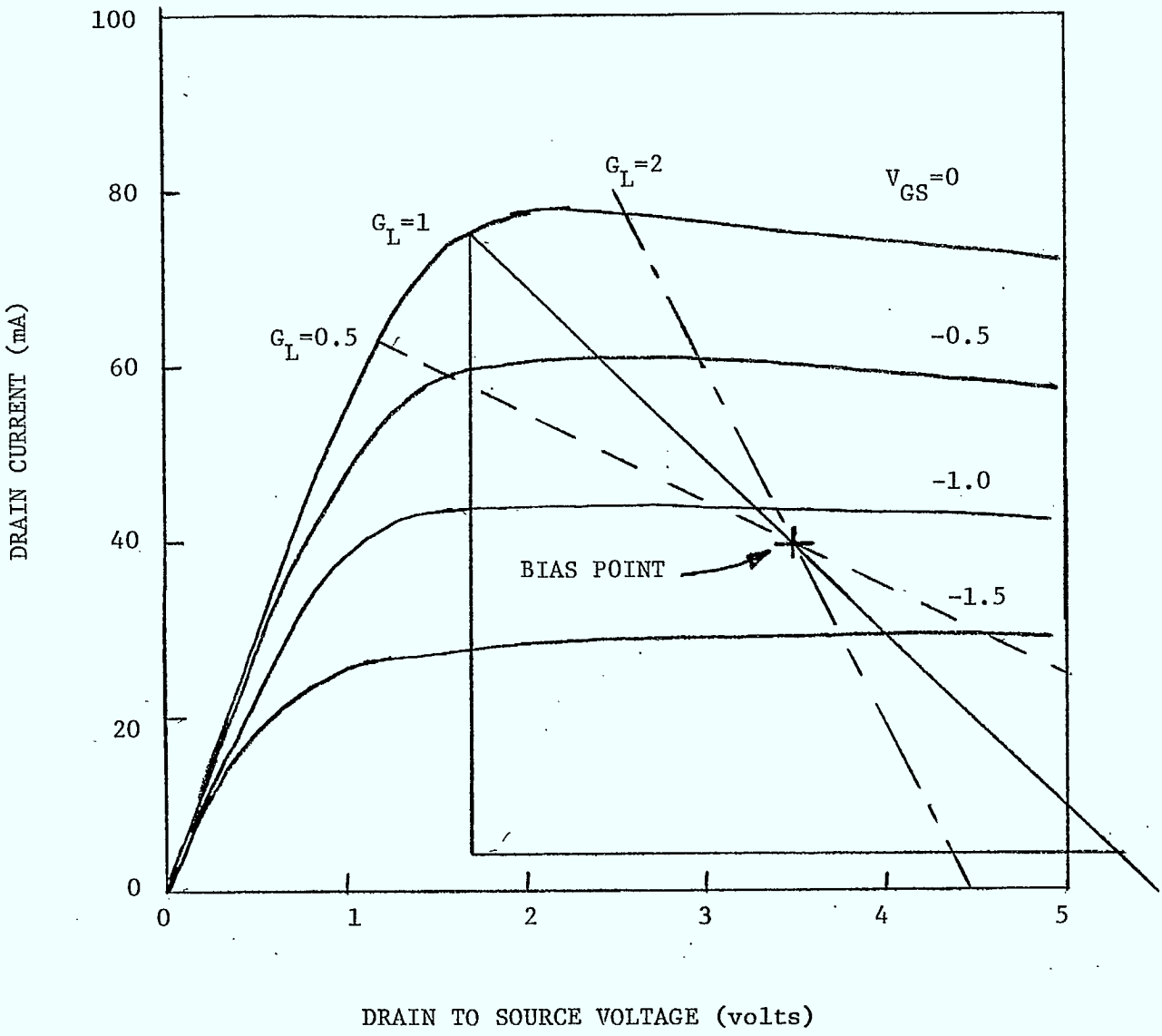


Figure 3.3 FET I-V Characteristics with Load Line Conductance (G_L) Normalized to .020 Mho.

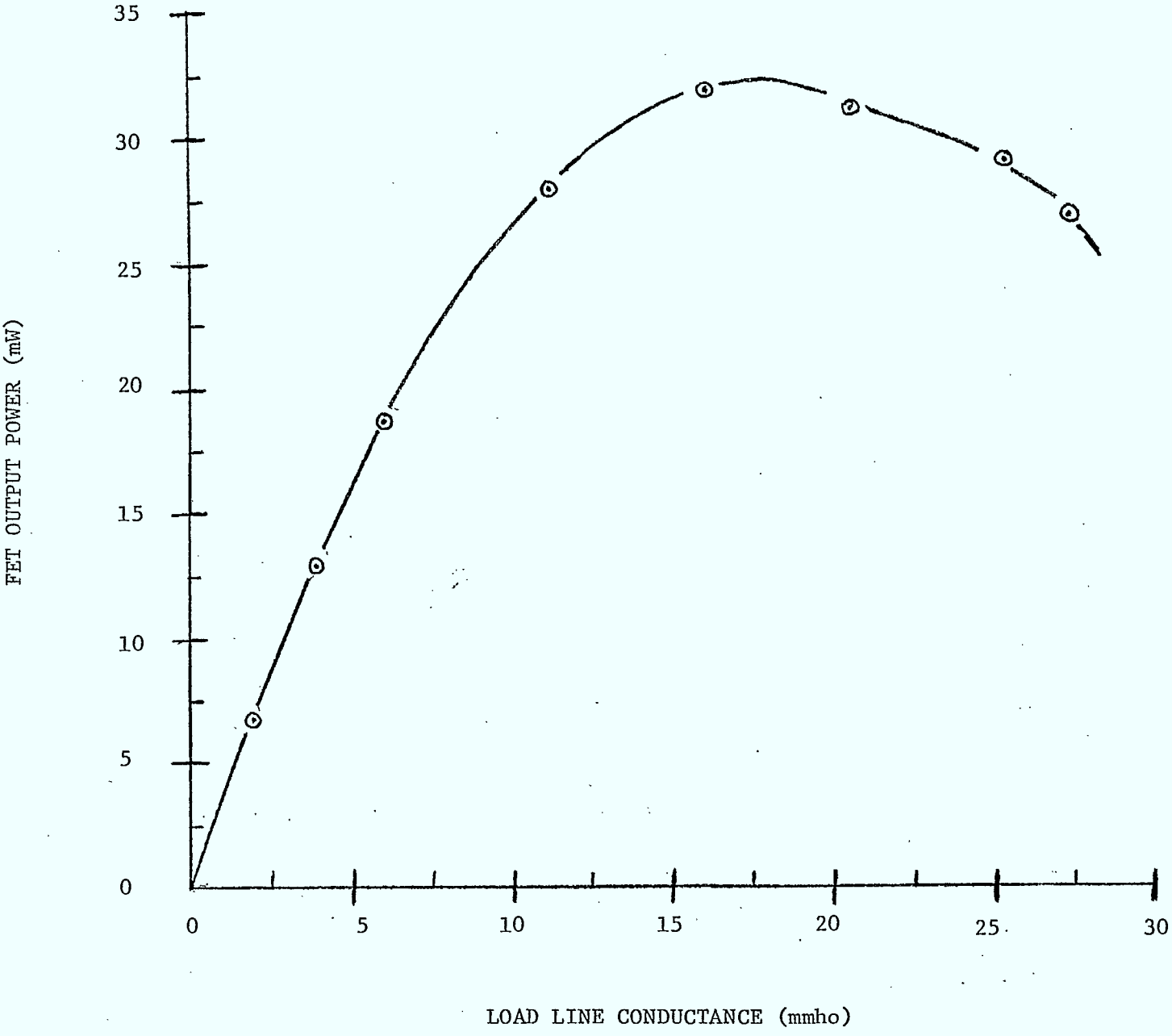


Figure 3.4 Output Power vs. Load Line Conductance

This load line conductance is not the desired value of G_L, however. It is the conductance which must be seen by the FET at its output terminals and consists of the load conductance G_L plus the conductance looking into the feedback network as seen in Figure 3.5. The admittance seen by the FET is designated Y_L' and is given by

$$Y_L' = Y_L + Y_F \tag{3-11}$$

If the amount of feedback required to sustain oscillation is too large then the feedback conductance, $G_F = R_e(Y_F)$, may be a substantial fraction of the desired load line conductance. This would result in less useful power available from the oscillator and, hence, a reduction in oscillator efficiency. This can be avoided by keeping the magnitude of B_3 as low as possible; although to achieve a given load line, this may not be possible.

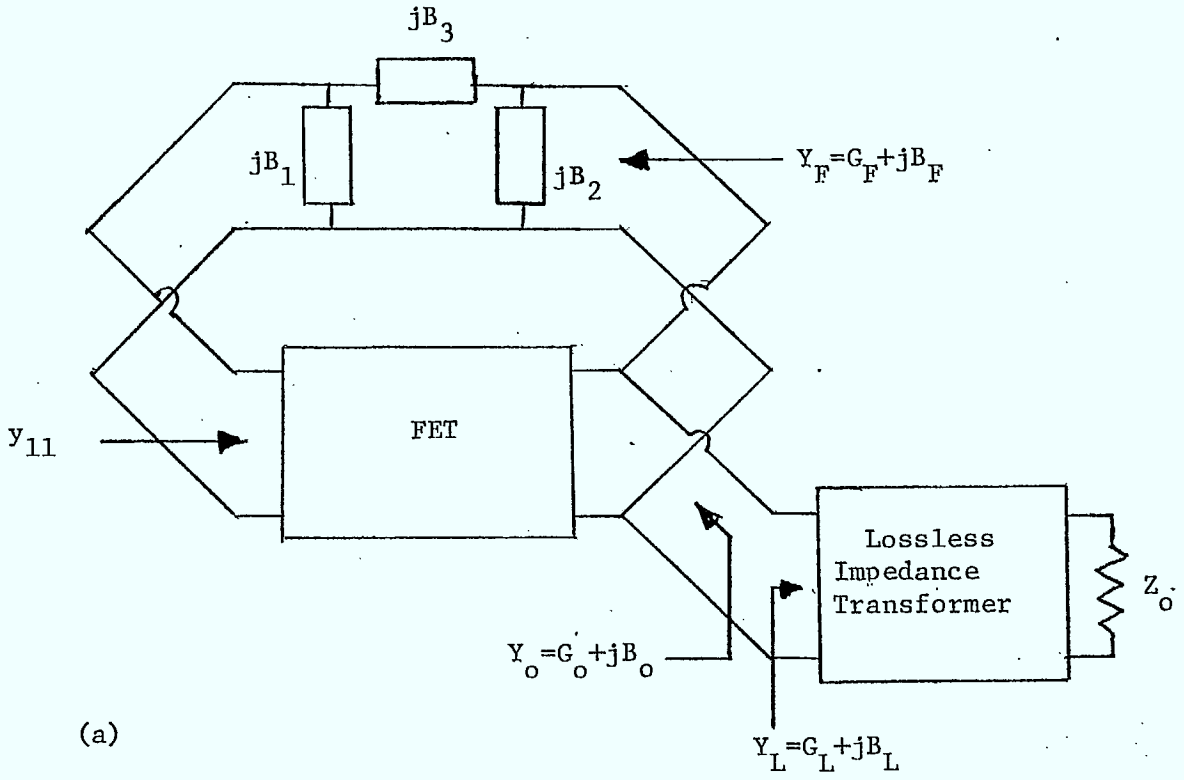
In general, achieving a maximum output power design requires selecting values of B_1 and B_3 which minimize the value of G_F while achieving an optimum load line conductance, G_L'. Figure 3.2 shows that, for this example at least, keeping $|B_3|$ as small as possible means accepting a lower value of G_o and sacrificing some of the margin by which $|G_o|$ exceeds G_L in the small signal limit.

In the small signal limit, we must have $|G_o| > G_L$ for oscillations to grow, but the two extremes

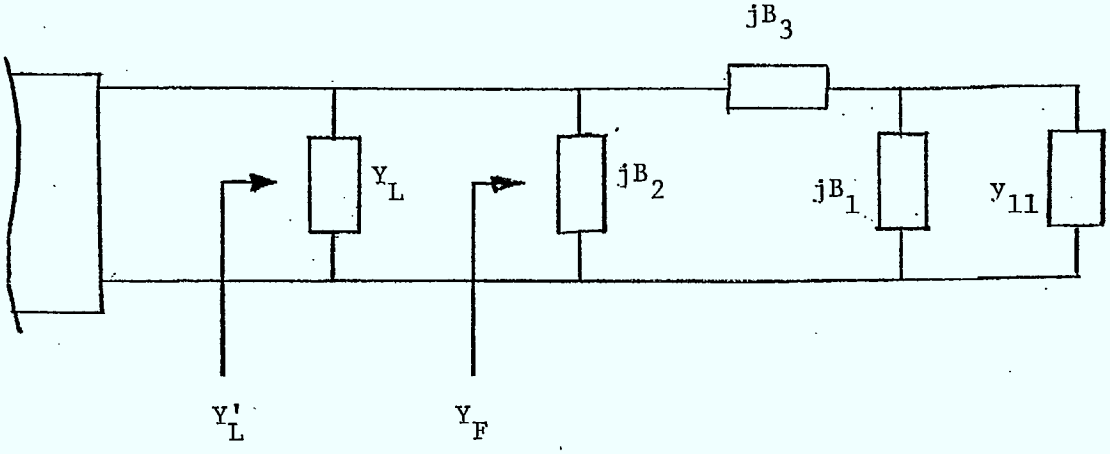
$$|G_o| > G_L$$

and

$$|G_o| >> G_L$$



(a)



(b)

Figure 3.5 (a) FET Equivalent Circuit
(b) Output Circuit with Feedback Admittance In Parallel with Load Admittance.

should be avoided. The first leads to low output power because only a small amount of saturation is needed to establish equilibrium. Another undesirable side effect of the first extreme is unduly high AM noise due to the poor amplitude stability. The second extreme leads to excessive voltage and current excursions and represents a circuit design which could lead to degraded oscillator reliability.

A reasonable compromise between the two extremes is given by

$$1.5G_L < |G_{o,ss}| < 2.5\ G_L$$

with the exact choice being experimentally determined.

4.0 EXPERIMENTAL OSCILLATOR CHARACTERIZATION

The principles presented in Section 3.0 can be used to interpret the behaviour of a practical GaAs FET oscillator. Such easily measurable quantities as the dependence of the output power on the drain current and the DC I-V characteristics can be used in conjunction with an estimate on the load conductance seen by the FET to determine whether or not an optimum design has been attained.

4.1 General Characteristics

Several Dexcel 501 FET's were used to test the performance of an MIC oscillator circuit on .025 inch thick alumina substrate. The circuit was designed by R. Hum of CRC and uses a bandpass filter as the feedback circuit. Figure 4.1 shows the complete circuit schematic except that the dimensions of the microstrip circuit are not shown. The absence of any impedance transformer on the 50 Ω line, at the output of the circuit sets the load conductance in the range of 20 mmho. As seen in Figure 3.4, the maximum output power would be obtained for an RF load line conductance of approximately this value. To estimate the effective shunt conductance of the feedback bandpass filter requires precise knowledge of the characteristics of the filter. It will be shown later, however, that the measurements indicate that this shunt conductance is fairly small. This is entirely reasonable and simply implies that the feedback network acts as an impedance inverter at resonance. The value of S_{11} for the FET in X-band is such that the input admittance of the FET is large and nearly real. A quarter wavelength section of line (or its equivalent) acting as an impedance

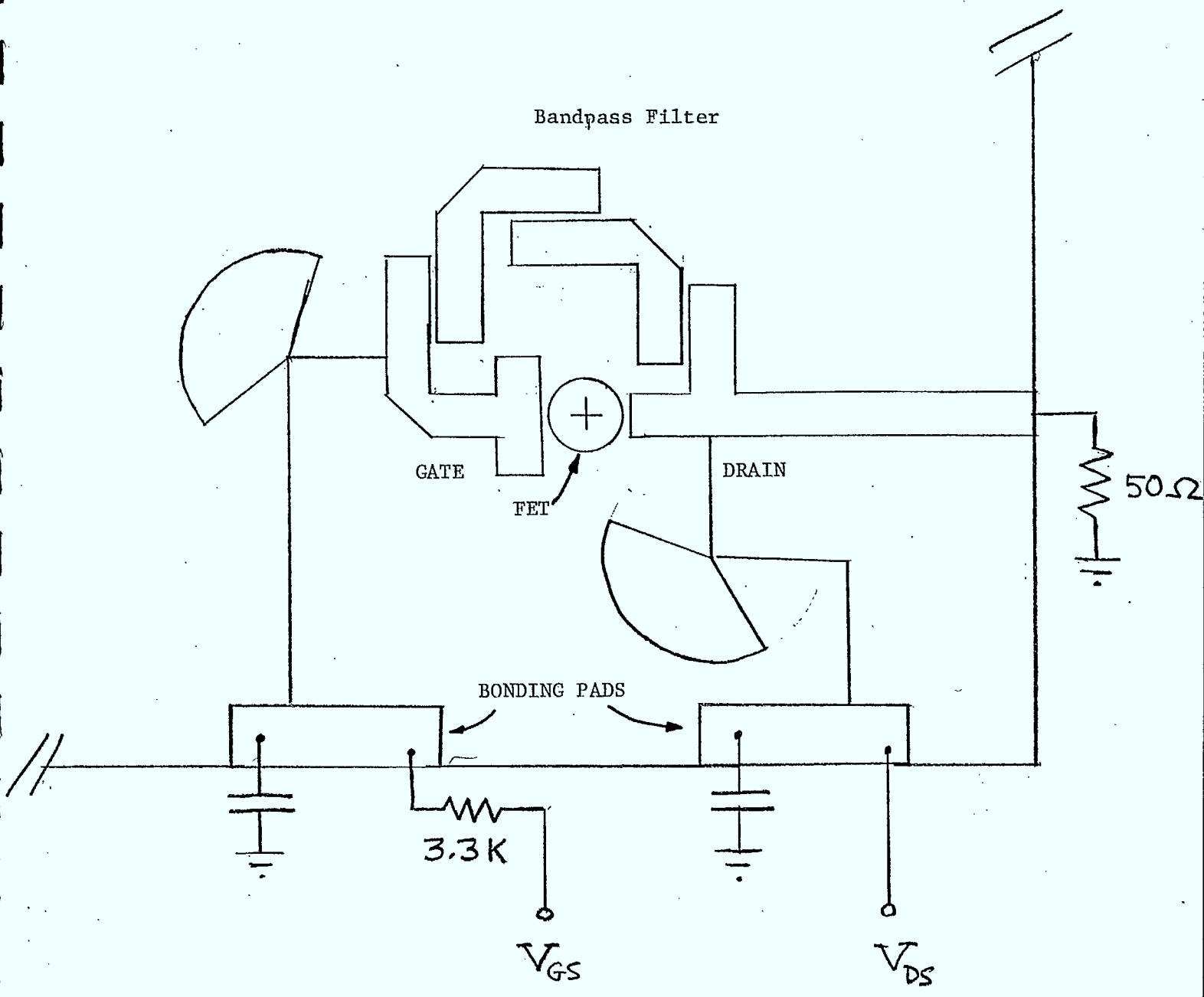


Figure 4.1 Schematic of Microstrip Oscillator Circuit.

inverter will transform this to a small conductance which will not appreciably disturb the oscillator load conductance.

Five FET's were installed in this circuit, and the frequency and output power of the resulting oscillators were recorded. The results, shown in Table 4.1, indicate the extent to which the available output power depends on the drain saturation current, I_{DSS}. In each case the gate voltage was adjusted to yield the maximum possible output power. The RF power spectrum of the oscillators was observed and showed clean spectra with no indication of low frequency bias oscillations present.

4.2 Detailed Analysis

It is instructive to analyse the results of the oscillator measurements further in light of the results presented in Section 3.0 to determine if the optimum load conductance has been realized. In doing so, it will be assumed that the FET S-parameters presented in Section 2.0 and used in Section 3.0 are valid. Although this may affect the quantitative accuracy of the results, it does not affect the validity of the approach. All that is needed are accurate S-parameters measured at the oscillation frequency of the results to be analysed.

As discussed at the beginning of this section, the load conductance seen by the FET will be approximately .020 mho. The microstrip T-junction at the point where the feedback circuit branches off the output line will only affect the output conductance if its equivalent circuit incorporates series reactances of a reasonable

DEXCEL 501 FET's

DEVICE NUMBER	I_{DSS} (V_{DS}=2volts)	eff(%)	P_{out} (mW)	at V_{DS} (volts)	I_D (mA)	freq. (GHz)
#18	105 mA	15.6	28	8	22.5	10.65
# 8	54	19.0	18	7	13.5	10.75
# 6	64	19.0	20	7	15.0	10.75
# 7	58	17.2	17.5	7	14.5	10.70
# 5	57	19.1	18	7	13.5	10.80

Table 4.1

Oscillator Results. Output Power and Frequency.

magnitude. The results to follow suggest that any such reactances, for the frequency in question at least, are negligible. More detailed oscillation characteristics were measured for FET #8 at a lower bias value of V_{DS} = 4.0 volts. The bias current was adjusted by varying the gate voltage while keeping V_{DS} fixed and the output power was measured. The result, shown in Figure 4.2 shows that the onset of oscillations is quite abrupt after which the output power remains fairly constant up to the maximum bias current, I_D = 42 mA, which was obtained at V_{GS} = 0. This current is substantially less than the value of I_{DSS} = 54 mA, the difference being due to rectification effects of the oscillation.

Using the assumed load conductance of .020 mho, the RF voltage swing at the FET terminals may be calculated. At the maximum power level of approximately 6 mW, the voltage swing would be 0.77 volts peak and the current would be 15.4 mA assuming a purely real load admittance. Since the frequency of oscillation is set by the net balancing of the load and oscillator susceptance, the assumption of a purely real admittance is reasonable. This assumption is not valid to the extent that the feedback circuit loads down the 50 Ω output line, because the load line conductance is determined by the sum of the feedback and load admittances (see Figure 3.4).

The calculated RF voltage and current swings at the bias point of maximum power V_{DS} = 4.0 volts and I_D = 17 mA can be superimposed on a plot of the I-V characteristics. This is shown in Figure 4.3. It is immediately obvious from this picture that the indicated bias point is far from optimum from the viewpoint of generating maximum power. The power is maximized by choosing a bias

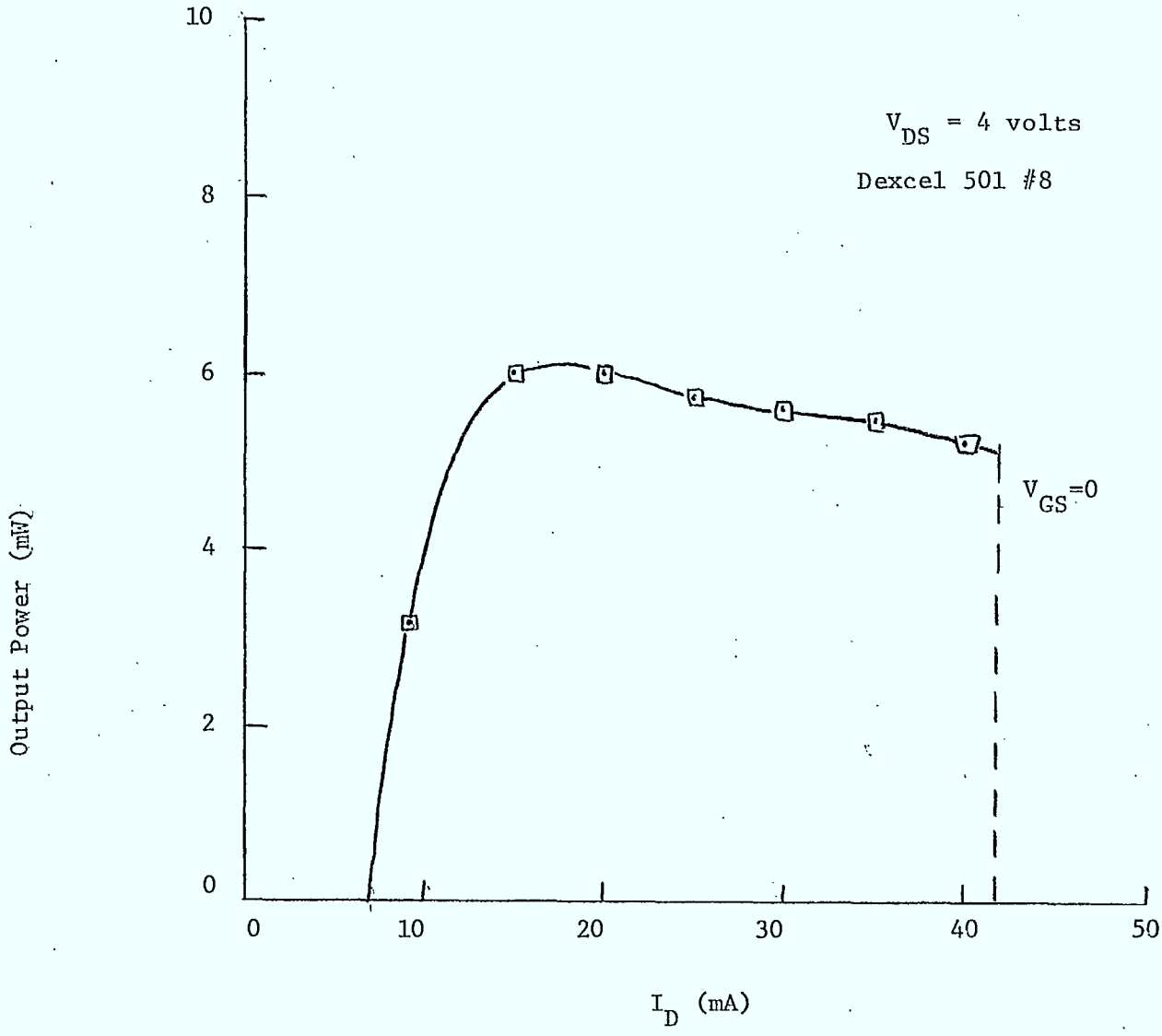


Figure 4.2 Output Power of Oscillator vs. Drain Current.

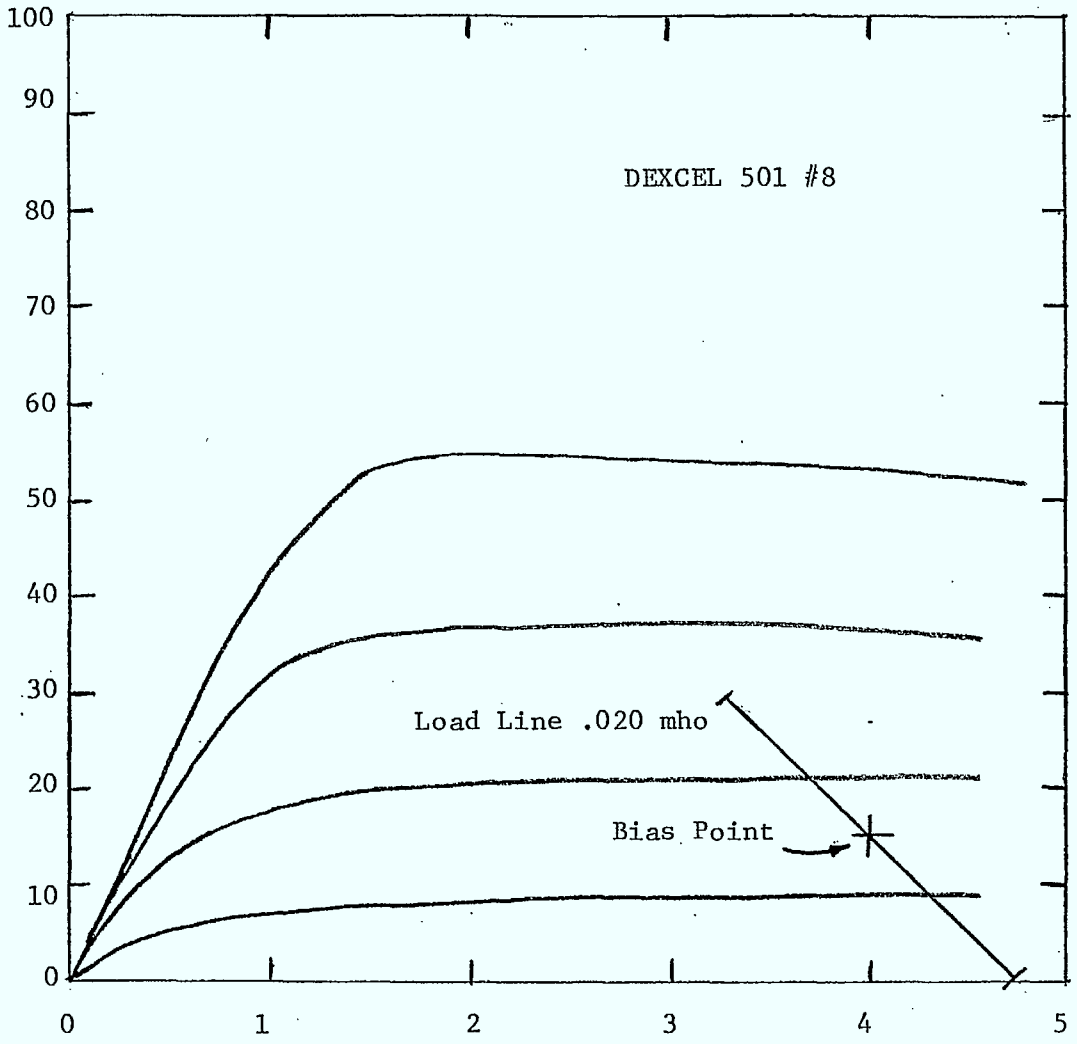


Figure 4.3 I-V Characteristics of Dexcel FET with Load Line and RF Voltage and Current Swing.

point of approximately ½ I_{DSS} which would be I_D = 26 mA. A rough calculation of the type used to generate Figure 3.3 shows that, for such an optimized bias point, the output power should be nearly 30 mW. Instead, we see a power of only 5.7 mW at that bias point. There are three possible explanations for the low output power of the oscillator. They are as follows:

(1) The RF load line may not be the optimum value to achieve maximum power

or

(2) The feedback circuit may load down the output circuit and rob power from the load

or

(3) The feedback circuit elements may not be the right value to present a small signal negative output conductance of large enough magnitude to allow the signal level to grow to full saturation,

or a combination of the above factors.

The first explanation may be discarded, because it is the least critical of the above. For the bias point at V_{DS} = 4.0 volts, I_D = 26 mA, the load line conductance would have to either decrease by a factor of 20 or increase by a factor of 3 to account for the reduced output power. Although the required increase is not too great to imagine, it would require too large an RF current swing to account for the power which was observed. Specifically, to generate 6.0 mW into a load conductance 3 times larger than the optimum of .020 mho would require a peak RF current swing of 27 mA which could not be

achieved at the measured bias value of I_D = 17 mA.

Therefore, the other two explanations are the only likely causes. In order to determine which of the last two causes (or what combination of both of them) is responsible, it is instructive to consider the significance of the results presented in Figure 4.2. The abrupt decrease in output power below a drain current of 15 mA can be explained as follows. Assume that the oscillator load line conductance is nearly .020 mho. This results in a peak RF current swing of 15.4 mA. This implies that, in order to maintain an output power of 6.0 mW, the DC bias current must be at least this value. If it is not, the channel will be pinched off during part of the RF cycle which will cause clipping of the RF waveform. Above I_D = 15 mA, there is no severe clipping, but the power will not increase above 6 mW because the oscillation has been limited at a relatively low RF current swing. This is due primarily to the last explanation presented above.

This area of circuit design is shown in Figure 4.4. The saturation of the FET as the signal level grows causes a drop in the magnitude of the output conductance. If the load conductance is too large, the output voltage and current cannot reach their full RF magnitudes and the output power is reduced. This was discussed earlier in Section 3.0.

It is now apparent that the explanation for the results presented in Figure 4.2 is that the FET output RF voltage and current cannot attain large enough values to achieve the full potential output power. It is quite possible that it is impossible to achieve a large enough small signal value of $|G_o|$, remembering that the results

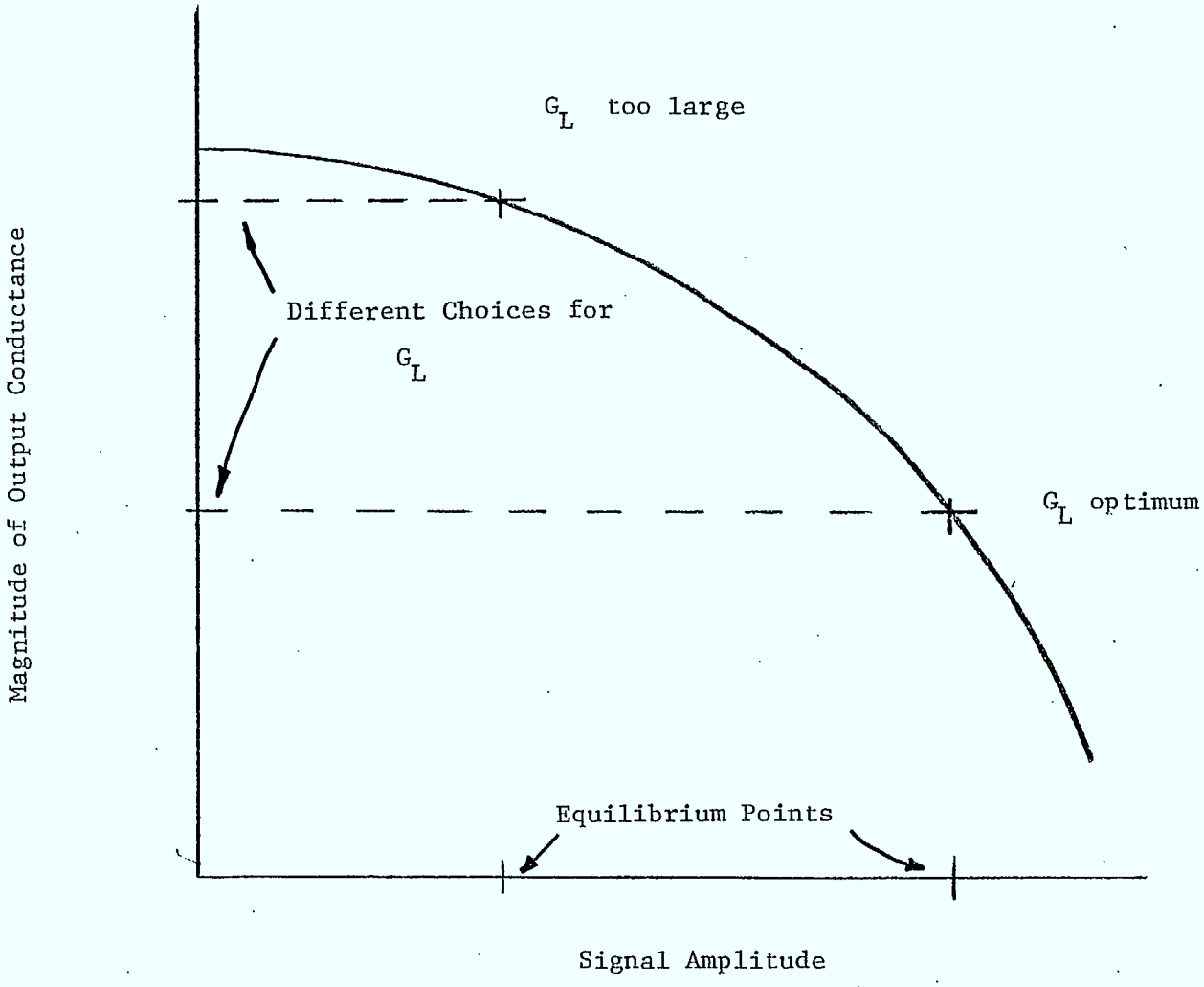


Figure 4.4 Saturation of Output Conductance vs. Signal Amplitude and Stability Points.

in Figure 3.1 indicated that there was a definite maximum value of $|G_o|$ which could be attained in the region of $G_o < 0$. If, however, the bandpass filter is not optimally designed for this FET, then it may be possible to increase the small signal magnitude of the output conductance so that the oscillator will saturate at a larger signal amplitude and generate more RF power.

5.0 SUMMARY AND CONCLUSIONS

A procedure for analysing grounded source FET oscillators in the microwave region has been presented. The method uses a lumped element pi-network representation of the feedback circuit which is connected in parallel with the FET itself. Using two-port network theory, the output admittance of the composite oscillator can be calculated and examined for regions where the oscillator output conductance is negative.

A specific example was calculated using the measured S-parameters of a Dexcel type 501 FET, and it was seen that the magnitude of the negative output conductance was limited to a value of only slightly more than .040 mhos. It was also shown how to estimate the optimum load line for a particular device given the DC I-V characteristics. Thus, the feedback circuit could be designed to generate a small signal negative conductance whose magnitude was sufficiently larger than the chosen load line conductance to result in fully saturated oscillation at the desired signal amplitude.

An evaluation of an experimental circuit led to the conclusion that the magnitude of the small signal output conductance was not sufficiently larger than the load line conductance established by the output circuit. The oscillator behaved as if the RF drain current amplitude was saturating at a much smaller value than would be imposed by the two extremes of pinch-off and drain current saturation. It might be possible to modify the feedback circuit to increase the available

output conductance, but not necessarily. Figure 3.2 showed that a certain maximum value of $|\tilde{G}_o|$ is reached and the circuit which was tested may have already realized this condition.

5.1 Reliability Factors

The primary circuit factors which could affect oscillator reliability are those which induce excessive voltage and current amplitudes at the terminals of the FET. Unavoidably, such conditions would exist in a highly non-linear region of operation rendering linear circuit analysis ineffective in treating this condition. On the other hand, it is quite possible to use the insight into oscillator operation presented in Sections 3.0 and 4.0 to identify potentially troublesome designs.

Such a potential design problem would be an oscillator with a small signal negative output conductance which was very much larger than the load line conductance. As shown by Figure 4.4, the signal level would have to increase to a level which was higher than optimum. Besides paying a penalty in reduced output power and increased harmonic levels, the higher than normal voltage swings at the output terminals might result in reliability problems. Severe clipping, for example, might be accompanied by forward bias conditions existing at the gate. These problems are best avoided by maintaining an adequate but not excessive margin between $|G_{o,ss}|$ and the load conductance. In this sense, adequate means that sufficient oscillator power is generated at equilibrium to satisfy the oscillator design requirements.

5.2 Application to FET Mixers

Another application of GaAs FET's is as the non-linear device in an RF mixer. Reports of several such circuits have been published [3-5], although the reported noise figures (typically 10 dB) have been high. An improved mixer circuit using a GaAs FET was reported by P. Ntake [6] who achieved a mixer noise figure of 4.8 dB at 4 GHz by optimizing the RF and IF circuit impedances as seen by the FET. The lowest noise figure was obtained by short circuiting the RF and IF signals at the drain and gate respectively.

It is not likely that the circuit factors which affect the reliability of FET's in microwave oscillators will have the same influence on the design of FET mixers. In an oscillator, the device operates in saturation with regenerative feedback. In a mixer, there is no external feedback and the waveforms need not drive the FET into saturation. Ntake's results indicated that a well designed FET mixer would have an RF short circuit connected to the drain. This circuit condition is drastically different than would be encountered in an oscillator design. In short, since the circuits and operating conditions for FET mixers and oscillators are not at all similar, the analysis presented in this report cannot be readily extended to apply to GaAs FET mixers.

APPENDIX A

DETAILED OUTPUT CONDUCTANCE EVALUATION

This appendix presents the complete derivation of the expression for the output conductance of an oscillator of the type shown in Figure 3.1. As pointed out in the text, the output admittance, Y_o is given by

$$Y_o = y_{22} + j(B_2+B_3) - \frac{(y_{12}-jB_3)(y_{21}-jB_3)}{y_{11}+j(B_1+B_3)} \tag{A-1}$$

The last term in the above expression must be rationalized by multiplying numerator and denominator by $y_{11} - j(B_1+B_3)$. Carrying out the required multiplications and expressing the resultant numerator in real and imaginary parts, we obtain, for the real part,

$$G_o = g_{22} - \frac{g_{11}[g_{12}g_{21}-(b_{12}-B_3)(b_{21}-B_3)]+(b_{11}+B_1+B_3)[g_{21}(b_{12}-B_3)+g_{12}(b_{21}-B_3)]}{g_{11}^2+(b_{11}+B_1+B_3)^2} \tag{A-2}$$

This expression is further modified by introducint the parameter

$$g'_{22} = g_{22}-G_o \tag{A-3}$$

Subtracting G_o from both sides of Eqn. (A-2) and multiplying through by $g_{11}^2+ (b_{11}+B_1+B_3)^2$ results in an expression which may be expanded and reformed into a quadratic equation which is

$$a(B_1)B_3^2 + b(B_1)B_3 + c(B_1) = 0 \tag{A-4}$$

where

$$a(B_1) = g'_{22} + g_{11} + g_{21} + g_{12} \tag{A-5a}$$

$$b(B_1) = (2g'_{22}+g_{21}+g_{12})B_1 + b_{11}(2g'_{22}+g_{21}+g_{12}) - g_{11}(b_{12}+b_{21}) - g_{12}b_{21} - g_{21}b_{12} \tag{A-5b}$$

$$c(B_1) = g'_{22}B_1^2 + (2g'_{22}b_{11}-g_{21}b_{12}-g_{12}b_{21})B_1 + g'_{22}(g_{11}^2+b_{11}^2) -g_{11}(g_{12}g_{21}-b_{12}b_{21}) - b_{11}(g_{12}b_{21}+g_{21}b_{12}) \tag{A-5c}$$

These expressions simplify to Eqns. (3-8) and (3-9) when the condition $y_{12} = 0$ is applied.

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