Spectrum Surveillance

System Architecture

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François Patenaude
Martial Dufour

Communications Research Centre
Centre de recherches sur les communications

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1. Introduction

The purpose of this technical note is to review the various alternatives available in developing a spectrum surveillance system. It stresses the architecture, computational power, and tools required to develop a system that is powerful, modular, expandable, transportable, and easy to use. Our success in achieving these objectives will depend greatly on the architecture of the analysis system. In order to minimise any limitations on the development and testing of the many techniques and concepts that will have to be implemented in this system over the short and medium term, we believe it will be best to use a radio receiver that is software and microprocessor-based [Mit95]. The advantages of this approach are its flexibility and accuracy and the ability it provides to execute a series of relatively complex functions. Its main disadvantages are that it may not be fast enough for the large volume of data that we will need to process in real time and for the complex processes that we wish to carry out on them. However, a flexible, expandable microprocessor-based technology should allow us to compensate for these drawbacks to a large extent.

With the current state of technology, we should be able to develop a system that can do the following:

1) Sample several MHz of bandwidth with adequate resolution, and
2) Process these samples in parallel.

In this technical note, we describe the implications of these two activities for a general, flexible system. However, if only certain features of the surveillance system are required, then we can specify or quantify values for several system parameters and thereby considerably reduce the range of variation in the system parameters are the complexity of the system as a whole.

The choice of system architecture will be largely determined by the applications that have to be implemented in the short term. Section 2 describes the main applications of this type. Section 3 describes the architecture of a flexible, generic system. Section 4 lists some components that could be used in this system. Lastly, section 5 offers some recommendations for various alternative kinds of spectrum surveillance systems.

2. Type of applications that can be implemented in a digital spectrum analysis system

Before going into the architectural details of the proposed spectrum analysis system, we will now briefly describe the applications that can be implemented in such a system in the short and medium term. We also propose a list of applications that can be implemented in the longer term. These longer-term applications may require more substantial research effort. They are listed here for the purpose of setting objectives consistent with the emerging priorities for future communication systems. Once this list is finalised, longer-term theoretical research could begin.

2.1 Wideband Applications

The term "wideband applications" is used here to denote applications that are applied to a set of individual signals of a few tens or hundreds of kHz, direct-sequence or frequency-hopping spread-spectrum signals, television signals, and other signals[1]. These applications include:

1) Detecting the number of carriers present and the average percentage spectrum utilisation for a set of signals;
2) Estimating the average individual power for a set of carriers;
3) Tracking the carrier of a frequency-hopping transmitter (characterising it in terms of frequencies and timing of hops);
4) Estimating individual carrier frequencies for a set of signals.

More details will have to be provided to define the limits of each of these applications. If budgets allow, more expensive applications, such as one that estimates the angle of incidence, could also be developed.

2.2 Narrowband Applications

The term "narrowband applications" is used here to denote applications that are applied to a signal of a few tens or hundreds of kHz, such as a 30 kHz cellular signal or a 200 kHz commercial FM signal. These applications include:

1) Determining average power, power variation, out-of-band power;
2) Determining average and maximum frequency occupation;
3) Identifying the type of modulation;
4) Estimating bits per seconds for digital modulation;
5) Other[2].

2.3 Applications To Be Developed in the Longer Term

The applications described in the two preceding sections can be developed in the short and medium term. Some more advanced applications or functions could also be developed in the longer term, but they should be taken into consideration now as we architect the system. These applications/functions include:

1) Demodulating narrowband signals;
2) Determining the sex of the person speaking and the language they are speaking;
3) Classifying messages into categories (voice, fax, data) and maintaining utilisation statistics for each of them;
4) Identifying or classifying the transmitting equipment.

These applications will take more time to develop and more computational power to implement. They can be exclusive or concurrent, depending on the computational power, the type of signals, etc.

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[1] To be discussed with the client.
[2] All other functions applied to individual signals. To be discussed with the client.

3. Architecture of the digital spectrum analysis system

The architecture of the digital spectrum analysis system must, if possible, support all of the applications identified as top priorities by the project partners. In practice, this requires flexibility both in the architecture itself and in the components selected to implement it, to facilitate future upgrades. It would also be desirable for a version of this system to be usable as a research tool for the longer-term projects. That said, several other criteria should be considered as well. The main ones are as follows.

Development: Developing the algorithms and transferring them quickly to a dedicated platform are major concerns. It would also be helpful to be able to develop the algorithms in an environment as similar as possible to the proposed implementation platform. For example, it would be preferable for the components (such as the DSP and the A/D converter) to be directly accessible in the development environment like Matlab™. Another advantage of this is that the interface to the system would be easy to design and adapt to the dedicated system. Also, the development time would be minimised if only software had to be developed.

Costs: We could reduce costs by using commercially available hardware and adopting a modular approach. This would also have the advantage of giving us quick access to new technologies. We must pay special attention to the interfaces between components. We can greatly reduce development costs and development time if the interfaces are programmable, especially if we adopt a modular approach.

Operating system: The choice of an operating system and development language is also important. The tools we use to develop the algorithms and interfaces should run under the main operating systems used today (Windows95/NT and Unix).

To better assess the architectural requirements for the digital spectrum analysis system, the details of this system will now be described. The CRC has already designed a generic digital spectrum analysis system. Figure 1 is a high-level block diagram of this system. In this system, signal processing is divided into four main stages. We will now describe each of these in order to highlight the major parameters. (The path that the monitored signal follows through the system is typical for both wideband and narrowband signals.) The filters determine the bandwidth of the processed signal. For wideband signals, the most complex processing takes place in the IF and baseband stages, whereas for narrowband signals, it takes place in the baseband stage. The following discussion is therefore designed to reflect this fact.

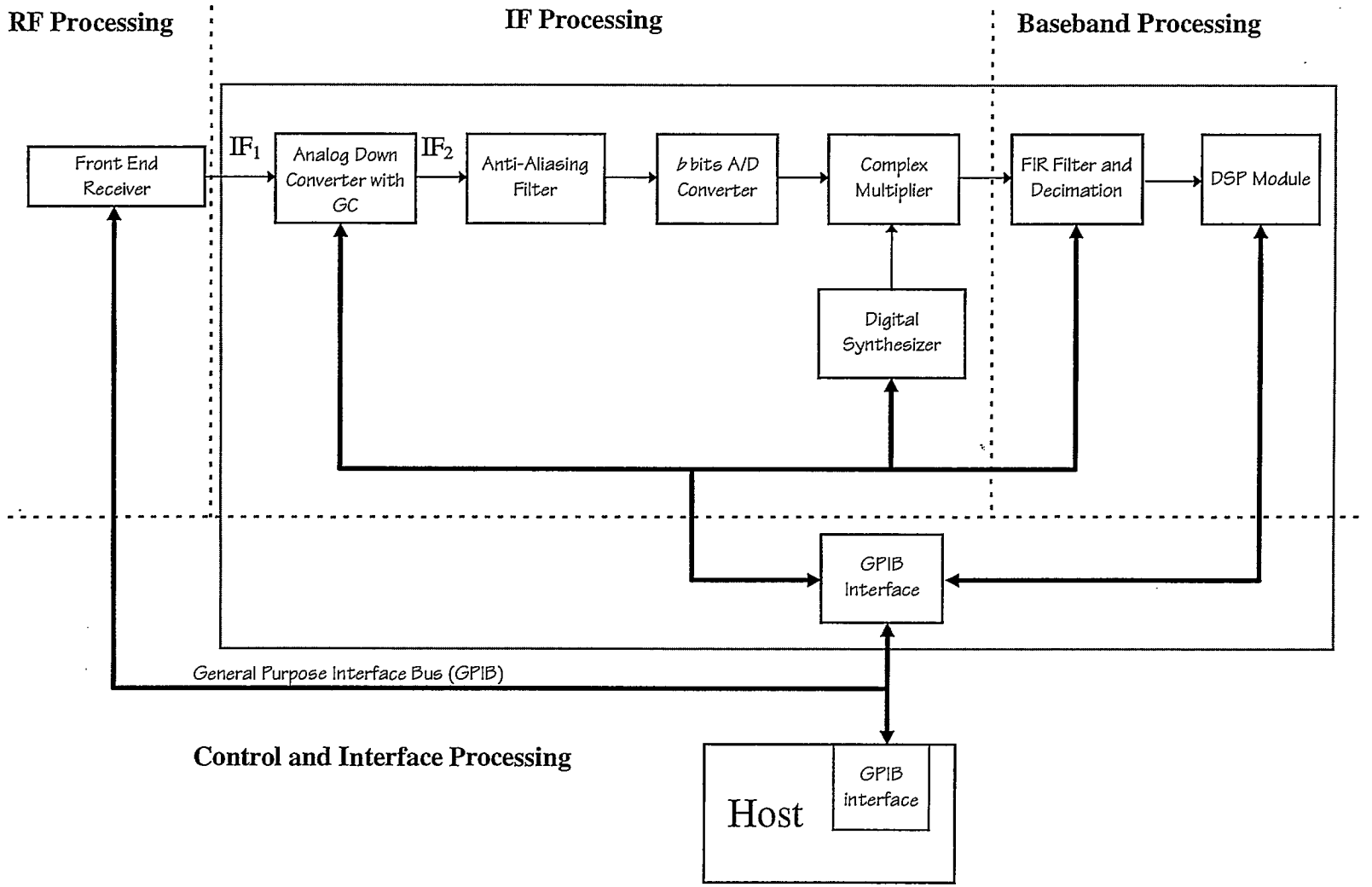

Figure 1. CRC digital spectrum analysis system (DAS).

3.1 RF Processing

The Radio Frequency (RF) processing is mainly composed of the antenna, Low Noise Amplifier (LNA) and RF to Intermediate Frequency (IF) 1 down converter. Those three functions are grouped in the Front End Receiver block. The choice of the carrier frequency[3] is under control of a computer and the characteristics (time to change carrier frequency, delay after change, amplifier bandwidth, distortion, ...) of the equipment are assumed not to be the limiting factors. Although they are very important characteristics that will affect the design of the rest of the system, they will not be discussed for the moment because the stage is highly dependent on the application and the range of the band that must be converted. Application specific requirements will be discussed as needed. This is not a stage where efforts will be focused on for the surveillance applications. Instead, the IF processing stage will be investigated more deeply.

3.2 IF Processing

The analog down converter translates the signal of bandwidth B around IF_1 to a lower IF_2 with Gain Control (GC) to ensure that the following A/D will not saturate or operate in a range of amplitudes near its quantization interval. It is important to note that the energy of the input signal at frequencies lower than $IF_1 - B/2$ have to be attenuated enough so that once translated to IF_2, the signal does not suffer from interference. If the filters prior to the down converter to IF_2 do not meet this requirement, then the down converter will have to have a complex output. The anti-aliasing filter attenuates the amplitude of the frequency higher than half the sampling rate f_s. In practice, the sampling rate has to be ≈ 2.5 time the bandwidth B of the signal or anti-aliasing filter. If the complex analogue down-converter is used, then two anti-aliasing filters[4] for I and Q must be used. The A/D converter samples the filtered IF_2 signal at f_s samples/s where each sample has b bits. The number of bits depends on the dynamic range required[5]. For example, in GSM a dynamic range > 90 dB is require in the system design. For a spectrum surveillance system, this means more than 15 bits at the Nyquist sampling rate and a very low Spurious Free Dynamic Range[6] (SFDR) larger than 90 dB. Typically, 12 bits with a SFDR of 80 dB is required. Note that these numbers are defined for a full scale input signal and that a reduction in nominal input power will degrade these SFDR. It is therefore essential to have some sort of GC that can ensure maximum achievable SFDRs. The total Signal-to-Noise Ratio[7] is also of importance for reliable low power signal estimation. If a complex path is needed, then two phase-locked A/D converters are necessary. The following element, in the block diagram, is a complex multiplier for 0 Hz IF. For the complex path case, the module must also eliminate any gain and phase imbalance in the I-Q as well as any mismatch between the two anti-aliasing filters. Note that depending on the DSP functions to be implemented, it might not be necessary to down convert the signal to 0 Hz IF. The analogue component design is the critical task in the IF processing stage, espe-

[3] The bandwidth is usually fixed.
[4] All filters are assumed to have linear phase unless mentioned.
[5] With the current technology, a trade-off between number of bits and sampling rate has to be counted for as well. Note also that the I-Q path has effectively 1 bit more resolution than the real path IF processing.
[6] Defined as the mean square signal power divided by the mean square power of the largest spurious product.
[7] Defined as the mean square signal power divided by the mean square power of the residual error.

cially the analogue filters and mixers. Special care will have to be taken to make sure the analogue processing does not accentuate the ADC deficiencies.

3.3 Baseband Processing

The 0 Hz complex IF signal is now processed. The Filter and Decimation block is used to reduce the sampling rate from a nominal value to the desired value. The DSP module can be one or more DSP chips to perform the various function computations for a given application. The processing in the stage could also be done in non-real time by providing a buffer or a path to a storage medium. This is more likely for the wideband path, where the decimation is absent or of low order, while the narrowband path will likely be processes in real time. The digital algorithms to be implemented will vary greatly with the applications in mind. Some of the baseband specific function could be implemented in hardware, but with sufficient flexibility to accommodate most signal. This is particularly true for Digital Down Converters (DDC) where the mixing frequency and the number of decimation stages that follow, can be set to accommodate the current and future narrowband signal systems. On the wideband side, the Fast Fourier Transform (FFT) can also be in hardware. The bottleneck will then likely be the interface to the module.

3.4 Control and Interface Processing

This stage of processing deals with the operator commands to the system and the visualisation of the results. In the current implementation, it is used to control the equipment and to send configuration parameters to different blocks. In a more advanced implementation, it could also display real time information by having a large bandwidth between the host and the DSP module. This stage can take advantage of a host processor to perform most of its functions, especially those related to the interface to the operator.

3.5 Advantages of a scanning receiver versus a channelizing receiver

The IF and baseband stages of the system can process either a sequence of carriers scanned by a scanning receiver or a set of carriers channelized by a channelizing receiver. It does not seem possible to design a scanning receiver to handle a large number of channels, mainly because of limitations in the receiver's local oscillators and delays in the filters that would make the time interval between samplings of a given channel too long. On the other hand, the computations needed for a channelizing receiver would require a sampler with a bandwidth and resolution that do not seem achievable in the short term. The remaining alternative is a hybrid receiver that scans a wide frequency range, sampling frequency bands within that range that contain several channels each. This approach leaves us with the flexibility to adopt one or the other of these two kinds of receivers in future system designs, depending on how the technology develops. Meanwhile, the hybrid receiver would allow us to achieve an acceptably small time interval between samplings of any given frequency band.

Scanning consists in changing the central frequency of a receiver from a group of channels periodically. Most of the processing therefore takes place in the RF stage of the system. The delays in the IF stage should be minimised in order to reduce the time between samplings of any given frequency band. The signal received in the baseband stage while the system is changing frequency band should be ignored. This will allow the use of an ADC module that processes data in blocks. After each frequency change, there will be a transitional

period during which the RF and IF stages must stabilise. The sampling should take place after this period has been completed, and the data can then be transferred to the DSP module during the transitional period following the next frequency change. A high transfer rate between these two units is therefore essential for continuous or block-based sampling.

The channelization method should be able to identify channels of uniform bandwidth whose carriers are multiples of either their full or their half-bandwidth. An important characteristic for a channelizing receiver is the ability to channelize a series of channels with the same bandwidth. Many current systems have limitations with regard to the nominal bandwidth, which is typically a multiple of 2 of a minimum bandwidth. The receiver architecture should enable users to select a wide range of nominal bandwidths. It would also be desirable to be able to define several bandwidth arrangements. This functionality can be examined in the longer term. It seems clear that, given the large volume of information to be processed, the only way to channelize the signals is by executing relatively simple functions at high speed. An algorithm based on an FFT with a resolution proportional to the bandwidth of a nominal channel is therefore the preferred approach.

3.6 Requirements for a flexible baseband processing system

- One constraint commonly found in channelizing receivers is the limited choice of bandwidths that can be channelized. Depending on the size of the FFT and the bandwidth of a channel, the sampling rate should be variable, or resampling should be done to obtain an exact bandwidth for channelization. Since the sampling rate and the desired rate for a particular channel may not be related by a simple rational number, an A/D with a sampling rate that can be varied over a range of 0.5 to 1 times a nominal sampling rate would provide flexibility in baseband processing.
- A hybrid scanning/channelizing receiver cannot be used to monitor a particular channel over a long time period, so a narrowband path is needed for baseband processing. The narrowband path should be independent of the wideband path to allow the scanner to cover several bandwidths B while continuing to monitor one channel in particular. It is therefore necessary to have two down-converter paths with A/D converters leading to the baseband processing stage. If several channels must be monitored in a nominal bandwidth B, then the IF narrowband path may, if necessary, be the same as the wideband IF path, followed by a series of down-converters and decimation filters. There are, however, some more effective methods for performing these functions. If no scanning is needed, then samples from the wideband path could be used to monitor a particular channel.
- The wideband IF path requires that the A/D converter be as close as possible to the microprocessors or that a high-speed path be provided between this converter and the other components (such as the microprocessors and a hard disk). If the microprocessors can process the information at the nominal rate, then it is preferable to place the A/D as close to them as possible. Using the microprocessors' data bus would simplify programming and reduce delays in propagating the data. A path that allows the samples to be stored on hard disk should still be provided in this scenario, however. If the microprocessors cannot support the flow of information from the A/D converters, then an explicit high-speed path will be necessary. A bus will therefore have to be specified to transfer the data from an A/D buffer memory to the microprocessors. Though this arrangement will introduce de-

lays in data transfer, it should still be possible to process the data in near-real time if the bus has a high enough transfer rate and if the data blocks being transferred are relatively small compared with the sampling rate. However, using small blocks usually entails a sacrifice in transfer speed. Figure 2 shows the transfer rate from DSP SRAM to DSP SRAM for a microprocessor as a function of block size. The maximum transfer rate is 160 MB/s, because the bus has a 32-bit data path and a clock speed of 40 MHz. The pattern for transfers from DSP SRAM to global DRAM is similar, if this RAM is fast enough.

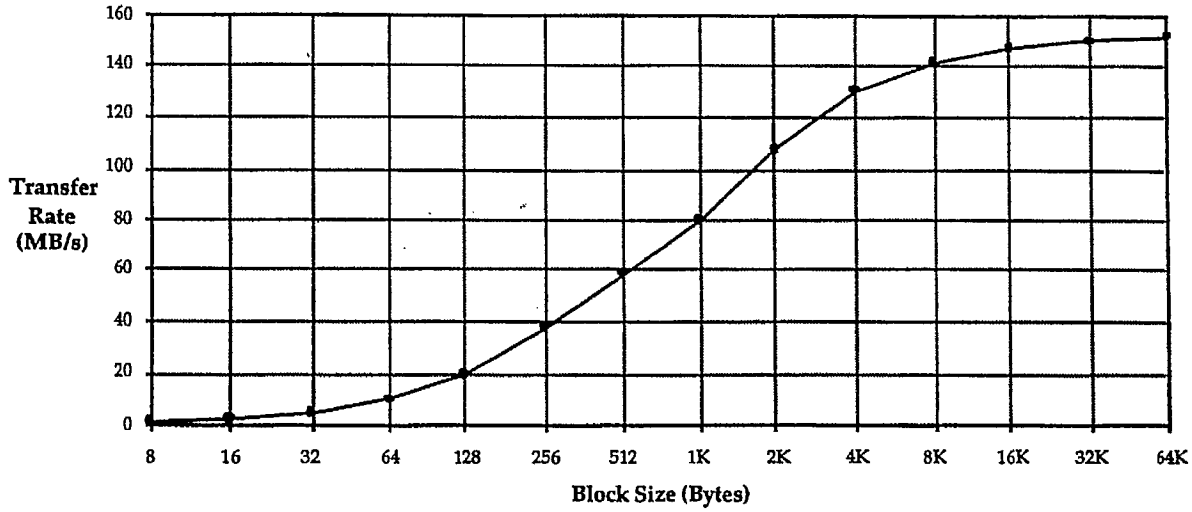

Figure 2. SHARC™ SRAM to SRAM transfers over SHARC™ bus. Transfer rates reflect a single DMA packet of the specified block size transferred by an on-chip DMA controller [Bou96].

- For the wideband baseband processing, it would be very important to have DSPs and the A/D buffer memory that have the equivalent of dual ported memory. This enables the DSP to perform the processing while it is transferring data at the same time from DSP SRAM to DSP SRAM or DSP SRAM to RAM (global). For the ADC, it enables the buffering of the current data samples while the previous buffer of data samples is being transferred.
- The current computational capacity of a single microprocessor is much too low for the volume of information to be processed in this system, so several microprocessors will be needed to perform most of the desired functions. Parallel processing thus becomes indispensable. Parallel processing usually takes the form of Multiple Instruction Multiple Data (MIMD) processing or Single Instruction Multiple Data (SIMD) processing. MIMD processing would be appropriate for executing several different functions on several processors. A typical example of MIMD would be the implementation of a modem. SIMD is designed for processes where a single function is applied to several groups of data. SIMD has the advantage of not requiring synchronisation between processes. A typical application of SIMD would be to calculate a FFT for several channels simultaneously. For high-speed applications, SIMD would probably be the more appropriate form of parallel processing. With sophisticated algorithms, MIMD should also be accessible. The performances

obtained with these kinds of processing depend on the topology of the processors[8]. MIMD is more applicable to a topology with a global bus and shared memory, whereas SIMD lends itself better to a link topology with distributed memory. It will therefore be important to use a flexible microprocessor topology that allows either form of parallel processing.

- Parallel processing is generally possible in an environment where the software and the number of processors are readily expandable. There are three reasons why expandability will be very important.

  1) in future, the sampling rate will probably increase;
  2) the complexity of the algorithms will increase as well; and
  3) the complexity and the cost of the analysis system can be reduced or increased by simply changing the number of processors.

  It is therefore very important that the software be designed in an environment where the tasks can be distributed across several processors and where the number of processors can be increased or decreased with minimal changes to the software. Parallel processing requires a very high communication capacity between processors. We will therefore have to choose a type of processor that simplifies such communications while minimising the impact on performance. Lastly, it would be advantageous to have as high as possible a density of processors on each card, to reduce the size, cost, and energy consumption of the system.

- The most difficult problem for this system from an architectural standpoint will be high-speed processing. To carry out this processing two architectures will be proposed. One could be used for the development system or for a lower-cost system, while the other would be more appropriate for a specialised system. Figure 3 shows how a system with the former type of architecture could be used to channelize the signals. The path for a separate narrowband signal is not shown here, but would be similar. This approach is more advantageous if the signal to be sampled is real. Given the sampling rate per second, the correction for gain and phase imbalance and for any mismatch between the two anti-aliasing filters must be done by a microprocessor, which is not very efficient. If this correction can instead be done by a specific hardware component, such as a Field Programmable Gate Array (FPGA), then the complex becomes more attractive. The hard disk in the host can be used as a storage device for measurement data.

[8] With an appropriate topology and appropriate software, functions that manipulate data blocks larger than the processors' internal memory can be implemented. For example, Alacron Corporation's multiprocessor cards can calculate a complex 1024 point FFT in 72 µs with 8 SHARC™s or a complex 65536-points FFT in 2,764 ms with 16 SHARC™s [Sgr96]. One SHARC™ normally processes a 1024 complex point FFT in 0.45 ms.

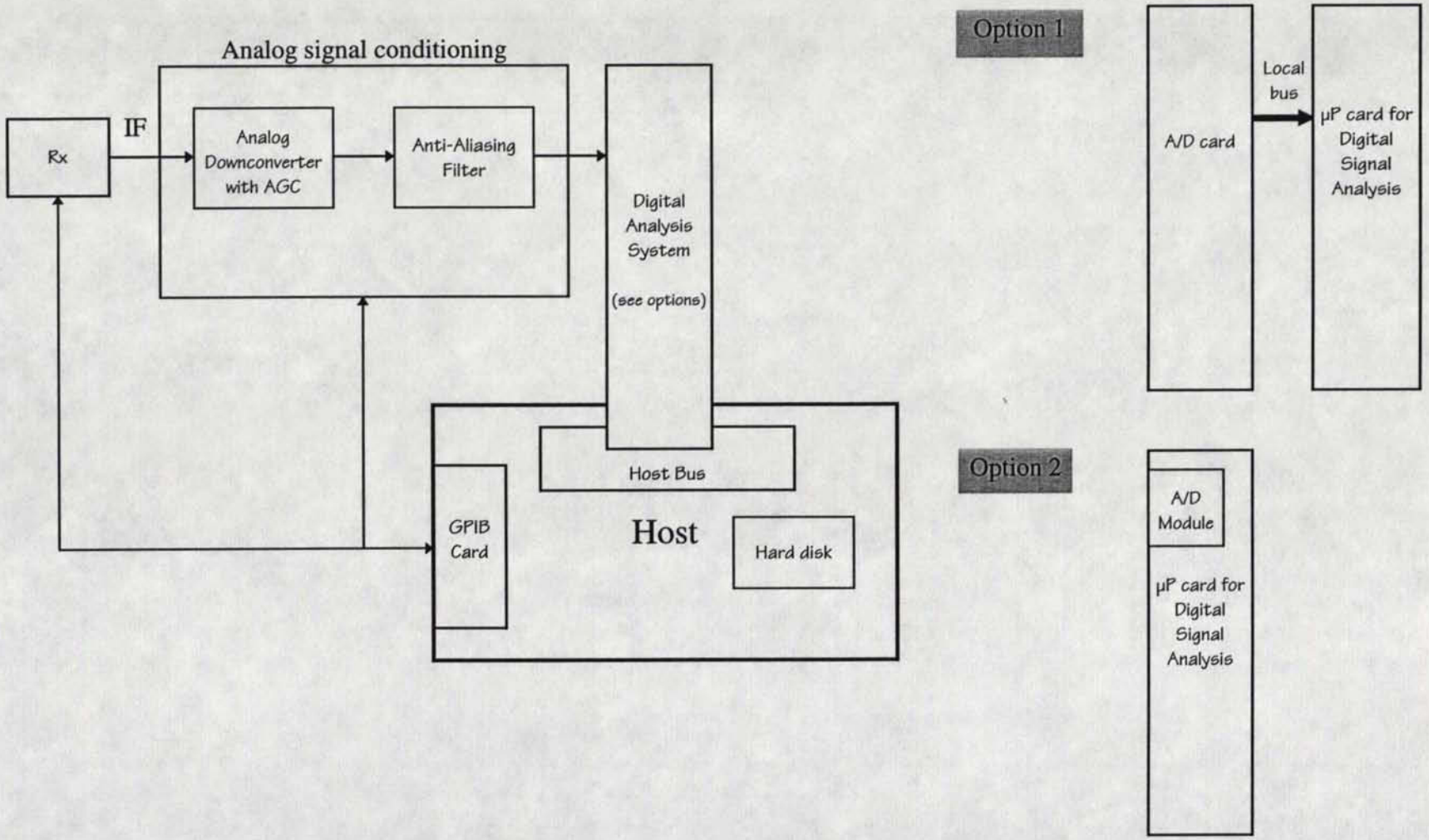

Figure 3. Development or low cost system.

The specialised system will likely use a dedicated bus to accept specialised cards with potentially more computational power than the system of figure 3. The system shown in figure 4 is typical of what such a system can be. The RF signal will enter a down converter card with GC for signal conditioning. For precise power measurements, the value of the GC gain will have to be fixed and available at the power computation point. The IF signal[9] will enter an ADC card where an anti-aliasing filter will limit the high frequency. It would be valuable if the ADC card output could have a variable sampling rate output to be controlled by the computer. This could allow for oversampling by a small rational number to accommodate the baseband processing. The sampling rate variation could be a factor of 2 only. A stable variable sampling clock may be a difficult thing to do with the dynamic range needed for spectrum surveillance, but it would greatly improve the generic nature of the instrument. It is desirable that the output of the ADC card for the narrowband path be a complex baseband signal with various bandwidths. This implies the presence of several decimation stages on the ADC card. The hard disk is optional but can be used to store data for post-processing or for experimental data acquisition. The WB DSP card(s) are intended for wideband signal analysis only. The reason for separating the wideband function from the narrow band ones is mainly the interprocessing requirements of the former. The task performed will likely be simple but very high speed while on the NB DSP(s) will likely be complex but low speed. The need for separate wide and narrow bandwidth paths can also be accommodate with two processor cards. Also it is possible that the NB DSP(s) not be on the VXI/VME frame but on the host computer itself. With the present control bus technology, it is possible to have a few (2-4) MB of transfer throughput between the VXI/VME controller and the computer. The advantage of having the NB processing on the computer is the access to more tools for development. Note as well that in figure 4, the host computer could be an embedded controller in the VME/VXI mainframe. The number of down converter cards and ADC cards can be more than one if more RF signals need to be analysed.

Finally, it is important to note that both systems have a requirement for a local bus to provide a fast path between component cards. The DSP cards also have a fast interprocessor bus for interprocessor communications. The local bus usually can not transfer data directly to a processor through the interprocessor bus. It must usually dump the data into a shared memory RAM buffer. This introduces a delay that may be unacceptable for some applications. Only option 2 of figure 3 would allow for such a transfer.

[9] The IF carrier will have to be in the sampling bandwidth of the ADC card or bandpass sampling will have to be used.

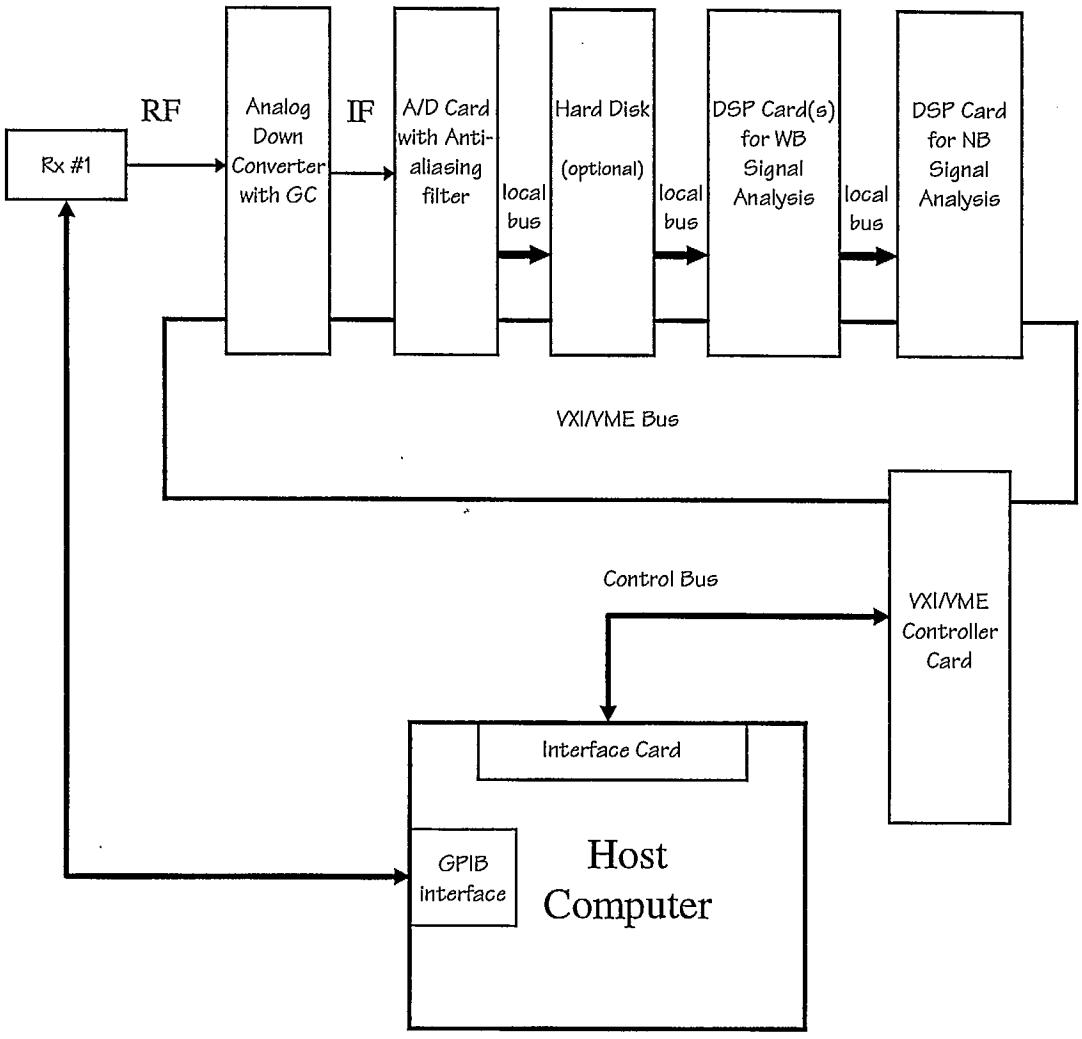

Figure 4. Specialised system.

3.7 Selecting a System Bus

One point that the two systems in figures 3 and 4 have in common is that it is nearly essential for them to have a fast local data bus to transmit data between the system. Conventional data buses are not fast enough to provide the transfer rates required. The only option that does not explicitly require a bus is option 2 in Figure 3. This section does not apply to that option. For all the other options, this bus is needed to maximise the transfer rate between components in order to perform processing in real or near-real time. The requirements for this bus will probably preclude the user of any widely available, generic bus. The following sections describe the main characteristics of the three best known types of buses for instrumentation and control: PCI, VME, and VXI.

3.7.1 PCI (Peripheral Component Interconnect) bus

This bus developed by PC industry leaders Intel, IBM, Compaq, DEC and NCR became open in 1992 with the foundation of the PCI SIG (Special Interest Group). The standard

revision 2.0 was released in April 1993 and a new revision 2.1 has recently been released. The PCI bus boasts a 32-bit data path (64 bits optional), 33.3 MHz maximum clock speed for a maximum data transfer rate of 133.3 MB/sec (266.6 MB/sec optional). A 66.6 MHz specification exists for new PCI designs, with a 32 or 64 bit data path to double the data transfer performance to 266.6 or 533.3 MB/sec [Rev. 2.1]. The PCI local bus takes peripherals off the I/O bus and connects them, together with the CPU and the memory subsystem, to a wider, faster pathway for data. The result is faster data transfer between the CPU and the peripherals.

The above transfer rates are theoretical and cannot be obtained in practice. The PCI bus treats all transfers as a burst operation. The memory or CPU is not always ready to send or receive data when the bus is, and the overhead needed to initiate a transfer cycle (address setup) is not always negligible. As a result, a real speed figure for the PCI bus is proportional to the burst length and realisable maximum throughputs are in the range of 80 to 100 MB/s (Rev. 2.0 32-bit path), which is comparable to the actual throughput of most other high performance buses. Another PCI specification provides for clearly defined bus mastering through a function called concurrency. With bus mastering, a PCI card with processing capability can take control of the bus and provide main memory I/O without CPU processing time. Concurrency will allow bus mastering to relieve the CPU of cycle time (which frees it for other services), and additionally allows an application to work out of cache memory.

3.7.1.1 CompactPCI

An industrial version of the PCI bus [Rev 2.0] known as the CompactPCI bus is starting to emerge. CompactPCI is high performance industrial bus based on the standard PCI electrical specification, on a rugged 3U or 6U Eurocard[10] packaging with twice as many PCI slots (8 versus 4) without using bridges. The CompactPCI effort was initiated in late 1994 by Ziatech Corporation under the auspices of the PCI Industrial Computers Manufacturer's group (PICMG). The CompactPCI Specification is the result of a concerted effort of the CompactPCI subcommittee composed of the following companies: DEC, GESPAC, I-Bus, Pro-Log, Teknor, VMIC, and Ziatech. CompactPCI is intended as an industrial bus for applications in real-time machine control, industrial automation, real-time data acquisition, instrumentation, military systems or any other application requiring high speed computing, modular and robust packaging design. The CompactPCI is not an open standard as far as I know.

3.7.2 VME (VERSAModule Eurocard) bus

The VMEbus is an industrial open standard system originated in 1981 from the Motorola M68000 bus signals and timing. VMEbus boards have data bus sizes of 16, 32 or 64 bits with a 10 MHz clock and are designed to be plugged into a backplane that has up to 21 slots for other boards. These other boards can be CPU boards or peripheral boards providing various functions. The VMEbus specification specifies the physical dimensions of the boards, backplane and the chassis as well as the electrical specifications of the bus and various communication protocols. The latest revision is C.1.

[10] The Eurocard standard describes a family of printed circuit boards and their associated DIN connector locations. The CompactPCI does not use the standard Eurocard connectors.

A VMEbus board can be either single or double height. A single height board is 100 mm × 160 mm with one 96 pin DIN 41612 connector called P1 on the rear that plugs into the backplane. A double height board is 233 mm × 160 mm and may have a second 96 pin DIN connector named P2. A single height board is also known as a 3U and a double height a 6U. There are 9U boards in existence but they are not part of the VMEbus specification. The front edge or face of a typical board is 20 mm wide and may incorporate RS-232 connectors, indicator lights and switches. The backplane can have up to 21 slots providing the J1 connectors for the boards to plug into. The J2 connectors (if required) can be supplied with a second backplane board or in one piece with both J1 and J2 connectors. A J1 (on the backplane) matches to a P1 (on the board) and a J2 to a P2. The spacing between slots is 20.32 mm (0.8 inches). Power is supplied to the VMEbus board through P1 and P2 (if used). The DIN plugs used are arranged in three rows (A, B, C) of 32 pins. These plugs are approximately 0.85 mm wide and 84 mm long. P1 supports 16 and 24 bit addressing and 8 and 16 bit data paths. P2 uses the centre 32 pins to support full 32 bit data and addressing paths. The two outer rows of P2 are user defined[11] and are used for I/O ports, disk drives and other external peripherals.

Table 1. VME bus pin assignments.

	J1/P1 Pin Assignments			J2/P2 Pin Assignments		
Pin #	Row A	Row B	Row C	Row A	Row B	Row C
1	D00	BBSY*	D08	User	+5v	User
2	D01	BCLR*	D09	defined	GROUND	defined
3	D02	ACFAIL*	D10	"	RESERVED	"
4	D03	BG0IN*	D11	"	A24	"
5	D04	BG0OUT*	D12	"	A25	"
6	D05	BG1IN*	D13	"	A26	"
7	D06	BG1OUT*	D14	"	A27	"
8	D07	BG2IN*	D15	"	A28	"
9	GROUND	BG2OUT*	GROUND	"	A29	"
10	SYSCLK	BG3IN*	SYSFAIL*	"	A30	"
11	GROUND	BG3OUT*	BERR*	"	A31	"
12	DS1*	BR0*	SYSRESET*	"	GROUND	"
13	DS0*	BR1*	LWORD*	"	+5V	"
14	WRITE*	BR2*	AM5	"	D16	"
15	GROUND	BR3*	A23	"	D17	"
16	DTACK*	AM0	A22	"	D18	"
17	GROUND	AM1	A21	"	D19	"
18	AS*	AM2	A20	"	D20	"
19	GROUND	AM3	A19	"	D21	"
20	IACK*	GROUND	A18	"	D22	"
21	IACKIN*	SERCLK*	A17	"	D23	"
22	IACKOUT*	SERDAT*	A16	"	GROUND	"
23	AM4	GROUND	A15	"	D24	"
24	A07	IRQ7*	A14	"	D25	"
25	A06	IRQ6*	A13	"	D26	"
26	A05	IRQ5*	A12	"	D27	"
27	A04	IRQ4*	A11	"	D28	"
28	A03	IRQ3*	A10	"	D29	"
29	A02	IRQ2*	A09	"	D30	"
30	A01	IRQ1*	A08	"	D31	"
31	-12V	+5V STDBY	+12V	"	GROUND	"
32	+5V	+5V	+5V	"	+5V	"

[11] For example, the A and C columns have been used by Mercury Computer Systems Inc. to build the RACE™ bus that can handle data rate up to 160 MB/s.

3.7.2.1 PMC (PCI Mezzanine Card)

A PMC is a proposed IEEE specification for a low profile mezzanine expansion bus for VMEbus, Multibus II and Futurebus+ systems. It has a 32 or 64 bit bus and has the same electrical specifications as the PCI bus. This bus is typically used for I/O, memory, processing or as a bus interface module. Many other types of expansion or mezzanine modules on VMEbus boards are available to provide for another level of integration modularity. The main ones are IP (IndustryPacks) Modules, CXC/ModPack, M-Modules. Some are VITA standards while other are waiting for approval.

3.7.2.2 VME64 bus

The theoretical limit for data transfer is 40 MB/s on the VMEbus. The regular VMEbus standard accommodates 32 bit address and data buses. One type of data transfer, called a Block Transfer, allow up to 256 bytes to be transferred with only the start address placed on the address bus once. For the rest of the transfer, the address bus is idle. The lower 32 bits are placed on the regular D0 to D31 and the upper 32 bits placed on the idle address bus A01 to A31. The VME64 standard utilises this unused bandwidth to enable 64 bit block transfers enabling theoretical throughput of 80 MB/s. The VME64 standard adds a few other advanced features. VME64 is a VITA[12] Standard. This standard, which has recently gained ANSI approval, is backwards compatible with existing VMEbus boards.

3.7.3 VXI (VMEbus eXtensions for Instrumentation) bus

The VXIbus is an instrumentation bus based on the VMEbus, the Eurocard and standards such as IEEE 488.2 and the HP GPIB (General Purpose Instrumentation Bus). It is an open architecture and is useful for automated test systems and data collection. The issue of electromagnetic radiation and cooling is part of the VXIbus specification. The VXIbus was announced in 1987 and the latest revision is 1.4. The VXIbus expands on the VMEbus so the two bus specifications are very similar. There are two more board sizes in addition to the VMEbus single and double sizes.

Table 2. VXI card dimensions.

Size	Height	Dimensions (mm)	Connectors	Slot Spacing
A	Single	100 x 160	P1	0.8 inch
B	Double	233 x 160	P1 & opt P2	0.8 inch
C	Double	233 x 340	P1 & opt P2	1.2 inch
D	Triple	366 x 340	P1, opt P2,P3	1.2 inch

opt = optional
P1, P2 & P3 are the same 96 pin DIN connector as in the VMEbus.

The increased width of the C and D sizes is to accommodate thick analogue modules and EMI shielding. The VXIbus uses the same pin assignments on P1 and the centre P2 pins as the VMEbus. The two rows (A & C) on P2 that were user defined on the VMEbus are assigned on the VXIbus. Features added include ECL (emitter coupled logic) and TTL trigger signals, a 10 MHz ECL clock, more supply sources (+-24, –2 and –5.2 volts), an analogue summing bus, local bus lines and a module identification line.

[12] VMEbus International Trade Association.

Reasons why the VMEbus and the VXIbus specifications are not totally compatible include:

1) conflicts may arise depending on the use of the A & C rows on P2,
2) VMEbus Double height boards are not as deep as VXIbus size C,
3) the VMEbus has no configuration registers while the VXIbus does.

A VXIbus system can have up to 13 modules consisting of a central timing module in Slot 0 and a maximum of 12 additional instrumentation modules. The assigned P2 connector is used to implement a VXIbus local bus provides a private module-to-adjacent module communication path. Except for the end slots, each slot has 2 separate local buses: one to the module on its left, and one to the module on its right. So it is a unidirectional left to right path. There are 5 classes of permitted local bus usage: TTL, ECL, analogue LOW, MED, and HIGH.

3.7.3.1 VXI*plug&play*

The VXI*plug&play* is a new standard developed by a Systems Alliance organisation[13] formed in September 1993, that is committed to increasing the ease of use and cost-effectiveness of VXI systems. It is thus based on the VXI hardware system definition. The new standard addresses hardware issues, but mainly software standardisation. The alliance has a commitment to maximise compatibility with the installed base.

Some of the core technologies currently embodied in the VXI*plug&play* system architecture philosophy are listed below. These core technologies will be reflected in VXI*plug&play* framework definitions:

- VXIbus mainframes and fixturing,
- VXIbus instruments and VME modules,
- High-speed VXI transfers (shared memory, Fast Data Channel),
- GPIB (IEEE 488.1 and 488.2) instruments,
- High-speed GPIB transfers (HS488),
- Industry-standard computers,
- Embedded VXI computers,
- MXIbus interfaces and extenders,
- DOS, Windows, Windows NT, HP-UX, and SunOS/Solaris operating systems,
- NI-VXI and NI-488.2 I/O interface software,
- LabVIEW and LabWindows instrument drivers in source code,
- Executable Instrument Front Panels,
- ANSI C, BASIC, ATLAS, and ADA programming languages,
- DLL, DDE, OLE, and other computer standards for communicating with other open software products and environments.

At the moment, there are much fewer VXI*plug&play* components than VXI or VME components. The main VXI hardware component manufacturer at the moment is HP, while the main

[13] Founding members are GenRad, National Instruments, Racal Instruments, Tektronix, and Wavetek.

software provider seems to be National Instruments. The development environments are referred as frameworks and are summarized in the following table:

Table 3. VXI*plug&play* System Framework Organisation.

ANSI-C	MS C++ Borland C++ LabWindows/CVI	MS C++ Borland C++ LabWindows/CVI	MS C++ Borland C++ LabWindows/CVI	LabWindows/CVI Sunsoft cc Sunsoft CC	POSIX c89 HP CC
Run-time link	MS C++ Borland C++ MS VB LabWindows/CVI LabVIEW HP VEE	MS C++ Borland C++ MS VB LabWindows/CVI LabVIEW HP VEE	MS C++ Borland C++ MS VB LabWindows/CVI LabVIEW HP VEE	LabVIEW HP VEE Sunsoft cc Sunsoft CC	LabVIEW HP VEE POSIX c89 HP CC
G	LabVIEW	LabVIEW	LabVIEW	LabVIEW	LabVIEW
	WIN	WIN95	WINNT	SUN	HP-UX

The G in the last row refers to support for the native G language of LabVIEW. For example the WIN framework which directly supports the G language is called the GWIN framework. Note that only LabVIEW and HP VEE are supported across the platforms. A VXI*plug&play* card has to meet at less one of the above framework.

3.7.4 PCI vs. VME vs. VXI

The three buses presented in the three previous sections have the capability to support the functionality required for a digital spectrum surveillance system. However, each has their relative advantages and disadvantages. The PCI bus has the largest bandwidth of the three buses. It is however limited in the number of cards that can be installed (3 to 4). This limitation is attenuated by the fact that most PCI bus systems come with a secondary bus (ISA[14] bus for PCs) were another 3 to 4 slots are available to put other cards. In a system where several processor cards have to be installed, the processor cards can usually be connected to each other with the processor links avoiding the need for a local bus. This is true for the three buses. The VMEbus has the largest expansion capability without having to add a second mainframe. The addition of a second mainframe is usually costly in data bandwidth. The VXI bus is probably the best one for instrumentation purposes because of its low electromagnetic specifications. It also has a defined expansion architecture for a multi-mainframe system. That can be a valuable asset for large systems. The VXIbus does not exclude the use of VME card, while the reverse is not possible. The move from one bus to another is simpler between the PCI and VXI bus if the VXI*plug&play* frameworks are available on the selected VXI platforms. The VME modules are usually more difficult to program and there is no compatibility guaranteed compare to VXI*plug&play*.

The cost of a system based on the buses can be very different. The PCI systems tend to be lower cost, faster updates or appearance of latest technology. It however has fewer choices in terms of analogue card components and extension capability. A VMEbus system would be a sure way to go for a specialised system because of the number or components available. Its drawback is its limited bandwidth even with VME64 or PMC capability, and a more difficult interface to it. The VXI is the most expensive but has the highest potential per-

[14] Industry Standard Architecture.

formance of the three. It has very good potential for future replacement of the VMEbus. The local bus can however bring compatibility problems.

As a last comment of this section, it is also important to note that the buses transfer rate in MB/s can be misleading since they usually assume 4 bytes wide (32-bit bus). If the samples can not be concatenated in a 32 bit word, then the throughput of the bus in mega samples per second can be much lower. As a general information note, figure 5 shows a mapping of the buses in the bus width — throughput plan.

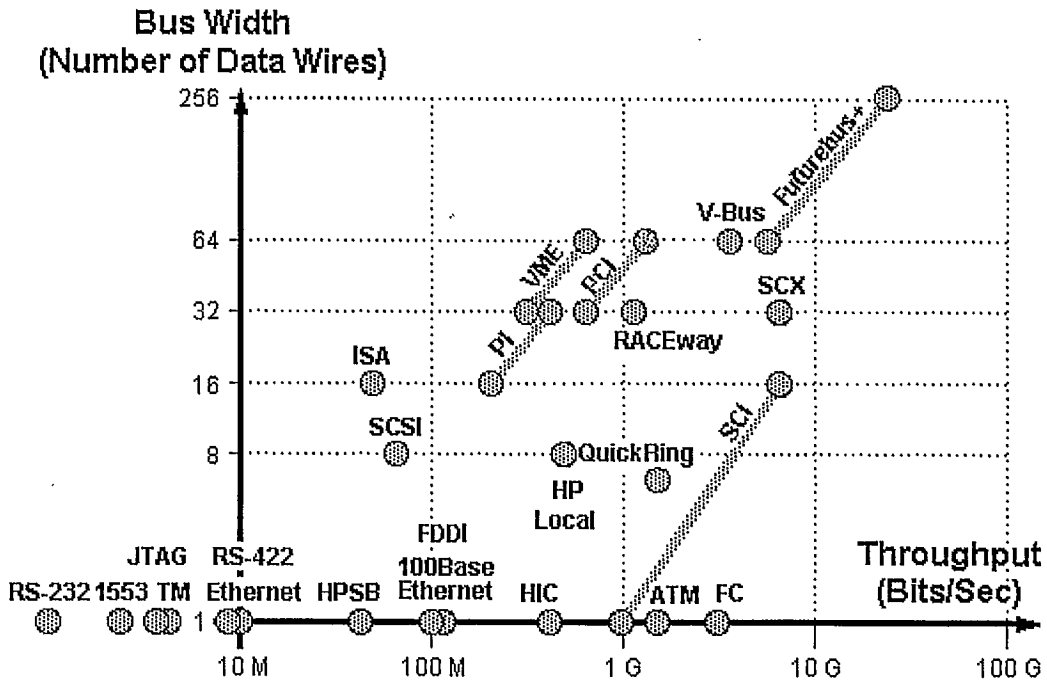

Figure 5. Bus width — throughput mapping.

3.7.5 The local bus issue

The local bus or fast data path is needed between the ADC and the processor board. It finds its place on row A and C for VME and VXI based systems. Several manufacturers have used those undefined connections to design their local buses. For VME systems, Alacron Inc., Mercury Computer Systems Inc. and others have used the bus for that manner. On VXI systems, Hewlett-Packard (HP) has implemented an ECL local bus. Those buses are very high performance but they tend to tight the rest of the system to be of the same nature because they are proprietary designs. Limited access to a variety of components due to low volume can be a problem. Like every other bus, they tend to be more bandwidth efficient when large blocks of data are transferred. The usefulness of a high bandwidth local bus can be questionable if small blocks are to be transferred with low delay for real time processing. The PCI bus revision 2.1 has an arbitration mechanism that is supposed to make it efficient for small data block as well. It is therefore possible that the local bus of figure 3 option 1 be the PCI bus itself. This may not ensure delay free transfer but certainly to quasi-real time processing assuming enough DSPs. This is conditioned on the assumption that all devices on the bus are revision 2.1 compliant.

3.8 Selecting a Microprocessor

To accommodate the dynamic range of input signals, to achieve the desired degree of accuracy, to support future applications, and to simplify the development process (by developing the algorithm in an environment very similar to the production environment) a floating-point microprocessor must be used for the main processing in this system. There are four main high-performance floating-point microprocessors on the market: the Texas Instruments TMS 320C40\C44, the Analog Devices ADSP2106x SHARC™ (Super Harvard Architecture Computer), the Motorola DSP96002, and the AT&T DSP32C\DSP32xx. The DSP32C has a maximum capacity of 20 MIPS or 40 MFLOPS[15] and does not have any interprocessor links. The DSP96002 can support up to 20 MIPS or 60 MFLOPS with interprocessor links limited by the external circuitry. It has only 2 banks of 512 32-bit words of RAM. For these reasons, neither of these microprocessors is appropriate for spectrum analysis. That leaves the C40\C44 and the ADSP2106x. The main characteristics of these two microprocessors are described in the next two sections.

3.8.1 TMS 320C40\C44

- 32-bit Floating Point processor
- Up to 60 MFLOPS or 30 MIPS[16]
- 6\4 communications ports
- 6 channel Direct Memory Access (DMA)
- single-cycle conversion to and from IEEE-754 floating point format
- single-cycle $1/x$ and $1/\sqrt{x}$
- 20 MB/s parallel data port[17]
- 512 bytes instruction cache and 8kB of single cycle dual-access program or data RAM
- 16GB\128MB program/data/peripheral address space.

The important aspect of the C40\C44 [C4x]is its large base of tools for developing all kinds of applications around it. It might be more suited to implement the narrowband functions because its communication port bandwidth is relatively low compare to the sampling rate needed for the wideband path. TI has developed a module standard called TIM-40 to increase the flexibility of system architecture. TIM-40 modules can hold a DSP, memory, or I/O ports with 2 or 3 connectors per module to the main board. The single width modules are 4.2×2.5 inches while the double width are 4.2×5.1 inches.

3.8.2 ADSP21060\2 SHARC™

- 32-bit Floating Point processor
- Up to 120 MFLOPS peak, 80 MFLOPS sustained or 40 MIPS
- 10 DMA channels for transfers between ADSP2106x internal memory, external memory, external peripheral, host processor, serial ports or link ports

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[15] MIPS: Millions of Instructions Per Second.
MFLOPS: Millions of FLoating-point Operations Per Second.
[16] To be released in Q1 1997. Currently 50 MFLOPS or 25 MIPS.
[17] 60 MHz part.

- 6 communications ports
- 40 MB/s bi-directional parallel link and port
- 4 Mbits\2 Mbits (128K\64K of 32 bit words) on chip SRAM dual-ported for independent access by core processor, I/O processor or DMA
- two 40 Mbits/s synchronous serial ports
- 4 GB program/data/peripheral address space.

The ADSP2106x [Shr] comes also with an open standard module specification called SHARCPAC™ which is a compact package measuring 4.5" X 3.1" (approximately 79 x 114 mm) used to put processors, memory or I/O depending on the application. The cards are inserted on a motherboard that can typically receive two or three modules. The ADSP2106x density on such is SHARCPAC™ is at maximum 8. The ADSP2106x is a newer generation of processor [Bai95] compared to the C4x. The main advantages of the ADSP2106x over the C4x is the amount of internal SRAM, link and port throughput and the on chip multiprocessor features. Development tools are available from Analog Devices.

3.9 Network Access and Control

An important feature of the surveillance system is the remote access and control. It is highly desirable that a network access to the system be provided for gathering results and issuing commands. The network can be the Internet or an Intranet. The major difficulty in the network access and control is to provide access to the hardware (DSP, ADC, ...) from the network itself without disturbing the normal activities, and keep fairly generic function calls independent of the actual hardware. Figure 6 illustrates the network access structure that is currently being developed for a spectrum surveillance system. It is generic and will also be used for a second generation version of the current monitoring system. With this structure, hardware can easily be changed or added without modifying the rest of the system. The hardware interface layer is where the software changes take place for the new hardware.

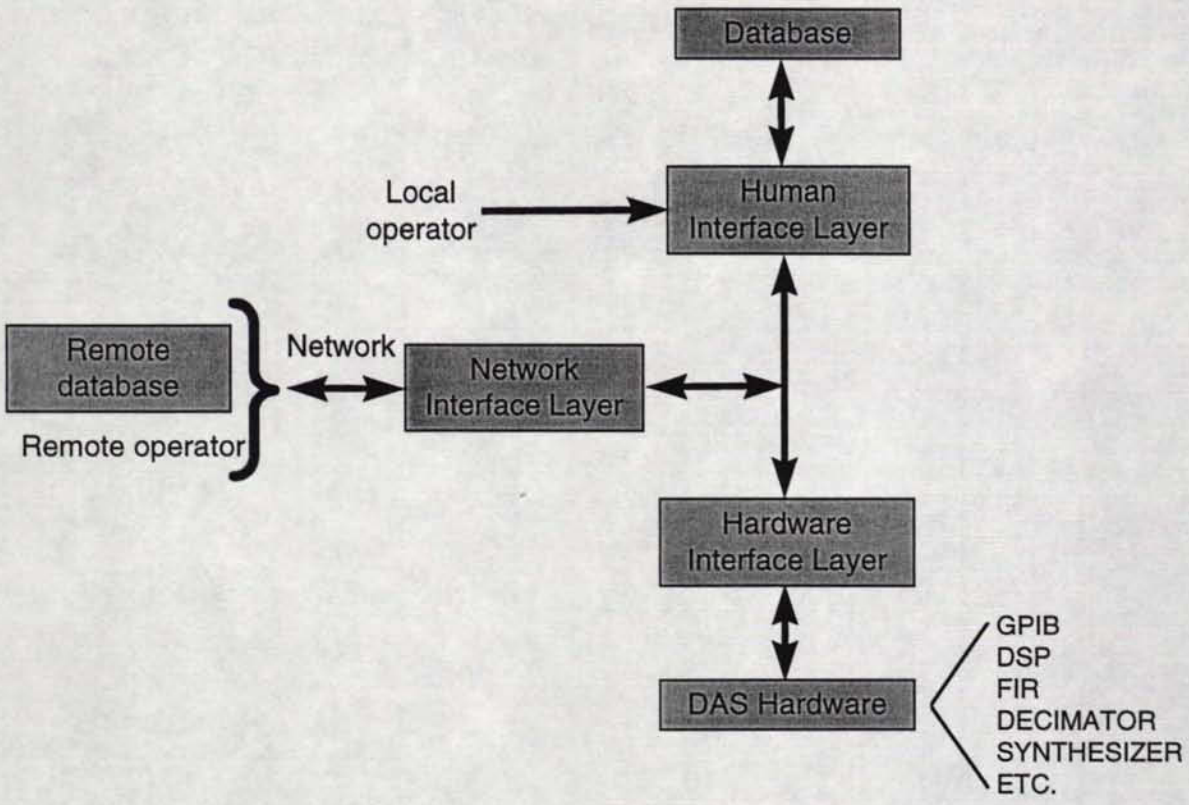

Figure 6. Network access.

The equipment necessary for network access is simply a network card, which should not cause any problem for either the VME/VXI or PCI based systems. Finally, it is also possible to make the system hardware available for development purposes, so that some of the software development can be done remotely.

4. Hardware and Software for Spectrum Surveillance

The DSP processor and the ADC are two critical components from several components necessary to have a full system working. A complete system[18] available from a manufacturer may also simplify the system development and maintenance. The software development tools are also of very high importance. Other specialised components like FFT boards, Digital Down Converter (DDC) may be of interest. This section lists some of the available components that may be of interest for spectrum surveillance. The components are microprocessor boards, ADC boards, FFT boards, complete systems, software development tools.

[18] It is unlikely that a complete solution will be available from one manufacturer especially if the latest technology is used.

Manufacturer	Price[19]	Component	Comments
3L Corporation [3LC]	≈ 2 K CAN	Parallel C compiler for C40	Superset of TI C compiler, latest version 2.0.2.
Alacron Inc [Ala]	—	FT-SHARC board series	Available in PCI, ISA, VME. FastTrack proprietary modules.
Alex Computer Systems [Alex]	6 K[20] to 12.5 K[21]	PCI SHARC board	Price with development tools. 2 SHARCPAC site, distributed memory.
Alex Computer Systems	5 K[22] to 8.5 K[23]	ISA SHARC board	Price with development tools. 3 SHARCPAC site, distributed memory.
Alex Computer Systems	5 K[24] to 11.5 K[25]	6U VME SHARC board	2 SHARCPAC site, VME 64, distributed memory.
Alex Computer Systems	2.5 K[26] to 14 K[27]	1, 2, 4 and 8 DSP SHARCPAC	Can be put on any board.
Alex Computer Systems	2.6 K[28] to 4 K[29]	FPGA-DSP SHARCPAC	Can be use for digital I/O and processing.
Altera Corporation [AlC]	—	FFT Engine	FFT function for Altera FPGA chips. Board may have to be built.
Analog Devices Inc. [ADI]	≈ 1 K	Compiler, Library and Debugger for SHARC	Based on GCC 2.x Available for PC and SUN, includes Numerical C.
Bittware Research Systems [BitW]	—	4 SHARC PCI board	With 0 or 32 MB of shared DRAM.
Bittware Research Systems	—	Single SHARC PCI or ISA board	Up to 3 MB of external SRAM.
Bittware Research Systems	—	Dual SHARC ISA board	Up to 3MB of external SRAM. 1 SHARCPAC.
Bittware Research Systems	—	1, 2, and 4 DSP SHARCPAC	2 DSP comes with up to 3MB of external SRAM.
Bittware Research Systems	—	SRAM and DRAM SHARCPAC memory	128K×32 SRAM to 4M×32 DRAM.

[19] In US dollars unless otherwise specified.
[20] One ADSP21062 with 768 KB of external SRAM.
[21] Two ADSP21060 with 3 MB of external SRAM.
[22] One ADSP21062 with 768 KB of external SRAM. Available with DRAM instead of SRAM as well.
[23] One ADSP21060 with 3 MB of external SRAM. Available with DRAM instead of SRAM as well.
[24] One ADSP21062 with 768 KB of external SRAM or 4MB or external DRAM.
[25] Two ADSP21060 with 3 MB of external SRAM and 16 MB of external DRAM.
[26] One ADSP21062 with 768 KB of external SRAM or 4 MB or external DRAM.
[27] Eight ADSP21060.
[28] One ADSP21062 with Xilink 4005 or Altera 8452A.
[29] One ADSP21060 with Xilink 4020E or Altera 81500A.

Catalina Research Incorporated Inc.[CRI]	—	FFT Engine: 6U VME board CRV1M40/50	Based on Sharp LH9124/LH9320.
Catalina Research Incorporated Inc.	—	FFT Engine: 9U VME board CRCV1M40/50	Based on Sharp LH9124/LH9320. 1024 complex point FFT in 25.6 μs or 65536 complex point (24 bits) FFT in 1.5 ms.
Catalina Research Incorporated Inc.	—	FFT Engine: 6U VME board CRP1M40	Based on Sharp LH9124/LH9320. Similar to CRV1M40/50.
Catalina Research Incorporated Inc.	—	FFT Engine: 6U VME board CRV1M60-2: Gemini	Based on Sharp LH9124. 1024 complex point (24 bits) FFT in 27.3 μs.
Catalina Research Incorporated	—	DSP 9U VME board	Based on more than 64 SHARC 2106X. 5 GFLOPS. PMC interface.
Cubic Communications Inc.	—	VHF/UHF Receiver VXI-3550/3555	Range from 20 - 1200/2400 MHz.
Gage Applied Sciences[30] [GAS]	10.5 K to 11 K CAN	ADC PCI board: 12 bits 80 MHz Compuscope 8012/PCI	1 channel at 80 MHz or 2 channel at 40 MHz. Can not operate in continuous mode. Up to 1 MB of memory LabView and Visual Basic drivers[31] for Win 3.1/95/NT.
Gage Applied Sciences	9.5 K[32] to 18.5 K CAN	ADC PCI board: 12 bits 60 MHz Compuscope 6012/PCI	1 channel at 60 MHz or 2 channel at 30 MHz. Can not operate in continuous mode. Up to 4 MB of memory. Up to 90 MB/s from board to PC DRAM, LabView Visual Basic drivers for Win 3.1/95/NT.
Gage Applied Sciences	8 K to 16.5 K CAN	ADC PCI board: 12 bits 20 MHz Compuscope 1012/PCI	1 channel at 20 MHz or 2 channel at 10 MHz. Can not operate in continuous mode. Up to 4 MB of memory, LabView and Visual Basic drivers for Win 3.1/95/NT.
Go DSP Corporation [GDSP]	—	TI DSP Debugger Code Composer	Available for Windows 3.1/95/NT, latest version 2.0.
Guide Technology Incorporated [GTI]	1 K CAN	Clock card ISA GT310	Stability has to be tested with the ADC.
HP [HPTM]	9.6 K CAN	Mainframe VXI C size HP E1401B	13 slots available.

[30] The same ADCs are also available in ISA cards with up 16 MB of RAM and a DSP LINK option (1.5K) as a local bus to a DSP card.
[31] The board can be controlled from within Matlab for direct data acquisition.
[32] From 512K to 4M of memory.

HP	5.8 K CAN	Mainframe VXI C size HP E1421A	6 slots available.
HP	—	VXI Embedded controller HP E1498A	Based on HP V743/100 processor, framework HP-UX.
HP	—	VXI Embedded controller HP RADEPC7B	Based on 100 MHz Intel 486[33] processor running Windows 3.1 or later, framework WIN/WIN95/WINNT.
HP	—	VXI External controller HP E1483A VXLink	Running under Windows 3.1/95/NT[34].
HP	2.5 K CAN	VXI Command Module HP E1406A HPIB	Running under Windows 3.1/95 or HP-UX, framework WIN/WIN95/HP-UX.
HP	—	ADC VXI board HP E1429B	12 bits and 20 MSPS, no decimation, HP local bus, VXI*plugandplay* framework WIN/WIN95/HP-UX.
HP	—	ADC VXI board HP E1430A	23 bits and 10 MSPS, – 110 dB SFDR, up to 24 stages of decimation, complex or real output to HP local bus, Up to 64 MB RAM, Not VXI*plug&play*.
HP	23.3 K[35] CAN	ADC VXI board HP E1437A	23 bits and 20 MSPS, – 110 dB SFDR, up to 24 stages of decimation, complex or real output to HP local bus, Up to 64 MB RAM, VXI*plugandplay* framework WIN/WIN95/HP-UX .
HP	20 K[36] CAN	DSP VXI board VX08	6 TIM-40 sites with HP local bus input. Maximum of 14 C40 per board. Framework TBD.
HP	—	VXI Data Disk and DAT E1562A	SCSI-2 with up to 4,2 GB, input from VXI or local bus.
HP	—	I/O fiber channel interface for VXI, HP E2749	VXI extension module with up to 50 MB/s links using HP local bus. Framework TBD.

[33] HP is coming up with two embedded controllers based on the Pentium® 133 and 166 MHz processors priced at 9 to 12 K.
[34] NT support only with HP VEE development software. Low throughput.
[35] With 8M of RAM.
[36] No TIM-40 modules.

HP	22 K CAN	Wideband down converters model for VXI, E6500A	20-1000 MHz (with opt.003 up to 3000 MHz 12.5 KCAN) frequency range (VHF/UHF), 2 slots C-size (3 slots with option 003). Option 001 for baseband output, 3,7 KCAN.
HP	—	HF Tuner WJC9119	0.1-32 MHz range, 4 MHz bandwidth.
HP	5 K CAN	Digital down converter (DDC) TIM-40	4 DDC per module. From 85 Hz to 174 kHz output with input at 20 MSPS.
Ixthos [Ixt]	—	DSP VME board IXZ8	Up to 8 SHARCs in clusters of 4, VME64 interface.
Ixthos	—	DSP VME board IXZ4 with I/O	Up to 4 SHARCs in clusters of 2, VME64 interface, 2 I/O mezzanines.
Ixthos	—	ADC mezzanine board	Dual 12 bits, 25 MHz A/D IXI mezzanine, FIFO buffer holds up to 64K samples.
Mercury Computer Systems Inc. [MC]	—	MCH6 6U motherboard[37]	Up to 12 SHARC DSP processors with VME64 and RACEway interlink interface.
Mercury Computer Systems Inc.	—	SHARC daughtercards S2T16B and S2T8B	6 SHARC with 32 or 16 MB of DRAM. Go on MCH6.
National Instruments [NI]	6.2 K CAN	VXI-1200 mainframe	6 C-size slots and 3 B-size (VXI and VME) slots.
National Instruments	26 K[38] CAN	VXI embedded computer, VXIpc-850 Series	Based on Pentium 133/166/200 MHz, framework WINNT, GWINNT, WIN95, GWIN95, WIN, GWIN.
National Instruments	11 K[39] CAN	VXI embedded computer, VXIpc-740 Series	Based on Intel 486 50/66/100 MHz, framework WINNT, GWINNT, WIN95, GWIN95, WIN, GWIN.
National Instruments	7 K CAN	VXI external controller, VXI-PCI8015 MXI	PCI based card, framework WINNT, GWINNT, WIN95, GWIN95, WIN, GWIN.
National Instruments	3 K[40] CAN	LabView development environment	All VXI frameworks and many other instruments
Pentek [Pen]	—	DSP VXI board model 4412	Up to 12 C40 with 12 MB of global SRAM, main SRAM, VME64 interface

[37] The Mercury system is based on the RACE architecture composed of RACEway Interlink modules; compute nodes; RACEway crossbars; third-party devices; and RACE and third-party I/O devices.
[38] Include Pentium 200 MHz, 16 MB RAM, 800 MB HD, 2 MD SGVA, WinNT, SCSI-2, 2 PCMCIA, FD, ISA/PCI exp., LabView and VXI Development System.
[39] Include Intel 100 MHz 486, 16 MB RAM, 800 MB HD, 2 MD SGVA, WinNT, 2 PCMCIA, FD, LabView and VXI Development System.
[40] Include Full Development System (FDS), VXI VI Library, and VXI Instruments Libraries.

Pentek	—	DSP VME board model 4285	8 C40 with 22 MB of SRAM, VME64 interface.
Pentek	—	DSP VME board model 4270	4 C40 with 8 MB of SRAM.
Pentek	—	ADC VME board model 6425	12 bits at 25 MHz.
Pentek	≈ 12 K CAN	ADC VME board model 6441	2 12 bits channels at 41 MHz, also available in VXI (5441).
Pentek	—	ADC VME board model 6470	10 bits at 70 MHz.
Pentek	—	ADC VME board model 6472	2 12 bits channels at 70 MHz, also available in VXI (5472).
Pentek	—	ADC VXI board model 4474	14 bits at 10 MHz, no frame-work specified but LabView driver available.
Pentek	≈ 23 K CAN	High speed memory buffer model 6099	64 or 128 MB of memory, used with 6441 or 6472, also available in VXI (5099).
Pentek[41]	≈ 17 K	VHF/UHF VXI receiver model 5101-B1	20 to 3400 MHz, 8 MHz bandwidth at 21.4 MHz IF analog, 8 MHz bandwidth digital at 28.5 MSPS (12 bits).
Pentek	—	VME Multiband Digital Receiver model 4272	One wideband and 2 narrow-band receivers.
Racal [Rac]	—	VXI/VME Mainframe Model 1269[42]	6 C-size slots and 3 B-size (VXI and VME) slots.
Spectrum Signal Processing [SSP]	—	DSP ISA board QPC40S	4 TIM-40 sites (8 C4x max), shared memory[43].
Spectrum Signal Processing	—	DSP PCI board PCI/C44	4 C44 processors with 128K or 512K of 32 bits external program and data SRAM.
Spectrum Signal Processing	—	DSP VME64 SHARC board V8	8 SHARC™s in 4 nodes ar-chitecture, 1 PMC site.
Spectrum Signal Processing	—	DSP VME64 C4x board CV6	2 TIM-40 sites (6 C4x max), shared memory.
Spectrum Signal Processing	—	DSP VME C40 board CV4	Up to 8 C40.
Spectrum Signal Processing	3.7 K[44] CAN	SRAM-DSP TIM-40 module MDC4xS	Single C4x with up to 8(C44)/1.5(C40) MB SRAM.
Spectrum Signal Processing	4 K CAN	ADC TIM-40 module MD70MAI	12 bits 50 or 70 MSPS, Glink serial output.

[41] This receiver will also be available from Andrew Corporation [AnC].
[42] Racal offers several other VXI mainframes.
[43] A non shared memory version is also available (QPC40).
[44] 60 MHz C40 part with memory 1.5 MB of SRAM.

Spectrum Signal Processing	15,5 K CAN	Digital down converter (DDC) TIM-40 module with dual C44	Glink serial input TX and RX, 4 DDC with decimation from 64 up to 131 072, double width TIM-40.
Spectrum Signal Processing	6 K[45] CAN	Dual C44 TIM-40 module MDC44T	Up to 4 MB of SRAM per processor.
Systran [Syst]	—	Fiber channel adapter FibreXpress	Available for PCI and VME buses.
Systran	—	Shared Common RAM Network SCRAMNet	Low latency fiber channel interface card available for PCI and VME buses.
Tartan[46]	≈ 3 K	C/C++ Compiler/Debugger for C4x	Available for PC and SPARC, only C++ DSP compiler.
Traquair Data Systems, Inc. [Trq]	—	DSP PCI C4x board HEPC4	Has 4 TIM-40 sites, drivers for Win 3.1\95\NT.
Texas Instruments [TI]	≈ 2 K	C Compiler/Assembler/ Linker for C4x	Available for PC and SPARC.
Valley Technologies [VT]	21 K	FFT Engine UltraDSP-1128 Wideband DSP Processor	Based on Sharp LH9124/LH9320. 1024 complex point (24 bits) FFT in 89 µs or 65536 complex point FFT in 6.57 ms. 2 slot 6U VME.
Valley Technologies	5.5 K	ADC VME board UltraADC	10 bits at 40 MSPS. Also has a D/A converter.
Valley Technologies	—	Dual Channel Wide Band Digital Receiver VT-412	50 MSPS input, 1 to 6 decimation stages.

5. Recommendations

In the preceding sections, we discussed several topics relating to the architecture of the spectrum surveillance system. We chiefly emphasised the system's wideband requirements to achieve significant performance improvements over current systems and to support new telecommunications applications. We also reviewed a variety of components and described the system architecture. Now we will present our general recommendations for a specialised system and a low-cost system.

5.1 General

The following recommendations apply in the case where one of the two systems (specialised or low-cost) has to be selected. These recommendations should enable us to reduce development time, to benefit from the synergy between the two current projects, to use the latest technologies, to keep an avenue open for future upgrades, and to implement several types of algorithms. Here are the main points:

[45] 60 MHz C44 part with memory 2 MB of SRAM.
[46] I believed that Tartan has been bought by TI recently.

- 2 processing paths: one continuous narrowband channel and one discontinuous wideband channel;
- software-based receiver;
- Processor: ADSP2106x;
- A/D converter: 12 bits or more;
- Operating system: Windows NT;
- Development language for real-time signal processing[47]: C/C++;
- Development language for interface, database and network access: Visual Basic;
- Development language for algorithms: Matlab/Simulink [Mat];
- Processor topology: variable.

The DSP choice is largely motivated by the technical superiority of the SHARC™ over the C4x. The only uncertain aspects of the SHARC™ are the efficiency of the development tools and the limited choice of DSP boards. This should be verified before a strong commitment. The operating system choice of Windows NT is motivated by the following arguments:

- large base and different platform support,
- stable and well supported operating system by many manufacturers,
- variety of development software (DSP, network and interface),
- availability of Rapid Application Development (RAD) tools,
- large pool of programmers,
- is and will be a major OS in the future.

The above development tools are more or less the standard for Windows NT and provide sufficient specificity and generality for our needs.

5.2 Combined System

Ideally, the specialised system and the low-cost system should be built with the same components to minimise the variety of equipment and to make the system as attractive as possible as a potential product. The combined system would represent a compromise between the specialised system and the low-cost system, designed to achieve these goals. However, for obvious reasons, it is very hard to make compromises between a system based on a VXI bus and a system based on a PCI bus. As a result, the first selection criterion should be the price of the system. The system based on VXI technology is presently technically superior, mainly because of the quality of analogue signal conditioning that it can achieve. The component that benefits the most from this is the A/D converter, and in particular the HP E1437A card, which has linearity up to −110 dB. The A/D cards available from the other manufacturers of VME/VXI products do not offer any marked advantage over the technology available for the PCI bus. Linearity is therefore the second selection criterion. On the basis of price and linearity, a system using VXI technology would be superior. The following paragraph presents a parallel between a specialised, VXI-based system and a low-cost, PCI-based system.

[47] With a few routines in Assembler if necessary. Preferably Microsoft Visual C++.

The spectrum analysis system must have an RF stage and an IF stage. The RF stage can be a Rhode & Schwartz ESN receiver or a Steinbrecher receiver, already used in current systems. If it is preferable to replace these receivers, then a down-converter such as the HP E6500A (which handles input frequencies from 20 MHz[48] to 3 GHz) would be a component of choice. No components of this kind are available for the PCI bus or for PCs in general, so choosing such a component would imply choosing a VXI platform as well. If the current receivers are retained, then an analogue conditioning stage for the A/D converter input can be expected to be required. For the VXI platform, the choice of an A/D converter is fairly simple, because only the HP 1437A card has the desired characteristics (sampling rate, number of bits, decimation, dynamic range, local bus). Its only limitation is a somewhat low sampling rate, since it covers only 8 MHz of useful bandwidth. The HP card can be used for the wideband and narrowband path, because it has a decimator. It is important to note that the signal must be real, because the HP 1437A has only one A/D converter. For complex signals, two HP 1437A cards will be needed. For the PC platform, the A/D cards from Gage Applied Sciences seem best for the wideband path, since they offer a high sampling rate, high number of bits, and use a PCI bus connector. Their limitations are that they have no decimator and that their SFDR is not so high as the dynamic range of the Rhode & Schwartz ESN at its optimum operating point. If the basic linearity criteria are met, the Gage cards would be appropriate for sampling a real IF signal up to 20 to 30 MHz or a complex IF signal up to 10 to 15 MHz. For the narrowband path on a PC platform, the choice is not so clear. For the moment, no A/D card with a decimator is available for the PC platform. One solution might be to have a single channel or multi-channel A/D card with a low sampling rate ($\approx$ 1 MHz) and do the decimation in software. With this approach, a signal with 0 Hz to 400[†] kHz of bandwidth can be sampled. This is less restrictive than the HP TIM-40 module with the VX08 card. Another option would be to use the DAS[49] as the narrowband path. The DAS offers excellent flexibility, and its development is already well advanced. If the DSP is not located on the DAS, an FPGA circuit could be used to provide the link between the DAS and the DSP card.

As regards the processor, in a VXI environment, the C40 is the only solution, because to our knowledge there is no SHARC™ board for this platform. An HP 6500A, an HP 1437A, and a VX08 would be recommended. For the PC environment, the SHARC™ is preferable, because it has a higher processor density and consumes less energy. We consider the cards from Alex Parallel Computer to be the most appropriate. The interface between the A/D card and the DSP card could be made via the PCI bus. The SHARC™ is available on the VME platform, but the interface with the A/D converter then becomes the main problem. We would then have to use the VME64 bus, which offers less performance than the HP local bus. If many processors are used, then a powerful multiprocessor environment is recommended for either platform.

[48] IC Spectrum requires 1.5 MHz minimum, which is less than the range of the HP E6500A.

[†] A signal with a 25 kHz bandwidth would require only 2 decimation by 2 stages and one decimation by 5 stage at f_s = 1 MHz.

[49] The DAS is the "Digital Analysis System" of CRC.

5.3 Low-Cost System

If linearity requirements for the system are reduced, either because of lack of support for a military project or because closer scrutiny of the operating conditions for a civilian system indicates that lower linearity would be acceptable, then a lower-cost version of the system could be used. On this platform, we could achieve linearity on the order of –60 to –70 dB at half the cost of the specialised system today. For the low-cost system, our recommendations are as follows:

- Platform: PC with a PCI Rev. 2.1 bus and a DSP SHARC™ card
- Using an improved version of the DAS or a multichannel A/D card for the narrowband path (focus on one channel for a prolonged period of time)
- Using a PCI A/D card for the wideband path (PCI is the local bus).

5.4 Systems To Be Investigated

Two potential DSP systems to investigate would then be (price in CAN $):

Table 4. Specialised and low cost systems.

Specialised system VXI (65 K) **Higher cost** **Higher linearity (– 110 dB)** **Medium effective RF bandwidth (≈ 5.5 MHz)** **Higher bus bandwidth (50 MB/s)**	**Low cost system PCI (27 K)** **Lower cost** **Lower linearity (< – 75 dB)** **Higher effective RF bandwidth (> 10 MHz)** **Higher bus bandwidth (60 MB/s)**
Pentium or Pentium Pro 166/200 MHz (5 K)	Pentium or Pentium Pro 166/200 MHz (5 K)
VXI mainframe with 13 slots (10 K)	—
VXI Controller card (7 K)	—
ADC HP 1437A with 8 MB (23 K)	ADC Gage 6012/PCI with 1 MB (10 K)
DSP HP VX08 with 2 c40s (20 K)	DSP Alex PCI 3000 with 2 SHARCs (12 K)
Upgrade to 14 C40s per VX08 (+ 36 K)	Upgrade to 18 SHARCs per PCI 3000 (+ 27 K or + 38 K)

Note that the above systems do not include the continuous narrowband path hardware. Several alternatives are available to integrate the narrowband path in the above systems, but the issue is not address here because the most challenging path is the wideband one. The specialised system is the first choice. It offers also an interesting potential for general research activities. As well, it provides excellent technical performances with an upgrade path for a more complex system. If the cost cannot be justified and the technical requirements are met, the low cost system can be an alternative. It also provides an upgrade path for a more complex system but with less dynamic range at the moment. In the next few months, both systems will be investigated in detail from a theoretical point of view to determine what are their limitations. Also, when possible, ADC equipment will be tested in the lab. After such a de-

tailed analysis and an exact performance requirement description, a commitment to purchase the appropriate piece of equipment in the fiscal year 97-98 should be put in place.

As a final note, both systems have a high bus bandwidth[50] capability. As a comparative example, the current DAS system is presented in Table 5. Figure 7 summarises the system comparison in terms of cost and linearity.

Table 5. CRC's DAS system.

CRC's DAS system (22 K) **Low cost** **Lower linearity (< – 65 dB)** **High effective RF bandwidth (≈ 10 MHz)** **Lower bus bandwidth (1 MB/s)**
Pentium PC (3 K)
VME like based (1 K)
GPIB based (1 K)
8 bits ADC (7 K)
DSP CARD (10 K)

[50] The table above gives the MB/s needed for a complex FFT and the number of such FFTs per second required assuming floating point representation.

	Number of FFT per second					
FFT size	100	200	400	500	1000	2000
128	0.1024	0.2048	0.4096	0.512	1.024	2.048
256	0.2048	0.4096	0.8192	1.024	2.048	4.096
512	0.4096	0.8192	1.6384	2.048	4.096	8.192
1024	0.8192	1.6384	3.2768	4.096	8.192	16.384
2048	1.6384	3.2768	6.5536	8.192	16.384	32.768
4096	3.2768	6.5536	13.1072	16.384	32.768	65.536

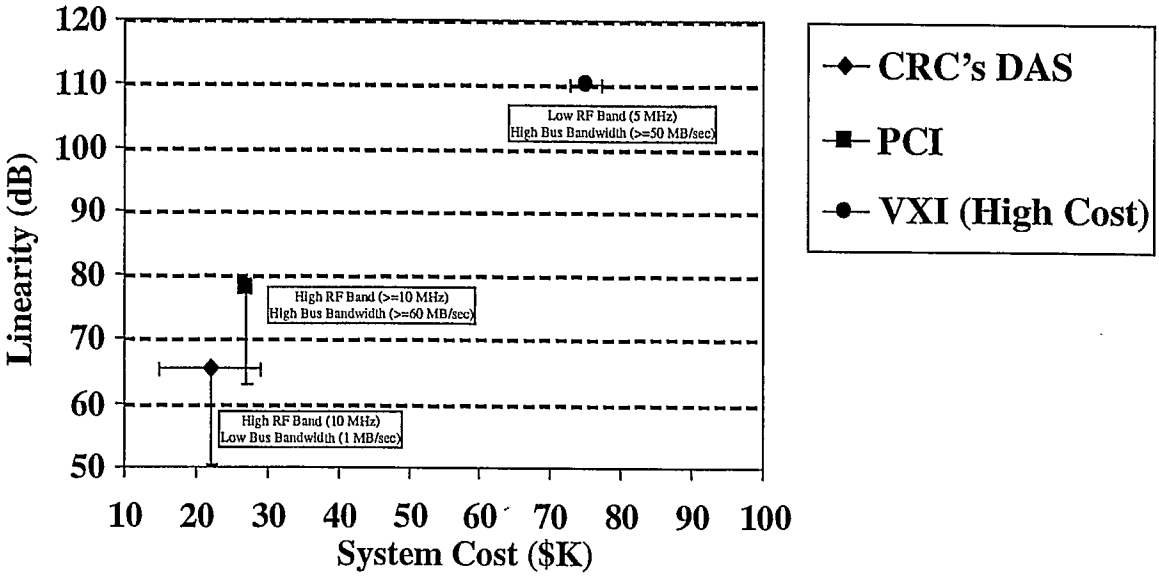

Figure 7. System comparison in cost-linearity plane.

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