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ISSUE A

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TECHNOLOGY SURVEY OF ON-BOARD PROGRAMMABLE DIGITAL COMPUTERS FOR SATELLITE ATTITUDE CONTROL APPLICATIONS

SPAR

ISSUE A

TECHNOLOGY SURVEY OF ON-BOARD PROGRAMMABLE DIGITAL COMPUTERS FOR SATELLITE ATTITUDE CONTROL APPLICATIONS

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In the course of this program and in the preparation of this report, extensive use has been made of Spar Aerospace Products Ltd.'s background data and material. In order to protect Spar Aerospace Products Ltd.'s commercial position, it is respectfully requested that the Government of Canada take this into consideration in dissemination of this report.

6/CCH/1

SUMMARY

The implementation of attitude control system control functions is usually made by special electronics design comprising discrete electronics in which each individual function is performed by a distinct part of the electronics. Such systems are usually inflexible in design and difficult to implement when sophisticated control schemes are required. Digital control systems permit precise control function generation (elimination of drift and noise), implementation of complex control algorithms and high reliability. Digital control systems are best implemented by a programmable control system processor.

This report, prepared under contract for the Department of Communications, presents the results of a study to determine the state-of-the-art of spaceworthy computer hardware and to make recommendations for an on-board computer for the multi-purpose bus satellite Attitude Control System.

TECHNOLOGY SURVEY OF ON-BOARD PROGRAMMABLE DIGITAL COMPUTERS FOR SATELLITE ATTITUDE CONTROL APPLICATIONS

TABLE OF CONTENTS

6/CCH/3

LIST OF ILLUSTRATIONS

LIST OF TABLES

6/CCH/4

GLOSSARY OF TERMS

ACEA	Attitude Control Electronics Assembly
ACS	Attitude Control Subsystem
AFP	Automatic Failure Protection
ALU	Arithmetic and Logic Unit
CAM	Content Addressable Memory
CPU	Central Processing Unit
CROM	Control Read Only Memory
DDA	Digital Differential Analyzer
DIP	Dual Inline Package
DMA	Direct Memory Access
EAROM	Electrically Alterable Read Only Memory
GPC	General Purpose Computer
IC	Integrated Circuit
K	Unit of 2^{10} = 1024 Memory Words or Bits
LSI	Large Scale Integration
MLB	Multi-layer Board
MTBF	Mean Time Between Failures
MWA	Momentum Wheel Assembly
PRC	Pseudo-Rate Controller
PROM	Programmable Read Only Memory
PWC	Pitch Wheel Controller
PWM	Pulse Width Modulator
RAM	Random Access Memory
RCS	Reaction Control Subsystem
RIG	Rate Integrating Gyro
ROM	Read Only Memory
SCR	Silicon Controlled Rectifier
SCS	Silicon Controlled Switch

6/CCH/5

1.0 INTRODUCTION

This report has been prepared under a contract with the Department of Communications (PL.36100-4-100, Serial OPL4-0176), commissioned to determine the state-of-the art of spaceworthy computer hardware and to make preliminary recommendations for a microprocessor for the Multi Purpose Bus satellite Attitude Control Subsystem.

The Attitude Control System for a 3-axis stabilized spacecraft represents approximately 10 to 15% of the spacecraft weight and approximately 25% of the total cost of the spacecraft. When power allotments, component volume and program difficulties are included in the program budget, attitude control system development becomes a pervasive influence in the final configuration of the spacecraft.

Experience with a 3-axis attitude control system has identified a number of serious deficiencies with the use of special purpose, hardwired, realtime controllers. Most of these deficiencies are a result of the very early definition of control laws and numerical parameters required for the design of the special purpose controller. At the early stages of a spacecraft design, many parameters to which the control system is sensitive, are poorly defined. Such parameters include moments of inertia, flexible appendage properties and prime mover performance. Costly and lengthy re-work may be required should these parameters change near the later stages of controller development. For application to a Multi-Purpose Bus satellite required to carry a variety of payloads, a controller capable of only a fixed operation with limited choices could impose undesirable restrictions on the payload operation.

For future applications it is highly desirable to consider the use of a general-purpose digital computer whose hardware development can proceed independently from ACS requirements. This would allow the optimization of control functions shortly before, during and after launch. Only interface

6/CCH/6

hardware will require early definition. The computer hardware package can be defined early, substantially independently of software requirements which need only be defined much later. In addition, a single computer can provide complex computation functions such as sensor noise reduction, and provide transfer orbit control and telemetry processing as well as non-ACS functions.

In some cases, simulation of the computer function by the dynamics analysts can be performed on the actual hardware or an existing simulation program eliminating the cost of developing a spacecraft peculiar controller simulation program.

The weight, power and other "housekeeping" parameters of a General Purpose Computer (GPC) are comparable with special-purpose processors and should incur no penalty along these lines.

2.0 PROCESSOR TASK REQUIREMENTS

The most important computer performance parameters are related to speed and capacity. Therefore, the processor task requirements will determine minimum acceptable levels of capability. It is expected that the following tasks may be performed by the processor and its interface unit:

(a) Real-time to processor time scaling;
(b) Spacecraft kinematics determination including yaw angle;
(c) Roll signal to offset thruster control;
(d) Pitch signal to MWA control;
(e) Array orientation logic;
(f) Transfer orbit control;
(g) Automatic failure protection (AFP);
(h) Thruster control;
(i) Power conversion;
(j) Power switching;
(k) Sensor clocking;
(l) Sensor data recirculation;
(m) Telemetry and command processing;
(n) Sensor noise reduction;
(o) North-South and East-West stationkeeping;
(p) Automatic attitude acquisition;
(q) Antenna orientation.

These items are explained below with reference to processor/interface loadings. Comparisons are drawn between the methods used on CTS and those proposed for the Multi-Purpose Bus satellite where applicable.

(a) Real-time to processor time scaling is a function performed by the interface unit. For processor data input (angular position, for example), pre-determined time delays may be introduced within the interface circuitry. This may be accomplished through a time scale clock which may also double as the processor clock. Output time scaling can be done by using an output number from the processor to preset a down counter whose outputs are logically "OR'ed" together for zero detection.

6/CCH/8

The down counter operating at a fixed frequency provides a pulse "on" time proportional to the input number.

This is predominantly an interface function requiring knowledge of computer hardware clocking speed.

(b) A kinematics program is the only analytical link between processor time and real time for the spacecraft attitude control functions. Error angle data are entered in pitch, roll and yaw. Angular velocity and acceleration may be computed simply through finite differences, or more complex algorithms. From a dynamic standpoint, the error angles represent the error to be corrected, the rate values give information for damping spacecraft motion and acceleration values allow direct measurement and balancing of force. Successive derivatives are obtained from the nested transversal filter which forms the kinematics program, and a balance between accuracy and transport delay must be maintained (differences which are closely spaced and therefore small in relation to measured values are apt to be swamped by noise; large differences introduce an undesirable transport delay which is a destabilizing influence on the control loop). This filter is a software item that may be separate from or integral with the controller programs.

(c) The CTS ACS used a digital differential analyzer (DDA) for pitch and offset (roll-yaw) control functions. The offset thruster control loop simulator was 68 statements long in BASIC language without rate term or noise filter and would be less than 200 statements in a typical assembly language for the pseudo-rate controller (PRC) function which was used. The basic first order lag program could be stored as a common subroutine accessible by the other task programs, reducing storage requirements.

6/CCH/9

The simultaneous availability of all nine kinematics outputs (three vectors in three axes each) could result in a simplified control program. The ability to introduce non-linear elements easily in a program could also be used to advantage. A large portion of any PRC function would have to reside in the interface unit, and a new control method compatible with regular updates would be preferable.

(d) The pitch wheel controller could also be implemented along similar lines to CTS and would probably take no more than 200 instruction words. (Program storage is expected to require 1,024 words = 2^{10} words of storage.) Otherwise, the same comments about kinematics and linearity apply as for roll-yaw control. The pulse width modulator (PWM) output could be a down counter realization as stated in Item (a). Automatic momentum dumping could be easily incorporated in this system.

(e) The array orientation functions were controlled by a separate unit in a separate subsystem on CTS. It may prove worthwhile to use the computer to perform the orientation functions using error data from digital sensors. This function would depend heavily on the interface unit for the power switching and clocking functions.

(f) Transfer orbit calculations are done on CTS by a separate controller. It would be practical to combine the transfer orbit calculations with the computer. This function takes sun sensor inputs and produces output commands to radial and axial thrusters. When a virtual ROM (Read Only Memory) is created by write-protecting a section of a RAM (Random Access Memory), this function could be erased after acquisition, resulting in the incorporation of an extra control function without influencing the memory capacity budget.

6/CCH/10

(g) It would be inefficient to require that the earth station be manned at all times in case of failure. On CTS, automatic failure protection (AFP) was introduced to prevent destructive spin rates or fuel loss from occurring in the event of some malfunction. The failure criteria consisted of any of the following conditions occurring:

(i) AFP command sent from the ground;

(ii) Loss of earth presence signals from both non-spinning earth sensors;

(iii) Failure of the 28 volt ACS supply line;

(iv) Pitch signals reaching maximum angle in either direction.

(v) Roll signals reaching maximum angle in either direction.

AFP would be disabled until after acquisition. In the event AFP conditions occur, the thrusters would be latched off and the wheel would be run in a speed control loop which would maintain the wheel speed at the last value before the failure occurred. Another command would be required to revert to normal control. The controller could not hold position during AFP but would prevent rates from building up. Software implementation of certain functions would require less hardware than on CTS. Memory self-test as covered in a later chapter may be part of the AFP system.

(h) Thruster control will be selectable from either the ground or the computer. It should be possible to command a variable pulse length on any thruster. North-South and East-West stationkeeping may require additional program control - for example, normal operation may be inverted so that certain thrusters are on continuously during stationkeeping except when an attitude correction signal is sent by the processor.

6/CCH/11

(i) To simplify the power interface design, it may be desirable to have the processor condition its power from a regulated 50 volt line. This would be purely a function of the interface unit or a separate assembly not requiring computer processing.

(j) Since power conversion is already included, power switching functions (including AFP) will have to be designed as well. It is the author's opinion that the use of relays for this function would be a serious error. Relays should be eliminated in favour of silicon controlled switches (SCS's) which use silicon controlled rectifiers (SCR's) incorporating gate-turn-off devices. Even if these devices have to be built up from memory cores or regenerative transistor circuits, their reliability will prove superior to relays. Computer memory of power switch status at any given time, could be used to control or reset devices in the event of power failure.

(k) Sensor clocking is expected to come from the main processor clock. In this case, synchronization of the sensors to the processor could result in hardware savings and reduced transport delay. This would be an interface function with computer input if programmed computer I/O is used. Otherwise, sensor inputs could be handled on an interrupt basis. Direct memory access (DMA) as used on large data processing machines is not necessary or recommended as the data rate does not warrant it. Serial to parallel conversion will probably be necessary in the interface unit.

(l) Sensor data recirculation would only be required for an unsynchronized interface. This is an interface or possibly a sensor hardware function.

6/CCH/12

(m) Command interfaces could be more efficiently handled using decoder logic. Thus, rather than a number of individual commands, a multi-valued command could be set up which would be decoded in the computer or interface by using demultiplexer integrated circuits (IC's).

Telemetry processing is presently done by dedicated counters and shift registers. Although counters and serial conversion are unavoidable, some counting can be done by software rather than hardware and some counting functions can be shared by the use of suitable scaling factors involving multiplication in the computer. Selected telemetry could be blanked or read on command and, in addition, a warning flag could be generated from any uncertain conditions so that certain detailed telemetry would only be transmitted if something was wrong. This area will require investigation when system definition is clearer. The computer may make certain of these features simpler to incorporate.

(n) Sensor noise reduction filtering techniques such as Kalman filtering are made possible with computer software in the likely event that transversal or large transport delay filters are unsuitable. It is expected that considerable arithmetic manipulation may be necessary for this function alone, and that the transfer function may be made considerably different in order to make efficient use of noise-reduced kinematic matrix values. The filtering may be implemented on all 9 entries of the kinematic matrix by filtering applied to the three inputs.

(o) North-South and East-West stationkeeping may require some computer processing to control thruster operation at pre-determined times and to provide inverse thruster modulation (thrusters firing continuously and shutting off only on actuation).

6/CCH/13

(p) Attitude acquisition is planned to be done after injection into synchronous orbit. In the event of ACS failure, reacquisition would be required. Either or both these functions may be made automatic with suitable programming since these are entirely ACS functions.

(q) Since the antennas are planned to be fixed, antenna orientation will not be required.

Many of the foregoing tasks cannot be defined in the time frame of this study even in the broadest terms. The availability, for example, of powerful noise reduction techniques may dictate a new type of controller transfer function. All presently known possibilities have been included in the above list without detailed comment on implementation or required memory and speed allotments. None of the processors studied thus far are yet ruled out by being incapable of performing these functions.

The interface unit will be a difficult unit to design since interfaces will remain undefined until all components have been specified. This may represent a larger part of the program effort than the computer, and will be designed and built later than the computer. It is the main controller for certain functions such as thruster control and power conditioning. Their functions do not interfere with the transfer function definition which is expected to be changeable for some time. It should be noted that the flexibility advantage of computers applies only to the software since the hardware is determined from the beginning of the program.

3.0 RESULTS OF TECHNOLOGY SURVEY

3.1 General Discussion

Enquiries were made with vendors who have been connected with the design of military computers in the past or who were known to be actively at work in the field. Many of these manufacturers were actively engaged in military electronics or space programs and were thought to be suitable candidates. Semiconductor houses known to be producing microprocessor IC's were also polled for their comments.

The first round of enquiries eliminated many manufacturers. Much of the military qualified equipment is designed for ground, airborne or missile use where power requirements are not very important and power dissipations into the hundreds of watts with forced air cooling are common. It was decided to not follow up units with power dissipations greater than 30 watts for the present purposes as several manufacturers could meet this requirement.

General Electric in Valley Forge, Pa. is reported to have designed a control unit for the Japanese Broadcast Satellite which had three-year radiation hardening for synchronous orbit, and consists of 40 multi-layer boards (MLB) and a variety of operating functions. The reported 6 watt power dissipation and 18 lb. weight is attractive but a contractual commitment to the Japanese Government prevents GE from releasing detailed information.

Surprisingly, it was found that very few companies are involved with microprocessor IC's. Several reasons were given for this:

(a) Many companies which are production oriented would not like to commit themselves to a device which may be discontinued due to further development of the technology.

(b) A "standard" microprocessor IC or architecture does not exist in the same way that "standard"

logic IC's of various families do. A change in processor would entail drastic design changes.

(c) The only IC's which have been second-sourced to date are 8-bit non-expandible processors unsuitable for the present intended use. A lot failure would not just necessitate replacement, it would mean redesign or lot startup charges.

Only a few of the microprocessor IC's produced to date are expandible to 16 bits. The National Semiconductor p-MOS and Texas Instruments I^2L devices are examples of suitable processors. But the p-MOS device is not guaranteed over the full military temperature range and the I^2L device is not yet available to military quality specifications. Complete computer schematics are available in the National Users' Manual, but the TI information was just being printed at the end of March, 1975. Thus, there are some gaps in the requirements and applications information which may block the development of this type of processor until the latter half of 1975. Of the remaining manufacturers of spaceworthy computers, visits were made to Honeywell in St. Petersburg, Florida, Bendix in Teterboro, N.J., RCA-AED in Hightstown, N.J.+ and Computing Devices Company in Ottawa*. All of these companies had versions of military computers which were capable of performing the necessary functions. RCA-AED has developed a spacecraft computer. Their features are discussed in the following sections.

3.2 Honeywell

Honeywell had several interesting computers of which the HDC301 was considered a suitable candidate. It is built from boards which are 6.25 X 6.35 X 0.5 in. The CPU consists of 15 p-MOS LSIC's on

6/CCH/16

+ Ruta, R.G.: "Report of Visit to USA Vendors of Attitude Control Processors".

* Ruta, R.G.: "Report on Visit to Computing Devices Company".

one board. The memory consumes a large amount of power (7 watts per board containing 2,048 words of instructions, 512 words of ROM and 256 words of RAM). More RAM may be required for the present purposes and the memory power requirement may be too high. The unit contains its own crystal clock and has an interface board (3 watts) available.

One of their larger computers is the LSI-2 which is a 16.5 lb., 220 cu.in. 20 watt package using the low power Schottky TTL logic family. It will be produced in quantity for missile guidance by November of this year. The interesting feature of this unit is the use of large 120 pin hybrid IC's for the CPU and memory. For initial program development, electrically alterable ROM's (EAROM's) from NCR are used. The final pattern is ordered on fixed ROM's as they do not consider the EAROM's to be sufficiently reliable, especially in a nuclear blast environment. The control ROM's (CROM's) are ordered mask-programmed and transplanted from DIP to hybrid packages at Honeywell.

3.3 Bendix

Bendix builds a series of computers which in some cases are combined in one box with 3-axis gyros to form a strapdown guidance unit. Their basic unit is the bulkiest of the ones considered due to the use of TTL DIP's with heat risers on each board (these disappear in the low power version). The CPU is two boards taking 7 watts in LPTTL form. A flatpack version of this unit would be from .6 to .75 of the board area. Bendix have their own MLB facility capable of making boards to 32 layers and they make minicomputers identical to the 920 series which they use to develop programs.

They have an interesting memory board containing 256 words of RAM and 3,840 words of ROM. The RAM takes 7 watts and the ROM takes 2 watts per board due to the use of read cycle only power application to the ROM. DMA is available, but they do not recommend it for our purpose. They also recommend redundancy be accomplished at the computer output.

6/CCH/17

Memory redundancy was not recommended by them as they claim redundancy hardware becomes very unwieldy.

3.4 RCA-AED

The RCA-AED computer, the SCP 234, was designed around an eight-year synchronous orbit mission for attitude control purposes. The largest LSI CPU component is a 2-bit ALU similar to half a 54181 (TTL ALU). They use memory hybrids which they stack two storeys high on the board and 1,024 words of write-protected RAM memory which acts as virtual ROM until a special "erase" order is given for control functions occurring before acquisition. Ordinary ROM is also used. The unit is designed to control all phases of flight from lift off. Memory isolation diagnostic techniques are used which can diagnose and work around bad sections of memory in the event the routine parity check fails. (Memory is rewritten and read again in an attempt to rescue the remaining data and the address of the IC is erased from the memory addressing registers. Thus, the failed IC "disappears" from active program control and remains "invisible" to the CPU.) No such protection is available for the CPU. Ten percent of the memory is set aside for this memory protection.

Two computers are powered all the time and controlled by a separate interface box which contains a power converter, prime/redundant switching and serial/parallel conversion.

In the SCP234, all data is handled on a priority interrupt basis with 14 interrupts accessible from the outside. (The two highest interrupts are used by the computer for internal diagnostics.) The computer is 300 cu.in. in volume, weighs 7.9 lbs. without radiation hardening (add 3 lbs. for hardening) and consumes 3.5 watts operating and 1.5 watts on standby, the lowest of any unit we have found to date. Radiation hardening is accomplished by the use of 30 mil lead sheet on top of the COSMOS and p-MOS IC's and 20 mil lead on the bottom.

6/CCH/18

Reliability was quoted as follows: CPU, 72,000 hrs. MTBF; 8K RAM, 46,500 hrs.; 8K ROM 69,000 hrs. The unit is qualified for 15-20g random vibration and -5C to +55C operating temperatures.

3.5 Computing Devices Company

CDC have several computers of interest to us. Data was obtained on model 469 which is the smallest computer we have seen to date - 4 X 4 X 2.5 in. with keyboard, display and 4K memory! Like RCA, they use write-protected RAM as virtual ROM and have self-healing memory.

They use 2-mil plated wire memory which is naturally radiation hard and are capable of meeting MIL-specs. They stated that I^2L would be the best microprocessor logic family if we decided to go that route and concurred with all other vendors in stating that environmental and "housekeeping" parameters would overshadow performance considerations as the requirements were quite simple. CDC expressed a great deal of technical interest towards a Canadian development of a microprocessor for this application.

The Model 469 weighs 3 lbs. and consumes 10 watts (13 watts with display) and is considered to be one of the best choices. The MTBF is quoted as greater than 25,000 hrs. for the complete assembly with 4K memory.

Table 1 gives comparison data from the four manufacturers.

6/CCH/19

TABLE 1. EXISTING COMPUTER TABLE

Item	Honeywell 301	Bendix 910/920	RCA-AED SCP 234	CDC 469
A. Flight History	Aircraft only	B1 aircraft, others	Qualified, due to fly next year	Navigation, Artillery use
B. Physical Characteristics	Aircraft package 6.25 X 6.35" cards	Cards only (2 cards/CPU) 7" X 7" X 3 1/2 for basics -no box, 8K RAM, CPU, no ROM, no I/O Cards 3.6 lb. harness 1/2 lb. box 2.5 lb. total 7.3 lb. no redundancy	Boards 8.1" X 8.5" single unit 16K RAM, 256 Word ROM - 300 cu. in. 7.9 lb. without radiation hardening 3 lb. for hardening	Size with display and 4K NDRO/DRO plated wire memory 4" X 4" X 2-1/2" Weight 3 lbs. unhardened
C. Logic Series	p-MOS completely - hybrids	TTL CPU, LPTTL available MOS memory - DIP's	p-MOS ROM; CMOS RAM, CPU - hybrids	245 CMOS and p-MOS devices
D. Radiation Hardening	none	none	30 mil lead on top of each chip, 20 mil lead on bottom penalty 3 lb.	none
E. Operational Role	GPC used for guidance of tactical missile/airborne computation	Guidance B1, BS3A-ASW aircraft, pershing missile, engine inlet geometry control B1	3-axis synchronous spacecraft attitude control, booster guidance	GPC used for navigation, artillery computation
F. I/O data rates/ limits	not available	Programmed I/O transfer 200 kHz, DMA 750 kHz	No DMA all I/O treated as interrupt 11 sec input 16 sec output, 10 sec overhead, 35 sec interrupt - 14 external interrupts priority encoded	16 Bit parallel party line I/O 1 serial input 1 serial output 4 bit address control, external clock input 400 kHz burst rate, 100 kHz continuous rate Interface Options: CMOS, PMOS, TTL, DTL

G.	Library	Assembler, Fortran compiler diagnostic, debug, library routines, load, dump -47 instructions	Assembler, simulator (Fortran) loader, dump, diagnostic, debut, 50 library subroutines -68 instructions	Assembler, simulator, loader, dump, diagnostic, debug, library subroutines, memory test and remote -52 instructions	Assembler, simulator diagnostic, debug, trig functions - 44 instructions
H.	Memory	32K total of RAM, ROM not easily extendible	2K/card RAM to 32K, 4K/card ROM to 32K	4K ROM/bd, 8K RAM/bd 256W ROM 16K RAM standard. Write protected virtual ROM 1K volatile - can be returned to RAM duty	4K plated wire RAM expandable to 65K. MOS ROM and RAM optional
I.	Word Length	16 bit dbl prec. +- software dbl prec. x ÷	16 bit dbl prec., floating point +-x ÷	16 bit double prec. +-x ÷	16 bit
K.	Ground Access	No DMA	Serial interface, DMA available	No DMA, priority interrupt 16 total, 14 external 55 sec load	Serial/parallel inputs
L.	Failure Rate/ Redundancy	15 LSI chips single unit CPU no MTBF available Honeywell does not believe in reliability calculations - they eliminate all single point failures	120 chips 50% LSI 50% MSI/SSI recommended output switching - memory switching to CPU not recommended	MTBF: CPU 72K hours 8K RAM 46,500 hours 8K ROM 69K hours - Interface box connects two units; both units powered at all times	MTBF: 25K hours with display single unit
M.	Power Interface	6W CPU 7W Memory 3W I/O	LPTTL CPU 7W 3840 words ROM-2W (TTL ROM) RAM - 7W/256 words	3.5W with 16K RAM, 256W ROM ± 10V - 10V 25ma (p-MOS) + 10V for COSMOS	10 watts (13 watts with display) Input ± 15VDC, ± 5VDC
N.	Environment	Shock, vib.-missile use	Shock, vib.-missile use	Qualified for space	MIL-E-5400K, Class 2
O.	Development Status	In use - airborne	In use - airborne	Qualified	Production item

4.0 REMARKS ON TECHNICAL INFORMATION

Based on the information obtained, RCA and CDC appear to have equipment more suitable for this program. The following remarks apply to the information received from various vendors:

The processor is required to do a very simple job as computer applications go. General purpose logic operations and arithmetic functions common to all computers and most microprocessors will suffice. The environmental, reliability, size, weight and power requirements will decide what unit will be chosen. Size and weight are overwhelmingly in favour of the CDC 469. The RCA SCP 234 is the lowest power unit available, but may be challenged by a CDC 469 with removal of the keyboard, display and certain interface options. The RCA unit appears to be an old design since it does not use their most modern devices. Its interface unit may not be suitable for our use. It contains booster guidance connections and may not have all the functions we require.

Provisions for large data handling capacity such as DMA are not necessary. Even programmed I/O is unnecessary; data can be handled satisfactorily on an interrupt basis.

A microprocessor has very little to offer over a computer which uses a lower degree of integration. The attraction of a small IC is overwhelmed by the fact that an interface, a clock, memory addressing and memories have to be added which make its size comparable to or larger than a computer using standard logic families.

The largest part of the computer hardware is memory. Plated wire and MOS memories are competitive for the present application, but plated wire has the advantage of being non-volatile and radiation hard (non-volatile means that a power interrupt will not erase it). Plated wire requires no standby power, ensuring that memory expansion does not create problems for the power conditioning

6/CCH/22

system. Power is, however, required to read or write.

It should be noted that sophisticated programming used to reduce memory requirements is expensive. It would be considered unwise to limit memory in the hope of reducing costs, but exact memory size cannot be determined yet. There is a rise in programming costs which occurs if the initial version of a program takes up more than about 70% of the memory allocation. Programmers report that expansion of the program during development due to improvements, changes and incorporation of forgotten or new functions occurs until it is seen that 90% of the memory is used (not counting the self-healing "spare" memory allocation) and then efforts to reduce the number of instructions so as not to overrun the memory area will fully occupy the programmers' time. Dr. Aukstikalnis of RCA AED states[+] that software may have to be started before the computer is fully specified not only in order to allow proper estimation of hardware requirements, but to allow hardware and software activities to be completed at the same time.

Vendors tended to minimize the importance of computer price compared to software considerations. However, our simple functional requirements and stringent quality specification may reverse this picture. We have several possibilities to evaluate in the managerial sense:

(a) Purchase of qualified unit with basic software (RCA SCP234).

(b) Adaptation of existing military unit with basic software (CDC#469).

6/CCH/23

[+] Aukstikalnis, A.J.: "Spacecraft Computers", Astronautics & Aeronautics, July/August, 1974.

(c) Adaptation of commercial microprocessor (National IMP-16).

(d) Development of processor with information unavailable as yet (TI SBP0400).

These options are evaluated in Table 2.

It should be noted that memory MTBF may be extended if failures do not result in loss of functional capability. This is the reason only two units will be needed for the projected 70,000 hour mission if memory self-healing routines are designed into the firmware. It is not possible to provide CPU protection of this sort. Redundant switching between memory and CPU is not recommended for most systems due to the complexity and unreliability of the switching units. Redundant clock switching is recommended for improved reliability.

It is usual for computers to operate from crystal clocks but other types may be substituted if shock and vibration are expected to be a problem.

If it is found that the computer throughput is higher than necessary it may be worthwhile to slow the unit down. Power consumption of most computers can be reduced if operating speed decreases. Operation of Metal Oxide Semiconductor (MOS) devices above .25 MHz, low power TTL above 1.5 MHz and standard TTL above 5MHz will incur a power penalty. Typical computers are clocked at 5MHz to achieve a 1MHz cycle. Throughput optimization may pay off in lower power consumption and reduced weight required for heat transfer.

6/CCH/24

TABLE 2. COMPUTER COMPARISON TABLE

Item	1. Qualified Unit RCA	2. Military Unit CDC	3. Existing Microprocessor P-MOS	4. Latest Microprocessor I^2L
1. Size	300 cu in/computer interface box unknown	40 cu in/computer interface box unknown	120-150 cu in/computer interface box unknown	100-130 cu in/computer interface box unknown
2. Weight	11 lb/computer	4 lb/computer	6 lb/computer	5.5 lb/computer
3. Logic Family	COSMOS processor, RAM p-MOS ROM	COSMOS, p-MOS Plated Wire memory	p-MOS processor, CROM TTL(5400,54L00,54H00) MOS memory	I^2L processor TTL MOS memory
4. Radiation Hardening	Lead sheet on all IC's	Lead sheet on MOS devices memory naturally hard	Lead sheet on MOS devices	Lead sheet on memory devices
5. Data Entry	16 bit parallel entry by 14 interrupts only	16 bit party line 1 serial input 1 serial output 3 interrupts, direct execute	DMA available control lines 16 bit party line 4 interrupts	16 bit entry buss 16 bit exit buss control lines
6. Software	Assembler, simulator diagnostic, debug load, dump, fault test, library routines	Assembler, simulator diagnostic, debug tape load, fault test, library routines	Assembler, simulator (FORTRAN) diagnostic, debug tape/card/TTY, load/dump ROM diagnostic for CPU	Not available yet
7. Instruction Speeds				
R-R Add	2.34 µsec	2.4 µsec	4.0 µsec	faster than others
R-R Mult	25 µsec	10.4 µsec	150 µsec	
R-R Divide	28 µsec	30.4 µsec	200 µsec	
8. Word Length Bits	16	16	16	16
9. Memory	16K RAM 256W ROM 4K ROM/BD 8K RAM/BD 1K write protected	4K RAM/ROM expandable to 65K in 4K steps, optional MOS ROM/RAM	4K expandable to 65K in 4K steps	expandable
10. Redundancy Method	2 units both on at all times	2 units	2 units	2 units

6/CCH/26

11. MTBF X 1000 hrs.	CPU 72K 8K RAM 46.5K 8K ROM 69K	CPU +4K ROM/RAM with Keyboard, display, on/off switch 25K	MIL-883B available MTBF unknown	MTBF unknown
12. Power Interface	3.5W operate 1.5W standby -10V @ 25ma +10V remaining power	10 watts ±15V, ±5V	CPU +5V @ 2.25A (11.25W) -12V @ .51A (6W) -9V @ .59A memory (5.4W)	+5V CPU lower power than item 3 +10V MOS RAM probable
13. Environment	-5° + 55°C	MIL-E-5400K Class 2 (-54° +71°C)	CPU IC -55° +85°C	CPU IC -55° + 125°C
14. Hardware Flexibility	none other than memory	some (display, keyboard, serial I/O unnecessary) memory expandable	can be custom tailored	can be custom tailored

5.0 MICROPROCESSOR CONCEPT TO MEET CHOSEN MULTI-PURPOSE BUS SATELLITE CONCEPT

5.1 Performance Requirements

The control function programs for all the tasks listed in Section 2.0 could be adequately stored in 1,024 words of ROM storage. This estimate is based on the controller simulator programs for CTS. For example, the CTS offset PRC program without noise filter or rate term was 68 instructions long in BASIC language and the pitch wheel controller (PWC) was 96 statements of which 19 simulated the PWM. Allowing for the conversion from a compiled language to an assembly language and the extra functions planned for the computer, 1,024 instruction words should be adequate. This is in addition to ROM storage for the assembler, library functions and memory self-healing features. Transfer orbit control may be stored in a write-protected section of RAM in order to free more ROM for other functions.

One should be attempting to design controller functions which would only require the computer to have 4K words of RAM. Simple controllers based on direct manipulation of kinematic matrix values require investigation for this purpose.

Telemetry would be selected for transmission by the computer in order to reduce the amount of information sent at any given time.

(a) Certain telemetry readings would be sent continuously.

(b) Direct read commands would be used to search variable and parameter arrays in the program. In this way, controller state could be completely determined when necessary.

(c) Other telemetry would be sent only by command or during AFP operation. As this is not a technology satellite, continuous monitoring of data such as fuel level, etc. would be unnecessary much of the time. Under AFP

6/CCH/27

conditions, an AFP alarm would be sent and data such as thruster pulse widths would be inhibited (RCS valves would be shut off anyway) and fuel tank level information substituted.

When the control station is not manned, only such things as AFP alarms and AFP trip condition identification would have to be sent in the event of failure. Thus, the computer could switch off ACS telemetry for scheduled periods and switch on only in the event of failure or a direct command.

Where it is found that ACS command decoding can be handled more efficienty by the computer, a standardized 16 bit command word could be sent serially on a single connector pin via the command receiver. Certain command words could be arranged to allow the computer to read the next command from separate 256-command tables. Thus, thousands of command allocations would be available. Other sequential commands could be arranged to provide value buss commands, name registers to be loaded and values to be entered.

It is presently believed that a fixed-point 16 bit processor is adequate for the accuracy requirements. This corresponds to a number range of -32768 to +32767 which gives sufficient resolution. Double precision and scaling operations can be used to handle any requirement for higher accuracy. It should be noted that certain machines use 18 or 20 bit words to provide storage for parity check bits along with the 16 bit data and control words.

As ROM's are already available which give 11-bit resolution for trigonometric functions with 12 $\pm$ 1 5/8 bit accuracy, the use of library routines to calculate these functions can be limited to machines which cannot read these values from ROM.

Hardware multipliers are not necessary for the intended application as the extra speed would not be worth the additional hardware unless the clock speed reduction thus permitted saves a substantial amount of power.

6/CCH/28

Parity check bits in memory may be required to implement the memory self-healing function which is recommended in order to allow the computer to operate beyond its normal MTBF. A spare memory allotment of 10 to 20% is usually allowed for this function.

The final transfer function will most likely be fixed in form with all parameters variable. This allows control law changes to be used after launch for experimental or optimization purposes and allows system test and throughput adjustment to be performed before the software is ready.

5.2 Housekeeping Parameters

It is envisaged that the ACS computer will consist of two redundant computers connected to an interface unit at shown in Fig. 1. It is felt that the interface unit should be mechanically separate from the computers, but the computers can be merged together in one housing. This would allow the development of the two units to proceed independently.

Since the CDC 469 unit weighs 3 lbs. in military form with serial interface, keyboard, display and on-off switch, it would be reasonable to expect a radiation hardened spacecraft version to weigh 4 lbs. Other computers would be heavier. If a plated wire memory is used, radiation hardening would only have to be applied to the remaining IC's which would reduce the weight of the radiation shield from the 3 lbs. used by RCA to approximately 1 lb. Extra cooling would probably not be required as the heat path in this unit is very short and power consumption could be reduced by optimizing the throughput.

The power requirement of the computer will depend on the clock frequency adjustment. The RCA unit has the lowest power requirement of the units which have been investigated at 3.5 watts operating and 1.5 watts standby, but since the two units are powered continuously, the total computer load is 5 watts. The CDC unit takes 10 watts in standard

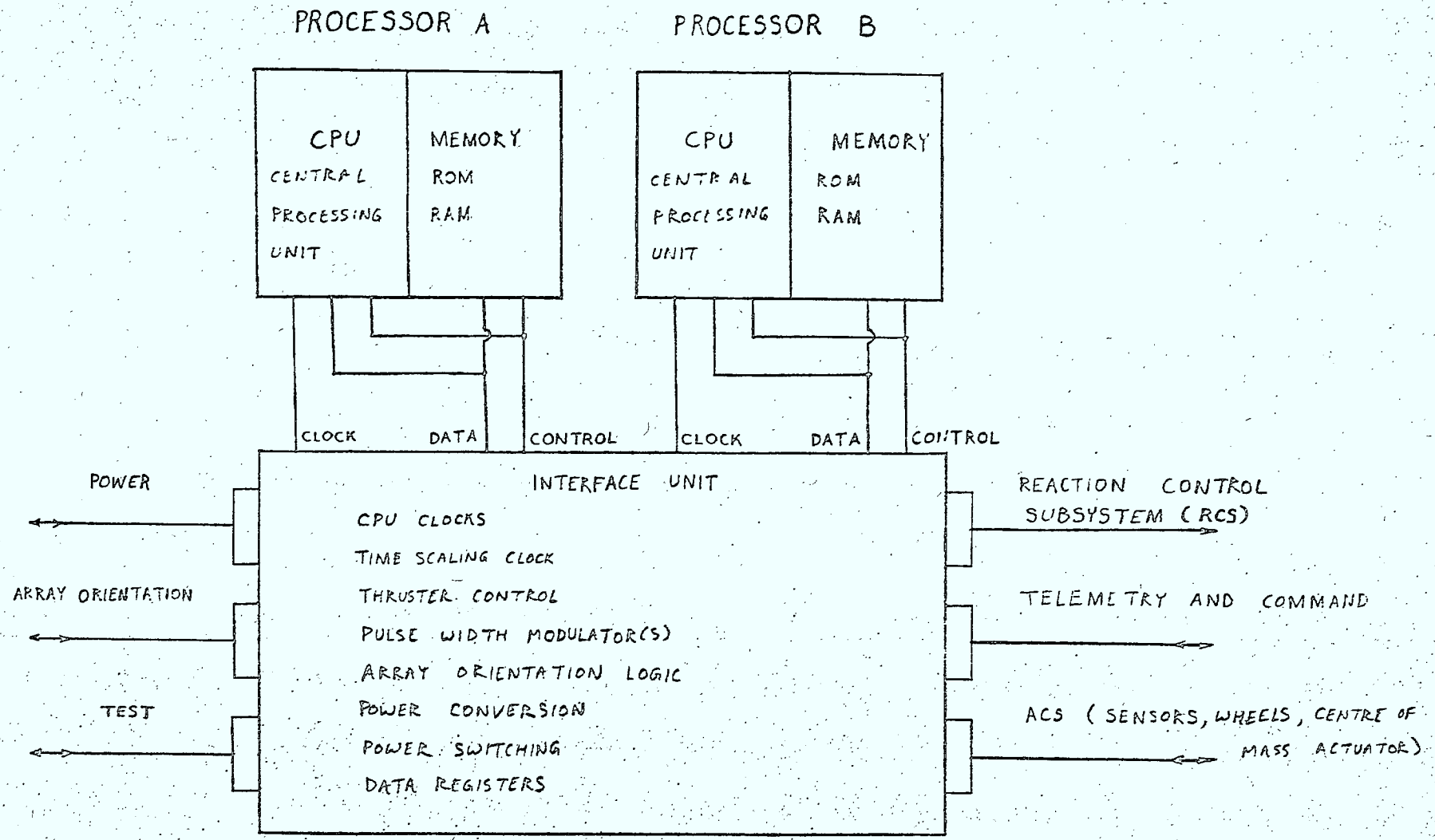

FIGURE 1 ACS COMPUTER BLOCK DIAGRAM

form, but this can probably be reduced to 8 watts by slowing the clock.

The interface unit is not as well defined as the computer but based on performance of all processor task requirements listed in Section 2.0, a weight of 10 lbs. and a power consumption of 6 watts (excluding power conversion efficiency) seems reasonable. If power conversion is done in a separate unit, the interface unit would weigh about 7 lbs. Power switching for the complete ACS would contribute 1 to 2 lbs. of this weight. Array orientation control and power switching contributes approximately 2 lb. of this weight.

The weights and powers listed above are reasonable estimates based on CTS experience and manufacturers' data. They are approximate and subject to change depending on environmental requirements. The values listed for the interface unit have a tolerance of several pounds and several watts and will depend on the implementation of EMC control and power switching functions. Each computer is expected to connect only to the interface unit via one or two connectors, but the interface unit will have connectors for ACS components, the reaction control subsystem (RCS), the power supply, the telemetry and command units and test equipment.

6/CCH/30

6.0 IDENTIFICATION OF DESIGN STUDY TOPICS

The concept of using a general-purpose computer for spacecraft guidance is well established. However, since there is no precedent for a modern computer surviving an 8-year mission in synchronous orbit, it is recommended that phenomena influencing the reliability of computers in this environment be investigated. The severity of the radiation environment, the long mission duration and the common usage of logic and memory families having little flight history in this environment necessitates further investigation in order to improve confidence in the survivability of the unit and to provide inputs required to achieve a cost- and weight-effective design. A task list is presented below which outlines the areas in which additional information is required and proposes methods of obtaining this information:

(a) The generation of a radiation profile for the mission to serve as a requirement specification against which the radiation hardening performance of the candidate microcircuit families may be evaluated.

(b) Evaluation of the known performance of the candidate microcircuit families (p-mos, CMOS, I^2L) in the expected radiation environment.

(c) Based on the foregoing, determination of the shielding requirements and a study of the implications and adequacy of device shielding rather than unit shielding.

(d) A study of the reliability of plated wire memory.

The output of (a) should be the energy distribution and dosage of high speed particles that the design should withstand through launch, acquisition and on-station phases.

6/CCH/31

Task (b) would consist of an evaluation of the performance of the microcircuit families in the expected radiation profile. Both long and short term effects would be considered, including failure modes.

Task (c) would primarily assess the implication on unit construction and design of device shielding. Particular attention will be paid to the effect of the added weight on board design and the effect of the unshielded field of view of the sensitive junctions through the edges of the microcircuits.

Task (d) will consist of a survey of the manufacturing methods and materials used in the plated wire memory to determine if there is any generic weakness in the construction and to identify predominant failure modes. A search will be made for flight history, reliability data and failure rates of this type of equipment.

6/CCH/32

APPENDIX A

COMPUTER HARDWARE ORGANIZATION

This appendix contains a brief dissertation on computers for readers unfamiliar with the topic.

(1) A digital computer operates on information which is digitized or converted to numerical form as opposed to analog form in which a voltage or current is used to represent a variable.

(2) Computer information is quantized in "bits" (binary digits). One bit is the unit of information required to differentiate between two alternative conditions and thus is the smallest unit of information. The bits are organized into binary numbers called "words". The computer performs sequences of Boolean logical operations and binary arithmetic in order to process these words. The type and sequence of operations are under the control of the program.

(3) Software is the programming which is loaded into the computer memory. Hardware refers to the actual device. Firmware refers to the programming functions that are implemented in both hardware and software.

(4) The computer consists of a central processing unit (CPU), a memory and input/output (I/O) hardware. The CPU performs the arithmetic or logical operations on the data which is arranged in words of a certain number of bits (in the present case, 16). The CPU consists of registers which hold data words and program instruction words and an arithmetic and logic unit (ALU) which contains gating to perform all of the operations on the words. It is under the control of the program.

A typical CPU contains accumulator registers which act as working storage for the ALU, a control read-only memory (CROM) which translates program instructions into ALU function commands, a program counter (PC) to store the address of the program instructions and possibly a last-in first-out stack (LIFO stack) from

which words can be retrieved in the opposite order that they were stored. A clock, flags which show various CPU conditions, and interrupt circuitry are contained in the CPU. Various memory address registers may be contained either in CPU or memory hardware.

Memory is the storage area for the program and data. There are many different types as explained below. Memory is sometimes connected directly to the CPU for high speed or where a "cache" memory is used to act as the fast read/write storage for limited information and sometimes connected through the I/O data lines where it acts like any other peripheral such as a tape reader or an interface unit.

Sometimes CPU input and output data lines are physically separate and sometimes a single party line buss is used to handle input and output data. Separate control lines are used to determine whether the CPU, a peripheral or memory is reading or writing at a given time.

(5) Almost any device that retains evidence of the previous input can be used as memory. Some early magnetic memories were destructive readout (DRO) types in which information could only be read once and would have to be restored after reading. Most memories now are of the non-destructive readout (NDRO) type.

Memory is divided into read only memory (ROM) and random access memory (RAM). The contents of ROM can be read by activating the appropriate address lines, but cannot be altered. The outputs are predetermined for each address. ROM is used for program, resident assembler, library and self-test storage.

RAM is also called read/write memory. It is in a random state until an input is written into a location. Any further command to read the contents at this address will retrieve the stored information. RAM is used for data and variable storage.

Other specialized memory types are: PROM (Programmable Read Only Memory) which is manufactured with all locations in one state. The customer programs it by applying pulse voltages to chosen addresses which blow out

6/CCH/34

fusible links that are part of the IC's interconnect metallization.

The electrically alterable ROM (EAROM) was designed to allow correction of PROM programming. It is programmed like PROM, but instead of fusible links, special materials are used which change conductive state in the presence of high voltage and can be restored to original condition by applying high-intensity ultra-violet light. These IC's are built with a quartz window in place of the usual metal cover over the chip.

A write-protected memory is a RAM that is specially gated either by firmware or software to prevent information from being written over it. It thus acts as ROM. If the protective gating condition is removed by command, it reverts to a RAM. This is useful for storing functions which are not needed for the duration of the mission such as transfer orbit programs.

Content addressable memory (CAM) or associative memory is used to determine if a particular word happens to be stored, which is useful for comparison purposes. It is presented here for information only as it is rarely used.

Memory can be organized in various ways to reduce addressing complexity. An IC with 256 bits arranged as 256X1 requires 16 lines of addressing and 16 IC's to store a word. If 16 bit words are to be stored, the memory may be organized to output 16 words of 16 bits each, reducing the number of IC's to be addressed and the number of lines to each IC. However, this is offset by the fact that more addressing is required outside of the IC. It is useful in ROM to power only the IC's being addressed during the "read" cycle of the CPU, and the 16X16 organization may save power for this type of memory.

ROM can also be used to implement multiplication and trigonometric functions and can thus implement firmware items.

(6) Various logic families are available with a full line of logic functions. The IC's in these families are

6/CCH/35

electrically compatible with one another but not necessarily with other families. The major division is bipolar (transistor) and metal oxide semiconductor (MOS) field-effect transistor logic. There are several families in each division. Bipolar is generally faster and requires more power than MOS logic. Table 3 shows some of the characteristics of these families.

Memories are available in all the above families and in addition, magnetic memories are common. These memories take the form of a ferrite core which is magnetized in either of two directions.

If the core is reduced to a layer of magnetic metal plated on a wire, it is called a plated wire memory. These are small enough to compete with semiconductor memories and draw comparable amounts of power. Magnetic memory unlike semiconductor memory is non-volatile i.e. it retains information even when power is removed.

TABLE 3. LOGIC FAMILY COMPARISON TABLE

Logic Family	Devices Available	Preparation Delay [a]	Power Consumption [b]	Special Features
Bipolar				
ECL 10000	Limited family of gates and memories	2/3.7 (NOR gate)	25	Fastest logic family
TTL 5400	Broadest family of functions	7/15	10	Least expensive family
LPTTL 54L00	Almost as many functions as TTL	31/60	1	Used extensively on CTS
HTTL 54H00	Many standard TTL functions	6.2/10	22.5	Made obsolete by Schottky devices
STTL 54S00	Most standard TTL functions	3/5	18.75	Fastest TTL compatible family
LSTTL 54LS00	Most standard TTL functions	10/20	2	Fastest LPTTL compatible family
I^2L	Clocks, microprocessors	25-250 variable	70μ W-6ηW variable	Most suitable for large scale integration
MOS				
n-MOS	Memories	slower than CMOS	Higher than CMOS	
p-MOS	Memories, microprocessors	slower than n-MOS	Higher than CMOS	Best radiation resistance of MOS
COSMOS CMOS	as large a family as TTL	50/75 @ 5V supply 25/40 @ 10V supply	10 W @ 10^3Hz 10mW @ 10^6Hz	Large voltage noise margins

(a) Typical/max. in nsec for a 2-input NAND gate

(b) Average in mW for a 50% duty cycle

(7) I/O can be handled in three ways: dynamic memory access (DMA), programmed I/O, and interrupt.

Dynamic memory access allows information on an I/O buss to be read into memory without interaction with the CPU other than clocking, at the expense of extra hardware. This is used where large volumes of data have to be transferred on a continuous basis e.g. data terminals and time sharing computer utilities.

Programmed I/O provides program instructions to read from or write into a peripheral other than memory. Thus, the interface has to be synchronized to the computer clock. This can be useful for moderate data rates.

We have recommended for our low data rates the use of interrupts for handling incoming data. Interrupt provisions are built into all computers to provide for inputting of information from diagnostic routines and signals which only appear occasionally. Interrupts can be used to interrogate the computer for output data, and this is probably more convenient than programmed output for the present purposes.

When an interrupt signal occurs, the computer moves the contents of all the CPU registers into memory. When the interrupt is processed, the CPU retrieves its register contents from memory and continues what it was doing before the interrupt occurred. The interrupt may be used to load or dump register contents.

One of the interrupt conditions is often a parity check for data. A parity bit of logical "one" may be attached to the end of a word if the sum of the "one's" in the word is even and "zero" if the sum is odd (or vice-versa). The parity bit assures that the sum of the "one's" in received data is either odd (or even) regardless of the data. This allows the computer to monitor received data. If the parity changes from what is required, an interrupt occurs. This interrupt usually takes precedence over others and therefore, priority gating is used to ensure that other interrupts are blocked when system fault interrupts occur. This is the reason that 18 and 20 bit machines are sometimes used for 16 bit arithmetic.

APPENDIX B

COMPUTER SOFTWARE ORGANIZATION

Computer software is usually more difficult to evaluate than the hardware and represents a larger portion of computer cost. A computer is a general-purpose device which must be programmed in order to perform the required function. This appendix contains brief definitions and examples of what the various programs do on a National IMP-16 microprocessor.

(1) OBJECT CODE or MACHINE LANGUAGE mean the same thing. This is the first level of language closest to actual CPU and ALU control line functions. All instructions are words of the same length as the internal data or multiples thereof and are indistinguishable from data except to the machine which time-shares data and instructions. The program functions are of eight general types:

(a) load and store
(b) arithmetic
(c) logical
(d) skip
(e) shifts
(f) transfer of control
(g) register
(h) I/O and miscellaneous

For example, a load immediate (LI) operation in an IMP-16 is represented by:

0100llrrsxxxxxxx

where 010011 means load immediate

rr — is the accumulator to be loaded (0, 1, 2 or 3)

s — is the sign of the number to be loaded and

xxxxxxx — are the bits of lower significance than the sign bit

6/CCH/39

Since the number is only 7 bits plus sign, this number (called the operand) has a range of -128 to +127. For example,

0100110100001110 means load immediate into accumulator one the value +14.

At the end of this operation the number,

0000000000001110 is in accumulator one which is +14 in 16 bit binary.

(2) The ASSEMBLY LANGUAGE or ASSEMBLER or RESIDENT ASSEMBLER is the next higher level of language above machine language. It automatically provides addressing and decimal or hexadecimal conversion. The operators are represented by letter combinations which are acronyms of the operations. The above load immediate instruction is represented in IMP-16 assembler as,

LI 1,14;

(3) The CROSS ASSEMBLER or SIMULATOR is a program designed to allow the user to simulate programming in a particular assembly language on another machine in another language which is usually of higher level. For example, a cross-assembler is available for the IMP-16 in FORTRAN (which is a compiled language) on the Tymshare computer utility. The simulator can usually run on any machine that will accept the compiled language e.g. any machine that accepts FORTRAN if the simulator itself is provided. (National has provided the IMP-16 simulator to Tymshare.)

(4) I/O routines are necessary in order to allow a machine to be programmed from or produce an output on a certain type of peripheral. The IMP-16 has paper tape and card reader routines called LOADERS. Teletype and control panel routines are provided for two-way I/O and a paper tape punch routine is available.

These routines are available for the IMP-16 in the form of ROM, making them firmware items.

(5) DIAGNOSTIC routines are available for many computers. These programs examine the user's program and determine

6/CCH/40

if mistakes in form e.g. invalid operations (opcodes) are being requested. The errors are written on an output in the form of numbers (for which a table is provided identifying the error) or in explanatory sentences. A diagnostic is probably not available for the IMP-16; the only diagnostic listed is really a debug routine.

A typical high-level diagnostic on a typical large computer may see the following statement in the language called BASIC:

```
180 GOSUM 200
```

and respond with

```
ILLEGAL INSTRUCTION IN 180
```

The programmer can then see that the line should read:

```
180 GOSUB 200
```

Note that operations the computer cannot do or understand are the only ones flagged by the diagnostic program; it cannot help a programmer whose program will run but does not do what he wants it to do.

(6) DEBUG routines are helpful when the hardware integrity is suspected. They test hardware and firmware in the same way that a diagnostic tests software. The IMP-16 has several debug programs available. ROMDI is a debug that is supplied in firmware form (four ROM's) to check CPU operation on a temporary basis. (The machine is normally operated without them.)

(7) COMPILERS are programs which translate high-level languages such as BASIC or FORTRAN into the appropriate machine or occasionally assembly language. No compiler is listed for the IMP-16, but a typical FORTRAN compiler would take about 5K of memory.

(8) LIBRARY routines are subroutines or special functions which can be provided optionally. A trigonometric function calculator is an example of a routine that can be provided as a library routine or in ROM hardware. A

6/CCH/41

trigonometric function routine might calculate Taylor series expansions and from them obtain the expressions for various trig functions.

(9) SELF-TEST AND ISOLATE is usually a firmware item which checks RAM memory parity. If errors are found, data is transferred out of the offending IC into another in an attempt to determine whether the fault is permanent (and not just the result of a voltage transient) and rescue all remaining data stored in that IC. The address of the failed device is obliterated and the CPU cannot read or write from it again. The address of the IC to which data was transferred is written over the old address (destroying the old address in the process) and regular operation continues with the validity of the data still unknown. But data tends to be "consumed" during processing and the errors caused by one item of invalid data will disappear after a finite time.

(10) Of the above software, the assembler and I/O routines are necessary, the simulator, debug and self test and isolate are desirable and other routines may be considered optional.

APPENDIX C

COMPUTER INTERFACE OPTIONS

The computer is expected to connect to the interface box and nothing else; the interface box provides all connections to the outside world. The computer requires a 16 bit data bus for party-line operation or two busses for separate CPU I/O lines. An external clock requires one or two lines (for redundant clocking) and possibly an external initialize. Interrupt and control lines are also brought out to the outside world. Power supply lines should be supplied through the interface box even if the power supply is separate. Certain other control lines may be brought out to the interface box, but a single connector should be adequate with party-line I/O or two connectors for separate busses. The leads should be short enough that specialized driver circuitry is not necessary although it is recommended for EMC reasons.

APPENDIX D

ENVIRONMENTAL PARAMETERS

(a) Radiation Hardening

Radiation effects are of two types: permanent degradation and transient level changes. Voltage levels will vary in the presence of radiation, but the transient changes are not expected to cause trouble. Permanent degradation is a possibility with MOS logic, but bipolar logic is considered to be safe in this operating environment. Of the MOS logic, n-MOS and COSMOS are more susceptible than p-MOS devices as the n-channel devices tend to switch on in the presence of radiation. PMOS devices will tend to switch off. Raising the p-MOS device operating voltage can overcome some of this problem, but all MOS devices should be shielded. In addition, most MOS families have been subject to certain manufacturing process changes. For example, the RCA CD4000 series has a maximum dosage limit of 2×10^4 rads. The RCA CD4000A series can withstand 2×10^5 rads. Transient limits are approximately 10^9 rads/sec. for CD4000 and 10^{10} rads/sec for CD4000A. The referenced application note [+] contains details and further references for readers interested in this topic.

It should be noted that process variations in a particular family are not generally announced and it would be wise to ensure traceability of parts to the process used.

6/CCH/44

[+] Vinkoff, M.N., "Radiation Resistance of the COS/MOS CD4000A Series", RCA Application Note ICAN-6224

(b) Part Qualification Status

Specifying the most stringent part quality standards MIL-STD-883, Class A inspection) does not guarantee that the parts will be more reliable. MIL-STD-883, Class B inspection should be adequate provided that the inspection is done correctly.

The microprocessor IC's represent a large part of certain computers, but are not on the preferred parts list. The IMP-16 IC's are available to MIL-STD-883, Class B but are guaranteed only over a -55°C to +85°C temperature range. The standard military temperature range is -55°C to +125°C.) The military version of the SBP0400 series of microcircuits is not available yet but is guaranteed over the full military temperature range. Texas Instruments plan to offer the ceramic package version of this device later this year. National has another device called "PACE" which is a single processor IC that handles 16 bit words. Its operation is very slow, however, due to the fact that control and data signals are time-shared on the same lines due to IC leadout constraints.

6/CCH/45