THE UNIVERSITY OF BRITISH COLUMBIA

The Department of Electrical Engineering

(2)

FINAL REPORT

on

A Study of Monolithic Microwave Integrated Amplifiers

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by

(1)

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Abstract

The objective of the project is to develop methods for the design, fabrication and testing of GaAs monolithic microwave integrated circuits. During the report period, work was carried out on the development of design, fabrication, and test methods for both active devices (MESFET transistors) and passive elements.

The project aims at using direct ion implantation into LEC (liquid encapsulated Cochralski) semi-insulating GaAs (such as is produced by Cominco at Trail, B.C.) rather than the use of epitaxial layers. So far implantations have been done at Optotek or Tektronix but our own (NSERC) ion implanter is now operational (50 μA for ^{28}Si). Encapsulation for post implantation annealing have been done using RF sputtered SiO_2. In the last stages of the report period a Plasmatherm RIE/PE/PECVD system was brought into operation and studies were started on the use of PECVD (plasma enhanced chemical vapour deposition) of Si_3N_4 films and double SiO_2/Si_3N_4 layers.

Introduction

This report contains sections on measurement, fabrication, and design.

The measurement section is concerned with the interfacing of the fabricated devices to an automatic network analyzer (kindly made available to us at Microtel Pacific Research). It deals with a test jig, its parasitics, a revised structure, and the de-embedding process (i.e. the process of separating the characteristics of the device from the measured parameters, which are a function of the jig as well as the device). Results are given for the experimental MESFETS.

The fabrication section indicates the technology involved in the fabrication of the first MESFETS and changes in the procedure which have just become available with the commissioning of the ion implanter and the RIE/PE/PD system. The various masks, plating technique, initial polyimide study, passive elements, and problems associated with fabrication are outlined in this chapter. The design section begins with a discussion of a graphics package which was created to deal with the special problems of geometry posed by microwave circuits. This is followed by a short discussion on the reasons for creating a data analysis file and the capabilities of such a file. The last file discussed in this section is a general circuit analysis program which has been adapted for easier access.

Measurement

The state-of-the-art is far from the desired one in which one could predict the characteristics of the device accurately enough from geometrical dimensions and material properties to avoid the need for measurement. Modelling of both passive and active devices is in need of development to aid in the design procedure.

The instruments used to make the measurements on various fabricated MESFETS were the HP8505A (500 kHz to 1.3 GHz) and the HP8409A (110 MHz to 18 GHz) network analyzers at Microtel Pacific Research. To couple the devices into the input connectors of the analyzers, a test jig was constructed for us by Microtel Pacific Research (Fig. M1). This test jig has been used to evaluate the initial active devices. For these first measurements connections to the microstrip line from the SMA connectors were made by using silver conducting paint. This led to a number of problems which included uncertainty of the position of contact to the microstrip, widening of the microstrip lines, lack of mechanical strength, and questionable reproducibility. To bypass these constraints a second generation of test jigs has been designed (Fig. M2) and fabricated. The center conductors of the SMA have been rounded off and shortened to reduce the parasitic capacitances of the corners. The pressure screws force the microstrip lines into contact with the center conductor of the SMA after the SMA has been tightened to the base. This pressure contact is reproduceable and the length of center conductor extending onto the microstrip may be minimized.

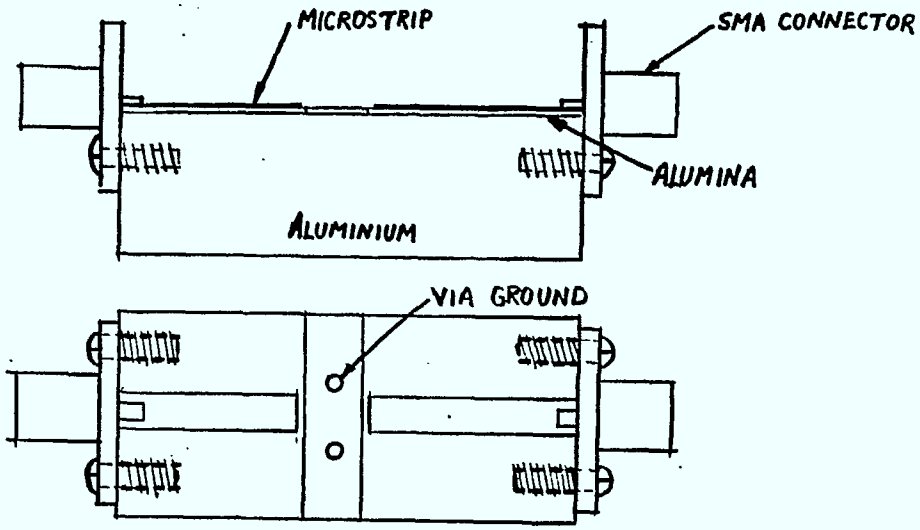

Fig. M1
ORIGINAL TEST JIG

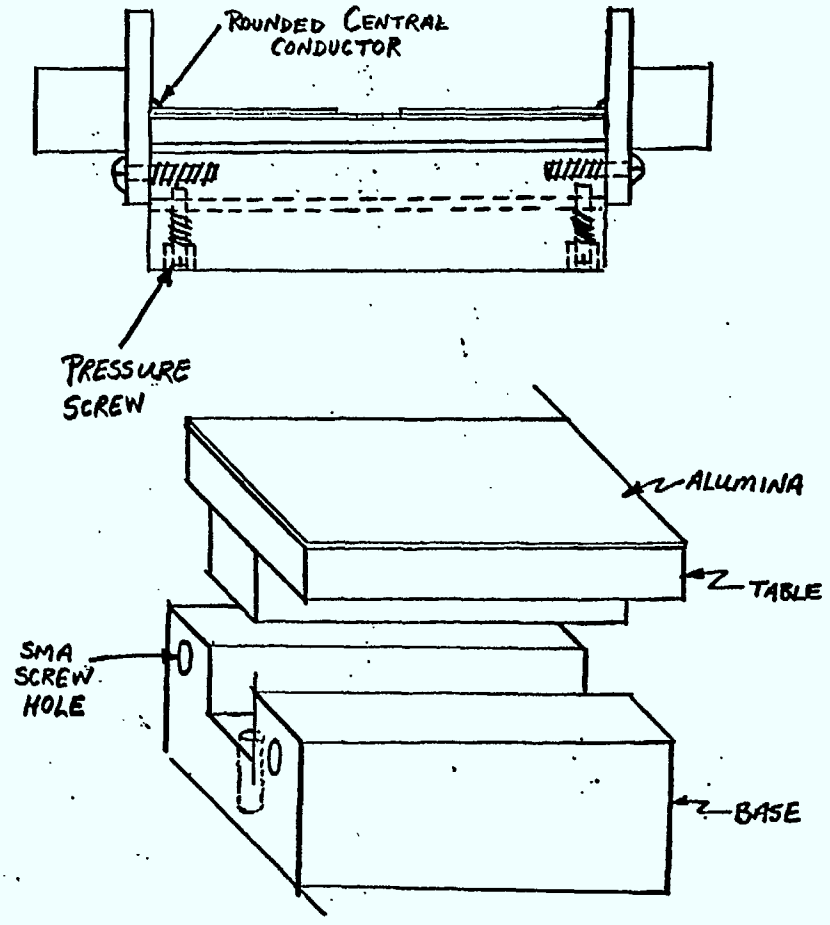

Fig. M2
REVISED BASE STRUCTURE

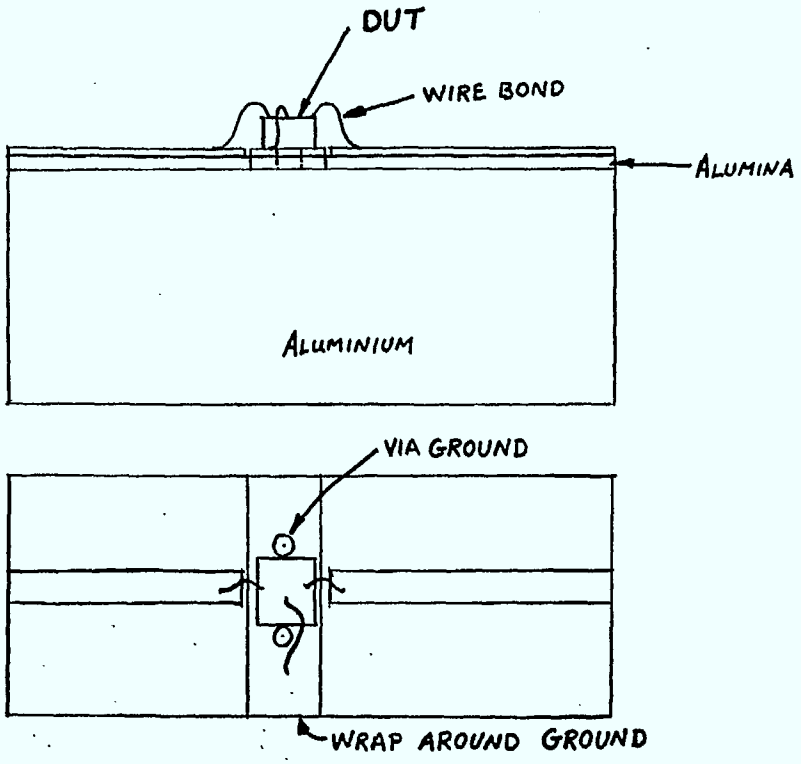
DUT
WIRE BOND
ALUMINA
ALUMINIUM
VIA GROUND
WRAP AROUND GROUND

Fig. M3

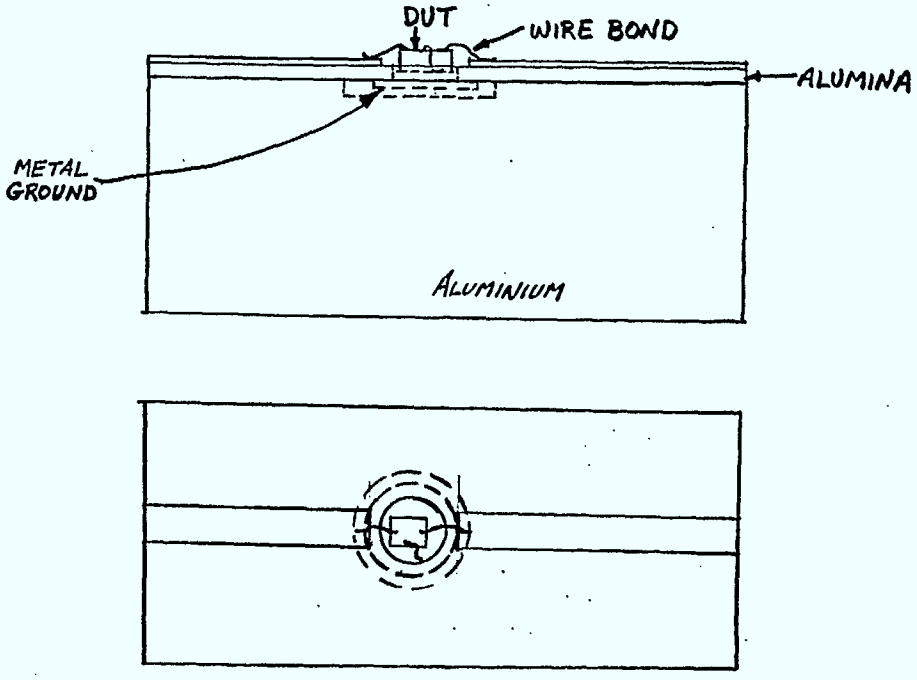
DUT
WIRE BOND
ALUMINA
METAL GROUND
ALUMINIUM

Fig. M4

The contact from the DUT (device under test) to the test jig has been made by epoxying the unit to the ground plane between the two vias, and ultrasonically bonding 25 micron diameter gold wire from the contact pads on the device to the microstrip feeds. (Fig. M3). This initial procedure has led to problems with the non destructive removal of the DUT, long grounding distances, and lengths of wire bonds. Fig. M4 illustrates the alternative design to be incorporated in the new generation of test jigs.

Two problems arise in the determination of useful device parameters; (a) The measurement planes of the network analyzer lie outside the planes of the test jig. (b) The effects of wire bonds must be removed to give the actual characteristics of the device in an MMIC circuit.

To characterize the connector the set up is Fig. M5 is used. The network analyzer gives the reflection and transmission coefficients (ρ and τ respectively) which are related to the connectors S matrix (assuming S_{22} is small) by,

$$\rho = S_{11} + S_{22}\, S_{12}\, S_{21}\, e^{-j2\beta\ell}$$

$$\tau = S_{12}\, S_{21}\, e^{-j\beta\ell}$$

where $\beta = \frac{2\pi}{\lambda_g}$ (λ_g = wavelength in the guide)

When two values of ℓ are used (ℓ_1 and ℓ_2) for a given β then the useful part of the connectors S matrix is determined:

$$S_{12}\, S_{21} = \tau e^{j\beta\ell_1}$$

$$S_{11} = \frac{\rho_1 e^{-j2\beta\ell_2} - \rho_2 e^{-j2\beta\ell_1}}{e^{-j2\beta\ell_2} - e^{-j2\beta\ell_1}},$$

and $$S_{22} = \frac{\rho_2 - \rho_1}{\tau e^{j\beta\ell_1}(e^{-j2\beta\ell_1} - e^{-j2\beta\ell_1}}.$$

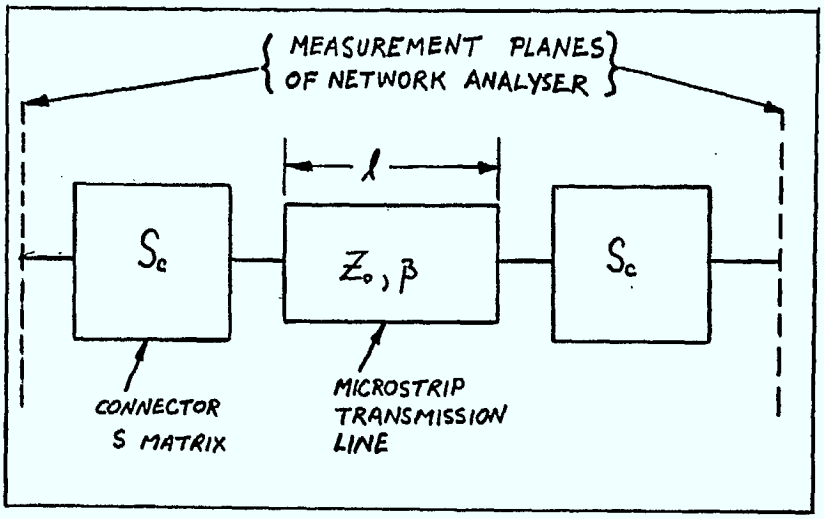

Fig. M5

These values are in the process of being measured for the new test jig. With these measured values it will be shown in the next few pages that the connectors may be subtracted from the network analyzer measurements. The connector is not only the SMA and junction. The connector also includes the variation of the measurement plane from the end of the SMA.

When the connectors have been taken into account then the resulting parameters are for the diagram in Fig. M6. The symmetry of Fig. M6 allowed

multiplying each of the S parameters by $e^{j2\beta d}$ to get the S parameters for the wire bonds plus DUT.

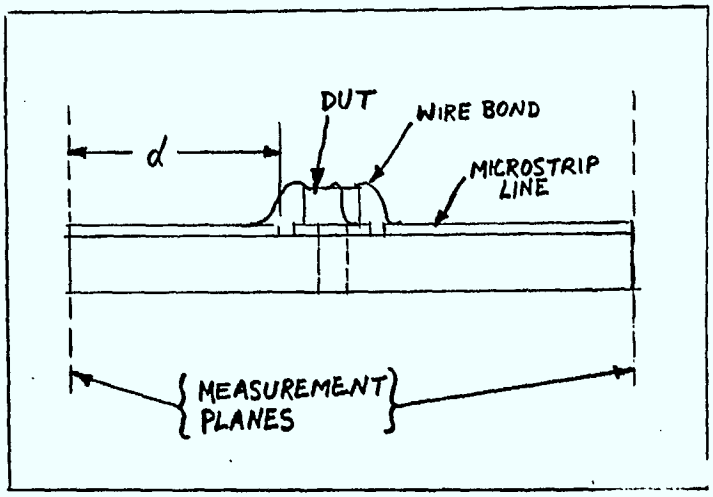

Fig. M6

To remove the wire bonds the de-embedding process was used†. This program removes the effects of the two wire bonds from the microstrip feed lines and a subsequent series connection de-embedding removes the wire bond to the ground strip. The inductance for the wire bond is seen in graph M1. The de-embedding program used to remove the connectors from the measured data is considerably simplified (Fig. M7) from the form given in the design section since $S_{\beta 1} = S_{\beta 2}$ is assumed.

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†K.C. Gupta, Ramesh Garg, Rakesh Chadha - Computer Aided Design of Microwave Circuits - Chp. 11.

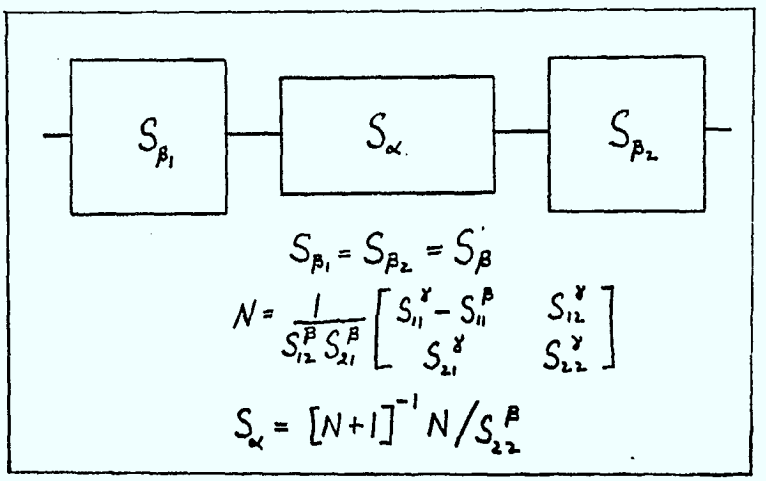
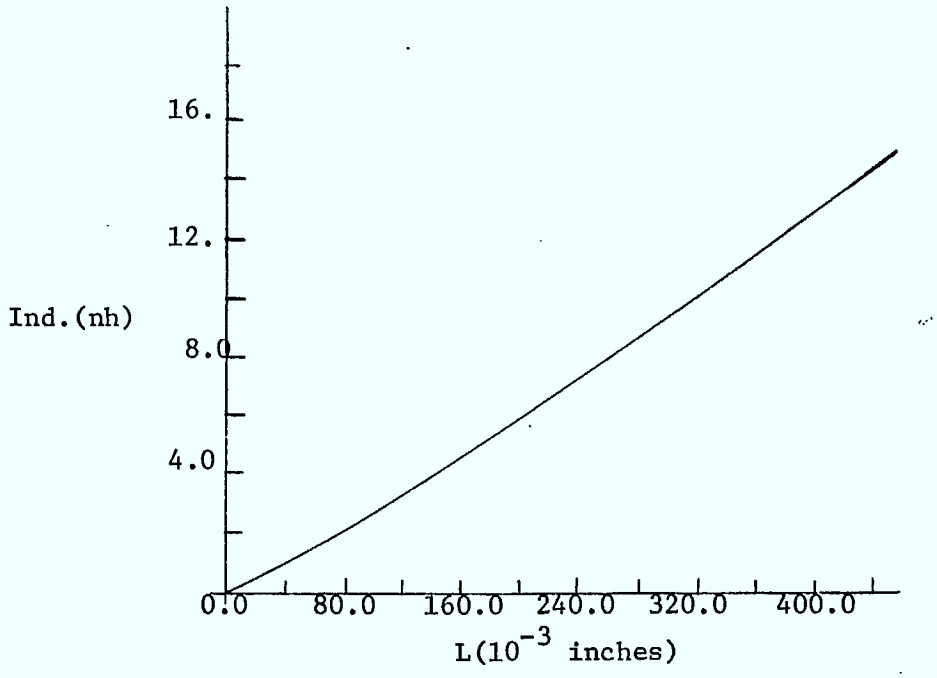


Fig. M7

The initial MPR data using the jig of Fig. M1 gave the data summarized in Table M1 for three separate calibration standards.

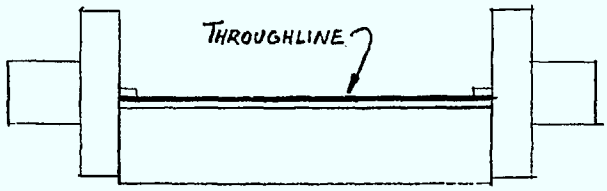
The information given in Table M1 implies the transition from coax to microstrip has very little influence in this frequency band. The model for the through line measurements (Fig. M8) gives the through line S matrix as

$$\begin{bmatrix} \phi & e^{-j\beta\ell} \\ e^{-j\beta\ell} & \phi \end{bmatrix}.$$



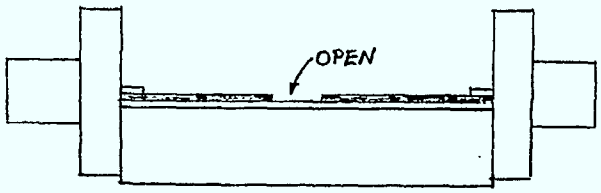
GRAPH M1

THROUGH LINE RESULTS



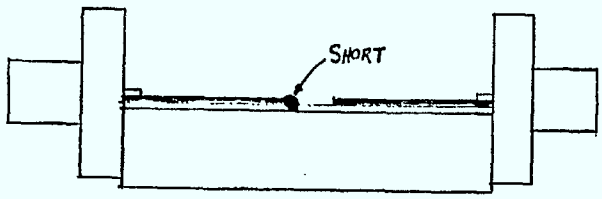
f	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	db	/degrees	db	/degrees	db	/degrees	db	/degrees
2	-14.7	/-18.0	-0.6	/67	-0.6	/68.0	-15.4	/-21.0
				-150°				
3	-15.4	/-157	-0.6	/-83	-0.7	/-82.0	-16.3	/-174
				-147°				
4	-20.7	/55	-0.7	/130	-0.7	/132.0	-20.0	/12
				-152°				
5	-22.2	/32	-1.0	/-22	-0.8	/-20.0	-25.1	/59
				-150°				
6	-13.8	/-92	-1.1	/-172	-1.1	/-172	-13.0	/-80

OPEN LINE RESULTS



2	-0.0	/73		-80.0	/-153	-79.6	/-156	-0.0 /73
			-139°					
3	-0.3	/-66		-79.9	/-158	-81.1	/-166	-0.3 /-66
			-143°					
4	-0.1	/151		-75.6	/-16	-75.9	/-14	-0.1 /151
			-141°					
5	-0.3	/10		-70.1	/-12	-69.8	/-12	-0.3 /10
			-151°					
6	-0.5	/-127		-65.4	/-128	-65.2	/-131	-0.5 /-127

SHORT CIRCUIT RESULTS



2	-0.5	/-107		-71.9	/-172	-71.3	/-168	-0.5 /-107
			145°					
3	-0.5	/106		-76.5	/64	-76.2	/65	-0.5 /106
			147°					
4	-0.4	/-41		-67.2	/-44	-67.1	/-46	-0.4 /-41
			150°					
5	-0.6	/169		-63.4	/-157	-63.4	/-155	-0.6 /169
			159°					
6	-0.8	/10		-61.8	/76	-61.9	/73	-0.6 /11

Table M1

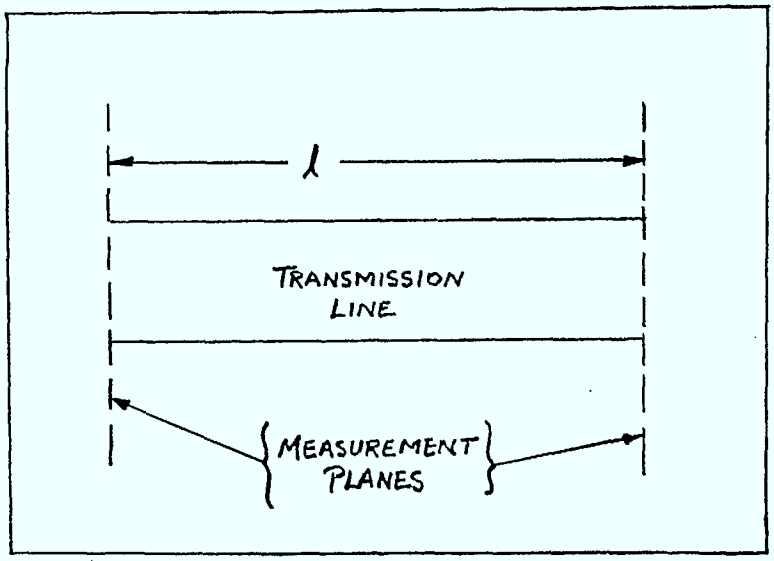


Fig.M8

The $\beta\ell$ factor measured is approximately equal to the $2\beta d$ factor required to move the S parameters from the network analyzer measurement planes to the wire bonds plus DUT. Under 6 GHz this approximation should be accurate to less than 10%. The approximation ignores the gap where the DUT is placed. The through line angles are $-\beta\ell$ radians and therefore must be subtracted from the measured S parameter angles to obtain the actual wire bond plus DUT values.

The removal of the wire bonds from the source drain and gate were accomplished using the de-embedding program. From the resulting device parameters were calculated availabe gain, stability, and matching networks. The results from 3 μm gate length MESFETS are given in Table M2. Earlier results for 30 μm gate length MESFETS are given in Table M3. The available gain of the 3 μm devices approached unity between 3 and 4 GHz as compared to

300 MHz for the 30 μm devices. The 3 μm devices are unconditionally stable over this frequency band. ($K > 1$, $\Delta < 1$).

The bias on the MESFET was applied through two bias tees attached to each two port of Fig. M9.

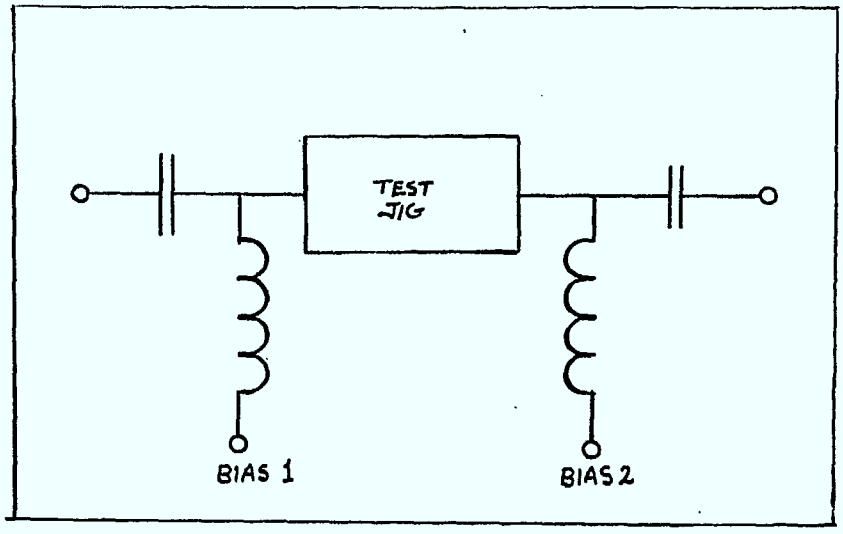


Fig. M9

Table M2

DEVICE 51 - t 132a r1 c6 v_{ds} = 3V v_{gs} = -3V

f=2 GHZ S = $\begin{bmatrix} .903\ /-20 & .051\ /73 \\ .536\ /145 & .88\ /-9 \end{bmatrix}$ Δ=.81 K=1.1 (MAXIMUM AVAILABLE GAIN) MAG=8.3 db

Z_{IN}(NORMALIZED MATCHING NETWORK)=(.6,4.1)

Z_{OUT}(NORMALIZED MATCHING NETWORK)=(1.7,6.1)

f=3 GHz S = $\begin{bmatrix} .846\ /-26 & .029\ /65 \\ .467\ /152 & .8\ /-9 \end{bmatrix}$ Δ=.68 K=4.0 MAG=3.1 db

Z_{IN} = (1.34, 3.6)

Z_{OUT} = (4.74, 4.2)

f=4 GHz S = $\begin{bmatrix} .853\ /-30 & .033\ /40 \\ .284\ /152 & .843\ /-14 \end{bmatrix}$ Δ=.72 K=4.6 MAG=-0.24 db

Z_{IN} = (1.1,3.3)

Z_{OUT} = (3.4,4.9)

f=5 GHz S = $\begin{bmatrix} .922\ /-28 & .076\ /6.0 \\ .088\ /158 & .837\ /-19 \end{bmatrix}$ Δ=.78 K=4.0 MAG=-8.3 db

Z_{IN} = (.73, 3.7)

Z_{OUT} = (2.5, 4.0)

DEVICE 51 - t132a r1 c6 v_{ds} = 3V v_{gs} = -1.5V

f=2 GHz S = $\begin{bmatrix} .893\ /-22 & .081\ /67 \\ .597\ /164 & .68\ /-15 \end{bmatrix}$ Δ=.61 K=1.17 MAG=6.2 db

Z_{IN} = (.57, 4.2)

Z_{OUT} = (1.1, 3.0)

f=3 GHz $S = \begin{bmatrix} .85\ \underline{/-27} & .082\ \underline{/49} \\ .368\ \underline{/-175} & .731\ \underline{/-29} \end{bmatrix}$ Δ=.61 K=1.9 MAG=0.95 db $Z_{IN} = (.86, 3.5)$ $Z_{OUT} = (1.1, 2.7)$

f=4 GHz $S = \begin{bmatrix} .89\ \underline{/-32} & .138\ \underline{/32} \\ .159\ \underline{/162} & .835\ \underline{/-29} \end{bmatrix}$ Δ=.75 K=1.7 MAG=-4.1 db $Z_{IN} = (.56, 3.0)$ $Z_{OUT} = (.88, 3.0)$

f=5 GHz $S = \begin{bmatrix} .862\ \underline{/-30} & .149\ \underline{/41} \\ .047\ \underline{/22} & .902\ \underline{/-26} \end{bmatrix}$ Δ=.78 K=3.8 MAG=-13.7 db $Z_{IN} = (1.3, 3.6)$ $Z_{OUT} = (1.2, 4.3)$

DEVICE 123 - S131a r2 c5 $v_{ds} = 2V$ $v_{gs} = -1.5V$

f=2 GHz $S = \begin{bmatrix} .89\ \underline{/-22} & .07\ \underline{/63} \\ .27\ \underline{/126} & .94\ \underline{/-13} \end{bmatrix}$ Δ=.85 K=1.2 MAG=2.9 db $Z_{IN} = (1.1, 3.4)$ $Z_{OUT} = (1.6, 6.2)$

f=3 GHz $S = \begin{bmatrix} .825\ \underline{/-25} & .07\ \underline{/59} \\ .24\ \underline{/125} & .9\ \underline{/-12} \end{bmatrix}$ Δ=.76 K=2.4 MAG=-1.2 db $Z_{IN} = (1.6, 3.1)$ $Z_{OUT} = (3.6, 6.5)$

f=4 GHz $S = \begin{bmatrix} .819\ \underline{/-31} & .073\ \underline{/56} \\ .2\ \underline{/116} & .914\ \underline{/-13} \end{bmatrix}$ Δ=.76 K=2.5 MAG=-2.4 db $Z_{IN} = (1.3, 2.7)$ $Z_{OUT} = (3.1, 6.6)$

f=5 GHz S = $\begin{bmatrix} .886\ \underline{/-28} & .094\ \underline{/-6} \\ .045\ \underline{/-160} & .79\ \underline{/-13} \end{bmatrix}$ Δ=.7 Z_{IN} = (1.0, 3.7)
K=10.0 Z_{OUT} = (4.2, 4.0)
MAG=-16.2 db

DEVICE 123 = S131a r2 c5 v_{ds} = 2V v_{gs} = -.5V

f=2 GHz S = $\begin{bmatrix} .89\ \underline{/-24} & .111\ \underline{/63} \\ .35\ \underline{/125} & .89\ \underline{/-15} \end{bmatrix}$ Δ=.82 Z_{IN} = (.67, 3.2)
K=1.1 Z_{OUT} = (1.2, 4.4)
MAG=2.9 db

f=3 GHz S = $\begin{bmatrix} .822\ \underline{/-28} & .112\ \underline{/62} \\ .315\ \underline{/127} & .823\ \underline{/-14} \end{bmatrix}$ Δ=.7 Z_{IN} = (1.2, 2.9)
K=1.9 Z_{OUT} = (2.9, 4.0)
MAG=-1.0 db

f=4 GHz S = $\begin{bmatrix} .831\ \underline{/-33} & .121\ \underline{/50} \\ .217\ \underline{/131} & .778\ \underline{/-18} \end{bmatrix}$ Δ=.66 Z_{IN} = (1.0, 2.8)
K=2.8 Z_{OUT} = (2.6, 3.2)
MAG=-4.7 db

f=5 GHz S = $\begin{bmatrix} .904\ \underline{/-32} & .145\ \underline{/21} \\ .077\ \underline{/91} & .777\ \underline{/-23} \end{bmatrix}$ Δ=.71 Z_{IN} = (.77, 3.3)
K=3.9 Z_{OUT} = (2.7, 3.1)
MAG=-11.6 db

DEVICE 123 - S131 r1 c8 v_{ds} = 2V v_{gs} = -1.5V

f=2 GHz S = $\begin{bmatrix} .893\ \underline{/-24} & .08\ \underline{/61} \\ .29\ \underline{/119} & .936\ \underline{/-15} \end{bmatrix}$ Δ=.85 Z_{IN} = (1.0, 3.2)
K=1.2 Z_{OUT} = (1.5, 5.5)
MAG=2.9 db

f=3 GHz S = $\begin{bmatrix} .801\ \underline{/-25} & .081\ \underline{/56} \\ .271\ \underline{/103} & .902\ \underline{/-13} \end{bmatrix}$ Δ=.74 K=2.2 MAG=-1.0 db $Z_{IN} = (2.0, 2.8)$ $Z_{OUT} = (3.4, 6.0)$

f=4 GHz S = $\begin{bmatrix} .516\ \underline{/-27} & .068\ \underline{/46} \\ .146\ \underline{/31} & .917\ \underline{/-13} \end{bmatrix}$ Δ=.48 K=6.1 MAG=-7.5 db $Z_{IN} = (2.4, 1.1)$ $Z_{OUT} = (3.1, 7.7)$

f=5 GHz S = $\begin{bmatrix} .652\ \underline{/-32} & .036\ \underline{/70} \\ .166\ \underline{/98} & .865\ \underline{/-14} \end{bmatrix}$ Δ=.57 K=12.6 MAG=-7.4 db $Z_{IN} = (1.7, 2.0)$ $Z_{OUT} = (3.6, 5.8)$

Device 123 = S131 r1 c8 v_{ds} = 2V v_{gs} = -.5V

f=2 GHz S = $\begin{bmatrix} .853\ \underline{/-28} & .166\ \underline{/60} \\ .317\ \underline{/110} & .804\ \underline{/-18} \end{bmatrix}$ Δ=.73 K=1.5 MAG=-1.29 db $Z_{IN} = (1.1, 2.9)$ $Z_{OUT} = (2.0, 2.9)$

f=3 GHz S = $\begin{bmatrix} .784\ \underline{/-33} & .188\ \underline{/54} \\ .304\ \underline{/98} & .77\ \underline{/-20} \end{bmatrix}$ Δ=.66 K=1.9 MAG=-3.5 db $Z_{IN} = (1.35, 2.35)$ $Z_{OUT} = (2.4, 2.6)$

f=4 GHz S = $\begin{bmatrix} .639\ \underline{/-37} & .191\ \underline{/51} \\ .237\ \underline{/66} & .775\ \underline{/-23} \end{bmatrix}$ Δ=.54 K=3.12 MAG=-6.9 db $Z_{IN} = (1.7, 1.6)$ $Z_{OUT} = (2.4, 3.1)$

f=5 GHz S = $\begin{bmatrix} .733\ \underline{/-42} & .182\ \underline{/42} \\ .171\ \underline{/84} & .736\ \underline{/-28} \end{bmatrix}$ Δ=.57 K=3.9 MAG=-9.2 db $Z_{IN} = (1.1, 2.0)$ $Z_{OUT} = (1.9, 2.5)$

(30 μm gate lengths)

Device R5C4 v_{gs} = - .2V v_{DS} = 5V

f(Mhz)	MAG(db)
3.0	15.5
15.0	10.1
212.0	6.9
400.0	-.8
1218.0	-9.1

Device R6C4 v_{gs} = -.5V V_{DS} = 5V

f(MHz)	MAG(db)
3.0	13.7
15.0	10.5
212.0	10.5
500.0	0.0
1218.0	-2.4

Table M3

Fabrication

The steps in the fabrication procedure for the MESFET's are listed in Table F1. Changes in the procedure in the next generation of devices include multiple implants, silicon nitride replacement of silicon dioxide encapsulation, multilayer gate metal, plating of contacts, recessed gates, submicron technology, and dry etching.

Degrease	5 min	Tricholorethylene (water bath)
	5 min	Acetone (boiling)
	5 min	2-Propanol
GaAs Etch	3 min	$4H_2SO_4 + 1H_2O_2 + 1H_2O$
	10 min	DI H_2O rinse
Oxide Etch	10 min	conc HCl (boiling)
	10 min	DI H_2O rinse
	N_2 Blow Dry	
	6000Å SiO_2 by RF sputtering	
Registration Mark Etch	AZ1350J Photoresist used	
	Oxide etch	
	GaAs etch 1 min	10% HCl
		DI H_2O rinse
	50 secs.	5% H_2PO_4 + 2.5% H_2O_2
		DI H_2O rinse
Implant	Open Windows for implant	
	^{28}Si 100 KeV	
	Strip Mask	
	Add 2000Å SiO_2 and anneal	
	Strip SiO_2	
Source and Drain Metal	Ohmic contacts - 3000Å AuGe + Anneal	
Gate Metal	Gate Metallization (Aluminum)	

Table F1

Experiments in the plating technique to form beam leads, air bridges, enhanced microstrip lines, and overlay capacitors have been performed using the four mask set shown in Fig. F1.

The first mask sets down the first layer of metallization for the overlay capacitor (B1) and the microstrip lines (A1). The second mask (B2) is used for the capacitor dielectric and thus there is no opening in the air bridge mask set.

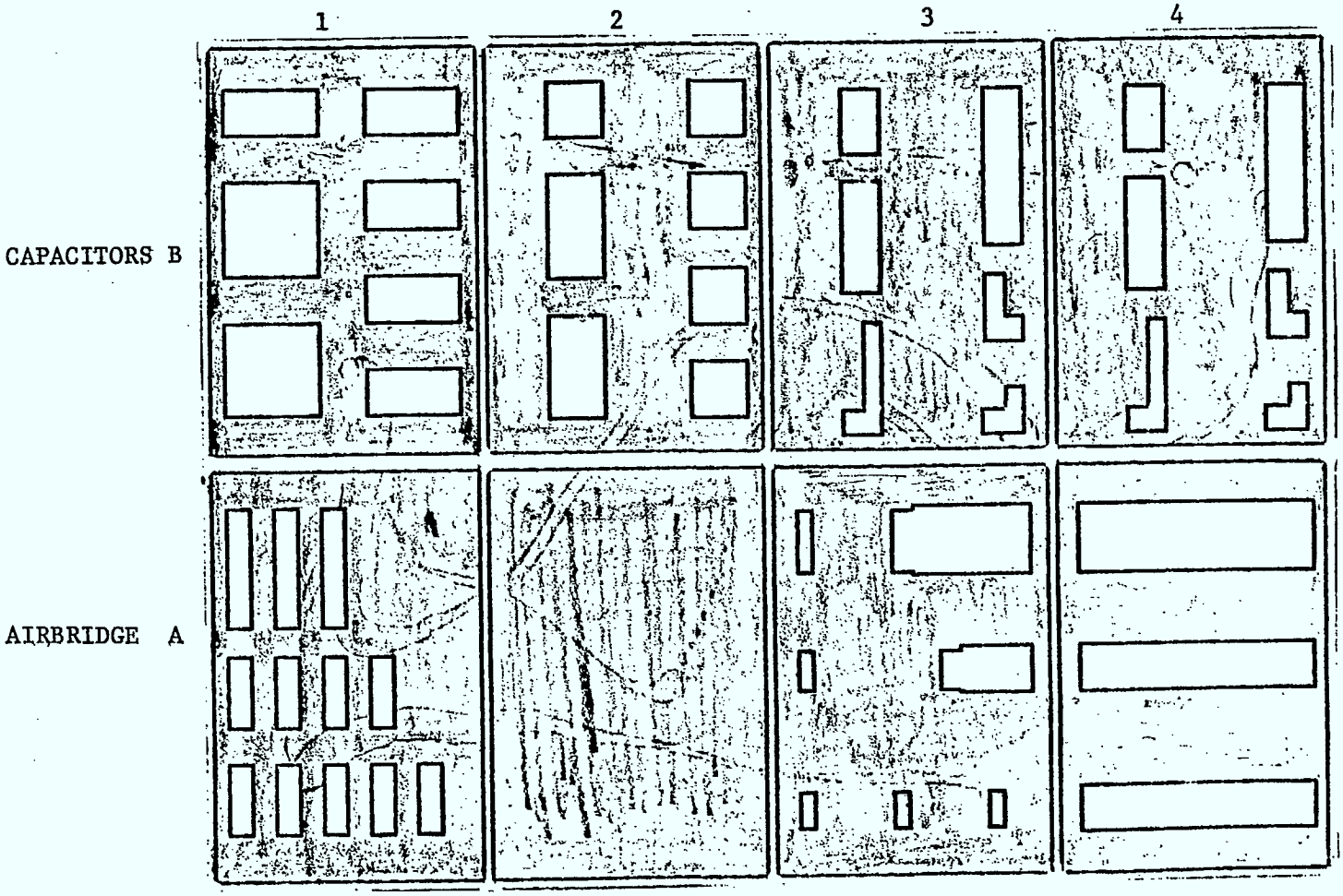


Fig. F1

Since positive photoresists are used throughout the processing it is possible to avoid using a lift off procedure at this stage by reversing the sense (i.e. positive or negative) of column 2 of Fig. F1. This implies laying down 6000Å of Si_3N_4, and etching away unwanted portion in a dry etch (CF_4+O_2) after blanking off the capacitor region with positive photoresist. This is the procedure being used to fabricate the mask set in Fig. F2. Both the positive and negative of the final mask have been generated. In Fig. F1, the next mask set (column 3) is used to expose the first layer metal or dielectric which is to be plated onto. A layer of 500Å Ti and 200Å AuGe covers the

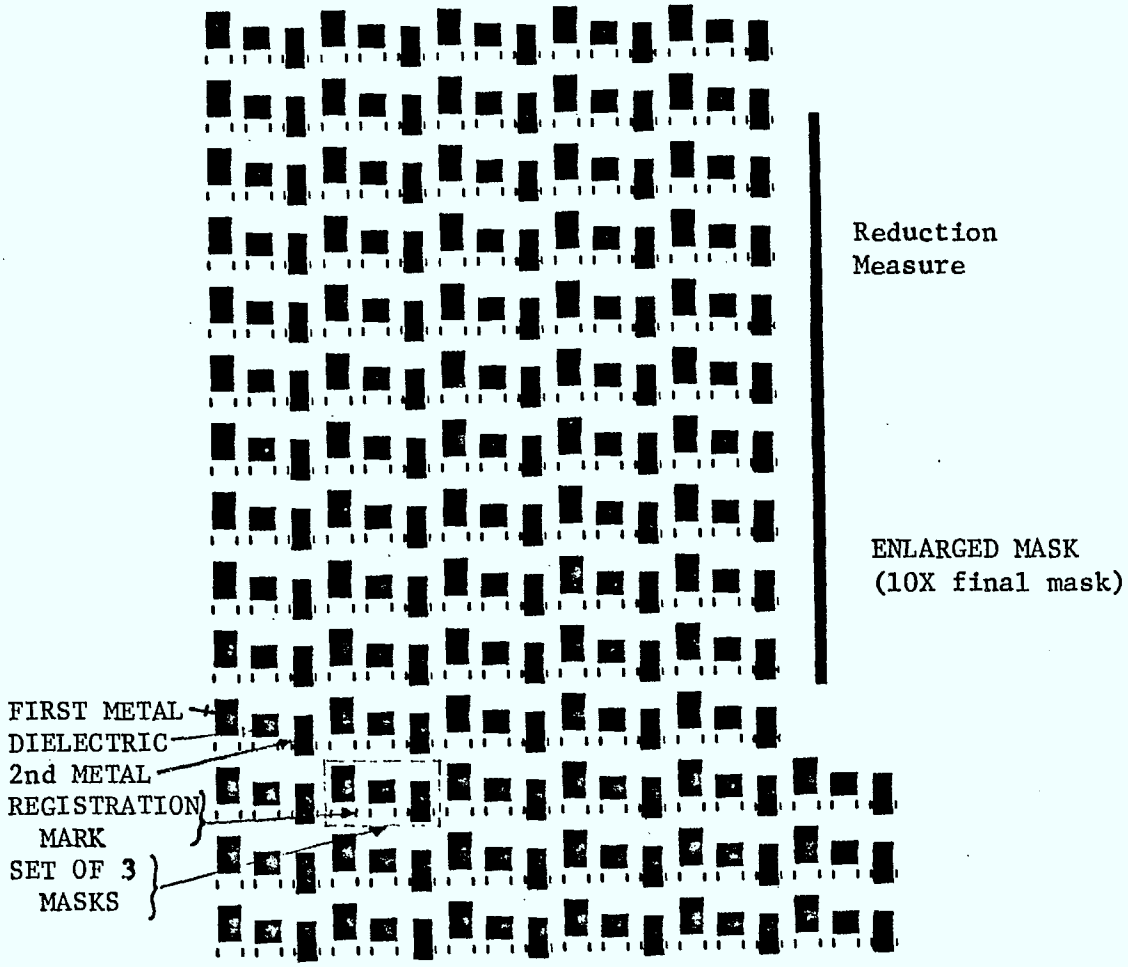
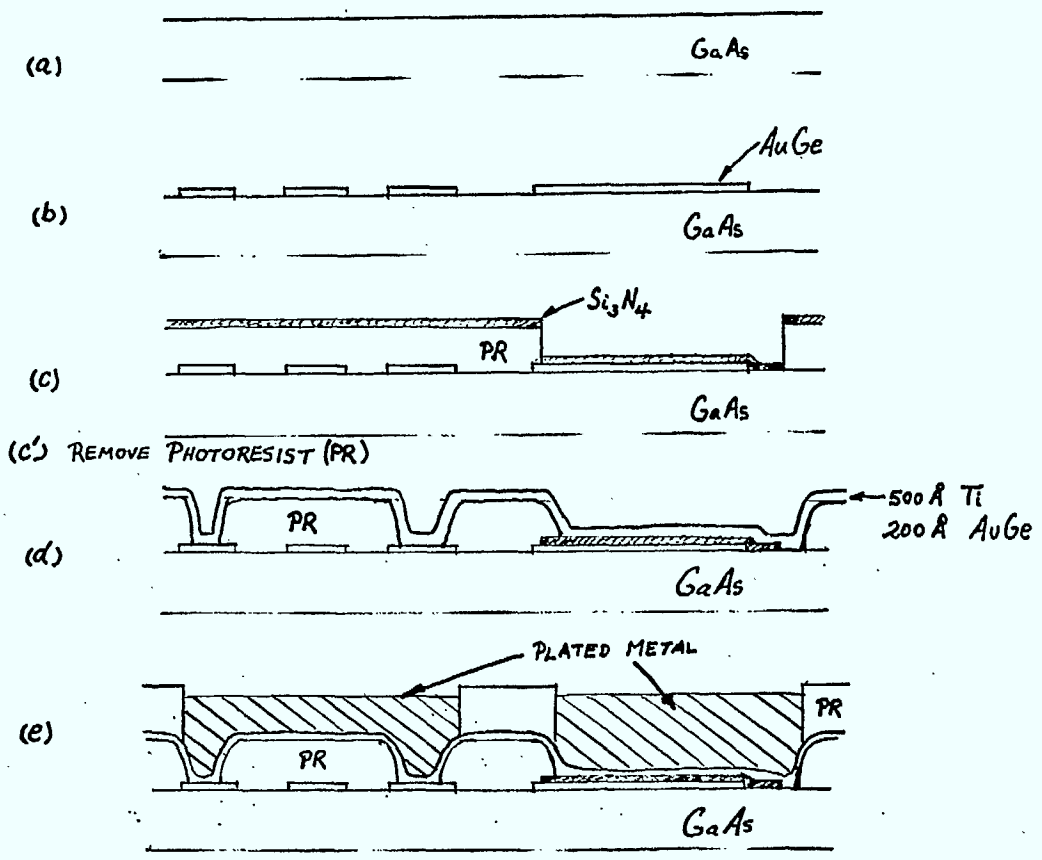


Fig. F2 Negative of the overlay capacitor test mask. This reduction has been done locally by Colorgraphics. In the final mask the reduction measure is 0.3 inches.

resist and holes and forms the contact for plating. A second layer of photoresist and mask 4 defines the area of plating. Fig. F3 diagrams the process. Problems have arisen due to an inadequate plating solution and contact problems of the first layer of metal with the plating layer. Recent experiments using oxygen plasma etching of the polymide P12550 has produced



(f) -top photoresist is removed
-followed by a light Au($3HCL+1HNO_3$) and Ti(type TFT;Transene Co. inc) etch
-lower layer of photoresist is removed

Fig. F3

a possible solution to this problem. Fig. F4 illustrates an oxygen plasma etch (white area-polymide-dark area substrate) where the polymide has been etched back 3 μm forming a ramp structure to the plateau area from the substrate. This will ensure continuity of the plating layer. Fig. F5 illustrates a 300Å layer of AuGe on the polyimide and is notable for the smoothnes of the metal layer (unlike the metal on AZ1350J which had a ridged appearance Fig. F6). The problem

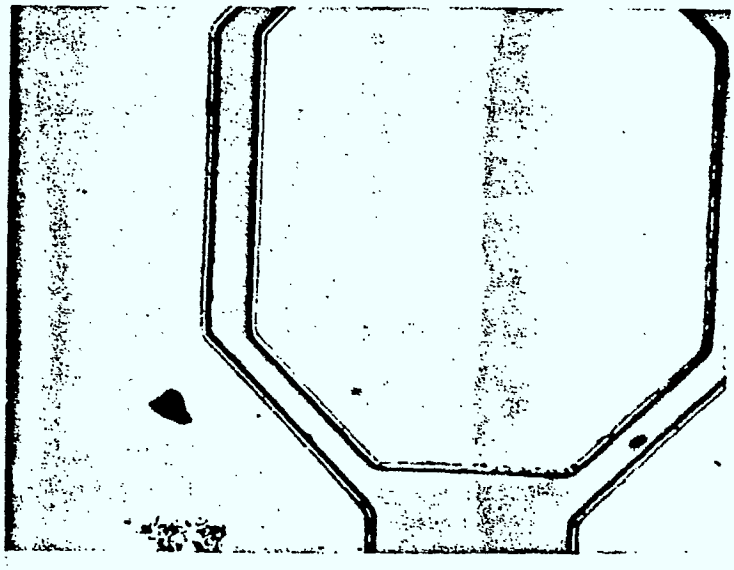


Fig. F4-O_2 plasma etch of photoresist and polyimide (290 scc O_2, pressure 3000 microns, power 250 W, time 30 minutes)
It is recognized that this might be an inverted cut in which case a wet etch would have to be made to achieve the desired result.

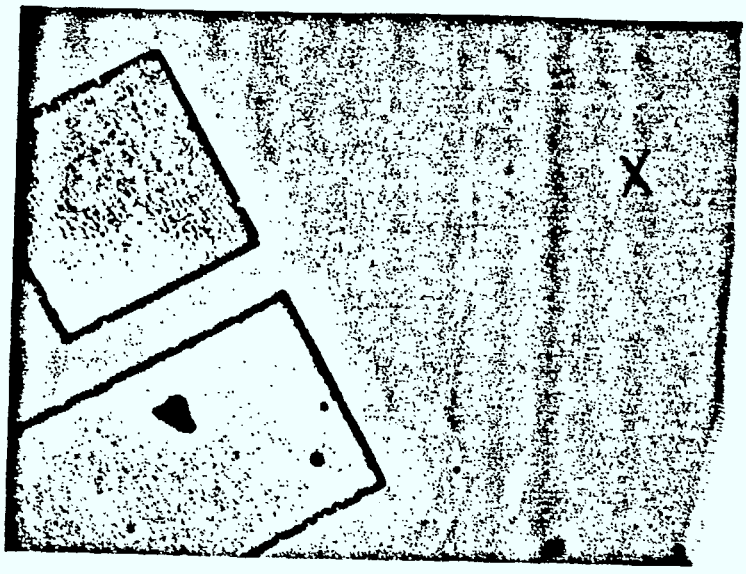


Fig. F5-AuGe on Polyimide the metal film is mark with an X in the photo.

of undercutting the plating metal by removing the top and bottom layer of photoresist at the same time is bypassed by using a polyimide as the first layer. To etch out the polyimide in the last step KOH or tetra-alkyl ammonium hydroxide should be used. The PI2550 is a very viscous material and must be mixed in even proportions with the pyrolin thinner T-9035 to obtain a film which is uniform after a 5000 rpm spin. The holder for the plating is illustrated in Figure F7.

Fabricated passive elements in the form of spiral inductors and interdigitated capacitors are illustrated in Fig. 8. The capacitance of the interdigitated structure is calculated from theory in Table F2 for some of the fabricated units. The theoretical inductance of the illustrated spiral inductor is 2.39 nH. The measurement of the passive elements over the

frequency range of interests (10-15 GHz) has not performed yet due to

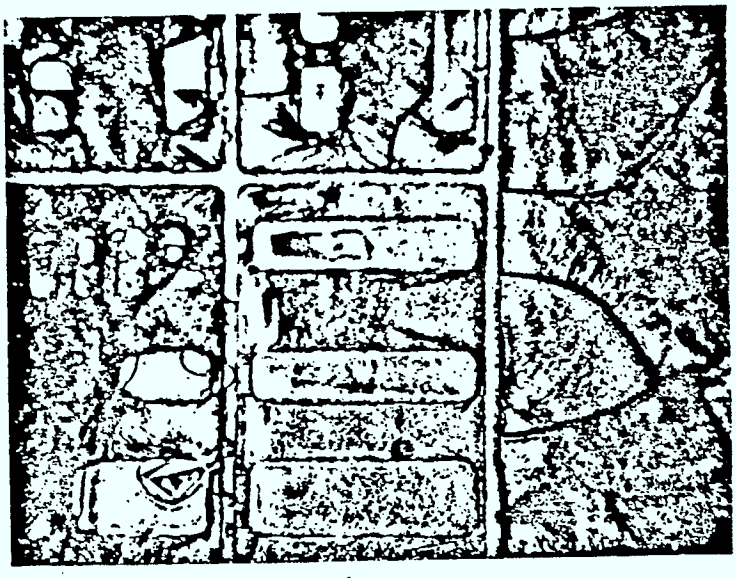


Fig. F6

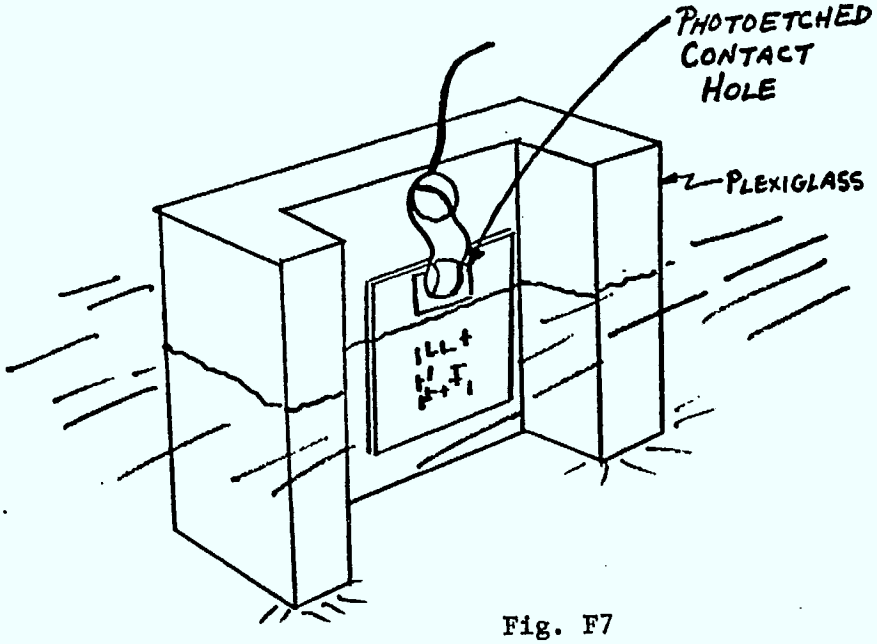
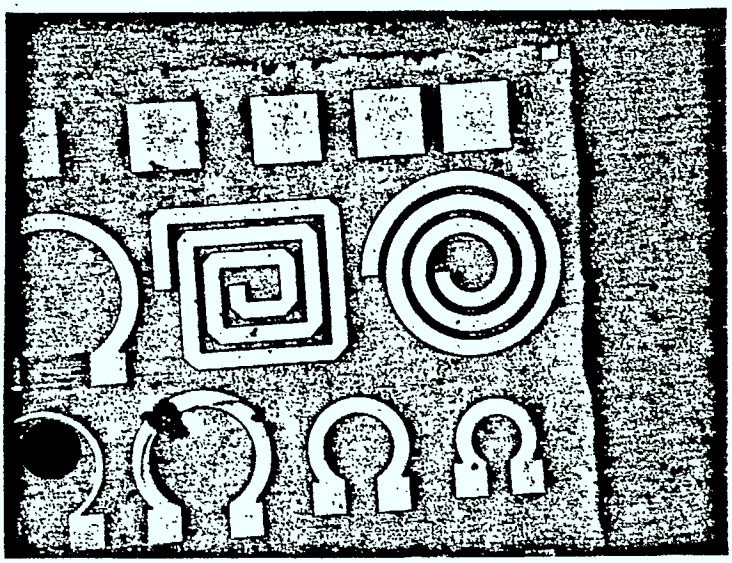


Fig. F7

Number of Fingers	Length of Fingers (mm)	Capacitance [pF] Theory
6	.6	.217
16	.32	.308
26	.16	.250
10	.16	.093

Table F2



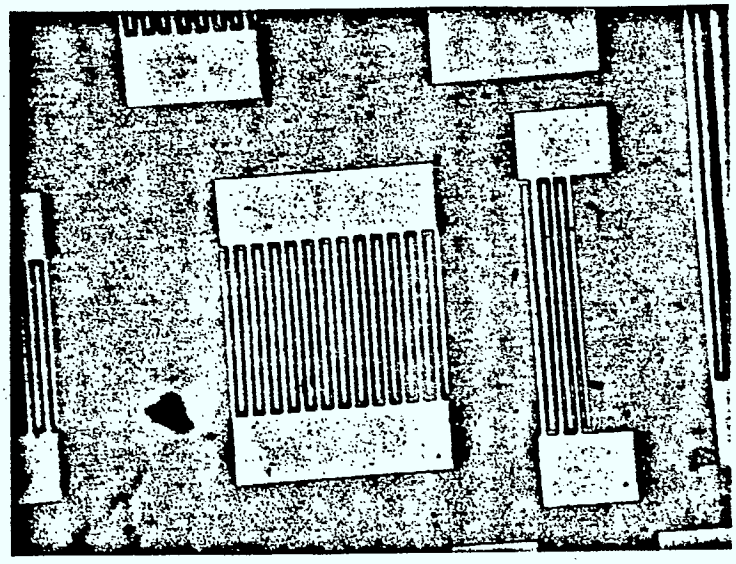


Fig. F8-4 micron fingers
and 4 micron spaces. for the
interdigitated capacitors
It is recognized that even finger
width and finger spacing does
not provide optimum capacitance.

previous commitments of the test jigs to active elements and the only recent availability of the 18 GHz network analyzer.

The scarcity of GaAs wafers and their fragile nature has led to the construction of the wafer holder illustrated in Fig. F9. The uniform perimeter pressure applied by the aluminum foil eliminates breakage when inserted into the daisy wheel in the metal evaporation system. The unit is

designed for half inch square wafers but could be adjusted by making a larger holding frame to take a smaller wafer size.

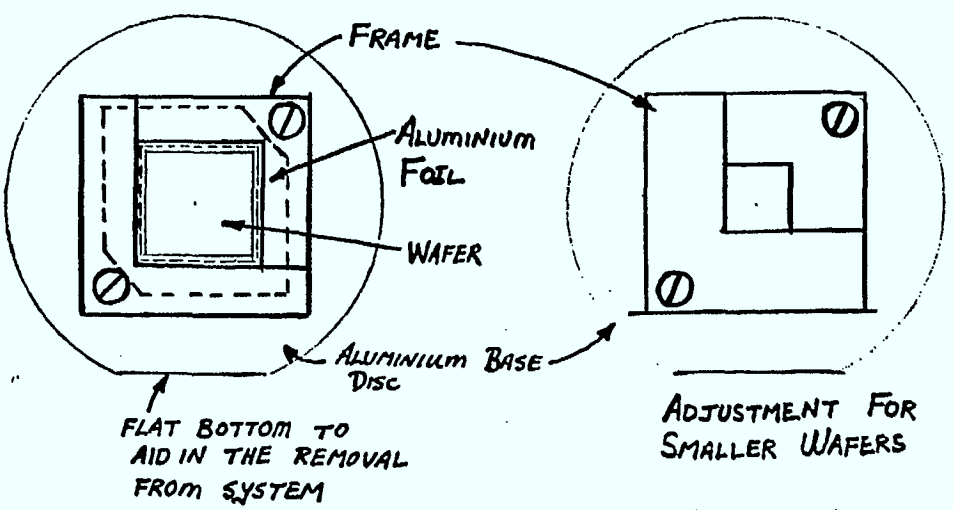


Fig. F9

Due to the smallness of the wafers, dicing is accomplished by wax bonding the wafer to a silicon blank and scribing the resulting unit on the tempress diamond scribing unit. The scribed unit is removed from the silicon blank by melting the wax and then broken by placing between two sharply curved aluminum sheets. Typical sizes of finished units are one millimeter by two millimeters with a .5 mm thick wafer.

The 3 μm gate active elements were fabricated from the mask set illustrated in Fig. F10. The next set of masks in the process of being fabricated (Fig. F11) have a smaller source drain spacing, an upper alignment

TEST PATTERN-2 GaAs

PLATE 1

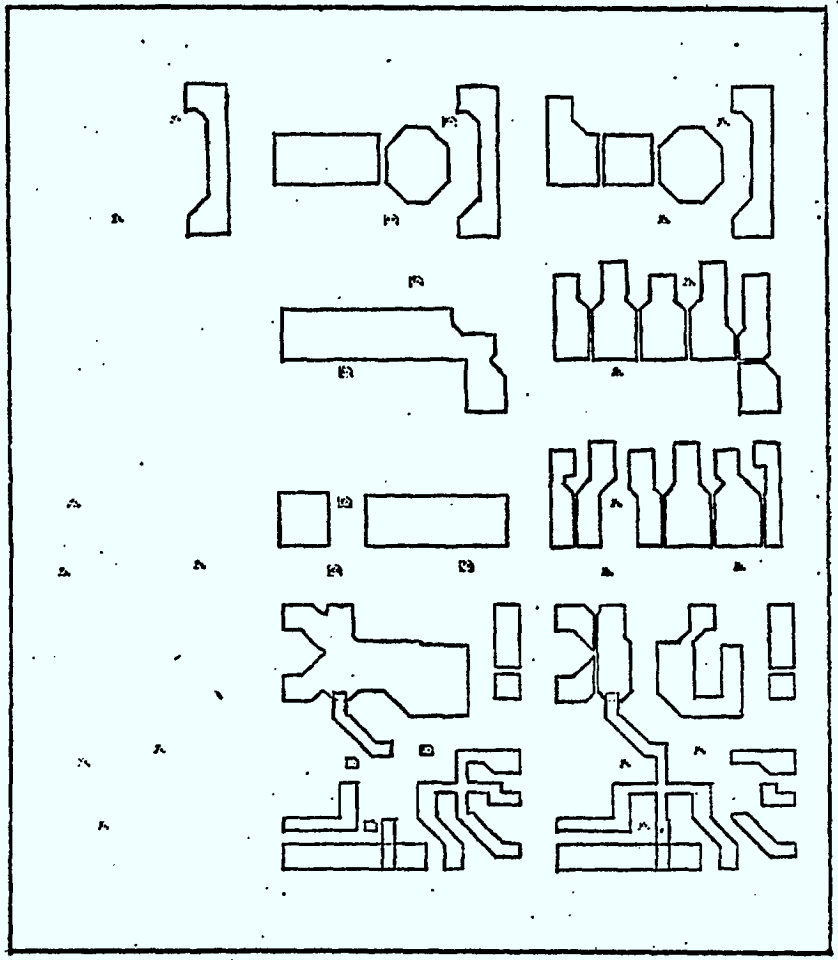
PLATE 2

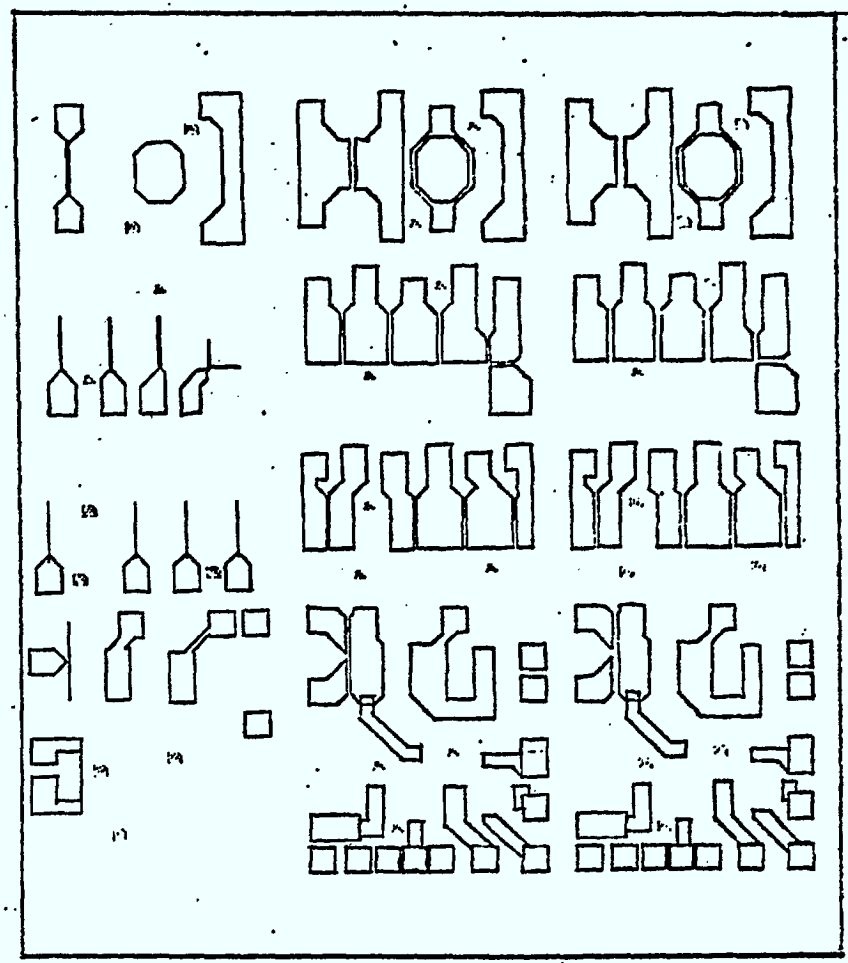
DUAL GATE - 4μm MESFET + CAPACITOR

MESFETS 6, 8, 10 μm GATES + 4μm CENTER FEED

MESFETS 1, 2, 3, 4 μm GATES

SUBSTRATE TEST PATTERN





REGISTRATION MARKS

n REGIONS

n^+ REGIONS

GATE METAL

OHMIC CONTACTS

SOURCE - DRAIN METAL

Fig. F10

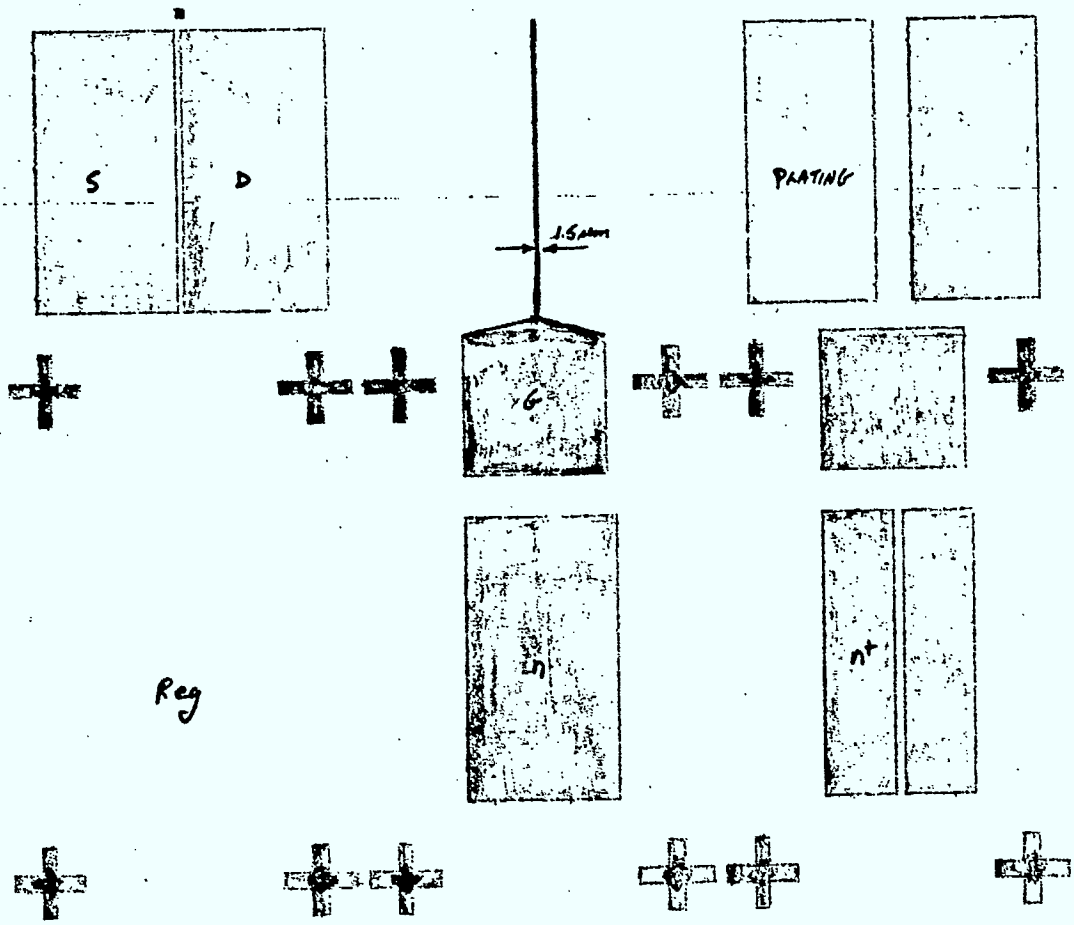


Fig. F11-Negative of actual mask

mark to offset the gate toward the source, a 1.5 μm gate length, and a longer extension of gate metal past the implanted region.

The gate recess etchant to be used to set the pinch off voltage is diglycolic acid (5 parts by routine $(CH(OH)COOH)_2$ + 1 part H_2O_2 at 26.5°C gives 100Å/2).

There have been a considerable number of problems wire bonding to the Al contact pads. All successful efforts up to the present time have been through ultrasonic bonding. Future changes in the gate metal and use of the thermal bonder should alleviate these problems. (Stage temperature - 225°C - tip temperature 150°C bonding force between 30 and 40 grams).

Die attachement is essential in future MMIC since a conducting bond is required for the microstrip lines. This is accomplished using a 300°C base temperature and a 80/20 gold/tin (25 μm thick) slab between base and chip.

Design

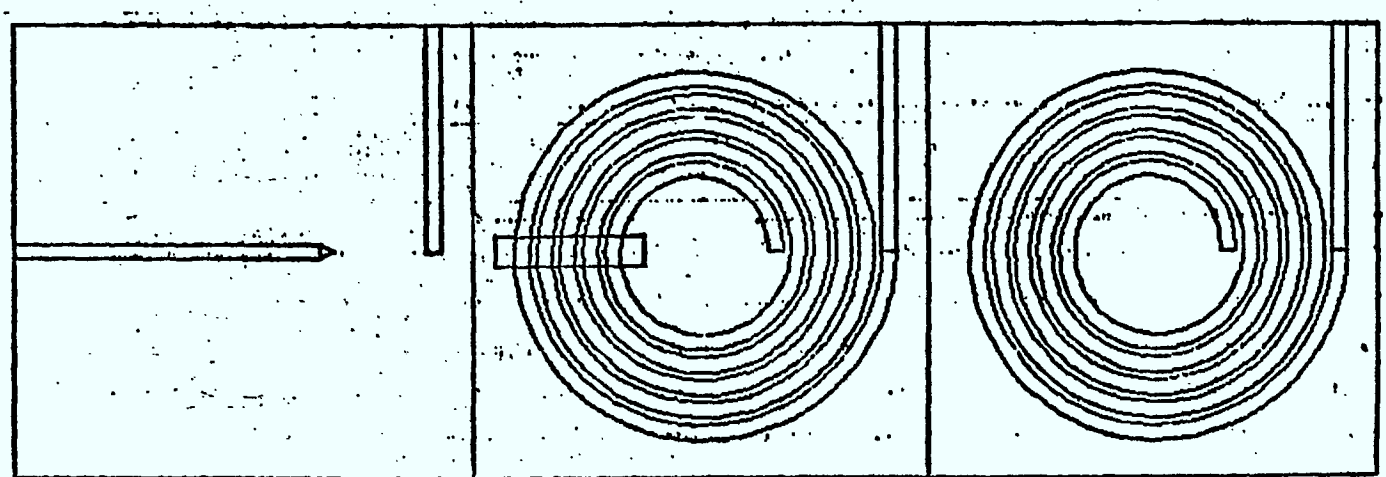
A number of computer programs have been written to aid in the fabrication and analysis of monolithic microwave integrated circuits.

The file 'SKETCH' contains sixteen subroutines which generate the artwork for microwave circuits on rubylith. Interdigitated capacitors, spiral inductors, Lange couplers, and rectangular spiral inductors are among the specialized units generated by this file. The re-sorting routine (sorts into vertical, horizontal, and skew cuts) and a check plot routine (acts on sorted or unsorted data) operate directly on the cutter data. The double layer metalization process, needed to connect multiple sources in parallel gate FET structures, overlay capacitor second metal with first metal lines, and spiral inductor leads to the external circuit, is illustrated, using the SKETCH subroutines, in Fig. C1. One of the advantages to using rubylith is seen in MASK 2 where simply the non stripping of the rubylith within the bridge area allows for an arbitrary exit from the spiral. The rectangular spiral routine has user declared truncated corners to avoid excessive capacitances. One of the major differences between MMIC and LSI graphics is the lack of square corners in the former masks.

A second file 'AMP' consisting of twenty five subroutines, has been created to aid in the analysis of the network analyzer data, synthesize models, and produce a data format which may be easily read into the MCAP program. An example of the raw data, for a single test jig mounted device, at one bias point and over a range of frequencies, is given in Table C1. Applying the subroutines to the 2 GHz component generates the analysis found in Table C2. The device data was converted to rectangular form, de-embedded

```
CALL SPIRAL(9.0,3.0,2.5,1.0,0.2.5,1.0,0.0,0.0,0.0)
CALL SPIRAL(15.0,3.0,2.5,1.0,( 2.5,1.0,0.0,0.0,0.0)
CALL RECT(2.0,3.0,4.0,0.2,0.0,0.0)
CALL RECT(5.5,4.5,0.2,3.0,0.0 0.0,0.0)
CALL RECT(5.5,4.5,0.2,3 0,6.0,0.0,0.0)
CALL RECT(5.5,4.5,0.2,3.0,12.0,0.0,0.0)
CALL RECT(7.25,3 0,2.0,0.4,0.0,0.0,0.0)
CALL RECT(9.0,3 0,18.0,6.0,0.0 0.0,0.0)
CALL BOX(9.0,3.0,2 0,0.0,0.0,0.0)
CALL LINE(4.0,2.9,4.1,3.0,0.0,3.0)
CALL LINE(4.1,3.0,4.0,3.1,0.0,3.0)
CALL HALT
CALL DRAW
CALL PLOTRL('SEND',0)
STOP
END
```

PROGRAM WHICH GENERATED SPIRAL INDUCTANCE EXAMPLE



LAYER OF POLYIMIDE PUT DOWN

FIRST METALIZATION LAYER

CUT THROUGH POLYIMIDE

NOTE: SPIRAL WHICH IS INSIDE THE LARGE RECTANGULAR BOX IS NOT REMOVED FROM THE RUBYLITH

SECOND METALIZATION LAYER

THREE MASK LAYERS FOR A SPIRAL INDUCTOR

Fig. C1

vds=3 vgs=-3

FREQUENCY	RETURN LOSS-IN S11		LOSS-FORWARD S21		LOSS-REVERSE S12		RETURN LOSS-OUT S22	
MHz	DB	ANG	DB	ANG	DB	ANG	DB	ANG
2000	2.1	47	3.5	-177	24.1	152	1.2	60
3000	4.5	-97	4.1	10	20.4	9	1.6	-86
4000	6.1	130	5.1	-156	16.5	-136	1.9	122
5000	6.7	-2	5.7	33	11.7	59	3.4	-27
6000	6.5	-146	6.0	-117	9.7	-98	5.8	-172
7000	6.9	99	4.9	58	4.0	72	15.5	-176
8000	3.6	-48	7.5	-111	6.2	-113	3.8	-14
9000	4.3	157	8.2	95	7.4	85	3.2	-170
10000	11.7	9	7.0	-80	6.8	-91	6.1	50
11000	3.2	-59	13.8	81	14.2	66	3.0	-61
12000	1.6	143	33.8	-10	42.4	48	1.8	156
13000	1.6	-22	13.3	-83	13.5	-90	1.7	10
14000	3.5	-160	12.2	52	14.2	31	3.4	-119
15000	3.0	16	15.8	-104	17.5	-55	4.1	45

TABLE C1 TYPICAL OUTPUT FROM AUTOMATIC NETWORK ANALYZER

FREQUENCY= 2.000 (GHZ)

S11=0.8479 -.3116
S12=0.1593E-01 0.4825E-01
S21=-.4372 0.3107 RECTANGULAR COORDINATES
S22=0.8693 -.1378

DELTA=0.8067 K= 1.104

TRANSDUCER POWER GAIN IN 50 OHM SYSTEM=-5.411 (DB)
TRANSDUCER POWER GAIN FOR ZS AND ZL GIVEN=-5.411 (DB)
UNILATERAL TRANSDUCER POWER GAIN=-5.411 (DB)
POWER GAIN WITH INPUT CONJUGATE MATCH= 1.942 (DB)
POWER GAIN WITH OUTPUT CONJUGATE MATCH= 1.060 (DB)
MAXIMUM AVAILABLE POWER GAIN= 8.272 (DB)
MAXIMUM UNILATERAL POWER GAIN= 8.412 (DB)
MAXIMUM STABLE POWER GAIN= 10.23 (DB)
UNILATERAL POWER GAIN= 7.935 (DB)

-3.65 < G/GUMAX < 6.42 (READINGS IN DB)

GAMMA IN =0.8479 -.3116
GAMMA OUT =0.8693 -.1378
GAMMA IN OF MATCHED INPUT =0.8376 0.4196
GAMMA OUT OF MATCHED OUTPUT =0.8782 0.2753
GAIN OF MATCHED CIRCUIT = 6.717 OR IN DB 8.272
CENTER OF LOAD CIRCLE = 1.182 0.3706 OR IN R,A 1.239 17.41
RADIUS OF LOAD CIRCLE =0.2202
CENTER OF SOURCE CIRCLE = 1.055 0.5283 OR IN R,A 1.180 26.61
RADIUS OF SOURCE CIRCLE =0.1650
ZIN MATCHED NORMALIZED=0.6048 4.145
ZOUT MATCHED NORMALIZED= 1.688 6.075

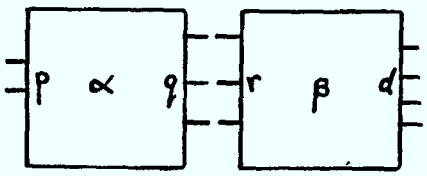
S11=-.8829 -20.18
S12=-25.88 71.73
S21=-5.411 144.6
S22=-1.109 -9.005

Db/ϕ

PRELIMINARY ANALYSIS USING AMP FILE
(the data has been deembedded from the test jig)
(only the 2 GHz analysis is shown)

TABLE C2

BLOCK DIAGRAM OF PORT LABELING



STATUS

beta component

$$\begin{bmatrix} b_r \\ b_d \end{bmatrix} = \begin{bmatrix} S^{\beta}_{rr} & S^{\beta}_{rd} \\ S^{\beta}_{dr} & S^{\beta}_{dd} \end{bmatrix} \begin{bmatrix} a_r \\ a_d \end{bmatrix}$$

S beta KNOWN OR PREVIOUSLY MEASURED

gamma component
(gamma=alpha+beta)

$$\begin{bmatrix} b_p \\ b_d \end{bmatrix} = \begin{bmatrix} S^{\gamma}_{pp} & S^{\gamma}_{pd} \\ S^{\gamma}_{dp} & S^{\gamma}_{dd} \end{bmatrix} \begin{bmatrix} a_p \\ a_d \end{bmatrix}$$

S gamma MEASURED

alpha component

$$\begin{bmatrix} b_p \\ b_q \end{bmatrix} = \begin{bmatrix} S^{\alpha}_{pp} & S^{\alpha}_{pq} \\ S^{\alpha}_{qp} & S^{\alpha}_{qq} \end{bmatrix} \begin{bmatrix} a_p \\ a_q \end{bmatrix}$$

S alpha TO BE CALCULATED

If one assumes d=q and there are no p ports then the S alpha matrix reduces to S^{α}_{qq} where

$$S^{\alpha}_{qq} = (NS^{\beta}_{rr} + 1)^{-1} N$$

$$N = S^{\beta}_{dr}{}^{-1} (S^{\gamma}_{dd} - S^{\beta}_{dd}) S^{\beta}_{rd}{}^{-1}$$

Note: the above notation is abbreviated; S and N are matrices

Fig. C2 Simplification of Guptas General Desegmentation Form.

(Fig. C2), then analyzed. All routines have been cross checked with known examples.

The response of MMIC's is very sensitive to the distributed and/or lumped matching network, thus a general program for evaluating circuit performance was needed. The Microwave Circuit Analysis Program (MCAP-GUPTA#) has been adapted for general use. The number of ports has been extended to a maximum of 100 and the number of components to 50. A datafile arranging program MRESORT takes the data in the format free manner of Table C3 and generates the input data structure for MCAP. The output from MCAP is the VSWR of each external port, their complex S parameters, and the magnitudes of the S parameters at the frequencies specified. An example of using this program is given in Fig. C3 and Fig. C4. A notable point about this program is its ability to read in internally declared S parameters thus allowing parallel, series, and hybrid circuit structures. An example is given in Fig. C5. It is recognized that transferring the S parameters to Z,Y,G or H, depending upon the circuit structure, adding the converted matrices and transferring back to S parameters produces the same results for these specialized circuits. This is inconvenient for the programs being used. Short circuits may be created by external declaration or by the appropriate choice of shunt admittance.

#GUPTA - computer aided design of microwave circuits - 1981.

Line Number	Data(Defined in table C4)
1	:M,N,L
2	:A1,A2,A3,A4
3	:TITLE OF THE PROBLEM
4	:1 or 0 1 if microstrip,0 if stripline
5(1)	:B1,B2,B3,B4,B5,B6,B7,B8,B9,B10
.	: :
.	: .
.	: .
5(M)	: .
6	:I
7(1)	:C1,C2
.	: .
.	: .
.	: .
7(N)	: .
8	:D1,D2,D3,D4,D5,D6
9(1)	:J,S matrix
.	: .
.	: .
.	: .
9(L)	: .

Note; the ':' does not appear in the file and is inserted in the above format to indicate the beginning of file line.

TABLE C3

MEANING OF THE SYMBOLS IN TABLE C3

M(integer).....number of components in the circuit

N(integer).....number of interconnections in circuit

L(integer).....number of S matrices declared

A1(real).....distance between ground planes in the stripline configuration(meters)

A2(real).....thickness of microstrip(meters)

A3(real).....dielectric constant of the substrate

A4(real).....thickness of substrate(meters)

component declaration

- B1(character).....name of element
- B2(integer) to B5(integer)....port numbers of device
- B6(character).....type of device...SA shunt admittance
  SI series impedance
  TL transmission line
  SW step in width
  GS gap in strip
  BS bend in strip
  RH round hole
  TJ T junction
  OE open end
  MT matched termination
  SP EXTERNALLY SPECIFIED S MATRIX
  CL coupled line section
- B7(real) to B9(real)...numerical values of devices
- B10(character).....device parameter type selection ie)width or impedance of the strip specified

I(integer).....number of external ports

C1,C2(integers).....C1 port is connected to C2 port

D1(character).....specifies frequency units

D2(character).....specifies if discontinuities are considered

D3(real).....starting frequency

D4(real).....end frequency

D5(real).....frequency increment

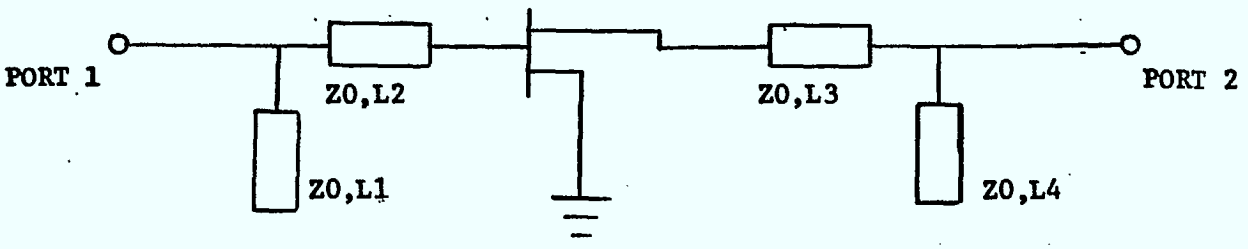
D6(character).....log or linear scale for incrementing

J(integer).....dimension of S matrix(less than 5)

S(complex matrix).....S matrix example: 0.1,0.9,0.1,0.01
0.1,0.5,0.1,0.9

TABLE C4

TEST OF 6 GHz CIRCUIT



Z0=50 ohms
L1=0.3518 radians
L2=0.6095 radians
L3=1.8033 radians
L4=1.2817 radians

S Matrix(at 6 GHz) 0.614/-167.4 0.046/65
2.187/32.4 0.716/-83

Redrawn Circuit

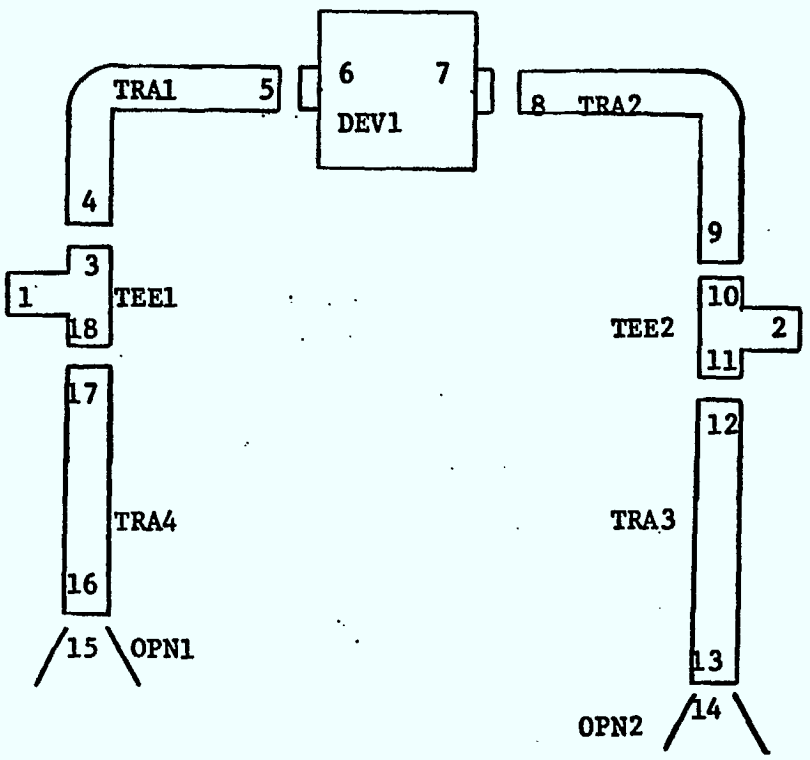


Fig. C3

INPUT TO MCAP FOR THE 'TEST OF 6 GHz CIRCUIT'

(this data is actually resorted by MRESORT before being fed to MCAP)

```
9,8,1
2.0,5.0E-04,9.8,0.635E-02
TEST OF 6 GHZ CIRCUIT
1
TEE1,18,3,1,0,TJ,50.0,50.0,0.0,0
TEE2,10,11,2,0,TJ,50.0,50.0,0.0,0
TRA1,4,5,0,0,TL,50.0,0.3518,6.0E09,R
TRA2,8,9,0,0,TL,50.0,0.6095,6.0E09,R
TRA3,12,13,0,0,TL,50.0,1.8033,6.0E09,R
TRA4,16,17,0,0,TL,50.0,1.2817,6.0E09,R
OPN1,15,0,0,0,OE,50.0,0.0,0.0,0
OPN2,14,0,0,0,OE,50.0,0.0,0.0,0
DEV1,6,7,0,0,SP,0.0,0.0,0.0,0
E
3,4
5,6
7,8
9,10
11,12
13,14
15,16
17,18
F,N,6.0E09,6.0E09,1.0E09,LIN
E,-0.5992,-0.13394,0.01944,0.04169
1.8465,1.1751,0.03726,-0.71066
```

OUTPUT FROM MCAP FOR THE 'TEST OF 6 GHz CIRCUIT'

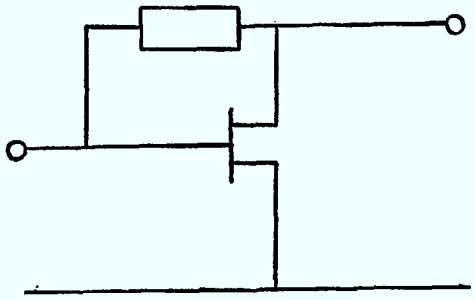
(the replication of the input data in the output is not shown)

```
DISCONTINUITY EFFECTS ARE NOT CONSIDERED

                5.999997E+09HZ

   EXTERNAL S-MATRIX FOR ELEMENT NUMBER  9 IS
-0.59900E+00  -0.13400E+00    0.19400E-01   0.41700E-01
 0.18500E+01   0.11800E+01    0.67300E-01  -0.71100E+00
 S-MATRIX FOR THE OVERALL CIRCUIT IS
 0.23670E-02   0.74486E-01    0.10484E+00   0.41702E-01
 0.52871E+01  -0.10112E+01   -0.41686E-02   0.62825E-01

  VSWR        -------MAGNITUDE OF S-PARAMETERS----
  1.16105     0.74525E-01                   0.11283E+00
  1.13439     0.53889E+01                   0.62963E-01
```

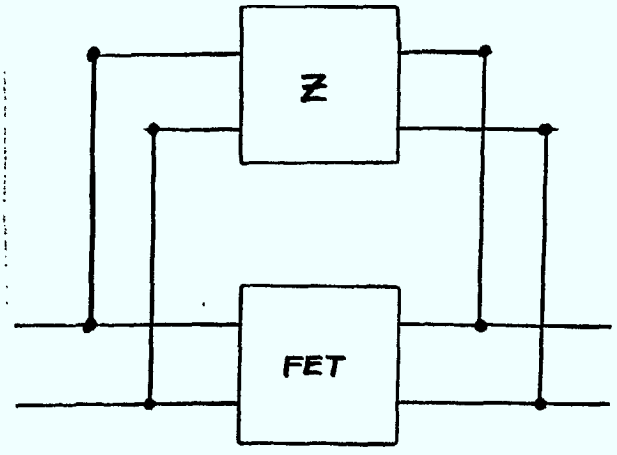
Fig. C4

A circuit optimization program from Advances in Microwaves (1974, pg. 385) is currently in the main frame but not documented due to lack of time.

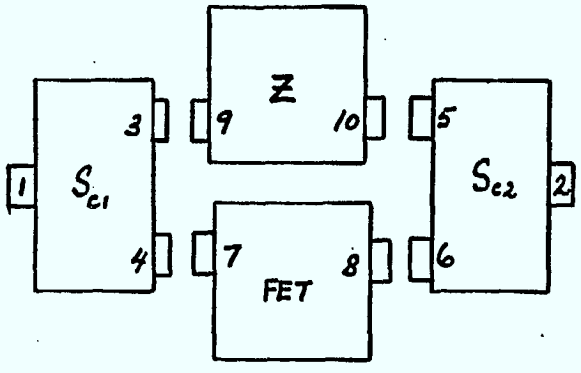
The object of the analysis program is to have a general means of evaluating the circuit performance given variations in the fabrication technique.



DESIRED STRUCTURE



EQUIVALENT STRUCTURE



PROGRAMMED STRUCTURE

Relevant Input To MCAP- Z and FET previously declared

connector	SC1,3,4,1,0,SP,0.0,0.0,0.0,0
S parameters	SC2,5,6,2,0,SP,0.0,0.0,0.0,0
declared	.
	.
	.
interconnections	
declared	3,9
	4,7
	10,5
	8,6

Fig. C5