THE UNIVERSITY OF BRITISH COLUMBIA

DEPARTMENT OF ELECTRICAL ENGINEERING

FINAL REPORT TO

DEPARTMENT OF COMMUNICATIONS, OTTAWA, ONTARIO

ON

# A STUDY OF MONOLITHIC MICROWAVE INTEGRATED AMPLIFIERS

CONTRACT SERIAL NUMBER OST83-00075

MARCH 31, 1984

REPORT PREPARED BY D.G. HUTCHEON

PRINCIPAL INVESTIGATOR L. YOUNG

**DEPARTMENT OF ELECTRICAL ENGINEERING**
**FACULTY OF APPLIED SCIENCE**
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ABSTRACT

This report describes the fabrication technique which was used to produce GaAs FETS of gate lengths between one and two microns. $Si^{28}$ ion implantation through an encapsulating $Si_3N_4$ film was used to produce the n and $n^+$ zones in LEC GaAs. Various process evaluation methods are illustrated in this report.

This is the first step in the technology definition procedure for the implementation of a GaAs I.C. capability.

FABRICATION

The first series of MESFETS were fabricated using direct ion implantation into bare GaAs. The registration marks were etched into the substrate and a photoresist was used as the implant mask. The problems with this procedure were the inability to remove the photoresist after the $n^+$ implant except by $O_2$ ashing and the destruction of the surface after the activation anneal (Photo 1).

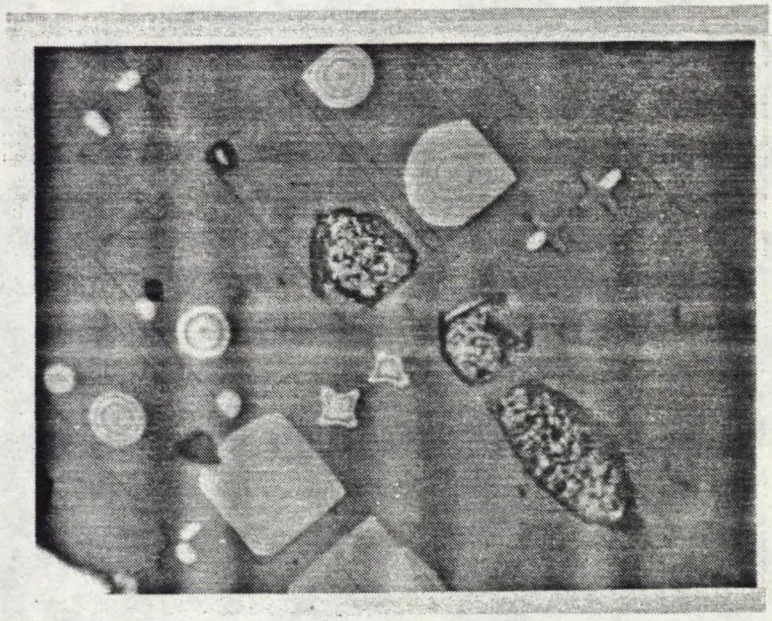
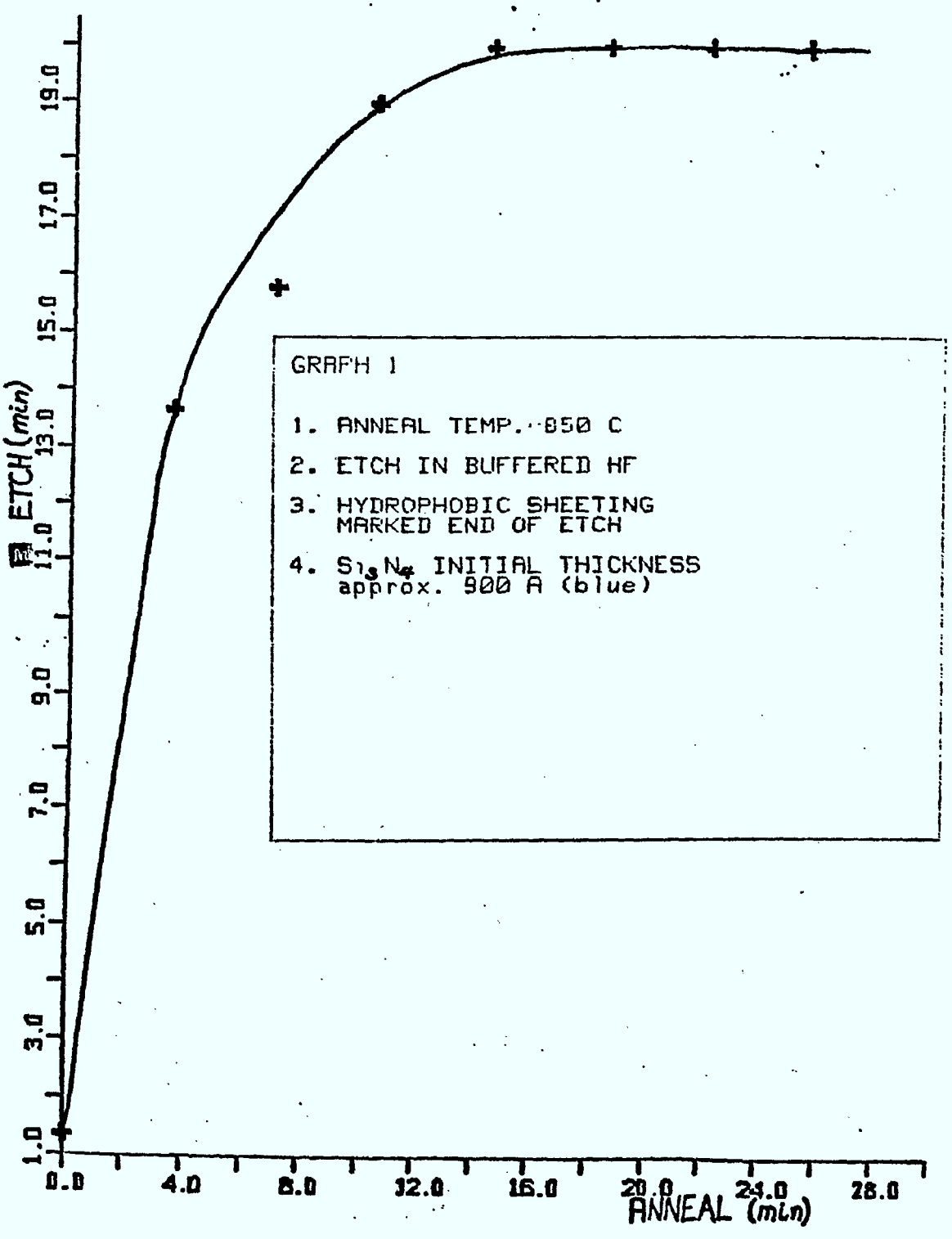


Photo 1: The ringlike patterns indicate the capping film has lifted but not separated. This destruction is highly correlated to the implanted zones.

The uncontrollable etch of the PECVD $Si_3N_4$ was solved when it was noted that the activation anneal changed the etch rate of the film (Graph 1). This change in the etch rate allowed the registration marks to be etched directly in the $Si_3N_4$ film. Enough control of the film etch was produced so that the




GRAPH 1

1. ANNEAL TEMP. - 850 C
2. ETCH IN BUFFERED HF
3. HYDROPHOBIC SHEETING MARKED END OF ETCH
4. $Si_3N_4$ INITIAL THICKNESS approx. 900 A (blue)

implants would take place through a thinned nitride surface. The contrast between the field and implant regions, for clear registration, was obtained by making the films blue (800 Å) and brown (400 Å) respectively.

The Mask Set

The mask set used for the majority of the FET fabrication is shown in photo 2a. The production of the plate from rubylith was done by Precision Photomask. The gate length is 1 μm and the gate width is 200 μm.

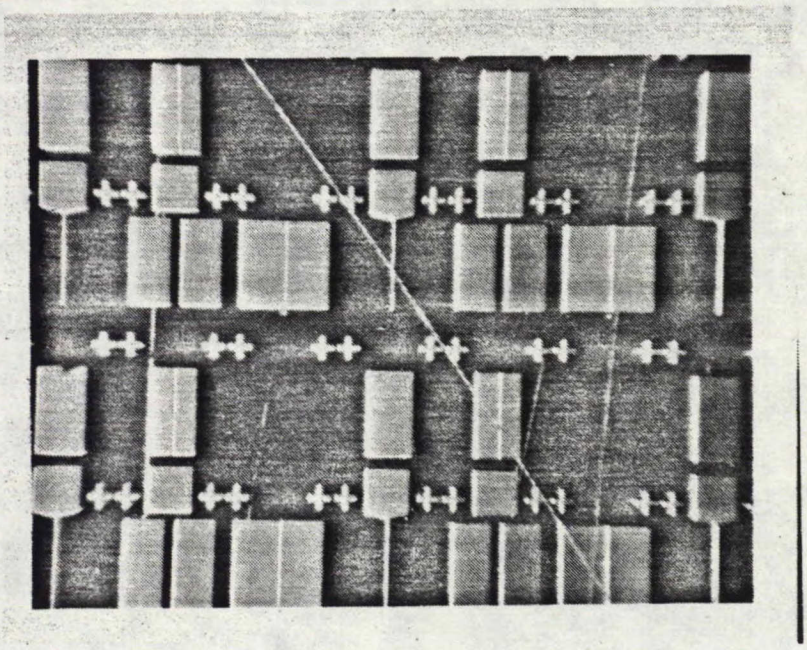


Photo 2 a

| SOURCE DRAIN | GATE | PLATING |
|---|---|---|
| BLANK | n | $n^+$ |

This pattern is stepped and repeated thus accounting for the extra images on the plate. The diagonal scratches come from usage in the contact aligner.

The source drain spacing was set to 5 μm. This proved to be too fine an alignment problem for the KASPER contact aligner as illustrated in photo 2b.

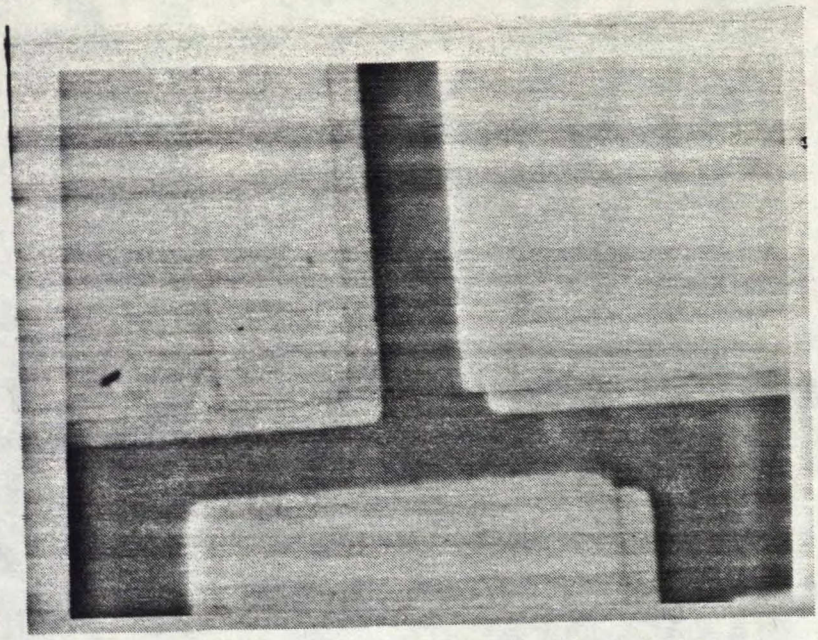


Photo 2 b: 3 μm misalignment of source drain pads and holes in $Si_3N_4$.

Better alignment could take place if the alignment marks had been changed to the pattern indicated in Fig. 1.

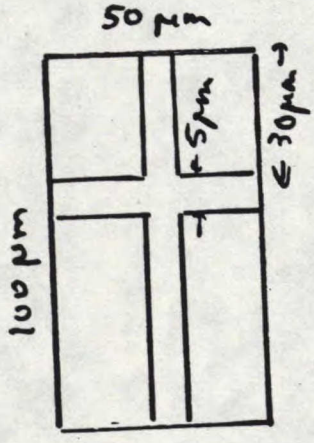
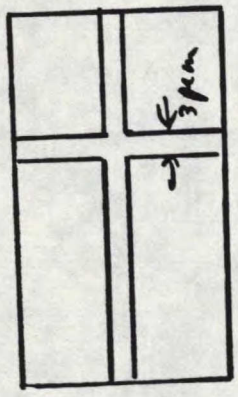



Fig. 1 Registration Mark in Nitride.




Registration marks in S-D, implant, and gate masks.

To compensate for the misalignment the plating mask had to be used for the $n^+$ and source drain metallizations. The gate plating pad could not be used under the gate pad during the $n^+$ implant and source drain metallization. The rotation of the plate by 180° corrected this problem but gave a misalignment to the registration marks. This 180° rotation can be seen in photo 3.

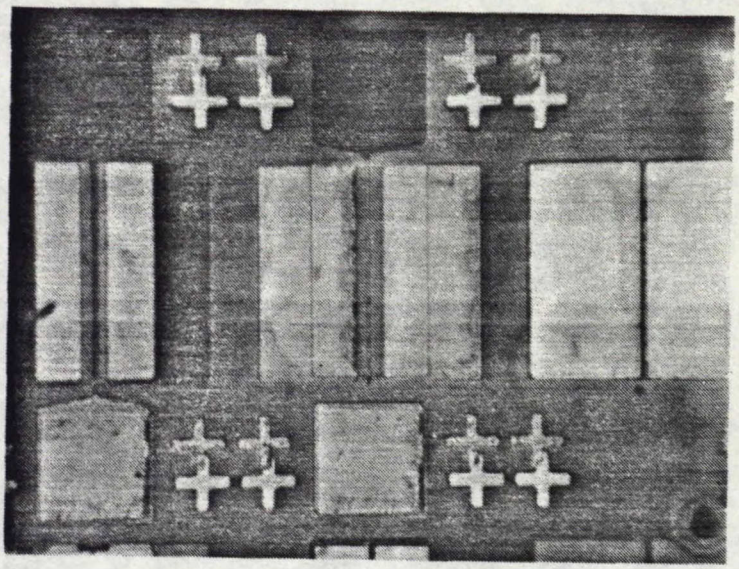


Photo 3: Source drain metal and gate etch completed.

FINAL FABRICATION SEQUENCE

With the ability to control the etch rate of the $Si_3N_4$ film the procedure adopted was an initial 740 Å coating of the GaAs wafer following a wafer clean. The wafer clean is very similar to one used by Rockwell (referenced by Gary Needham, Cominco). The wafer was baked at 850°C for 14.5 minutes to alter the etch properties. It was found that there was no visible deterioration of the surface after this procedure. The film was blue indicating a thickness of between 730 and 930 Å (refer to color chart Table 1). This turned out to be 800 Å according to the ellipsometer data.

| COLOR | $Si_3N_4$(Å) |
|---|---|
| SILICON | 0 - 200 |
| GOLDEN BROWN | 200 - 400 |
| RED | 550 - 730 |
| DEEP BLUE | 730 - 770 |
| BLUE | 770 - 930 |

Table 1

The implant zone was then etched with buffered HF($NH_4F$(40%):HF(49%),6:1) for 9 minutes. This gave a brown film indicating 200 to 550 Å. The ellipsometer measurement indicated 490 Å. Leo Lau (UWO Surface Science) ran a SIMS scan on the PECVD $Si_3N_4$ films which have been used throughout the fabrication sequence. The result is given in Fig. 2. This sample is $Si_3N_4$ over $S_i$. Fluorine (probably from the $CF_4$ clean) and oxygen show local maximums at the $Si_3N_4$/S: interface.

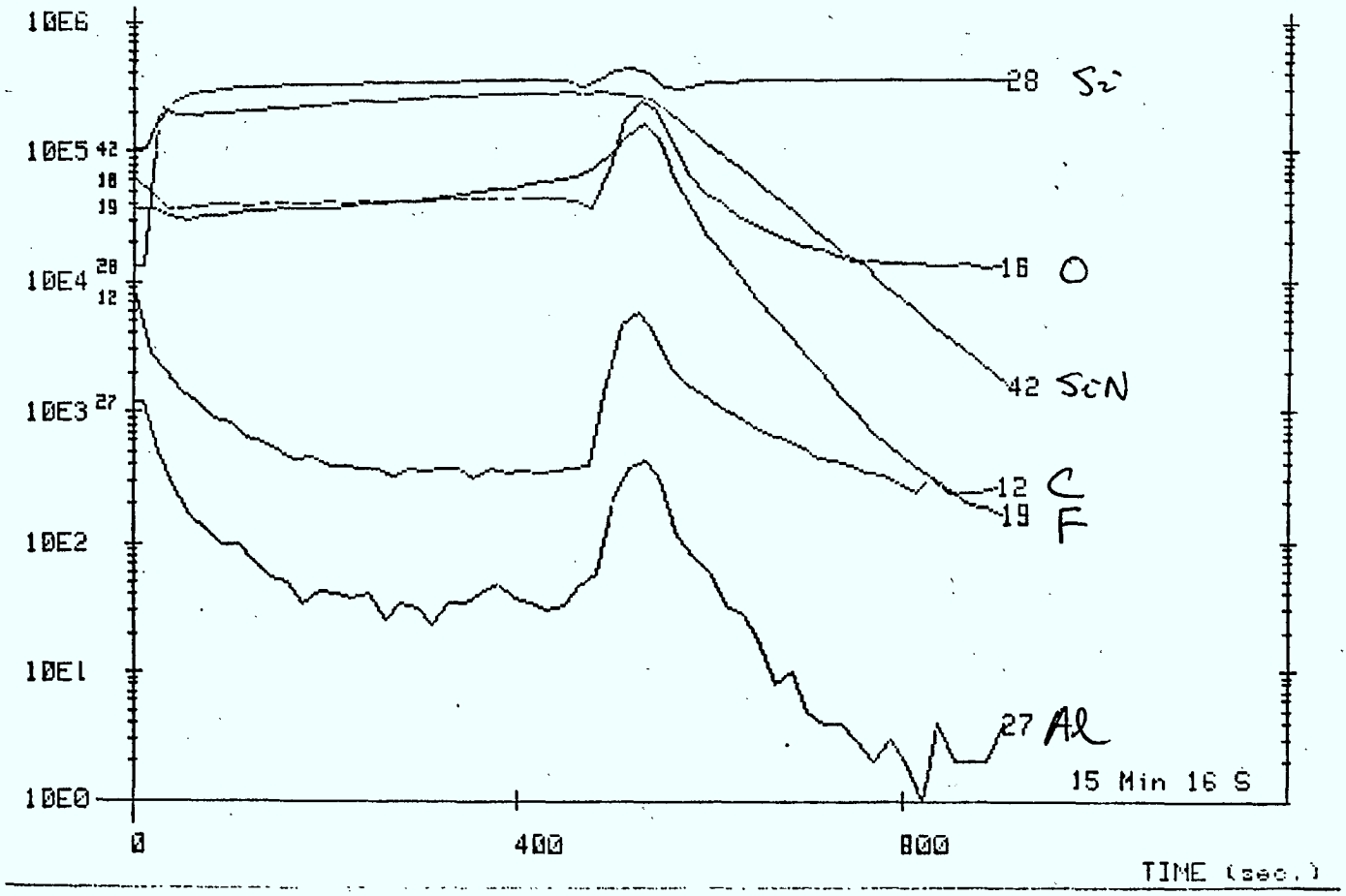



Fig. 2: SIMS on $Si_3N_4/Si$

Photoresist

The implant zone was defined in Shipley Microposit 1450J positive photoresist. The photoresist procedure begins with a 30 minute, 200°C prebake. This is followed by a 5 minute cooling period in a desiccator. The spin parameters for the photoresist application were 4000 rpm for 30 s. This procedure gives a film thickness of 1.8 μm. The cone illustrated in Fig. 3 was used to avoid the splashback of the expelled excess photoresist.

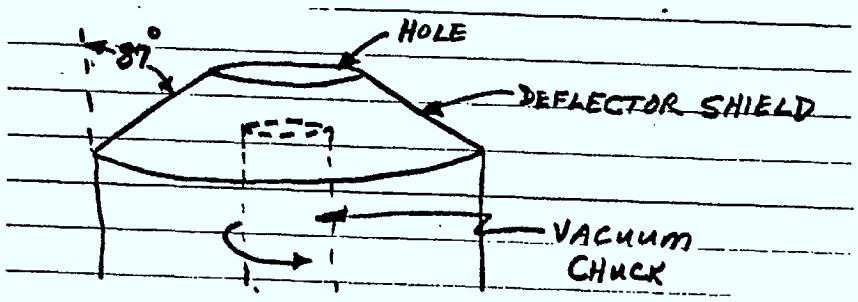



Fig. 3: Deflector Cone

The wafer was then baked at 100°C for 25 minutes. The exposure time was 30 s and the development time in Microposit MF 312 developer was 2 minutes. Good resolution was obtained on all but the 1 μm lines. The 5 μm source drain spacing on the mask became a 4 to 5 μm spacing in the implant etch. No post baking was required.

n implant

The wafers were mounted on 2" silicon blanks with photoresist. The mounting resist was hardened at 70°C for 30 minutes. The n implant was $3.75 \cdot 10^{12}$ [$cm^{-2}$] of $Si^{28}$ ions at 120 keV. The photoresist used to define the implant etch is also used to mask the implant. The range of the Si ions in the 1.8 μm thick photoresist is approximately 5400 Å with a standard deviation of 930 Å. The range of $Si^{28}$ at 120 keV in $Si_3N_4$ is 1015 Å with a standard deviation of 320 Å. The range is $Si_3N_4$ seems to indicate that the majority of the implant gets through the nitride film. It is uncertain what the mean energy and distribution of the implant is when entering the GaAs and thus predictions using tables for the depth of implant are questionable.

The photoresist layer is removed using hot acetone. A second resist

layer is applied for the $n^+$ implant of the ohmic contacts.

$n^+$ implant

The $n^+$ implant is $3.75 \cdot 10^{13}$ [$cm^{-2}$] of $Si^{28}$ at 100 keV. This dose creates cross linking in the 1450J resist and thus its removal can only be accomplished reliably uisng an $O_2$ plasma ashing procedure. The $Si_3N_4$ protects the GaAs surface since it is impervious to $O_2$.

Activation Anneal

A 1000 Å of reactively sputtered $SiO_2$ is laid down on the $Si_3N_4$. The reason for this is the possibility that pinholes may have formed in the implant film during etching.

The wafer is then annealed in an $N_2$ (1 litre/min) flow at 850°C for 20 minutes to activate the implant. From the data given in Table 12 and the formula for activation, $\eta = \frac{BI}{DqV}$ ,

B: magnetic flux density in tesla

I: measured current A-A'

V: measured voltage B-B'

q: $1.6 \cdot 10^{-19}$ [C]

D: dose [$m^{-2}$] ,

the activation is found to be 24%. There is no film destruction if the anneal is performed in this manner. The $SiO_2$ is then etched off in buffered HF since further processing requires the selective etching of $Si_3N_4$.

The Ohmic Contacts

The source-drain photoresist is applied in an identical manner to the implant etch resist. The holes through the nitride are etched with a 10 minute buffered HF etch. The photoresist is then stripped and a second

resist with a 2 minute chlorobenzene predevelopment soak is applied to assist the liftoff procedure. Initially the etch and liftoff were attempted with the same resist but poor results were obtained. The original source drain metal contacts were made of Au:Ge (88:12). This resulted in a roughened surface (Photo 4) after the ohmic anneal.

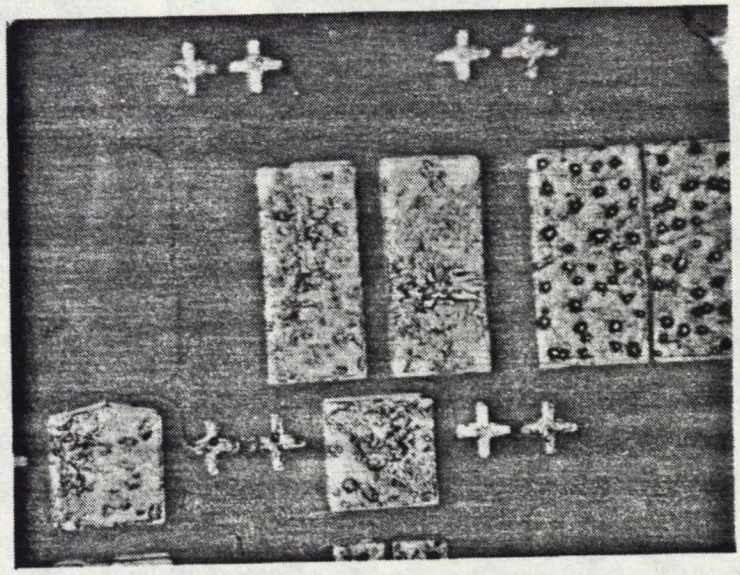


Photo 4: AuGe ohmic contacts after heat treatment

The process was changed to Ni (500Å) over AuGe (1500Å) and Photo 5 indicates the improved smoothness of the contact.

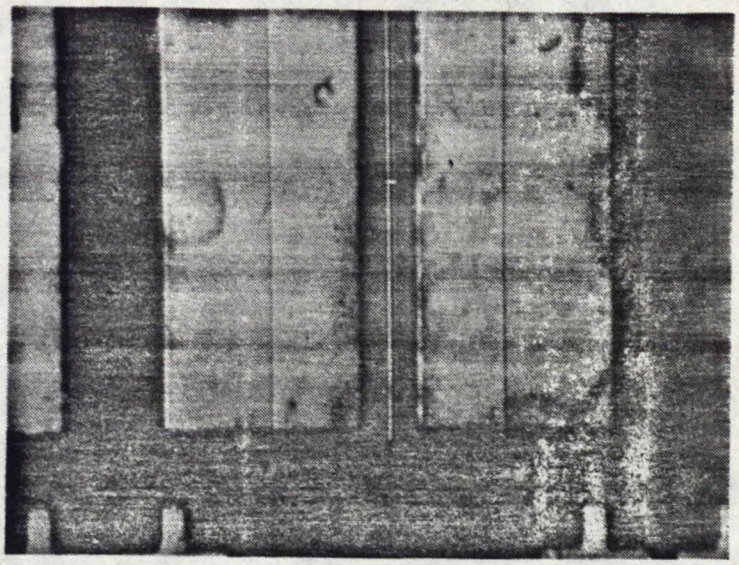


Photo 5: Final ohmic contacts Ni(500Å)/AuGe(1500Å)

The Ni was e beam evaporated from a graphite crucible. The Ni charge was fabricated using an arc welder in an argon atmosphere. The AuGe was thermally evaporated from a graphite boat.

The maximum chamber pressure was $3 \cdot 10^{-5}$ torr which indicates an impingement rate of the residual gases to be about $10^{16}[cm^{-2}s^{-1}]$*. The impingement rate of Ni with a deposition time of 1 minute, for 500 Å, is $8 \cdot 10^{15}[cm^{-2}s^{-1}]$. With a similar deposition rate for AuGe the impingement rate is $6 \cdot 10^{15}[cm^{-2}s^{-1}]$. This seems to indicate there is a reasonable amount of contamination of the films evaporated at these pressures and that future work should strive for lower pressure evaporations.

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* Handbook of Thin Film Technology - Maissel & Glang

The linear characteristics typical of these ohmic contacts is given in Photo 6 (resistance of 200 Ω in channel).

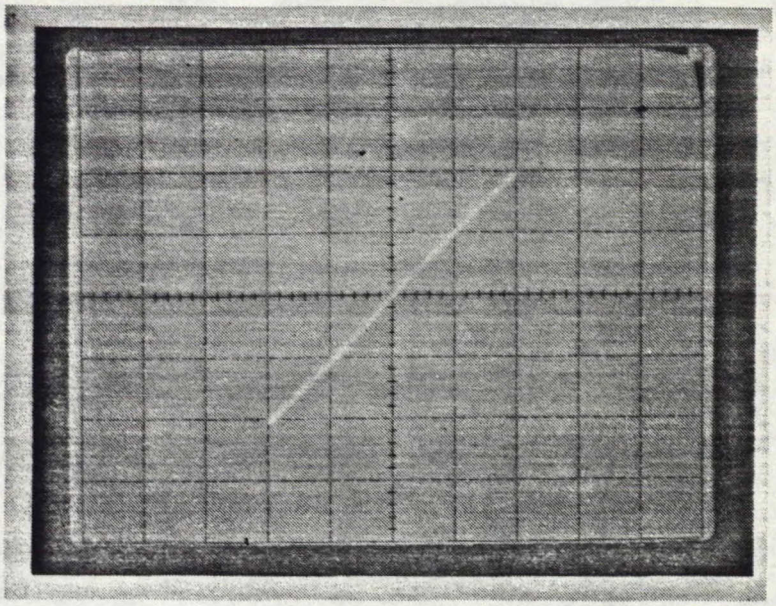

Photo 6: Linear IV characteristics (ac mode)
V = 0 center of screen
Vertical 5[mA/div]
Horizontal 1[V/div]

The B = 0 data of Table 12 and the formula for sheet resistance, $R_s[\Omega/C] = \frac{\pi}{\ell n 2} \frac{V}{I}$, gives $R_s = 24[K\Omega/C]$. This would imply a resistance in the channel of 120 Ω. This discrepancy has not been explained at the present time.

Gate Metallization

The photoresist procedure for the gate metallization is somewhat different from that used in the implant etch due to the 1μm line demand.

The differences are the 8000 rpm spin, the 1 minute soak in chlorobenzene, and the three minute exposure. This method gave a 70% yield of 1 to 2 μm gates.

A ten minute etch in BF HF was used to etch the $Si_3N_4$ off the channel (Photo 7).

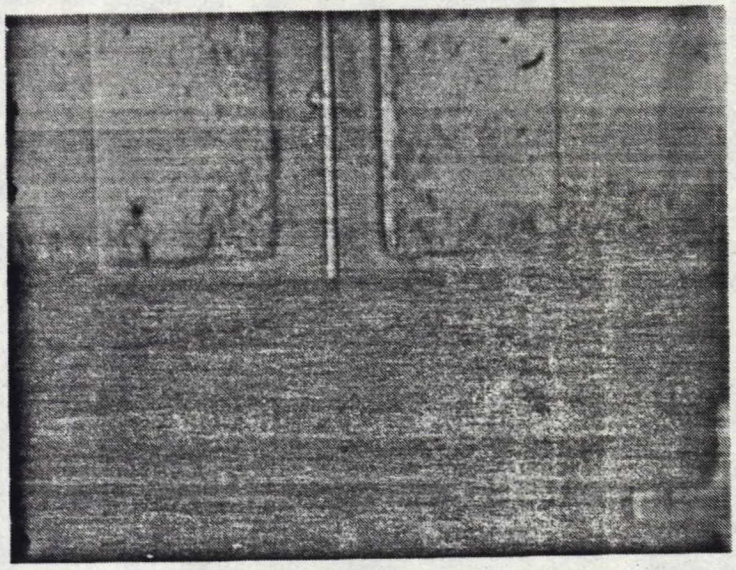

Photo 7: BF HF gate etch

The same resist was used in the liftoff since it would be impossible to align again to the etched channel.

Aluminium was thermally evaporated to a depth of 1500Å. The liftoff was accomplished using hot acetone. A good yield of the clearly defined photoresist patterns was obtained (Photos 8 & 9).

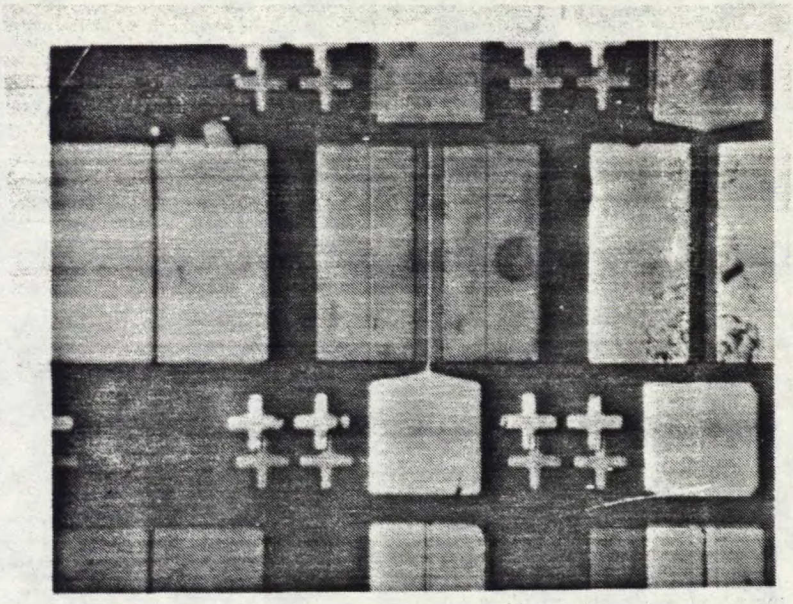

Photo 8: One of the final FETS, gate width 200 µm

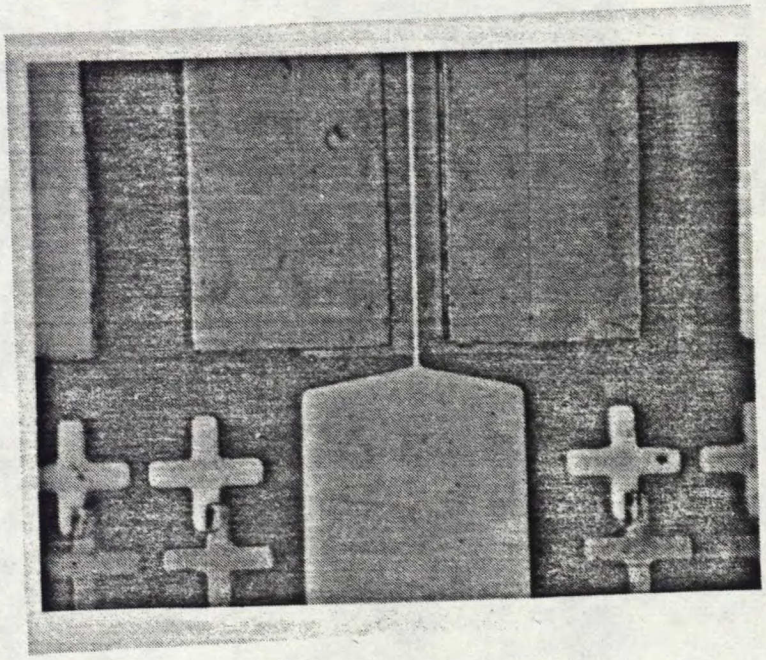

Photo 9: Detail of one of the final FETS

## A SUMMARY OF THE FINAL FABRICATION SEQUENCE

1. CLEANING degrease acetone (5 min)
   transene 100 (5 min)
   alconox (monosodium dihydrogen phosphate) filtered 1% solution (4 min)
   DI $H_2O$ (15 sec)
   $H_2O_2$ - $HN_4OH$ - 240 $H_2O$ (30 sec)
   DI $H_2O$ (15 sec)
   transene 100
   $N_2$ blow dry
   put immediately into plasmatherm

2. $Si_3N_4$ PLASMA DEPOSITION (6 min)

| settings | | |
|---|---|---|
| | $NH_3$ | 75 sccm |
| | He | 500 sccm |
| | 5% $SiH_4$/He | 550 sccm |
| | pressure | 1525 μm |
| | $T_{SUBSTRATE}$ | 308°C |
| | $P_{RF}$ | 100 W |

3. FILM ANNEAL 850°C for 14.5 min in $N_2$ atmosphere

4. PHOTORESIST - implant - trichloethylene boiling (5 min)
   acetone boiling (5 min)
   transene 100 (5 min)
   30 min 200°C
   5 min cooling in desiccator
   4000 rpm, 1450J resist
   30 s exposure
   2 minute development
   30 s DI water rinse
   blow dry

5. IMPLANT ETCH buffered HF time 9 min

6. IMPLANT - 120 keV - 3.375 x $10^{12}/cm^2$ - $Si^{28}$

7. PHOTORESIST ASHING -

| | |
|---|---|
| $O_2$ | 200 sccm |
| pressure | 250 μm |
| $T_{SUBSTRATE}$ | 120°C |
| $P_{RF}$ | 200 W |
| 10 minutes | |

8. CLEAN - implant - trichloethylene boiling (5 min)
   acetone boiling (5 min)
   transene 100 (5 min)
9. REACTIVELY SPUTTERED $SiO_2$ - 1000 Å

10. ACTIVATION ANNEAL - 850°C for 20 min

11. 60 SECOND BF HF STRIP OF $SiO_2$

12. CONTACT MASK ETCH

13. PHOTORESIST - source drain etch (same procedure as used in step 4)

14. BUFFERED HF - 10 minutes

14. REMOVE PHOTORESIST HOT ACETONE

15. PHOTORESIST - source drain metal - Ni[500Å] e beam/AuGe[1500Å)
    - same procedure as used in step 4 except
      bake 80°C for 30 minutes
      2 min soak in chlorobenzene for single step liftoff
      30 s exposure
      2 min development (see footnote on previous page)

16. Ni[500Å] e beam/AuGe[1500Å] thermal evporation

17. LIFTOFF WITH HOT ACETONE

18. ANNEAL - 450°C for 5 minutes

19. PHOTORESIST - gate etch and metallization*
    - same procedure as used in step 4 except
      8000 rpm spin
      bake 100°C for 25 min
      1 min soak in chlorobenzene
      3 min exposure
      2 min development (see footnote on previous page)
      10 min BF HF
      $NH_4OH$ : 10 $H_2O$ (15 s)

20. Al THERMAL EVAPORATION ~ 1500 Å

21. LIFTOFF - HOT ACETONE - 2 minutes

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* It was initially assumed that exposure of the entire wafer to BF HF would thin down the $Si_3N_4$ implanted regions to the substrate and allow only the metallization to be attempted with this layer. The results were poor so both processes must be attempted with the same mask step.

D.C. Measureents of Characteristics

The looping characteristics illustrated in Fig. 4 are often seen in studies of the MESFET devices. It is recognized that these hysteresis patterns are caused by traps being filled and depleted by a rather slow moving $V_{DS}$ sweep of the curve tracer. Useful characteristics for bias positioning of microwave devices are obtained from a slow $V_{DS}$ sweep which allows the traps to be saturated at any particular point of time. This slow sweep is illustrated in Photo D2. The scan is manually swept using the storage ability of the curve tracer. The intensity is then turned to zero, $V_{DS}$ is returned to zero and $V_{gs}$ is changed. The broadening of the lines is due to a high frequency signal on the $V_{gs}$ line which is seen as an $I_{DS}$ broadening.

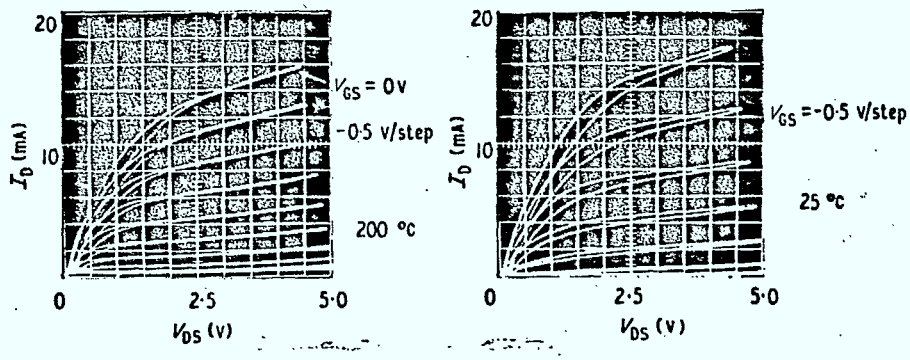



Fig. 4 (Older FET structure)

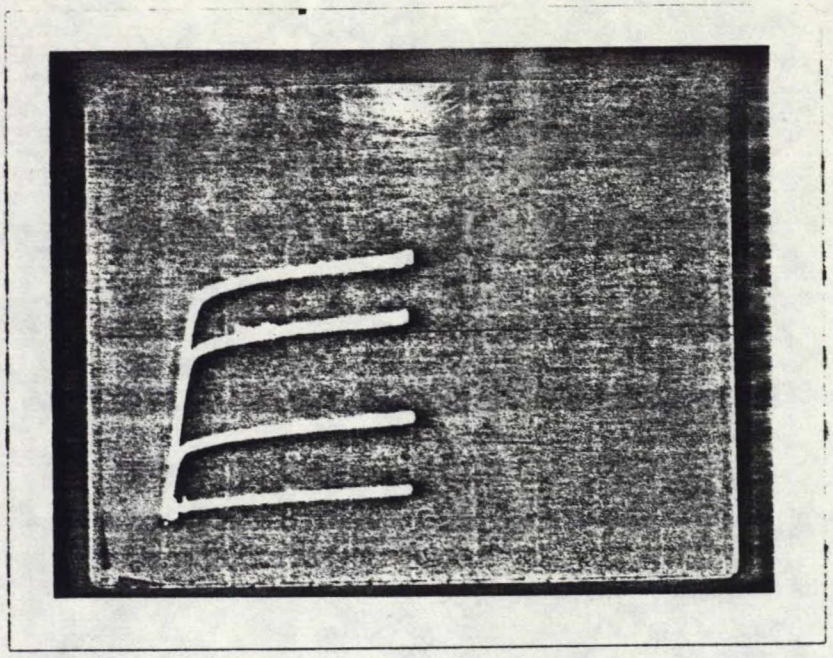


Photo 10
(FET from final fabrication sequence)

The characteristics for various FETS from the same wafer are given in photos 11, 12, 13.

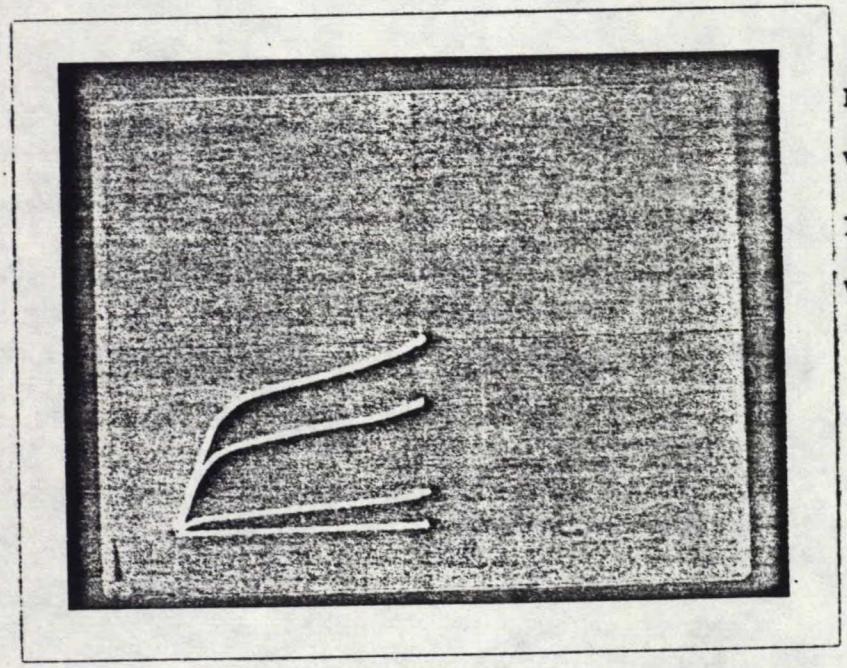


Photo 11

$V_{DS}$(Horiz) .5v/div

$I_{DS}$(Vert) 50 μA/div

$V_{gs}$ - .1v
- .2v gate voltages
- .4v
- .6v

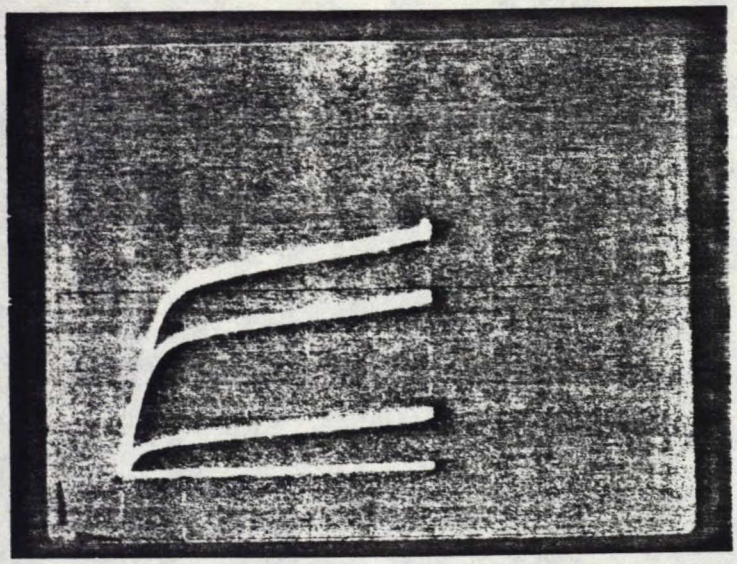


Photo 12

$V_{DS}$(Horiz) .5v/div

$I_{DS}$(Vert) 50 μA/div

$V_{gs}$ - .1v

- .2v gate voltages

- .3v

- .4v

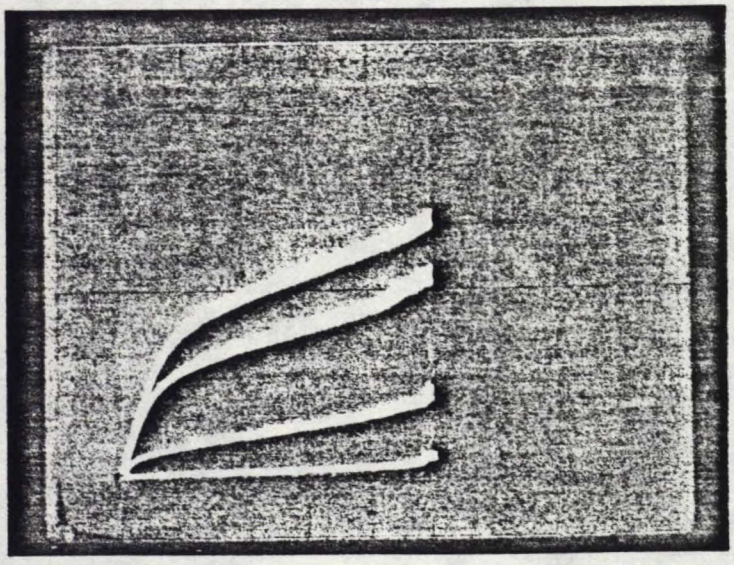


Photo 13

$V_{DS}$(Horiz) .5v/div

$I_{DS}$(Vert) 50 μA/div

$V_{gs}$ - .1v

- .2v gate voltages

- .3v

- .4v

The transconductance for the curve in photo D5 biased at 1.5 volts $V_{DS}$ is approximately .5 mmhos. The gate is 200 μm in width implying the

transconductance per mm is 2.5 mmhos/mm. This is very low when compared to commercially available FETS which have transconductances between 50 and 100 mmhos/mm. This discrepancy could be caused by a low doping density in the channel which constricts $I_{DS}$ and thus the possible variations of $I_{DS}$. Normal channel currents for FETS of this size are in the mA range where the maximum currents observed here are 0.2 mA. Pinch off voltages are also in the 2 to 4 volt range for commercial FETS* where the units produced here have a pinch off voltage of 0.6 volts. This doping problem could have been a result of the thickness of the $Si_3N_4$ film which was initially believed to be between 200 and 300 Å.

Van Der Pauw Cross

During this process evaluation procedure it became clear that one of the bottlenecks was the mounting of the cross to obtain fast and reproducible results for implantation activation and sheet resistance studies.

The criteria for a good testing structure are:

1. a good alignment of the cross in the magnetic field
2. fast mounting of die
3. ease of connection
4. reusability of die and test structure.

It was noted that, unlike silicon, the wires of connection to the pads could be laid across the surface since the substrate is insulating. Minor corrections to printed circuit boards and microwave hybrid tweaking of

*Raytheon RL C832 LNA GaAs FET, 500 μm wide, $g_M$ 50 mmhos, pinchoff voltage − 3 v.

designs are often accomplished using silver print (a fast drying suspension of silver particles). Figure V1 shows the PC board mounting of a GaAs wafer using this technique. Originally the die was mounted to the board using a double sided tape. This proved to produce a capillary type of action which on smaller die tended to short the leads underneath the substrate. A beeswax mount is being used at the present time and bypasses this constraint. The silver print is removed in toluene and the beeswax in trichloroethylene. A certain amount of technique is needed to connect to the smaller test patterns. This operation is carried out using a binocular microscope. The usual procedure is to have a reservoir of silver print near the die and draw the line, using a metal probe, from the pad outward to the edge of the die and to the PC board. When making the connection from the die to the PC board it is best to wait until the print has hardened somewhat to avoid a flow of material along the edge of the die.

The mounting structure for the PC board is illustrated in Fig. V2 and the positioning of the unit is illustrated in Fig. V3.

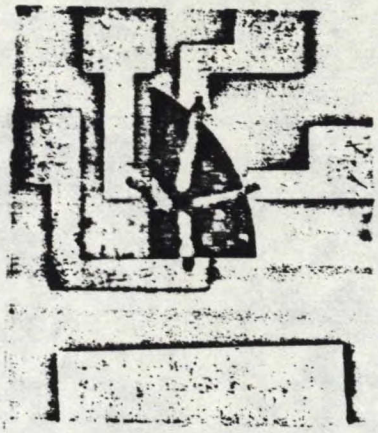


Fig. V1: Wafer mounted on PC board

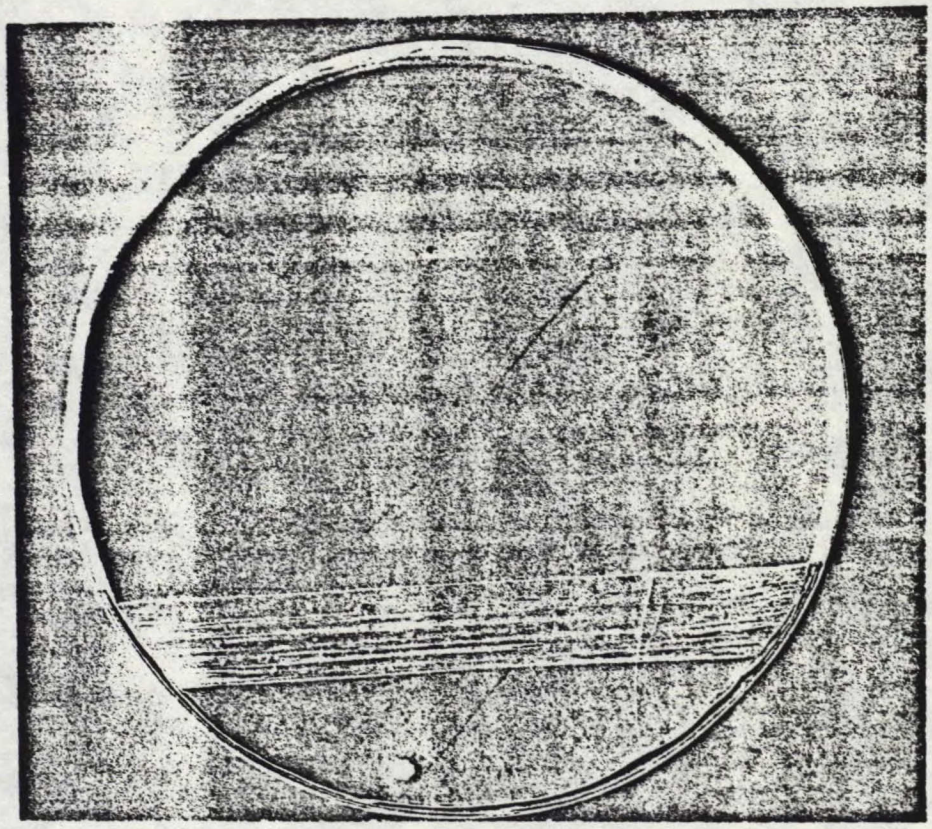


Fig. V2: Front view of mounting structure

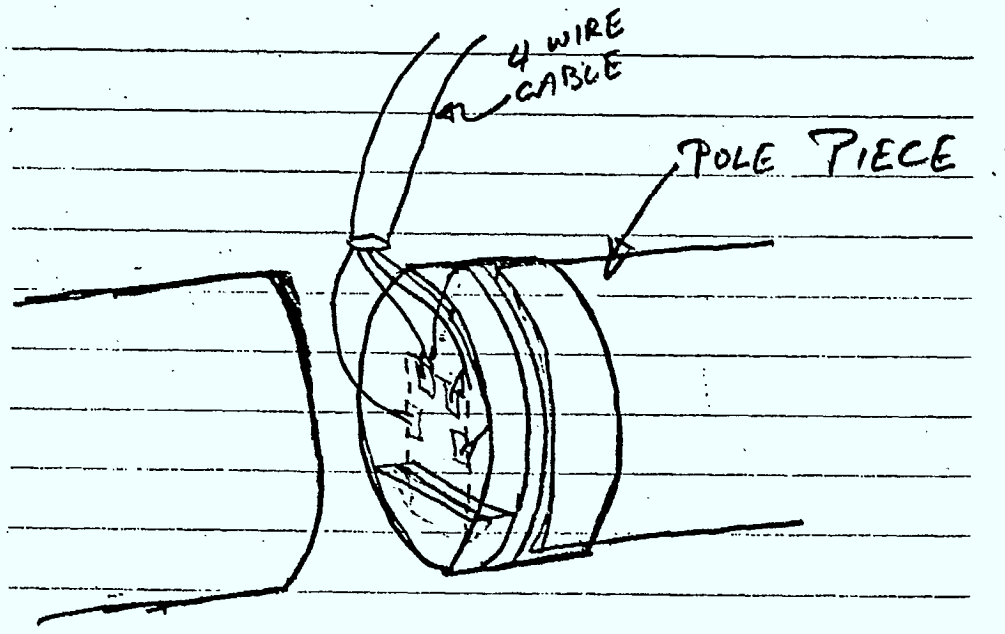
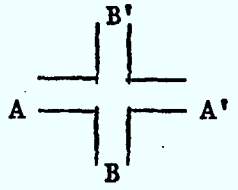



Fig. V3

The results from the device in Fig. 1 are quoted in Table V1.



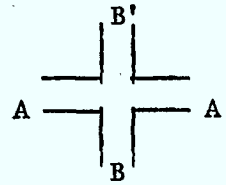

B = .2T

| Current [mA] A-A' | Voltage [V] B-B' |
|---|---|
| 6.0 | .282 |
| 5.0 | .232 |
| 4.0 | .184 |
| 3.0 | .138 |
| 2.0 | .094 |
| 1.0 | .049 |

Table V1

Since an implantation process evaluation sample would have to be produced with each FET fabrication run it was decided that an optimum mask set should be generated which contained only cross structures and was compatible with the mounting procedure. This mask pattern is illustrated in Fig. V4. The

actual size of the plate is illustrated in Fig. V5. This mask was designed to produce 25 crosses on a 1 $cm^2$ piece of GaAs. The data obtained from these structures is illustrated in table V2, for the final FET fabrication sequence, and a photograph of the final structure is given in photo V1.




| | | B = 0.2 T | | B = 0 | |
|---|---|---|---|---|---|
| | | I[mA]A-A' | V[mV]B-B' | I[mA]B-A' | V[mV]A-B' |
| | | 0.2 | 30 | 0.2 | 104 |
| | Sample | 0.4 | 60 | 0.4 | 204 |
| | 1 | 0.6 | 82 | 0.6 | 307 |
| | | 0.8 | 101 | 0.8 | 413 |
| | | 0.2 | 22 | 0.2 | 114 |
| | Sample | 0.4 | 48 | 0.4 | 225 |
| | 2 | 0.6 | 78 | 0.6 | 337 |
| | | 0.8 | 106 | 0.8 | 450 |

Table V2

The calibration of the Alpha Scientific 7500 W magnet was done using a RFL Model 1890 Gaussmeter.

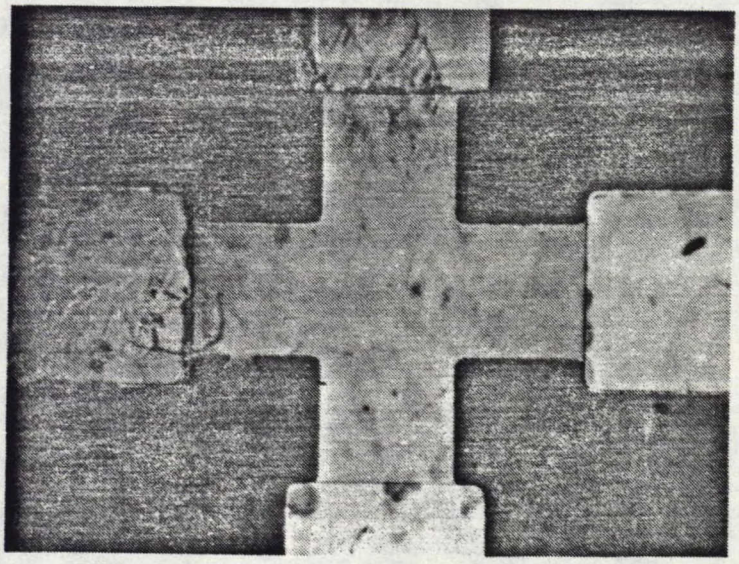


Photo V1: Cross structure from the final FET fabrication sequence. Source drain metal used $n^+$ mask.

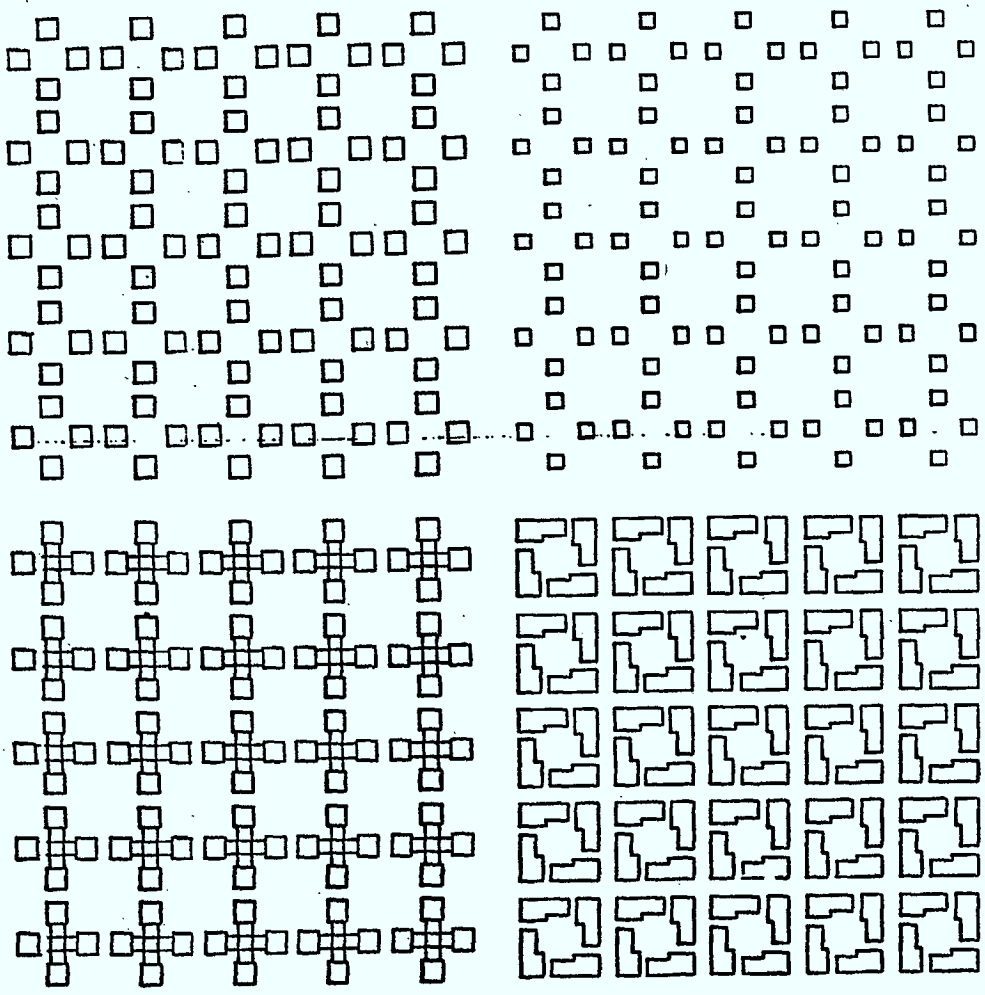


Fig. V5: Plate for cross fabrication

Source-Gate Channel

This processing procedure produces a $Si_3N_4$/GaAs interface over the source gate channel region (and gate to drain region). This was assumed to constrict the channel and thus increase the resistance. A study of this nitride substrate interface was begun using it as the dielectric in a MIS capacitor.

The mask which is illustrated in Fig. C1 produces 25 MIS capacitors on a 1 cm x 1 cm piece of GaAs. The capacitors formed have areas of .1 $mm^2$. This gives a rough nitride capacitance of approximately 60 ρF. The photoreduction was done by Colorgraphics. The actual size of the plate is given in Fig. C2 and the completed capacitor is seen in photo C1. The

capacitance bias and capcitance vs. frequency were taken using thhe HP LCR meter through a program written by Dr. Paul Van Halen.

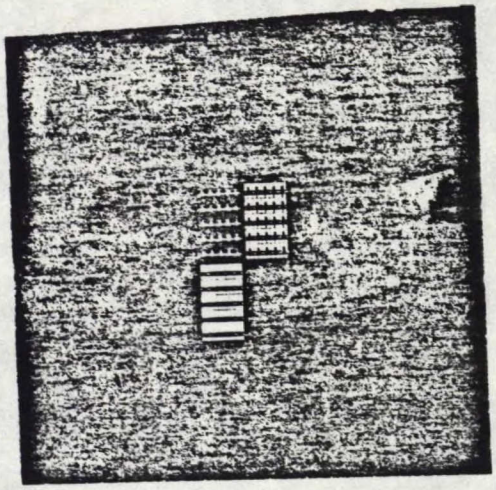


Fig. C2
Capacitor plate
Actual size

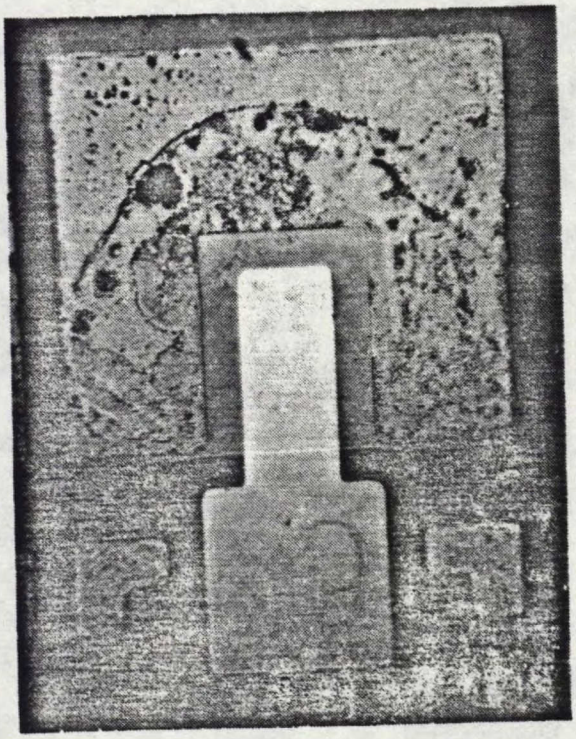
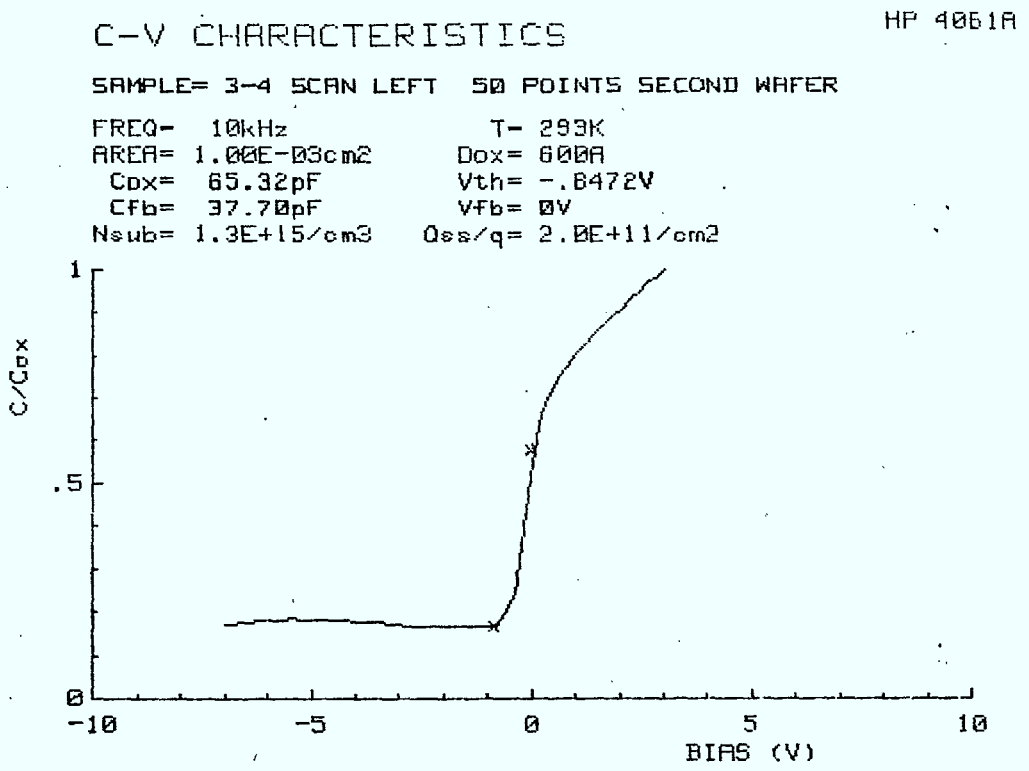
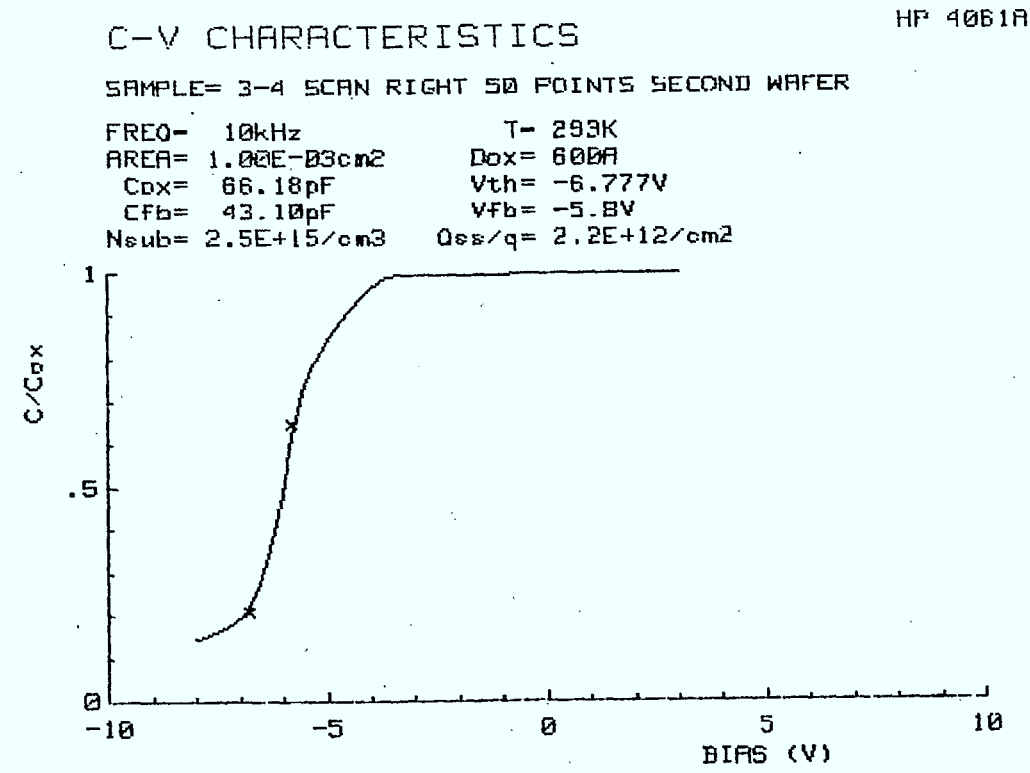


Photo C1
Capacitor from the final FET fabrication sequence.



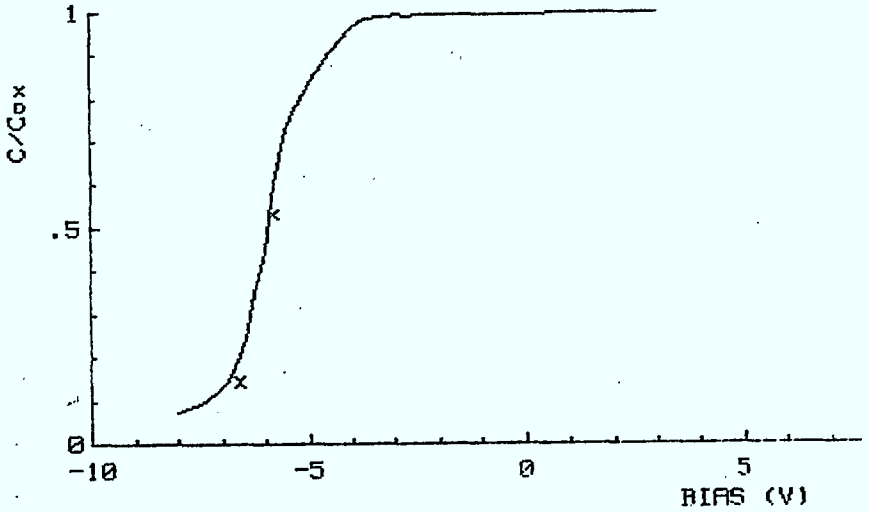




Noteable variation in the differential capacitance as a function of the direction of the bias sweep.

C-V CHARACTERISTICS

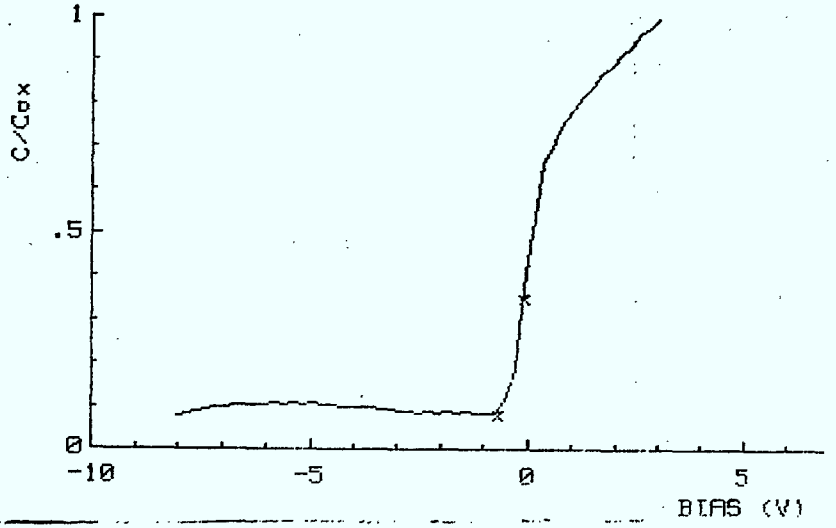
SAMPLE= 3-4 SCAN RIGHT 50 POINTS SECOND WAFER

FREQ= 1MHz T= 293K
AREA= 1.00E-03cm2 Dox= 600A
Cox= 60.28pF Vth= -6.576V
Cfb= 32.07pF Vfb= -5.8V
Nsub= 7.7E+14/cm3 Oss/q= 2.0E+12/cm2

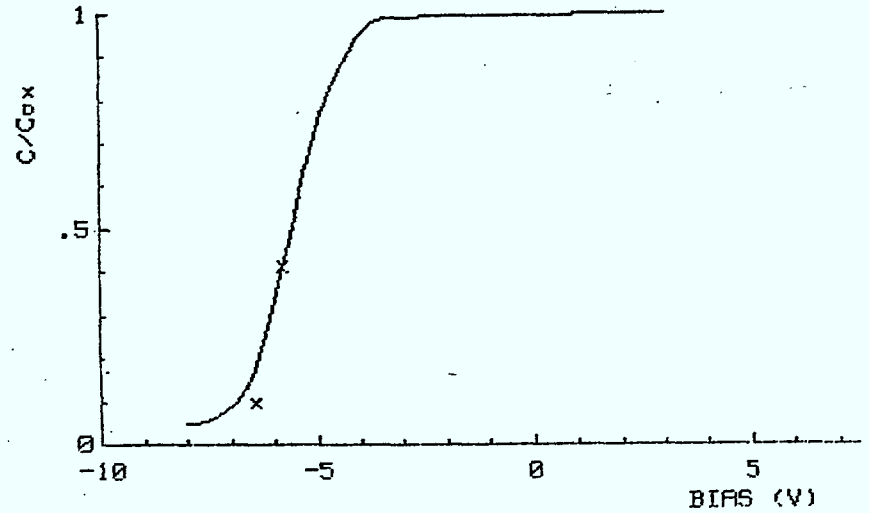



SAMPLE= 3-4 SCAN LEFT 50 POINTS SECOND WAFER

FREQ= 1MHz T= 293K
AREA= 1.00E-03cm2 Dox= 600A
Cox= 59.42pF Vth= -.6674V
Cfb= 20.58pF Vfb= -.08V
Nsub= 1.6E+14/cm3 Oss/q= 1.7E+11/cm2

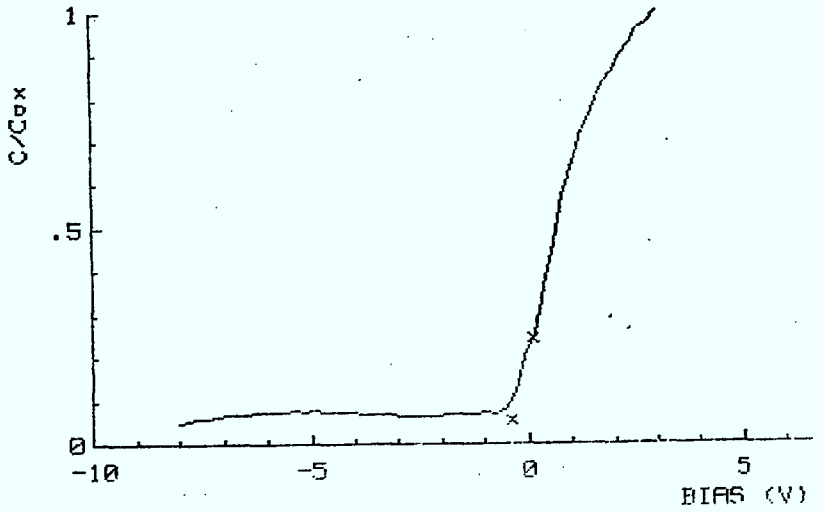



FREQ= 10MHz T= 293K
AREA= 1.00E-03cm2 Dox= 600A
Cox= 56.97pF Vth= -6.442V
Cfb= 23.49pF Vfb= -5.8V
Nsub= 2.6E+14/cm3 Oss/q= 1.9E+12/cm2




SAMPLE= 3-4 SCAN LEFT 50 POINTS SECOND WAFER

FREQ= 10MHz T= 293K
AREA= 1.00E-03cm2 Dox= 600A
Cox= 55.90pF Vth= -.3546V
Cfb= 13.59pF Vfb= .14V
Nsub= 5.3E+13/cm3 Oss/q= 2.5E+11/cm2






The $C_{ox}$ (nitride capacitance) falls slightly with higher frequency but not appreciably

HUTCHEON, D.G.
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