Analysis and Design of Land Mobile Communications Systems Based on Digital Techniques

Final Report

Contract: OSU79-00060

Submitted By

Professor Samy Mahmoud (Principal Investigator), and

Professor Cyril Leung

Department of Systems Engineering and Computing Science

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ABSTRACT

Integration of Voice and Data Communications over land mobile radio channels is regarded as a promising approach towards efficient spectrum utilization. The research reported here represents a step towards achieving such integration in a digital land mobile radio system. Four aspects have been investigated: (1) the use of forward error correction schemes for data messages to improve channel throughput in the face of fading conditions, (2) the implementation of low power microprocessor controller for integrated mobile terminals, (3) testing the performance of two modulation systems (DPSK and FFSK) for transmitting data at speeds of 9.6 kb/sec. and 16 kb/sec. under simulated fading conditions, and (4) the construction of a TFM modulator which will be tested later to compare the performance of this technique to that of the FFSK technique in fading channels.

ACKNOWLEDGEMENTS

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CHAPTER 1

Introduction

The use of land mobile communications channels has so far been largely confined to voice communications. However, recent years have witnessed a rapid growth in the need for data communications mobile systems. Such a demand on the scarce frequency spectrum resource has motivated the search for new techniques to achieve better utilization of the radio frequency spectrum.

It is predicted that the demand for data transmission on mobile radio channels will be steadily increasing over the current decade. Examples of the applications demanding such a service include automatic vehicle location systems, control of channel assignment in cellular systems, police applications, taxi and other dispatch systems. As an indication of the expected demand, it is anticipated that a large fraction of the 350,000 radio users which constitute the Canadian private mobile radio community will add to their system a data transmission capability in the next five years.

The congestion of the available spectrum, coupled with the growing demand for mobile data transmission motivates the search for feasible techniques for integrating speech and data within a single land mobile radio channel. Attempts to investigate such techniques for general data networks have been published recently [1, 2, 3, 4]. The remaining sections of this chapter explore such techniques and serve as an introduction to the research effort intended to accomplish the objective of integrating

voice and data communications over mobile radio channels.

1.1 Integration of Voice and Data Over Mobile Radio Networks

In existing commercial mobile communications systems, data messages and speech are transmitted on separate dedicated channels. Voice communications (mobile telephone) is carried out using frequency modulation techniques. This led to the standardization of the transmitter/receiver units in which FM channels have 30 KHz bandwidth. The need to transmit data messages over mobile communications systems was accommodated by using an IF modulation technique (e.g. DPSK) for the input data messages. The output of the IF stage is then inserted in the audio input section of the FM transmitter unit. Figures 1 and 2 illustrate the components of mobile data terminals and a fixed base station. Data buffering and transmission is controlled by a microcomputer unit which interfaces serially with the modem.

The above technique places severe limitations on the speed of data transmission since the spectrum of the IF signal has to be limited to the bandwidth of the audio input of the transmitter. Increasing the speed of the input signal will lead in this case to higher bit error rates. In random access techniques, the transmission of messages at low rate increases the probability of errors and message retransmissions, which leads to rapid deterioration of the throughput performance of the channel. As well, the scarcity of the available spectrum resources makes it difficult to satisfy the increasing demand for mobile data communications.

Recent research in the speech communications field indicates the existence of gaps between talk spurts of average durations ranging from 0.6 to 1.2 m.sec, depending on the applications. The channel becomes idle

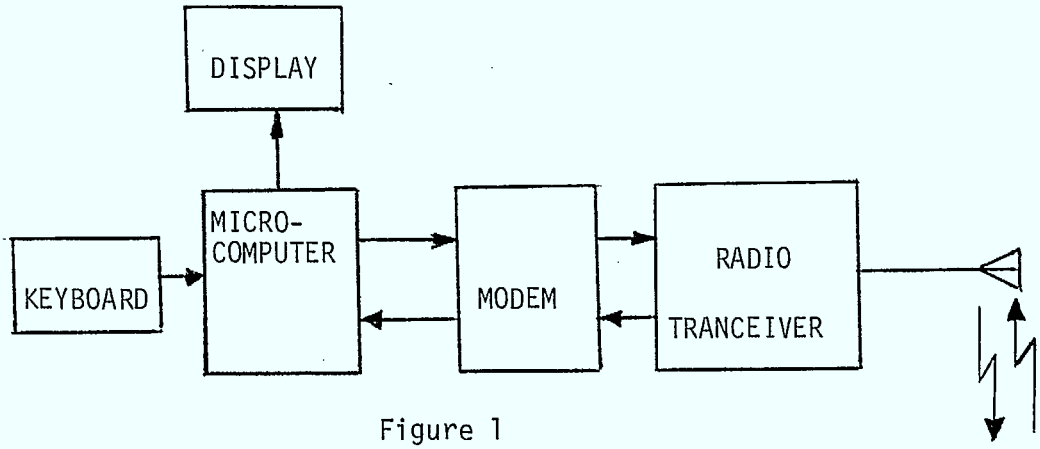

Figure 1

REMOTE TERMINAL

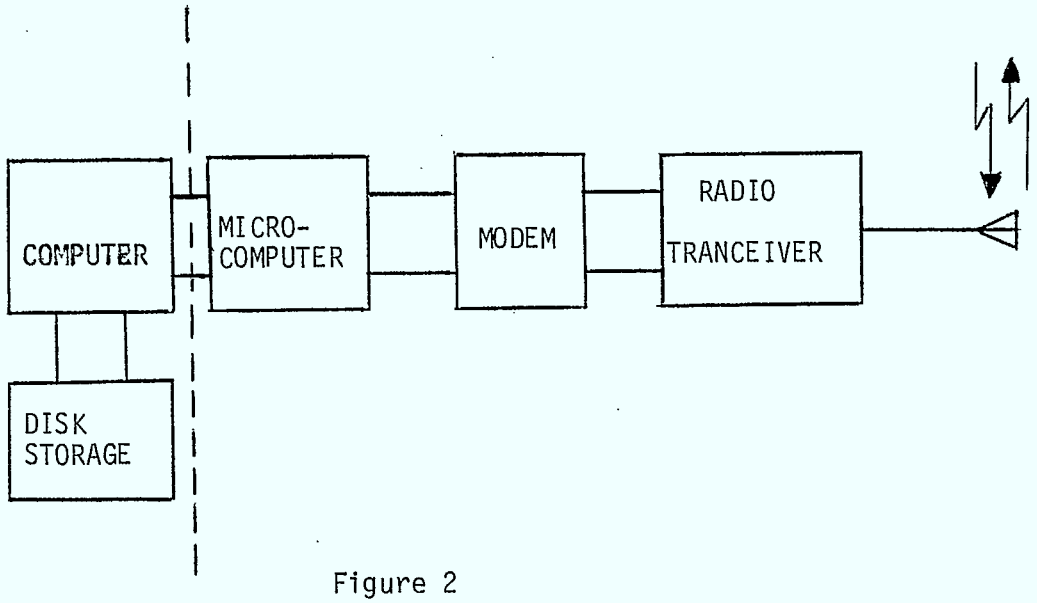

Figure 2

BASE STATION

during these gaps. Transmission of voice and data simultaneously over the same channel can obviously be made possible by transmitting data packets during the silent intervals of the channel which is used primarily for voice communications.

Assuming data packet lengths ranging from 1000 to 2000 bits (as is the case in most applications), it is possible to fit these packets into the silent intervals of the channel using appropriate transmission rates. This is feasible at transmission rates of 8 k.bits/sec or higher.

The realization of the above scheme in mobile radio applications is feasible only under the following conditions:

(1) The availability of low cost modem sets that can transmit data at rates higher than 8 k bits/sec over 30 KHz channels with low BER.

(2) The availability of accurate speech detector in voice terminals so that the carrier is suppressed when no input speech is detected.

(3) The ability of the data terminals to sense the voice carrier on the channel to determine if the channel is busy (talk spurt) or free (gap). The data terminal will transmit its packet only when a gap is detected.

Integration of voice and data transmissions in existing mobile communications systems will require the use of different modulation technique in RF band for the data signals. This is needed since data transmissions will be an 'added on' service to an existing FM mobile communications system.

The objective of the on-going research report here is to construct an all digital voice/data mobile communications systems for the 800 MHz

frequency band. Thus the same modulation technique is used for both voice and data signals. To explain the general concept of such a system, we consider the general structure of the base station and each mobile unit.

The Base Station:

Figure 3 illustrates the basic components of the base station. When a speech signal is transmitted to over a channel the station adds to it a narrow band tone and a clock signal. When a data signal is transmitted, only the clock signal is added to it (in the frequency domain).

The Mobile Station:

Figure 4 illustrates the basic components of each mobile unit. The mobile transmits speech signals after the channel is assigned to it by the base station. The mobile unit transmits data packets only after it senses the carrier on the channel and determines, by examining the busy tone, if the channel is busy or free. The speech detector is used to suppress the mobile carrier when it is not transmitting in the speech mode.

Figure 5 illustrates the structure of the mobile terminals proposed for future research. The voice encoder/decoder circuit will be implemented using the CVSD technique and voice will be digitized at 16 k bits/sec. The modem set to be used will be based on the TFM technique, which will be discussed in section 4.4

1.2 Objectives of Current Research

The ultimate objective of the research reported here is to demonstrate, both theoretically and practically, the feasibility of integrating speech and data transmissions over mobile radio channels. Such an integration will lead to better utilization of the available frequency

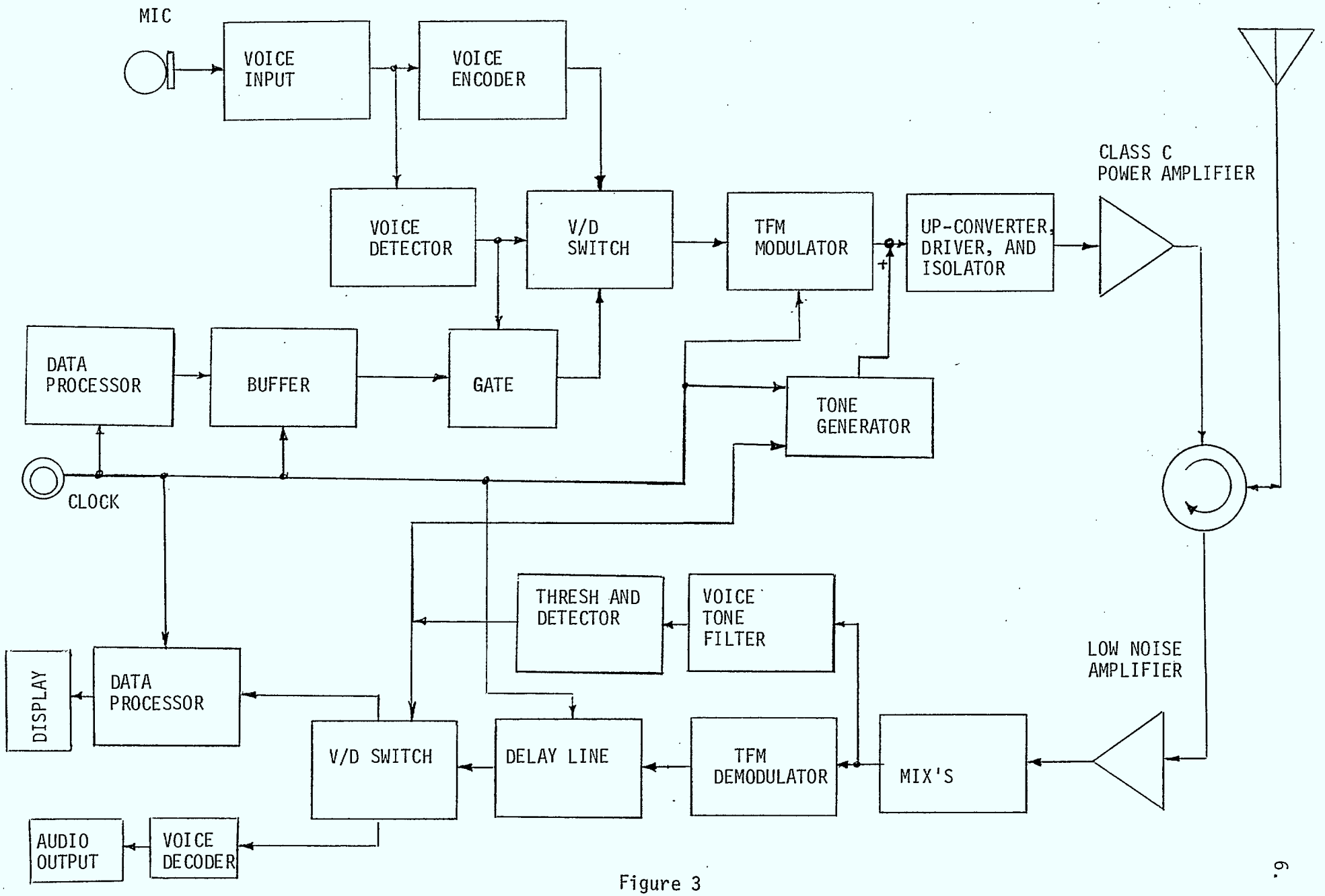

Figure 3

BASE STATION COMPONENTS

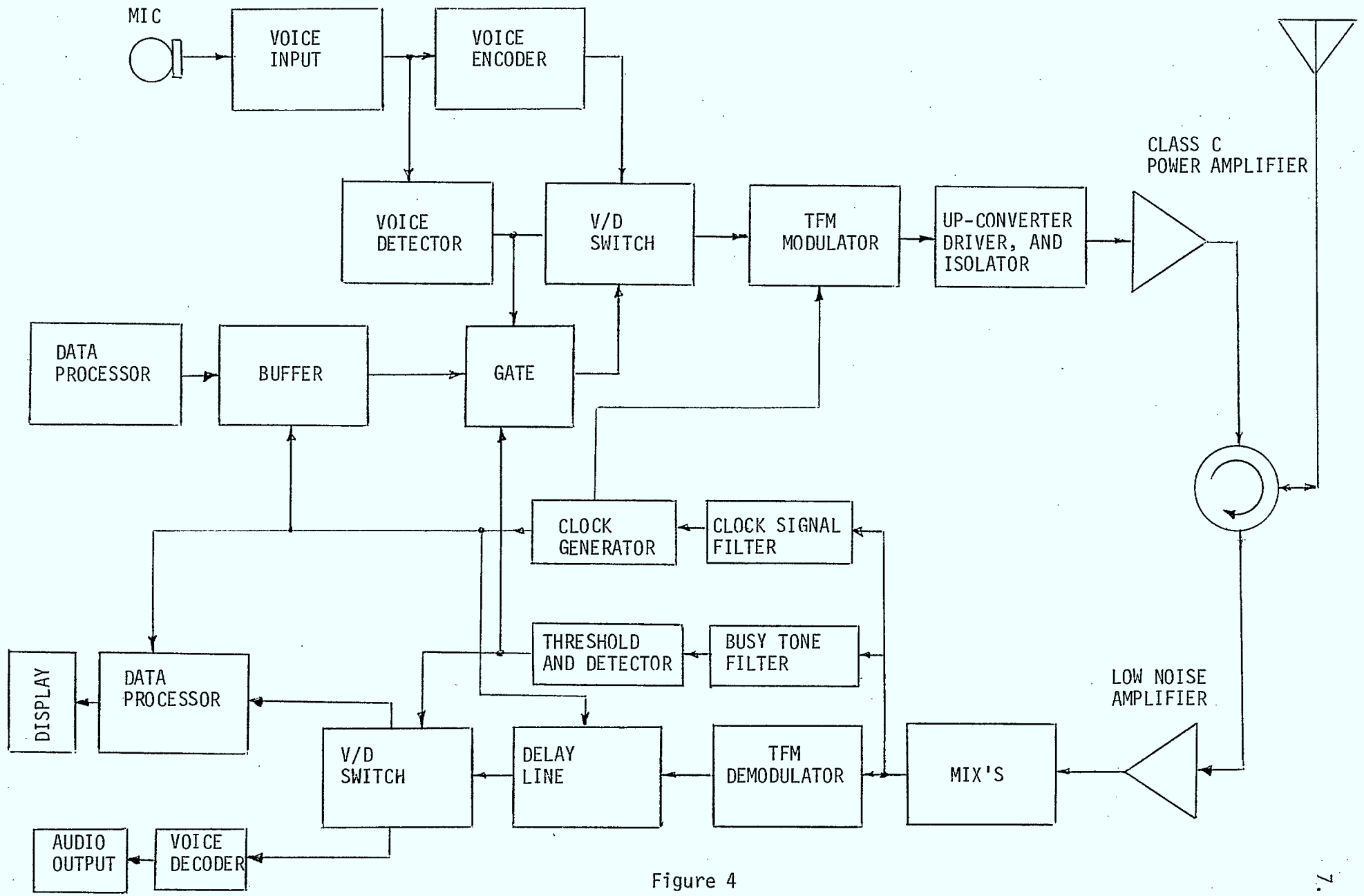

Figure 4

MIXED DATA AND VOICE TERMINAL COMPONENTS

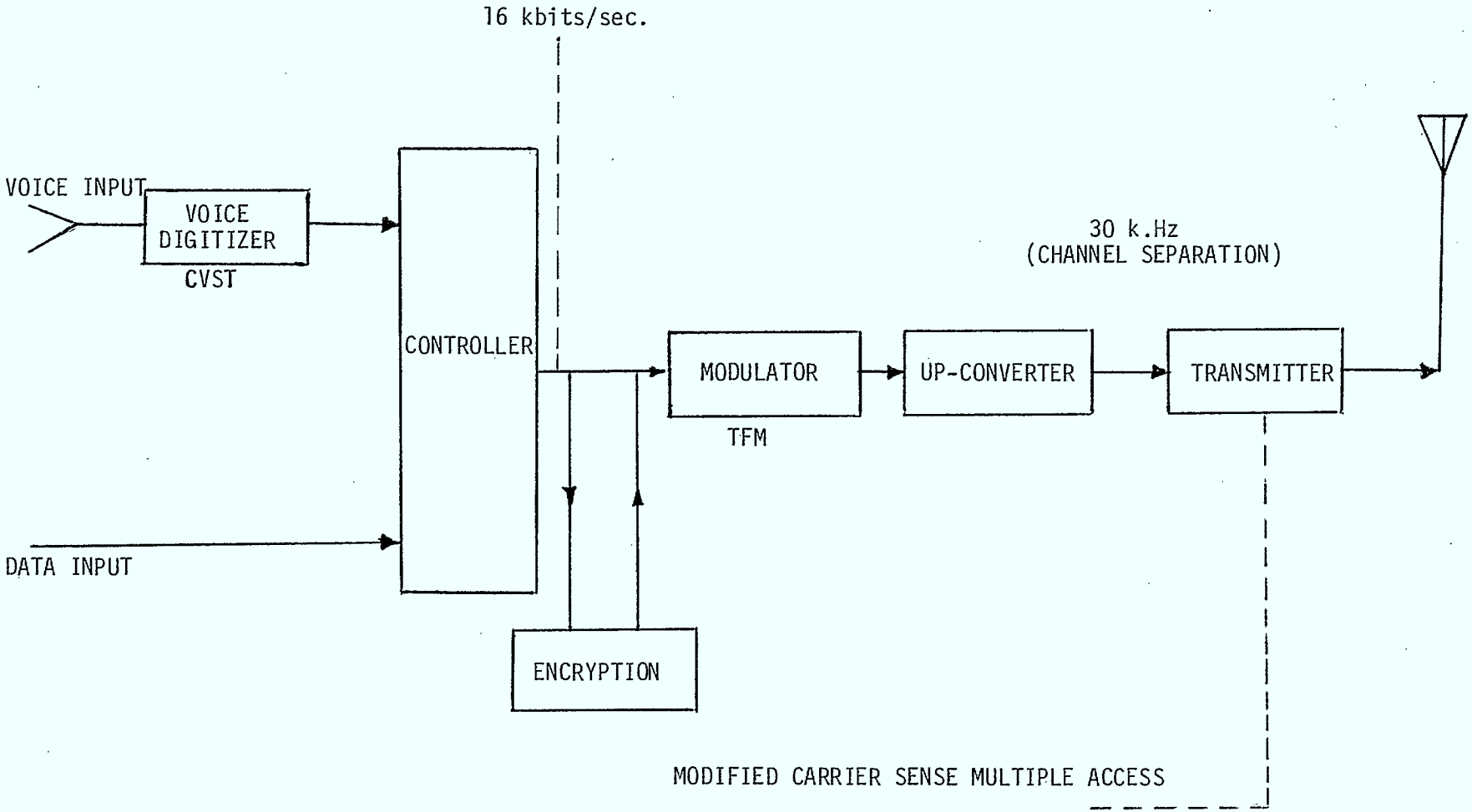

Figure 5

PROPOSED EXPERIMENTAL MOBILE TERMINAL

spectrum and provide flexibility in channel use for applications involving voice and data communications. The research reported here can be considered as a step in the progress towards achieving the final objective. Specifically, three research aspects have been addressed:

(1) Improvement of channel throughput - delay performance with respect to packet data traffic;

(2) Design and implementations of low power, small size micropower controller units; and

(3) Measurement of the BER performance of specific modulators under simulated fading conditions.

The following is a summary of the research conducted in each of the above three aspects.

1.2.1 Improvement in Throughput of Packet Data Traffic

The poor throughput-delay performance of random access channels is attributed to the loss of data packets due to collisions or noise and the increase in the total traffic input resulting from packet retransmissions. When fading effects are taken into account, the number of packets received in error increases, which leads to further deterioration of the performance of the channel. One approach for improving the throughput - delay characteristics is accomplished through the use of forward error correction schemes. By correcting some of the packets received in error, the total number of retransmissions will be reduced, leading to improvement in the throughput-delay performance of the channel. Chapter 2 of this report examines the result of investigating the applicability of forward error correcting codes to random access channels under fading conditions.

1.2.2 Design of Mobile Radio Terminals

It is apparent from the discussion of section 1.1 that the controller of the mobile terminals will be performing a number of time critical functions. In practice, microprocessors are used as controller units. However, microprocessor boards that are based on I^2L technology tend to have high power consumption and relatively large size, two factors that mitigate against using them in portable mobile terminals. The power consumption and size of the microprocessor board can be substantially reduced by using the CMOS technology. In this research, a general purpose CMOS microprocessor board has been designed, implemented and tested for mobile terminal functions. This board will be used as the controller unit of the mobile terminals that will be deployed in future field experiments. The design, implementation and testing of the microprocessor board are discussed in Chapter 3.

1.2.3 BER Performance of Two Modulation Systems Under Fading Conditions

As mentioned earlier, fading and multipath effects introduced errors to digital signal transmitted over radio channels. In data transmissions, such errors will lead to frequent retransmissions and subsequent deterioration in the throughput - delay performance of the channel. In the transmission of digitized voice, such errors will adversely affect the quality of the received speech, particularly if the voice is encoded at low sampling rates. In this research, two modulator/demodulator sets have been tested to determine the effects of fading signals on the BER of each set. Both sets have been used previously in experimental mobile radio systems as explained in Chapter 4.

1.3 Structure of the Report

The remaining chapters of this report are organized as follows:

Chapter 2 examines the distribution of packet transmission errors introduced by channel fading conditions. Forward error correction methods are applied and their performance is examined. The feasibility of using forward error correction to enhance the performance of random access techniques is discussed in the conclusions of the chapter.

Chapter 3 reports the design implementation and testing of a CMOS microprocessor which has much lower power consumption and smaller volume relative to an I^2L microprocessor (INTEL 8020) with comparable functional capabilities.

Chapter 4 reports the results of testing the BER of two digital modulation systems in the existence of fading signals and receiver (Gaussian) noise. The first system is based on the DPSK modulation technique and the second system is based on the FFSK modulation technique. A tamed frequency modulator (TFM) circuit implementation is also reported in this chapter.

Finally, Chapter 5 contains concluding remarks and an outline for the future continuation of the research reported here.

1.4 References

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CHAPTER 2

ERROR CONTROL FOR RANDOM-ERROR AND RAYLEIGH FADING CHANNELS

2.1 Introduction

Error detection and retransmission schemes are quite commonly used in many data communications because they can provide high reliability at a small cost [1,2]. Such schemes are particularly effective when the probability of a retransmission P_r is small. However, as the channel error rate (and therefore P_r) increases, they yield lower and lower throughput. To preserve an acceptable throughput, various techniques can be used, such as diversity transmission or coding.

In this chapter the use of random and burst error correcting codes in improving the performance of a stop-and-wait Automatic Repeat-Request (ARQ) scheme over random-error and Rayleigh Fading channels is investigated. Two models are examined. The first model is similar to the one in [1] and is used to analyze the effect of forward error correction on the mean wasted time. The second model assumes a Poisson arrival process for fixed length messages and determines the effect of forward error correction on the mean time between the arrival of a message and its successful transmission.

2.2 Effect of Forward Error Correction on Mean Wasted Time

In this section, a model of a stop-and-wait ARQ scheme similar to [1] is used to examine the reductions in the mean wasted time obtainable by the use of forward error correcting codes. Two channel models, one with random errors and the other with Rayleigh fading, are considered.

We assume that measages have random lengths L which are geometrically distributed, i.e.

$$P_L(\ell) = pq^{\ell-1}, \ \ell = 1,2,3 \ldots; \ q = (1-p) \qquad (1)$$

with average length $\overline{L} = \frac{1}{p}$. The message is split into blocks of size B bits. These are then assembled into packets of length (B+b) bits, where b represents overhead required for synchronization, addressing, error detection, etc. The mean number of packets per message is given by

$$\bar{N}(B) = \sum_{n=1}^{\infty} n. \ P([n-1]B < L \leq n \ B)$$

$$= \sum_{n=1}^{\infty} n \sum_{\ell=(n-1)B+1}^{nB} pq^{\ell-1}$$

$$= \frac{1}{(1-q^B)} \qquad (2)$$

Let $P_e(B+b)$ denote the probability that the transmitted packet will be received incorrectly. We assume that the error-detection code is able to detect all errors [3]. Of course, $P_e(B+b)$ depends on the channel noise characteristics.

In the stop-and-wait transmission scheme, the transmitter sends a packet and waits for an acknowledgement from the receiver. If a positive acknowledgement is received (indicating the packet was successfully received), the sender proceeds to send a new packet. Otherwise, the transmitter repeats the same packet until it receives a positive acknowledgement. Throughout this chapter, the acknowledgement delay is assumed to be a con-

stant, denoted by A.

There is a trade-off involved in selecting the packet size. On the one hand, it is desirable to choose a large packet size so as to reduce the acknowledgement delay. On the other hand, a long packet is more likely to be corrupted by the channel, and hence require a retransmission. Also, in the case where the unused portion of the last packet of a message is filled with dummy bits, a long packet results in more waste. This can be avoided by using an end-of-message character.

Assuming that an error in the transmission of a packet is independent of that of any other packet transmission and that the last packet is filled with dummy bits, it can be shown [1] that the expected wasted time (i.e. the difference between the actual time for transmitting the packetized message and the time it would take to directly transmit the (unpacketized) message over an error-free channel with the same baud rate) is given by

$$\overline{W}(B) = \frac{1}{(1-q^B)}\left[\left(1 + \frac{P_e(B+b)}{1-P_e(B+b)}\right)(A+T)\right] - \frac{\overline{L} + b}{R} \qquad (3)$$

where R = channel baud rate in bits/sec

$T = \frac{B+b}{R}$ = packet transmission time in sec.

We now consider the effect of forward error correction on the mean wasted time as described by equation (3). The use of an error-correcting code involves a trade-off: On the negative side, parity-check bits representing additional overhead have to be used; however this may be more than offset by the reduction in the probability of a packet retransmission P_r.

The choice of an error-correcting code C and its effect on the

mean wasted time is now examined. We confine our attention to Bose-Chaudhuri-Hocquenghem (BCH) codes [4,5]. For a given packet length n, (preferably of the form $n = 2^m-1$, $m = 2,3,4, \ldots$ corresponding to the codeword lengths of BCH codes), we obtain the distribution of the number of channel errors in the packet. This can be derived analytically for the random-error channel. For the Rayleigh fading channel, simulations were used to obtain the desired distribution.

From this distribution, we can determine the number of bit errors t that should be corrected for a given packet retransmission probability $P_r(n)$. Of course, the smaller $P_r(n)$ is, the larger t will be. The number of parity-check bits p required to correct these t errors can be easily determined from BCH code parameters [5]. By comparison with equation (3), the resulting expression for the mean wasted time is

$$\overline{W_C}(n,p) = \frac{1}{\left(1-q^{n-(b+p)}\right)} \left[\left(1+ \frac{P_r(n)}{1-P_r(n)}\right) (A+T)\right] - \frac{\overline{L}+b}{R} \qquad (4)$$

where $T = \frac{n}{R}$ = packet transmission time in seconds.

2.2.1 Numerical Results for the Random-Error Channel

The distribution of the number of bit errors N in a packet of length n sent over a random-error channel is given by

$$P_{random}(n,N) = \binom{n}{N} p_b^N (1-p_b)^{n-N} \qquad (5)$$

where p_b is the bit error rate. We assume $p_b = 10^{-2}$.

Letting $P_e(B+b) = 1 - P_{random}(B+b, 0)$ in equation (3), the expected wasted time for $\overline{L}$ = 1000, 2000 and 5000 bits was calculated as a function of B.

The results are plotted in figures 6, 7 and 8 (curves labelled no error correction). For each value of $\bar{L}$, there is an optimal value of B which minimizes the expected wasted time as suggested by the discussion at the beginning of section 2.2. BCH random error correcting codes were then used to correct enough channel errors say t to ensure that the probability of retransmission P_r is no larger than 0.05. The codes used for various packet lengths are given in table 1.

packet length n	BCH (n,k,t) code used to achieve $P_r \leq 0.05$
255	(255, 215, 5)
511	(511, 430, 9)
1023	(1023, 863, 16)
2047	(2047, 1739, 28)

TABLE 1: BCH Codes Used for Random-Error Channel

We then use equation (4) to calculate the corresponding expected wasted times. The results, shown in figures 6, 7 and 8, indicate that error-correction can substantially reduce the expected wasted time. For example, figure 7 shows that with error-correction, the minimum expected wasted time is reduced from about 17 seconds to 0.8 second.

2.2.2 Numerical Results for the Rayleigh Fading Channel

To obtain the distributions of the number of channel errors in packets of various lengths, a simulation program was written [6,7]. The results are displayed in figure 9 which gives the cumulative distribution function (CDF) of the number of errors in packets of lengths 255, 511, 1023 and 2047 bits. A channel bit error rate p_b of 10^{-2}, a channel rate of 4000 bits/sec, a Doppler frequency f_D of 25.5 H_z (corresponding to a vehicle speed of 20 MPH and carrier frequency of 850 MHz) and non-coherent FSK modulation were assumed. Fig. 10 shows the probability of getting one or more bit errors as a function of the packet length.

Using fig. 10, equation (3) was evaluated as a function of B for $\bar{L}$ = 1000, 2000 and 5000 bits. The results are shown in figures 11, 12 and 13 (curves labelled no error correction). It can be seen that for each value of $\bar{L}$ there is an optimal value of B which minimizes the expected wasted time.

BCH random error correcting codes were then used to correct enough channel errors say t to ensure that the probability of retransmission was no larger than 0.05 (or 0.1). The choice of the code to be used is made based on the packet length n and t (see table 2). Equation (4) was then used to calculate the corresponding expected wasted times. The results are shown in Figs. 11, 12 and 13. They show that the use of error-correction gives a substantial reduction in the expected wasted times. For example, Fig. 12 shows that with error-correction, the minimum expected wasted time per message is reduced from about 5.5 seconds to about 1 second. Similar improvements were found for $\bar{L}$ = 1000 and 5000 bits.

Packet Length	BCH (n,k,t) code used P_r=0.05	P_r=0.1
255	(255, 187, 9)	(255, 199, 7)
511	(511, 376,15)	(511, 412, 11)
1023	(1023, 808,22)	(1023, 838,19)
2047	(2047,1662,35)	(2047,1695,32)

TABLE 2: BCH Codes Used for Rayleigh Fading Channel

2.3 Effect of Forward Error Correction on Mean Time to Successful Transmission

In this section, we examine the same stop-and-wait scheme of the previous section from a different view point. Messages of fixed lengths (the case of variable lengths is being developed) are assumed to arrive at the transmitter according to a Poisson process. Messages are transmitted on a first-in, first-out basis. The effect of using error-correcting codes on the mean time S between the arrival of a message and its successful transmission (i.e. positive acknowledgement sent back by the receiver) is examined.

Using the Pollaczek-Khinchin mean value formula for M/G/1 queues [8], we obtain

$$S = \frac{1}{\mu}\left[1 + \frac{\frac{\lambda}{\mu}(1+\mu^2\,\sigma_b^{\,2})}{2(1-\frac{\lambda}{\mu})}\right] \qquad (6)$$

where λ = arrival rate

$\frac{1}{\mu}$ = mean service time

$\sigma_b^{\,2}$ = variance of service time

For the stop-and-wait scheme, the distribution of the number of transmissions D required till a message (packet) is successfully transmitted (assuming independent transmissions) is given by

$$P\ (D = i) = (1 - P_r)\ P_r^{\,i-1}\ ,\quad i = 1, 2, 3, \ldots\ldots \tag{7}$$

The mean and variance of the distribution of (7) is given by

$$\bar{D} = \frac{1}{1 - P_r} \tag{8}$$

$$\text{Var } D = \frac{P_r}{(1-P_r)^2} \tag{9}$$

Each transmission (and acknowledgement) takes (A + T) seconds.

Therefore in equation (6),

$$\frac{1}{\mu} = \frac{1}{1 - P_r}(A+T) \tag{10}$$

$$\sigma_b^{\,2} = \frac{P_r}{(1-P_r)^2}(A+T)^2 \tag{11}$$

2.3.1 Numerical Results for the Random-Error Channel

For packet lengths n = 255, 511 and 1023, the BCH codes used to achieve a probability of retransmission $P_r \leq 0.05$ can be obtained from table 1. Equation (6) can then be used to determine S when error correction is used, assuming A = 0.2 sec and $T = \frac{n}{4000}$ sec. Plots of S against the arrival rate λ are shown in figs. 14, 15 and 16 for B = 185, 400 and 833 bits (b = 30 bits assumed). The number of information bits B in a packet is of course n - b - p.

With no error correction, the packet lengths n' would be given by n' = 215, 430 and 863 bits. The corresponding P_r is determined from equation (5). As before, equation (6) is then used to calculate S. The results are plotted in figs. 14, 15 and 16 (curves labelled no error correction), and show that for a given arrival rate λ, S can be significantly reduced using forward error correction. Also the maximum (asymptotic) value of λ is increased with error correction, e.g. in figure 15, λ_{max} increases from 0.04 to 2.85.

2.3.2 Numerical Results for the Fading Channel

From table 1, we know the BCH codes to be used for achieving a value of $P_r \leq 0.05$ for packet lengths n = 255, 511 and 1023. Assuming a transmission rate of 4000 bits/sec, the transmission time $T = \frac{n}{4000}$ sec. This together with an acknowledgement delay A of 0.2 sec were used to determine S in equation (6). The results are shown in figures 17, 18 and 19.

If no error correction was used, the packet lengths n' would be given by n' = 187, 376 and 808 respectively. The corresponding P_r can be determined from fig. 10. As before this was used together with $T = \frac{n'}{4000}$ sec, and A = 0.2 sec in equation (6) to solve for S. The results are shown in figures 17, 18 and 19 (curves labelled no error correction) and indicate that performance is substantially enhanced by using error correction. As an example, in figure 18 with error correction, the maximum (asymptotic) value of λ is increased from 0.94 to 2.9.

2.4 Concluding Remarks

The results obtained in the last two sections indicate that the use of error-correcting codes can lead to significantly better system performance in a stop-and-wait ARQ scheme. In practice this improvement has to be weighed against the cost and complexity of using the error-correcting code. The results presented so far used BCH codes as random error-correcting codes. These can also be used as burst-error-correcting codes for the fading channel [9]. However we consistently found that using the BCH code in a random-error-correcting mode yielded a higher fraction of correctable packets. This agrees with the general conclusion in [10] based on actual channel error measurements on a mobile radio channel. It might be pointed out however that decoders for burst error correction are simpler and less expensive.

We conclude this chapter with a few remarks about other methods for improving the transmission of data over fading channels. Bit interleaving [5] may be used to disperse the errors that occur in "bursts" when the received signal fades. As the degree of interleaving increases, the fading channel packet error distribution approaches that of the random error channel. Therefore as indicated by the results in section 2.2.1, bit interleaving coupled with (random) error correction can be quite effective. It should be noted however that with bit interleaving, a packet is received essentially only when all interleaved packets have been received.

Another technique for combatting the fades on a Rayleigh-fading channel is diversity transmission [11]. In time diversity, the same packet is repeated several times (after some appropriate time interval) in the hope that not all transmissions will be hit by a deep fade. Another common

implementation is space diversity in which several antennas are used to reduce the probability that the received signal at all the antennas will be simultaneously subject to a deep fade. It is planned that space diversity will be used in the Bell System Advanced Mobile Phone Service (AMPS) currently being tested [12].

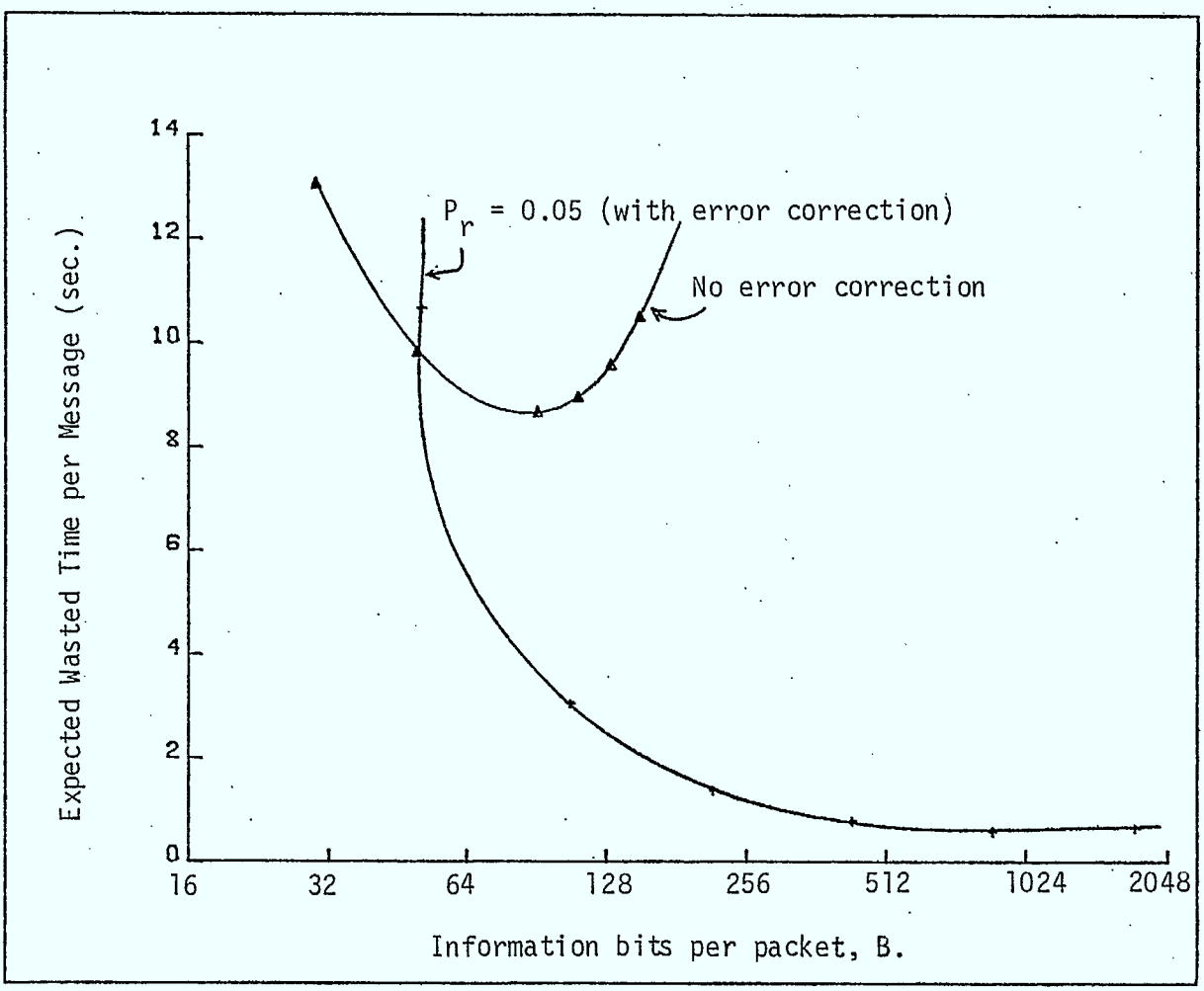

Figure 6

Expected Wasted Time Against B for random error channel

with $p_b = 10^{-2}$

R = 4000 bits/sec.

$\bar{L}$ = 1000 bits

A = 0.2 sec.

b = 30 bits

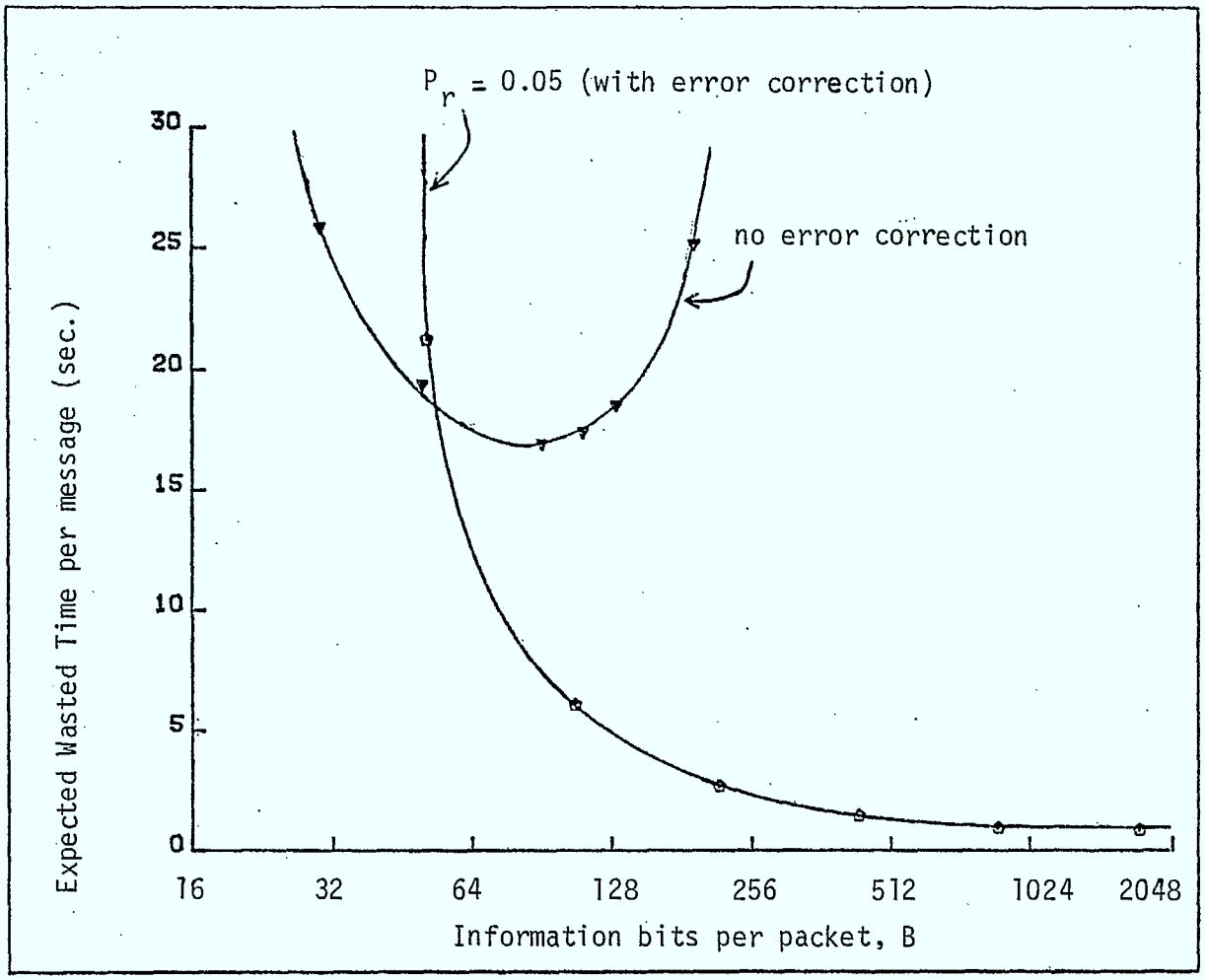

Figure 7

Expected Wasted Time against B for random error channel

with $p_b = 10^{-2}$

R = 4000 kits/sec.

$\overline{L}$ = 2000 bits

A = 0.2 sec.

b = 30 bits

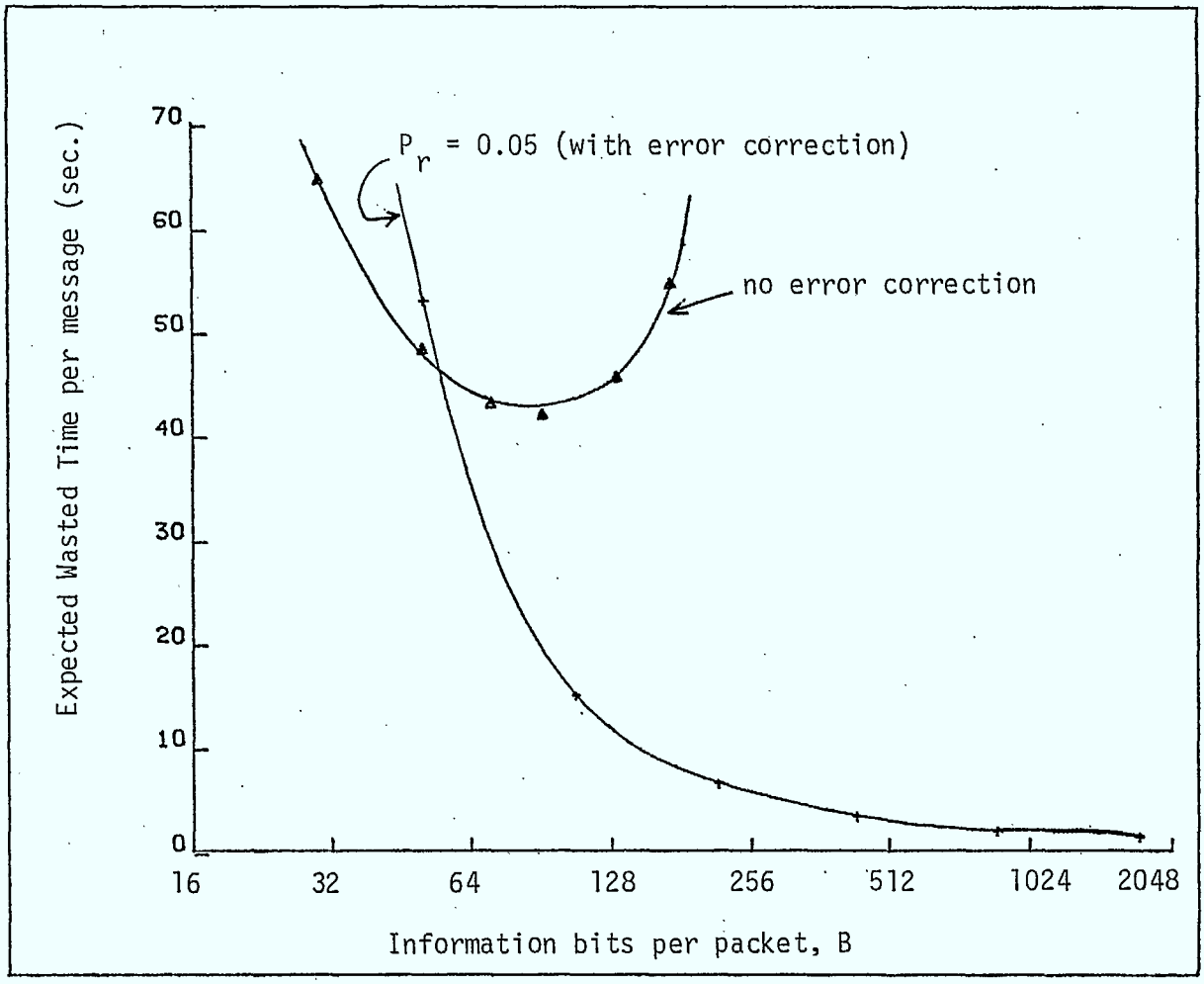

Figure 8

Expected Wasted Time against B for random error channel

with $p_b = 10^{-2}$

R = 4000 bits/sec.

$\overline{L}$ = 5000 bits

A = 0.2 sec.

b = 30 bits

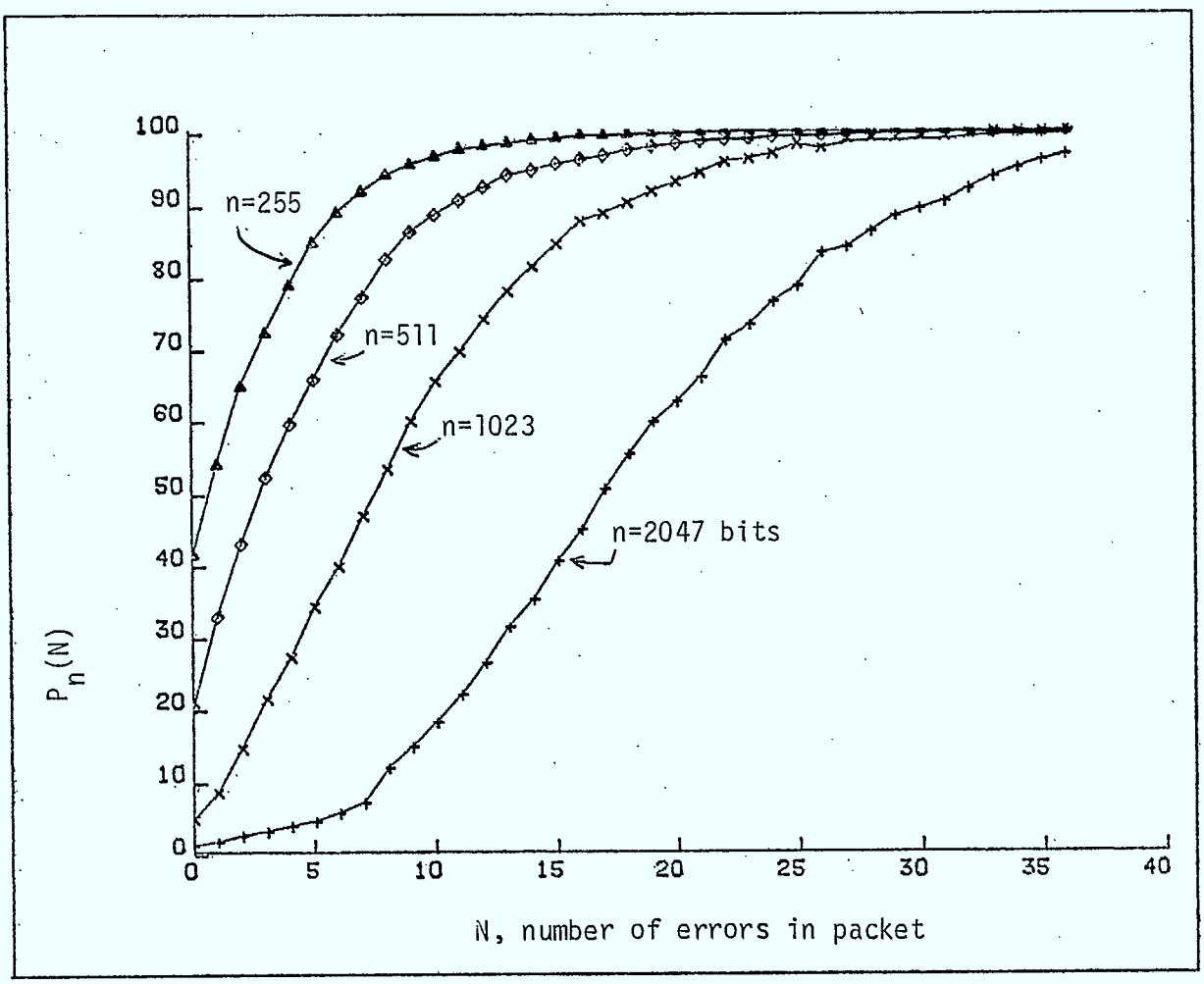

Figure 9

CDF, $P_n(N)$ of number of errors in packets of lengths n for Rayleigh fading channel with $p_b = 10^{-2}$, $f_D = 25.5$ Hz and transmission rate R = 4000 bits/sec.

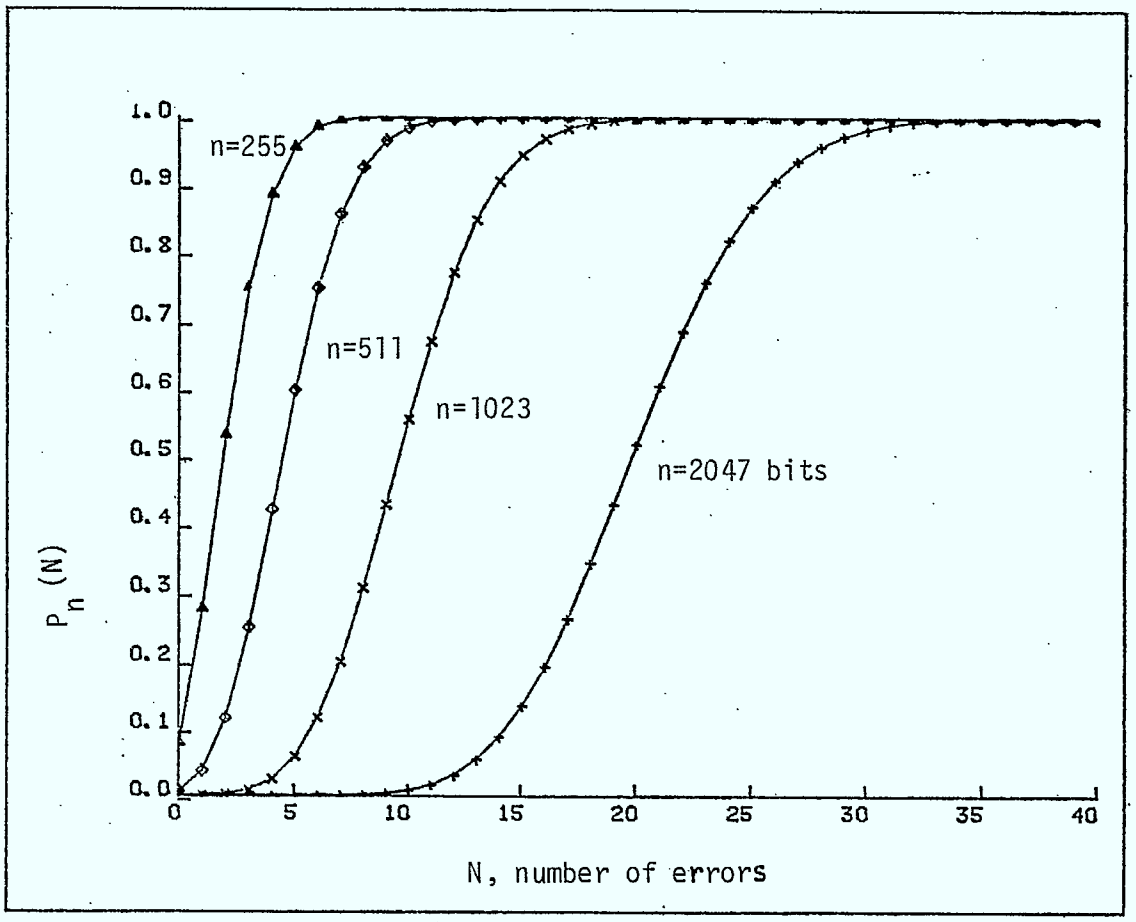

Figure 9(a)

CDF, $P_n(N)$ of number of errors in packets of lengths for n Random channel with $p_b = 10^{-2}$ and transmission rate R = 4000 bits/sec.

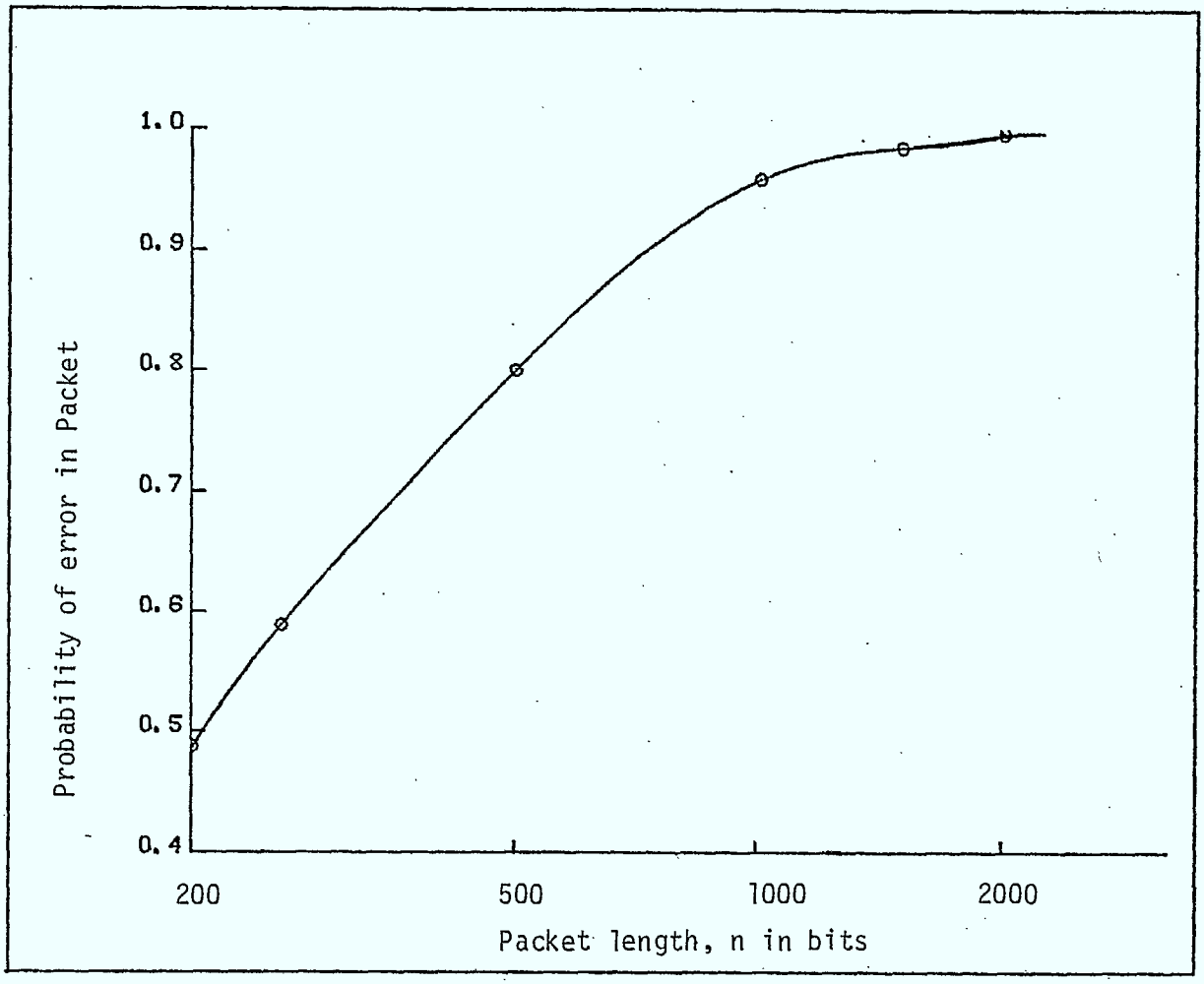

Figure 10

Packet error rate as a function of packet length for Rayleigh fading channel with $p_b = 10^{-2}$, $f_D = 25.5$ Hz, transmission rate R = 4000 bits/sec.

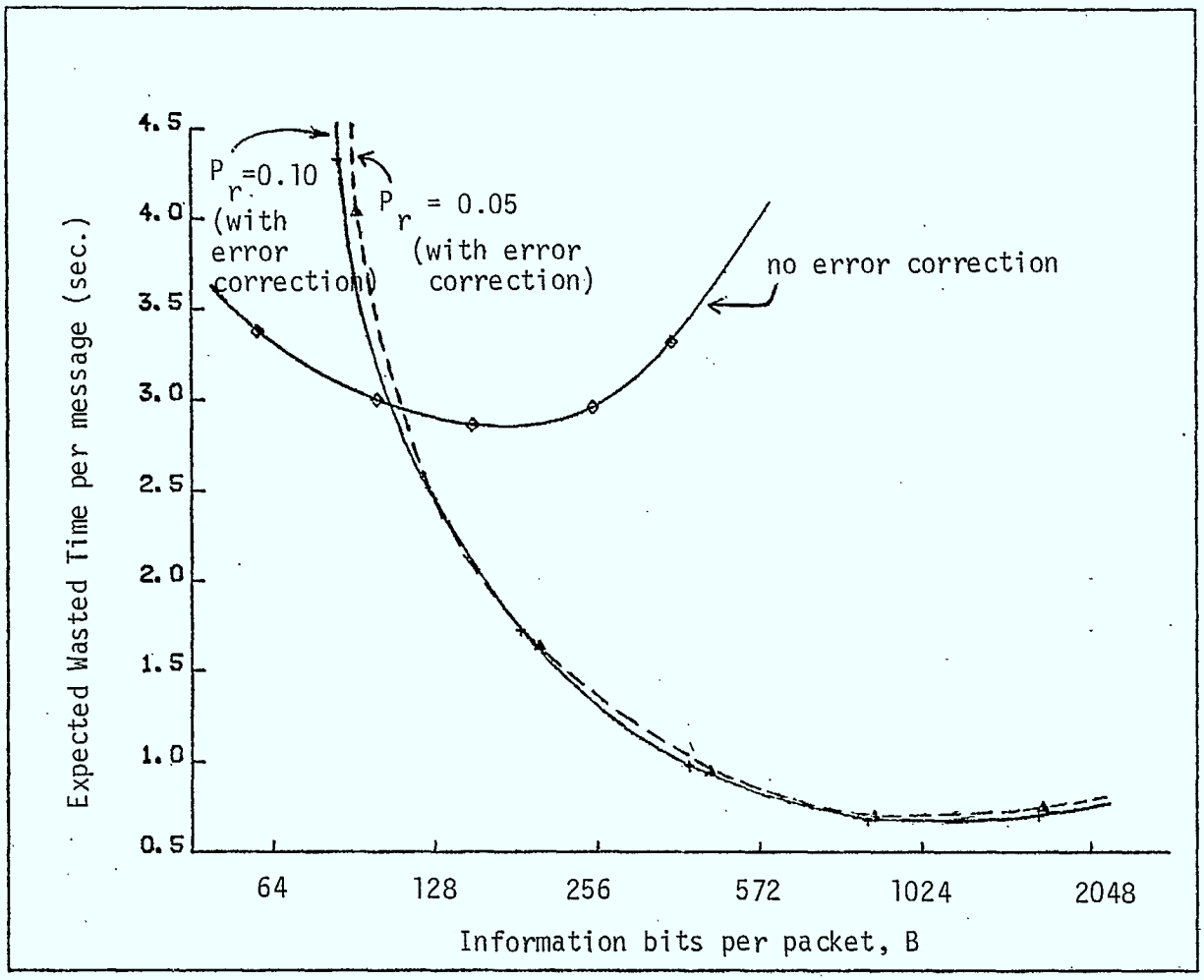

Figure 11

Expected Wasted Time against B for Rayleigh fading channel with $p_b = 10^{-2}$

R = 4000 bits/sec.

$\overline{L}$ = 1000 bits

A = 0.2 secs.

b = 30 bits

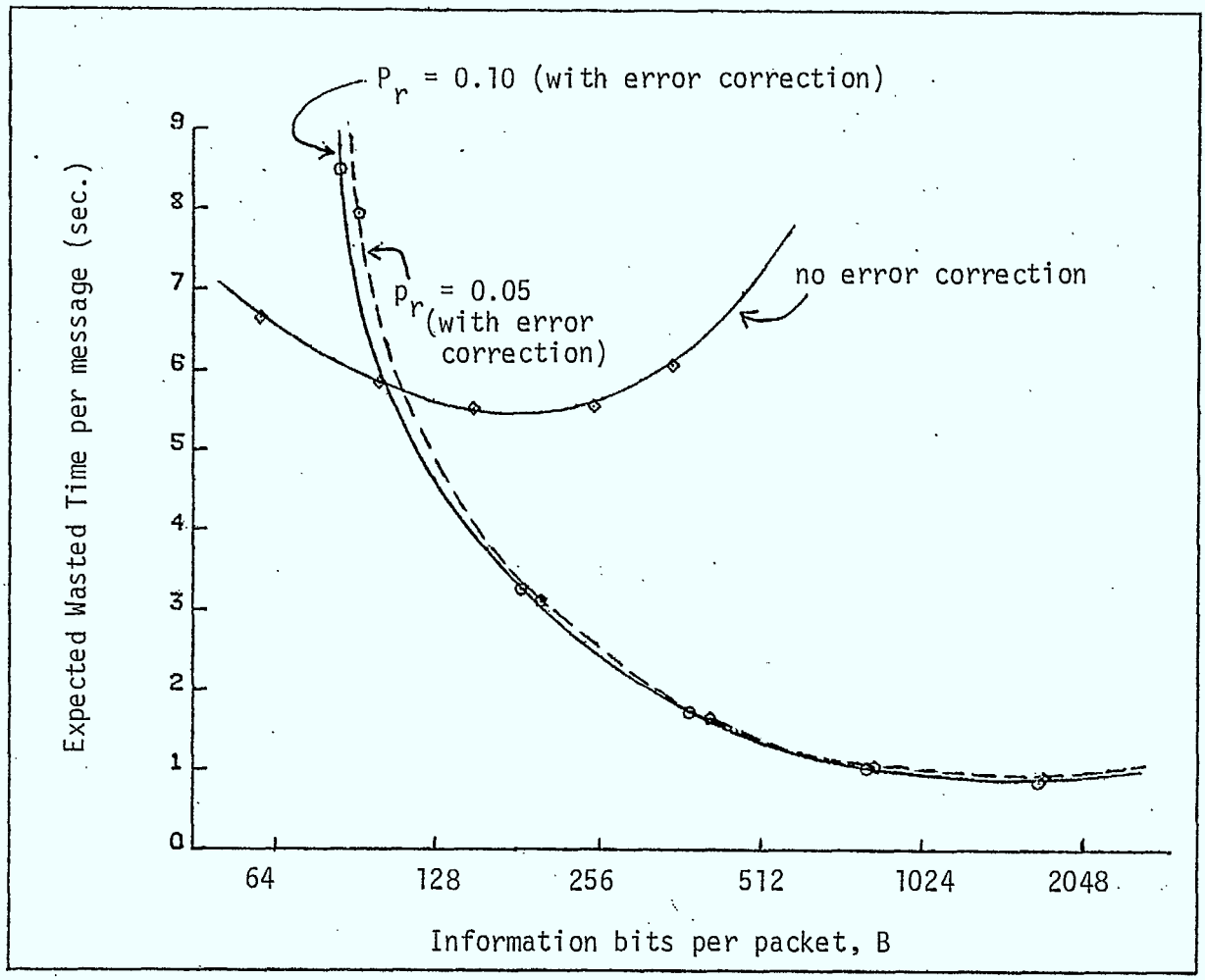

Figure 12

Expected Wasted Time against B for Rayleigh fading channel with $p_b = 10^{-2}$

R = 4000 bits/sec.

$\bar{L}$ = 2000 bits

A = 0.2 sec.

b = 30 bits

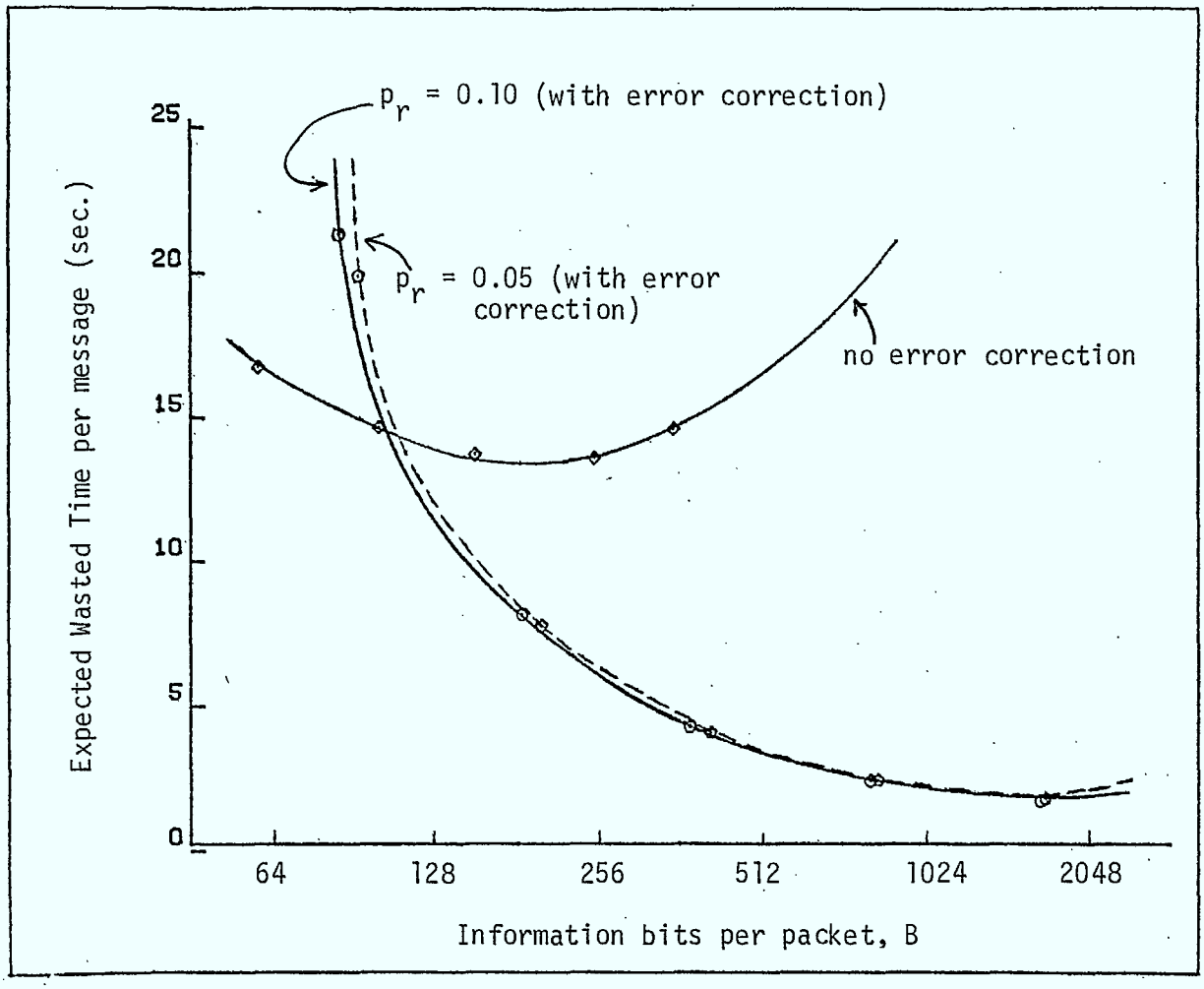

Figure 13

Expected Wasted Time against B for Rayleigh fading channel

with $p_b = 10^{-2}$

R = 4000 bits/sec.

$\overline{L}$ = 5000 bits

A = 0.2 sec.

b = 30 bits

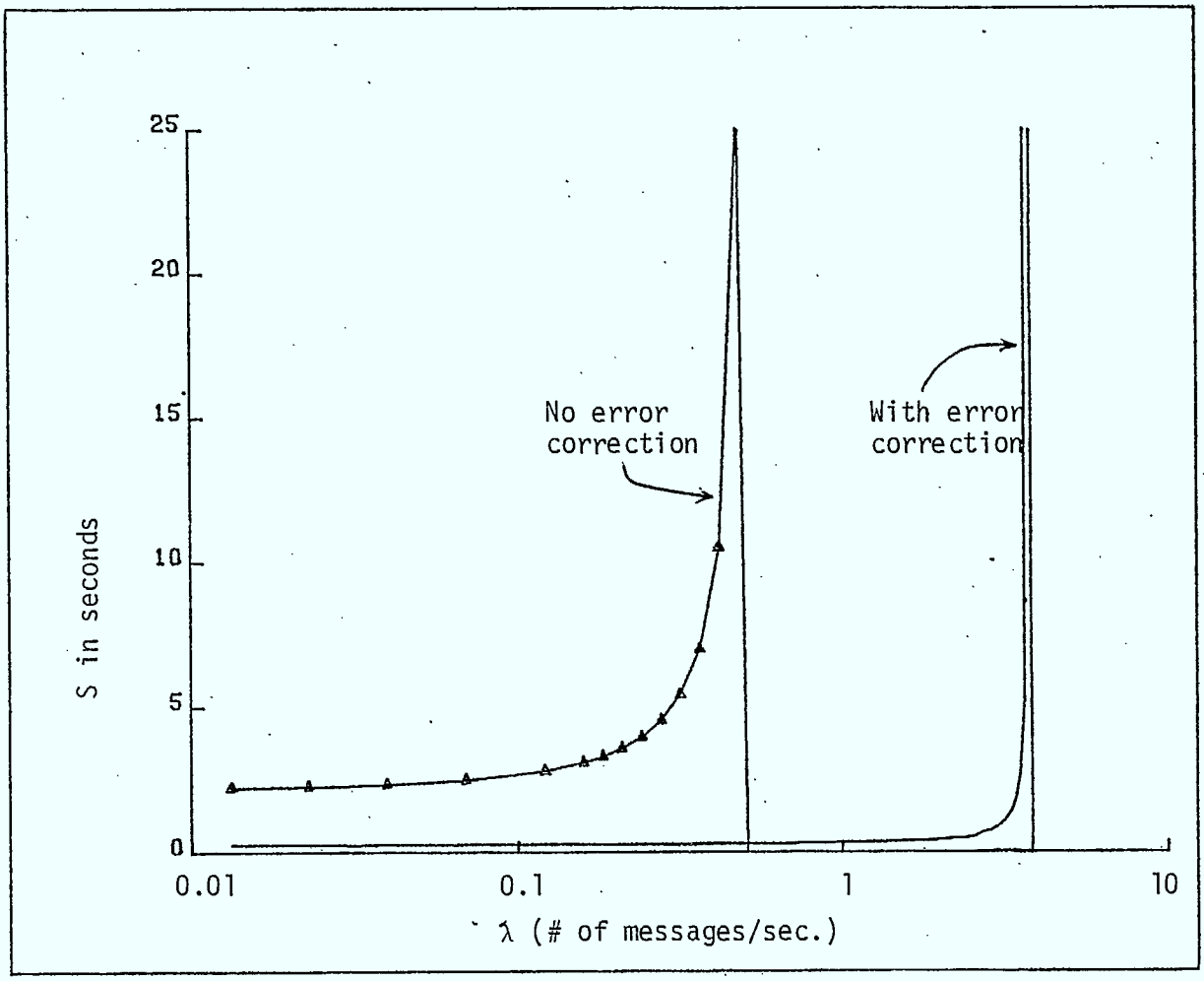

Figure 14

Plot of mean time to successful transmission against arrival rate for random error channel with A = 0.2 sec.

B = 185 bits

$p_b = 10^{-2}$

R = 4000 bits/sec.

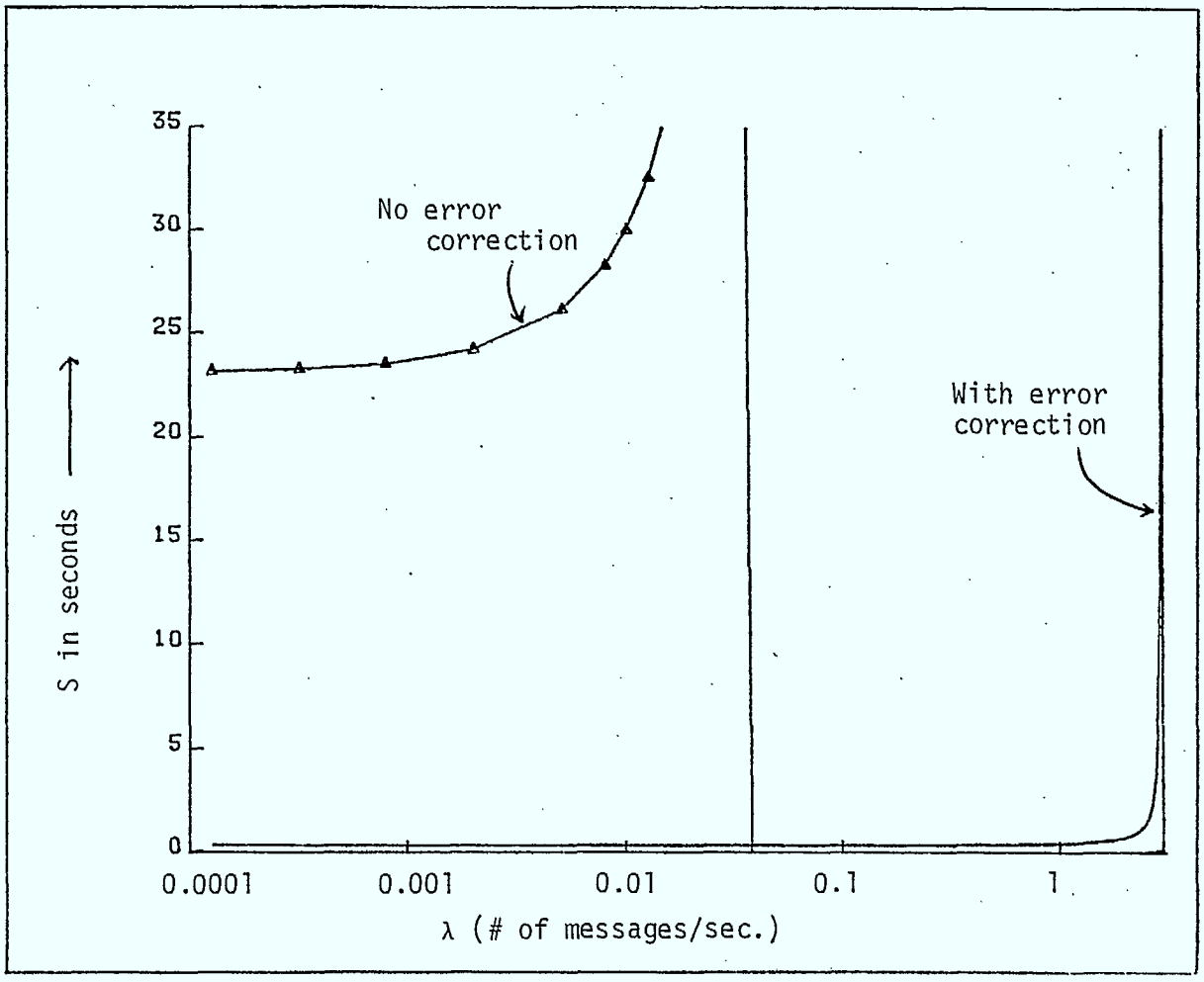

Figure 15

Plot of mean time to successful transmission against arrival rate for random error channel with A = 0.2 sec.

B = 400 bits

$p_b = 10^{-2}$

R = 4000 bits/sec.

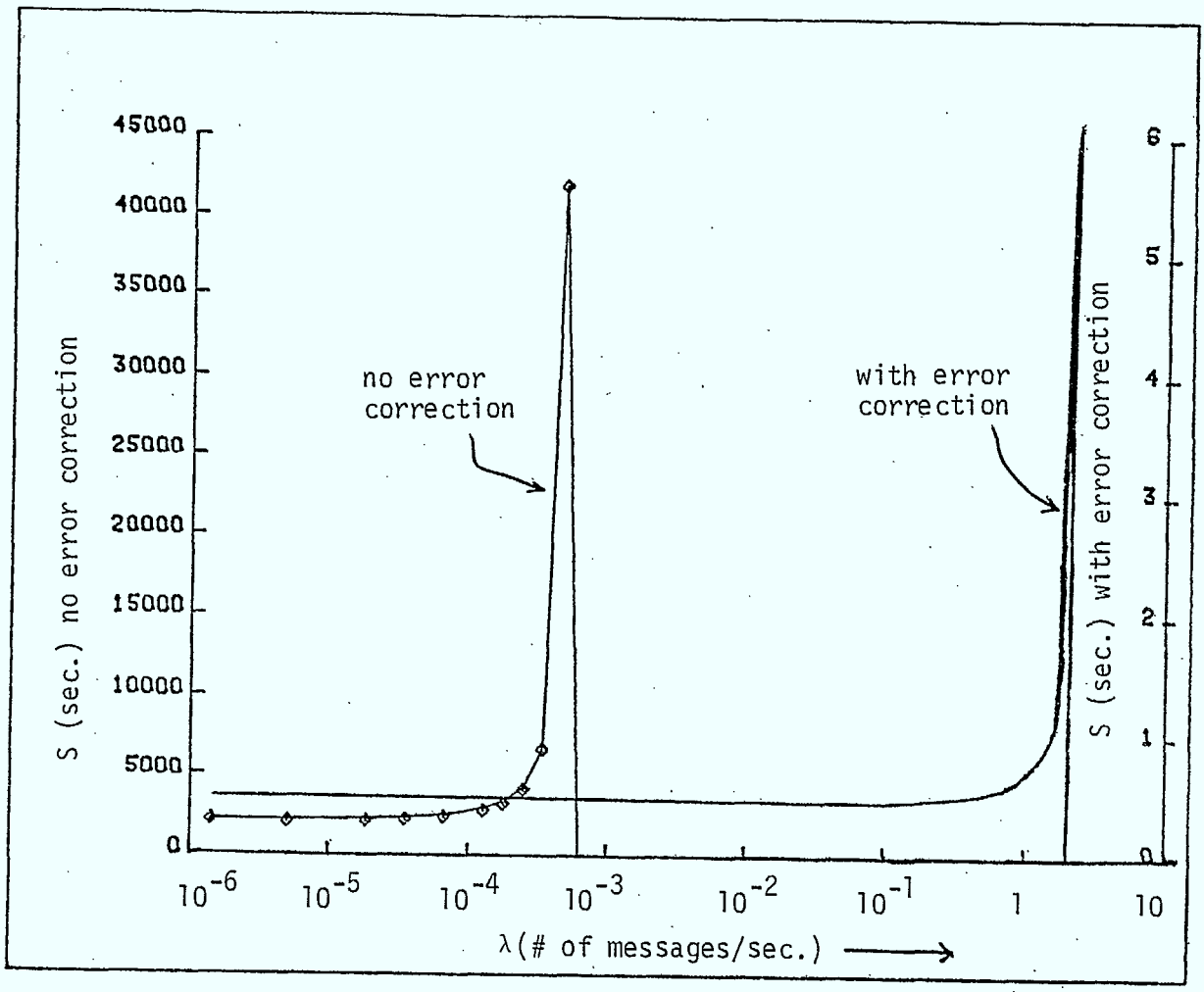

Figure 16

Plot of mean time to successful transmission against arrival rate for Random Error Channel with A = 0.2 sec.

B = 833 bits

$p_b = 10^{-2}$

R = 4000 bits/sec.

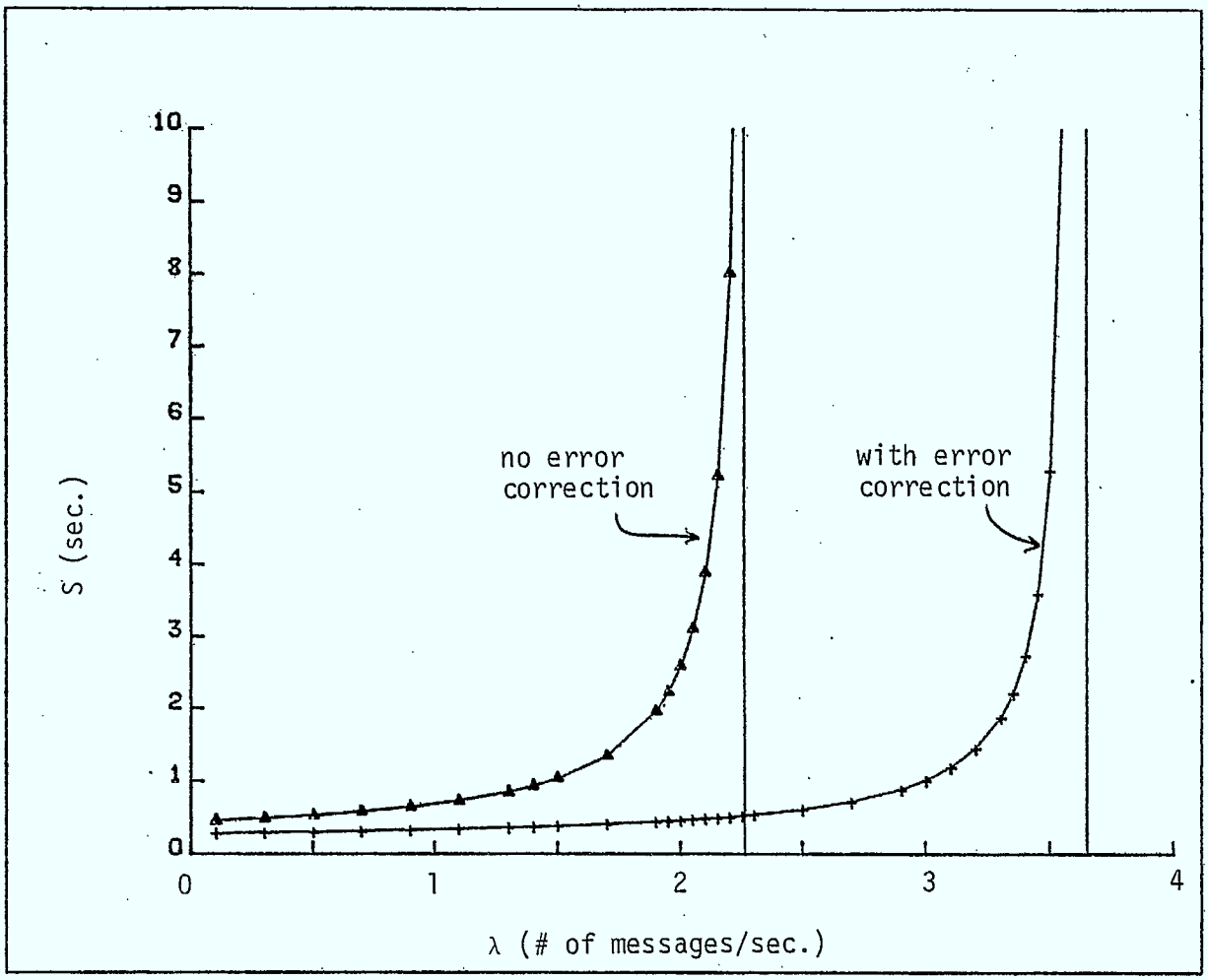

Figure 17

Plot of mean time to successful transmission against arrival rate for Rayleigh fading channel with A = 0.2 sec.
B = 187 bits
$p_b = 10^{-2}$
R = 4000 bits/sec.

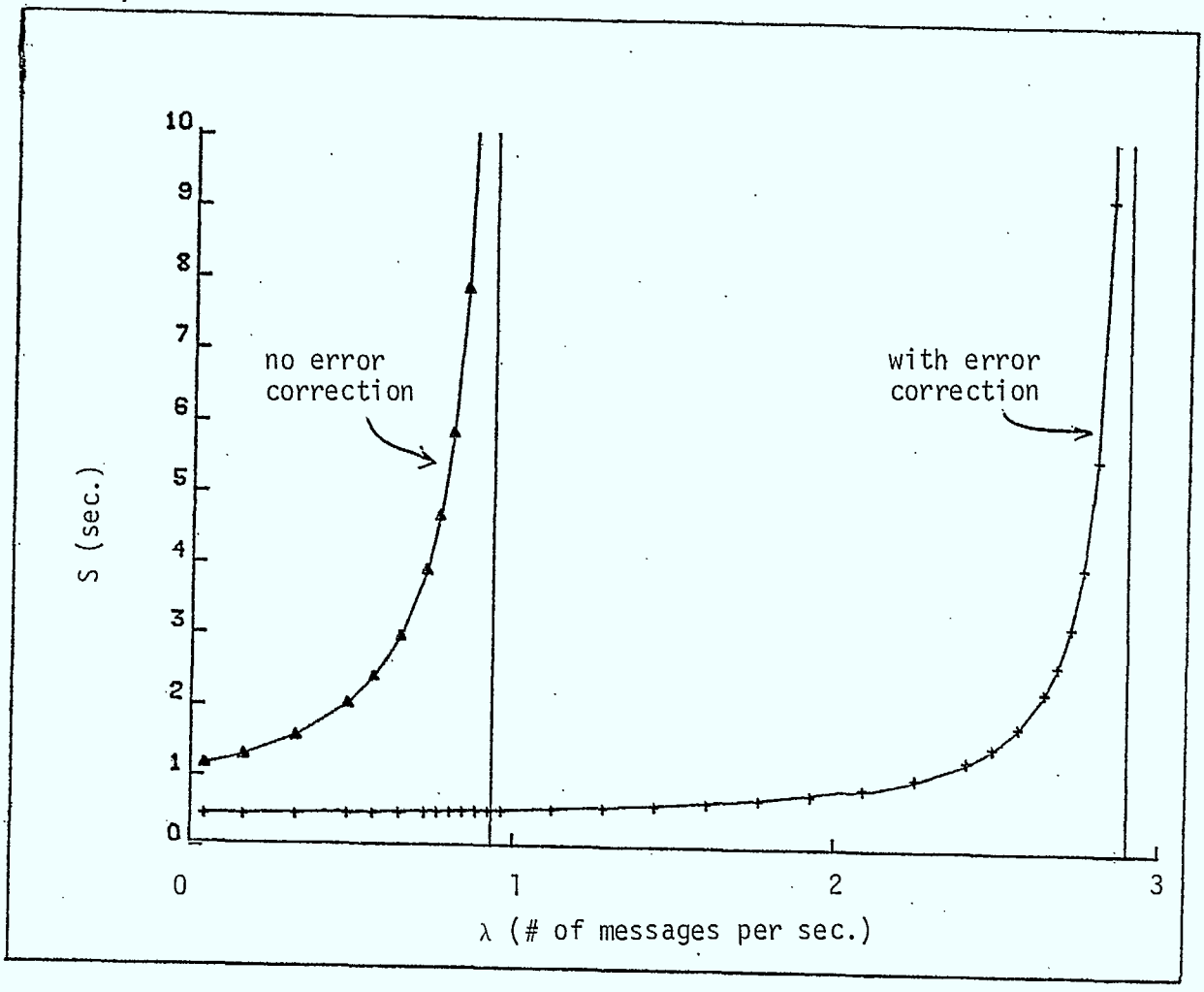

Figure 18

Plot of mean time to successful transmission against arrival rate for Rayleigh Fading Channel with A = 0.2 sec.
B = 376 bits
$p_b = 10^{-2}$
R = 4000 bits/sec.

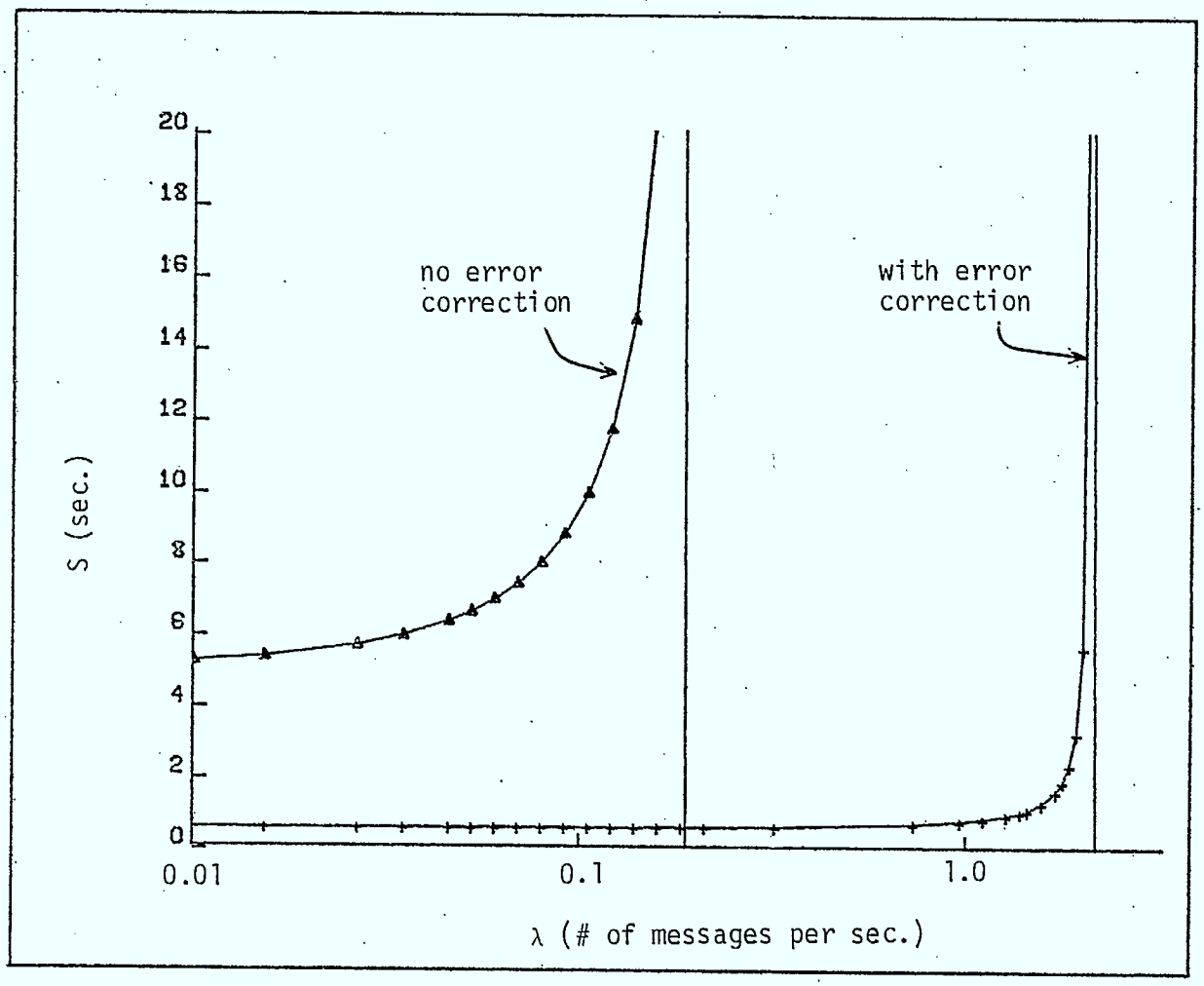

Figure 19

Plot of mean time to successful transmission against arrival rate for Rayleigh fading channel with A = 0.2 sec.
B = 808 bits
$p_b = 10^{-2}$
R = 4000 bits/sec.

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CHAPTER 3

Design and Implementation of Low Power Microprocessor

3.1 Introduction

This chapter describes a CMOS microcomputer which was developed as a replacement for the Intel SBC 80/204 CPU board used in portable Packed Radio Terminals. The main design goals were: reduced power dissipation, compatibility with previously developed software code (for the 8080 processor) and small size. The CMOS microcomputer described here contains 8K bytes of EPROM, 4K bytes of RAM, two 8 bit I/O parts, one serial RS-232 port and a CPU. The power consumption was reduced from 33.64W to 0.771W at no loss of performance (compared to Intel SBC 80/204). The only N-MOS part in the whole board is the 8085 CPU. Replacement of this CPU by the National Semiconductor NSC-800 CMOS CPU will result in further reduction of power dissipation to about 0.375W for the whole CPU board.

3.2 Architecture of the CMOS Microprocessor

The term computer architecture refers to the programmers' view of a particular machine, i.e. its instruction set, I/O arrangement and register set.

The architecture of the CMOS microcomputer is shown in Figs. 20 and 21. In addition to the CPU, static RAM and EPROM modules, the architecture contains one serial port for interfacing to the modulator/demodulator circuit, and two parallel ports for keyboard interface and radio transmitter control.

The instruction set of the CMOS microcomputer board (8085 CPU) is exactly the same as that of the SBC 80/204. This assures software compatibility between the two CPU boards. The NSC 800 CMOS CPU which will replace

the 8085 CPU used in the CMOS microcomputer has an Z-80 instruction set. The Z-80 instructions are a superset of the 8080 instructions, containing within it all seventy eight 8080 instructions. The NSC 800 CPU will be available in June 1980.

The CMOS CPU board has one serial port, two parallel ports and buffers to interface the display board controller.

The serial port is interrupt driven for both the transmitter and receiver port. The RS 232 interface enables it to be directly connected to the modem of the Packet Radio Terminal. Both receiver and transmitter clocks are derived from the modem. RS 232 buffers are provided for the clock input.

One of the 8 bit parallel ports is connected as an input from the keyboard, while the other controls the radio transmitter (one bit output).

The display board controller is seen by the CPU as memory locations. Therefore, only buffers were needed to facilitate its connection to the address and data buses of the computer.

The ICM 755 timer is used as a real time clock for process switching. It is connected to interrupt 5.5 of the CPU.

A detailed description of the components used in the microprocessor board is included in Appendix B.

3.3 Implementation of the Microprocessor Board

The prototype of the CMOS microcomputer board was implemented on an Intel SBC-905 prototype board. The physical dimensions of that board are the same (12 x 6.75 inches) as the standard SBC 80/204 board size. All the circuitry of the CMOS microcomputer occupies approximately two thirds of the board, leaving enough room for future expansion of memory or I/O. All connections between integrated circuits were wire wrapped. This method of interconnection is very reliable, and allows quick changes needed during prototype development.

The memory chips used for the RAM memory banks are Harris HM 6514 static 1024 x 4 CMOS RAMS with an access time of 300 nsec. This RAM chip is housed in a 18 pin dual in-line package.

The EPROM section uses the Intersil IM6654 CMOS EPROM. This device has an organization of 512 x 8 bits and is housed in a 24 pin dual in-line package. The programming of the IM6654 EPROMS was done on a Data I/O programmer, using a special personality module. The erasure time for these EPROMS is 30 minutes, using the UVS-11 ultra-violet source.

Serial interface uses the Intersil IM6402 UART. This CMOS UART consumes only 10 miliwatts and can operate up to speeds of 200K bits per second. The UART uses an external clock, supplied by the modem. The two parallel I/O ports were implemented using the RCA CDP 1852 eight bit I/O port.

The N-MOS CPU used is the Intel 8085. This CPU runs with a crystal 6.144 MHZ and has four interrupt lines. Two of the interrupt lines are used for the UART transmitter and receiver respectively, the third one is used for the systems clock and the fourth interrupt is used for the keyboard.

The whole microcomputer board, with the exception of the RS 232 interface, runs on single 5V power supply and a current of 135 miliamperes. The RS-232 serial interface requires ± 12v at 4 miliamperes.

3.4 Testing and Performance

The testing was performed initially with a HP logic analyser up to the point where the CPU was accessing the EPROM memory bank. From that point on, software test routines were used for the testing. These software routines were first burned into the EPROMS and then plugged into the microcomputer where they performed the testing together with the CPU. For this reason, software routines were written and used to test and debug all the EPROM sockets, all the RAM sockets, the parallel I/O ports and the serial I/O port. To verify the proper operation of the serial RS 232 port, a complete I/O routine has been written and a serial communication link with a LA 36 Decwriter has been successfully tested. A sample of the test routines is given in Appendix A.

3.4.1 Speed

The 8085 CPU is running at a clock frequency of 6.144 MHZ. This gives a minimum instruction cycle of 1.3 microseconds.

3.4.2 Power Dissipation

The actual power dissipation was measured in the HALT state and also while the CPU was running a typical program. The program used is shown in Appendix A under the heading of "Memory Test Routine".

The power dissipation under running condition is approximately 50 miliwatts higher than in the stopped state. This is typical of CMOS

circuits. These circuits dissipate negligible power during idle states with the major power dissipation occuring during switching.

Power dissipation

	5V	+12V	-12V	Total W
CPU idle	125mA	4mA	4mA	0.721
CPU running	135mA	4mA	4mA	0.771

3.5 Future Improvements

Several improvements are expected to be incorporated in the CMOS microprocessor board in the near future. A summary of these improvements follows:

1. The power dissipation could be drastically reduced (by approximately 0.4 watts) by replacing the Intel 8085 CPU with a National Semiconductor CMOS CPU P/N NSC 800.

This CPU dissipates a mere 0.05 watts, operates at the same speed and has the same pinout as the 8085 CPU.

2. Replacement of the 6514 4K RAM chips with the RCA 16K CMOS RAM would reduce the number of RAM chips required from eight to two.

3. Using higher density EPROMS would also reduce the chip count.

4. The RAM and ROM space (combined) can be enlarged to 64K. The maximum I/O port capability is 256 ports.

5. Changing the computer architecture into a pipeline organization would increase the speed of the computer to a point where real time digital signal processing would be possible. Thus some of the modulator/demodulator functions could be incorporated into the CMOS microprocessor. This would

result in further reduction in the total power consumption of the packet radio terminal.

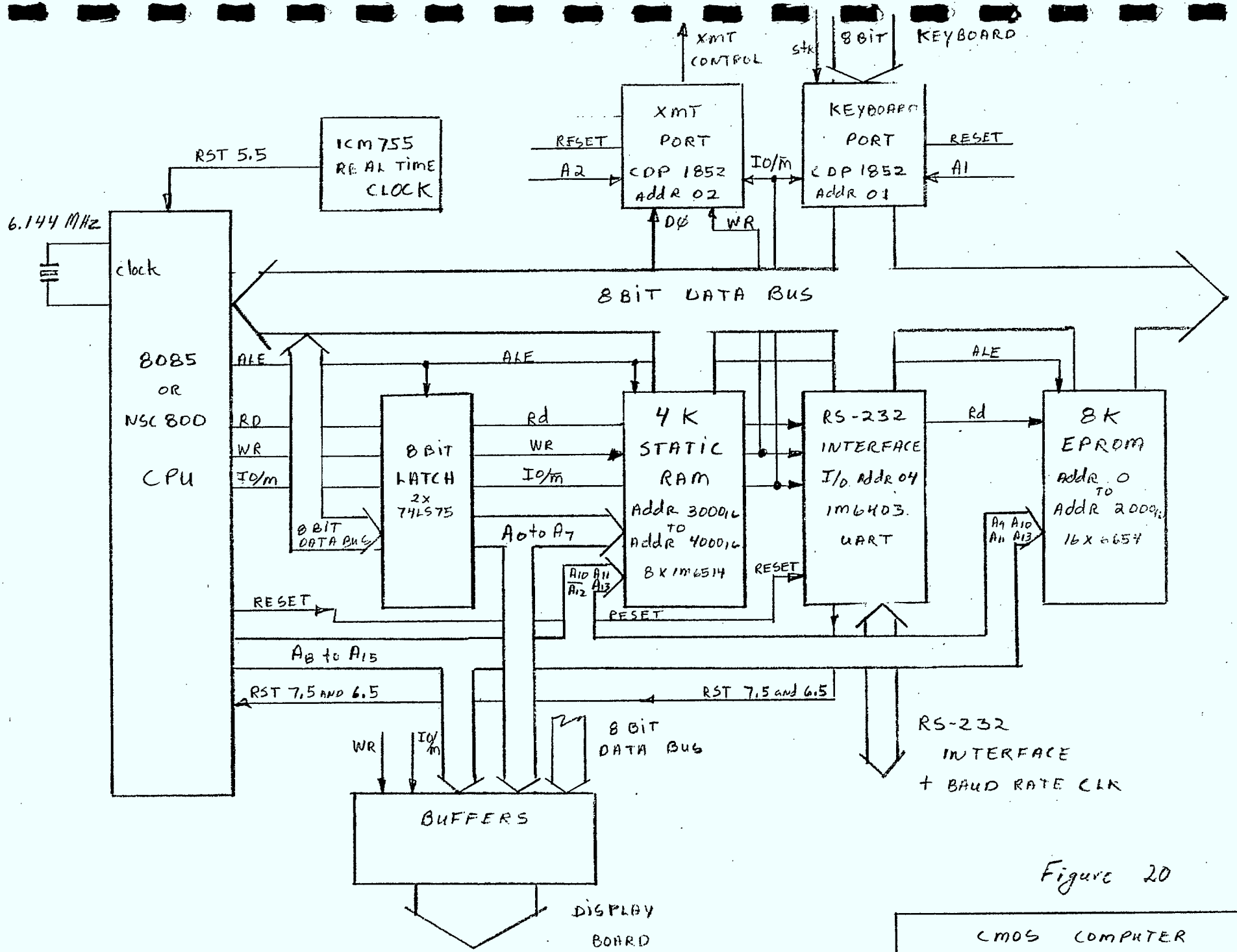


Figure 20

CMOS COMPUTER BLOCK DIAGRAM	
FEB 80	

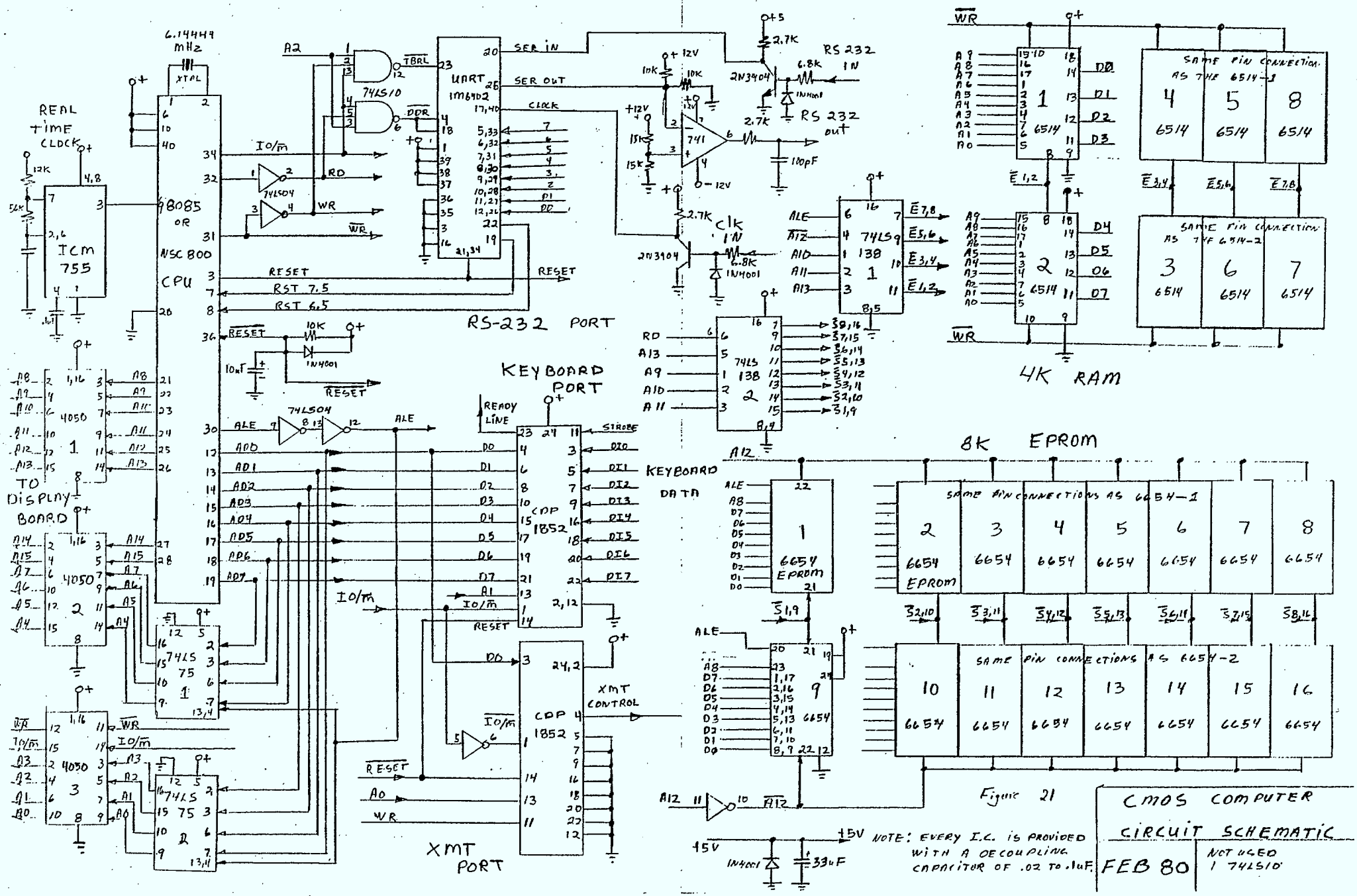
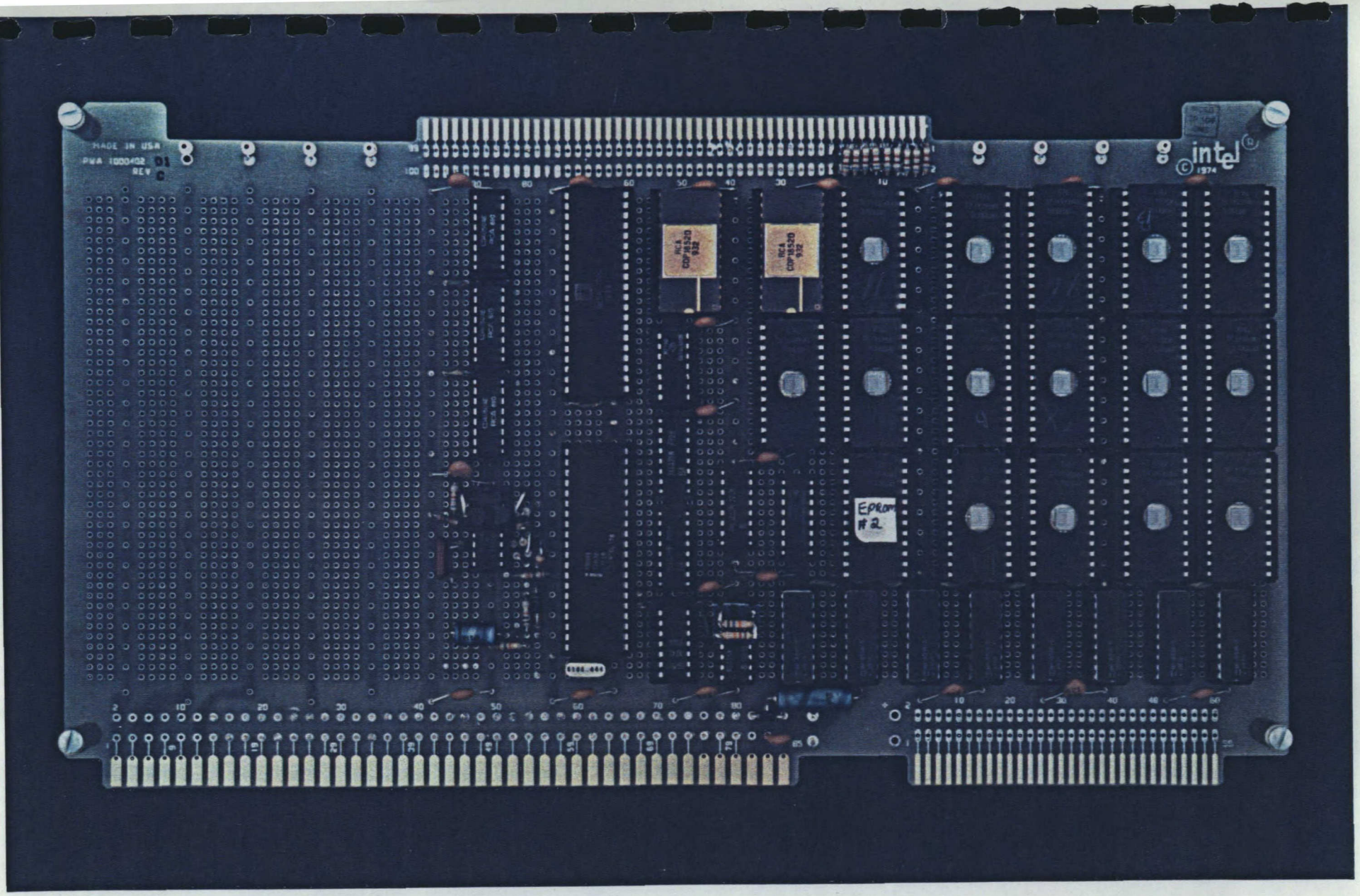
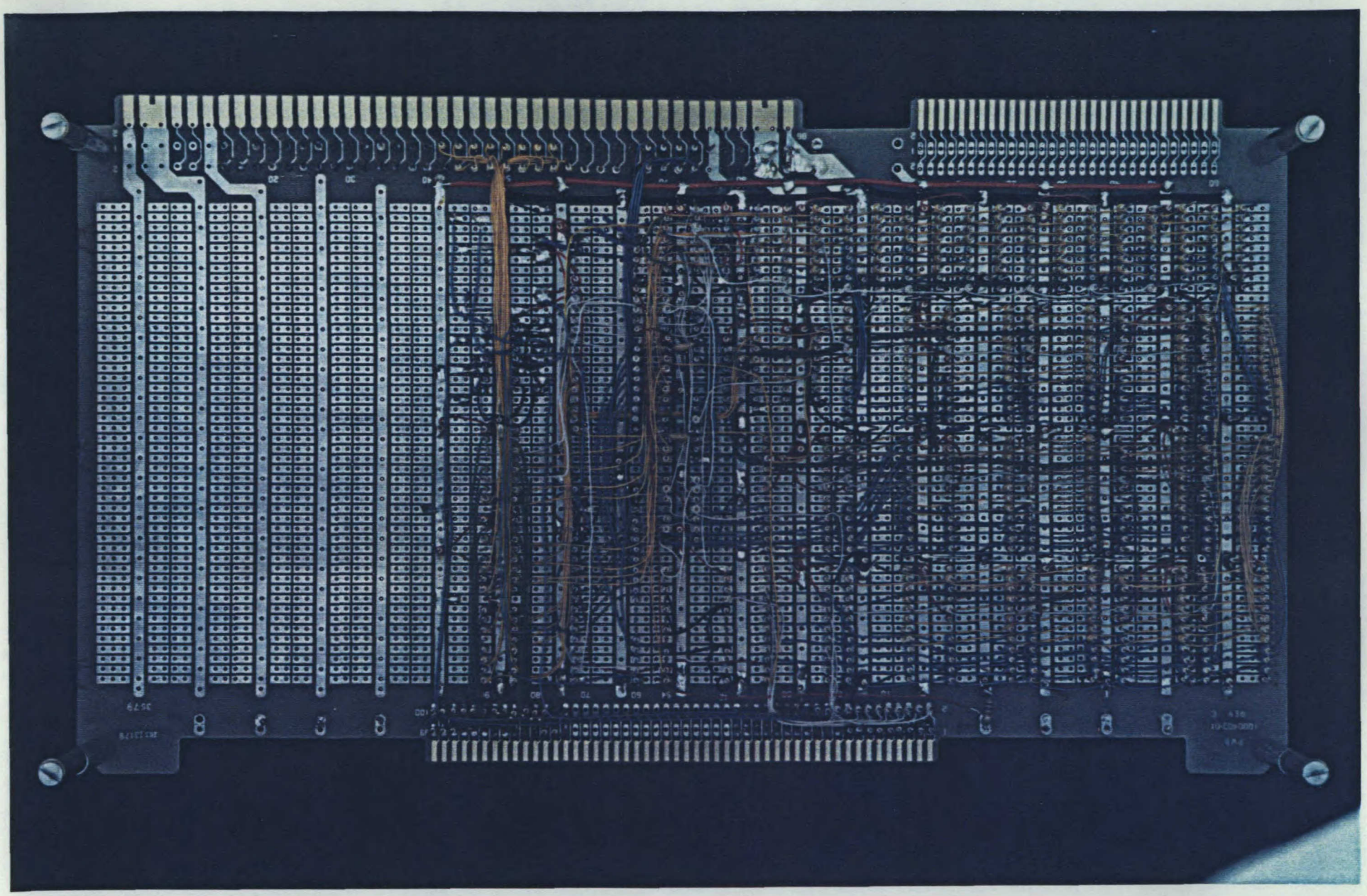

6.144MHz
XTAL
REAL time CLOCK
ICM 755
8085 OR NSC 800 CPU
74LS10
UART 2B IM6402
SER IN
SER OUT
CLOCK
RESET
RST 7.5
RST 6.5
RS-232 PORT
RS 232 IN
RS 232 out
2N3904
2N3906
741
clk IN
74LS04
74LS138
4050
4030
74LS75
KEYBOARD PORT
READY LINE
STROBE
CDP 1852
KEYBOARD DATA
XMT CONTROL
XMT PORT
TO Display BOARD
4K RAM
8K EPROM
6514
6654 EPROM
SAME PIN CONNECTION AS THE 6514-1
SAME PIN CONNECTION AS THE 6514-2
SAME PIN CONNECTIONS AS 6654-1
SAME PIN CONNECTIONS AS 6654-2
NOTE: EVERY I.C. IS PROVIDED WITH A DECOUPLING CAPACITOR OF .02 TO .1uF
NOT USED 1 74LS10
CMOS COMPUTER CIRCUIT SCHEMATIC
FEB 80

Figure 21


MADE IN USA
PWA 1000402 01
REV C
intel
©1974
RCA COP8520 932
RCA COP8520 932
Epron #2



CHAPTER 4

MEASUREMENTS AND RESULTS

4.1 Introduction

This chapter describes the laboratory experiments which were set up to study the effects of Gaussian noise on differentially coherent phase-shift keying (DPSK) and Fast Frequency Shift Keying (FFSK) modulation schemes for non-fading and fading channels. The DPSK modem was obtained from the University of Hawaii Electrical Engineering Department where it was used in the ALOHA experiments. The data transmission rate is 9600 bits/sec. The FFSK modem with a data rate of 16 K bits/sec was designed at the Communication Research Center, Ottawa where it was used in field experiments involving transmission of digitized voice. Sections 4.2 and 4.3 present the experimental results obtained with the DPSK and FFSK modems used. In section 4.4, the fading simulator is described, along with tests for verifying its proper functioning. Continuing work on the design of a Tamed Frequency Modulation (TFM) modem is outlined in section 4.5.

4.2 DPSK Modem Experimental Set-up and Results

4.2.1 Theoretical Background

The DPSK modulation scheme makes use of the carrier phase of the preceding signaling interval to obtain a phase reference for use in demodulation [1]. The bit error rate for DPSK over an additive white Gaussian noise channel with two-sided noise spectral density $\frac{N_o}{2}$ is given by [2]

$$p_b = \frac{1}{2} e^{-\frac{E_b}{N_o}} \tag{12}$$

where E_b is the energy per bit.

This may be contrasted to coherent PSK (with a modulation index m = 1) for which the bit error rate is [1,3]

$$p_b = Q\left(\sqrt{\frac{2E_b}{N_o}}\right) = \frac{1}{2} \operatorname{erfc}\left(\sqrt{\frac{E_b}{N_o}}\right) \tag{13}$$

Using the approximation

$$Q(\alpha) \approx \frac{1}{\sqrt{2\pi}\alpha} e^{-\alpha^2/2} \tag{14}$$

which is quite accurate for $\alpha \geq 2$, equation (13) becomes

$$p_b \approx \frac{1}{2\sqrt{\pi\, E_b/N_o}} e^{-E_b/N_o} \tag{15}$$

Thus for $\frac{E_b}{N_o} \geq 2$, the bit error rates for DPSK and coherent PSK differ only by a factor $\sqrt{\pi E_b N_o}$. For $p_b \leq 10^{-4}$, this amounts to a loss of less than 1 db in signal-to-noise ratio. This makes DPSK a convenient means of providing a carrier reference for demodulation.

The probability of bit error when DPSK is used over a Gaussian noise channel which is subject to Rayleigh fading can be derived as in [3] and is given by

$$p_b = \frac{1}{2(1+\bar{E}_b/N_o)} \tag{16}$$

where $\bar{E}_b$ is the mean value of the received energy.

4.2.2 Experimental Set-up and Results

The block diagram of the experimental set-up is shown in Figure 22. Details of the fading simulator are given in section 4.4 and schematic diagrams for the DPSK modem are in Appendix C.

The experimental bit error rates for non-fading and fading channels as a function of the signal-to-noise ratio (mean SNR in the fading case) are shown in Figure 23. Also plotted are the theoretical curves obtained from equations (12) and (16). It can be seen that the experimental error rates are slightly higher than the theoretical values; however, there is generally good agreement between them with a maximum difference of about 1 dB in SNR.

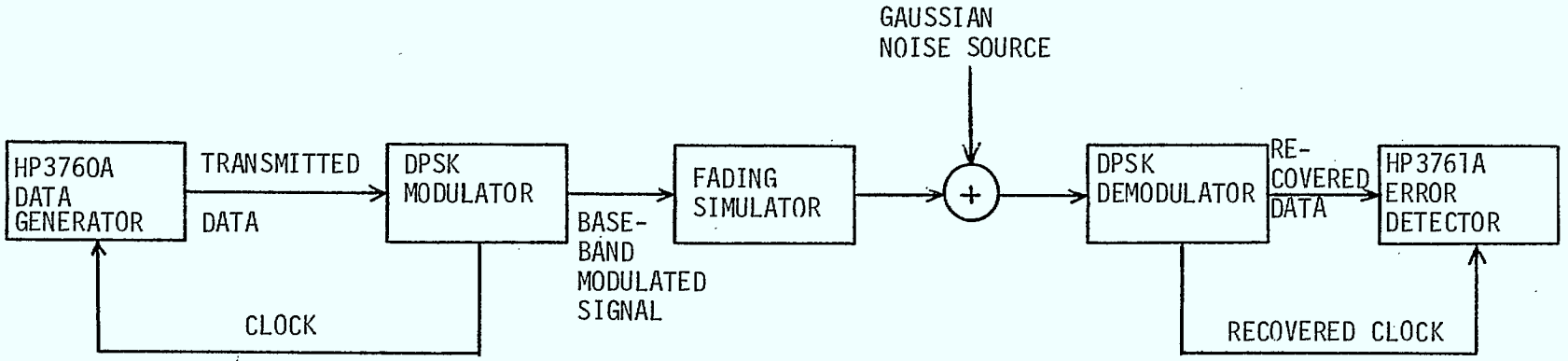


FIGURE 22: DPSK Experimental Set-Up

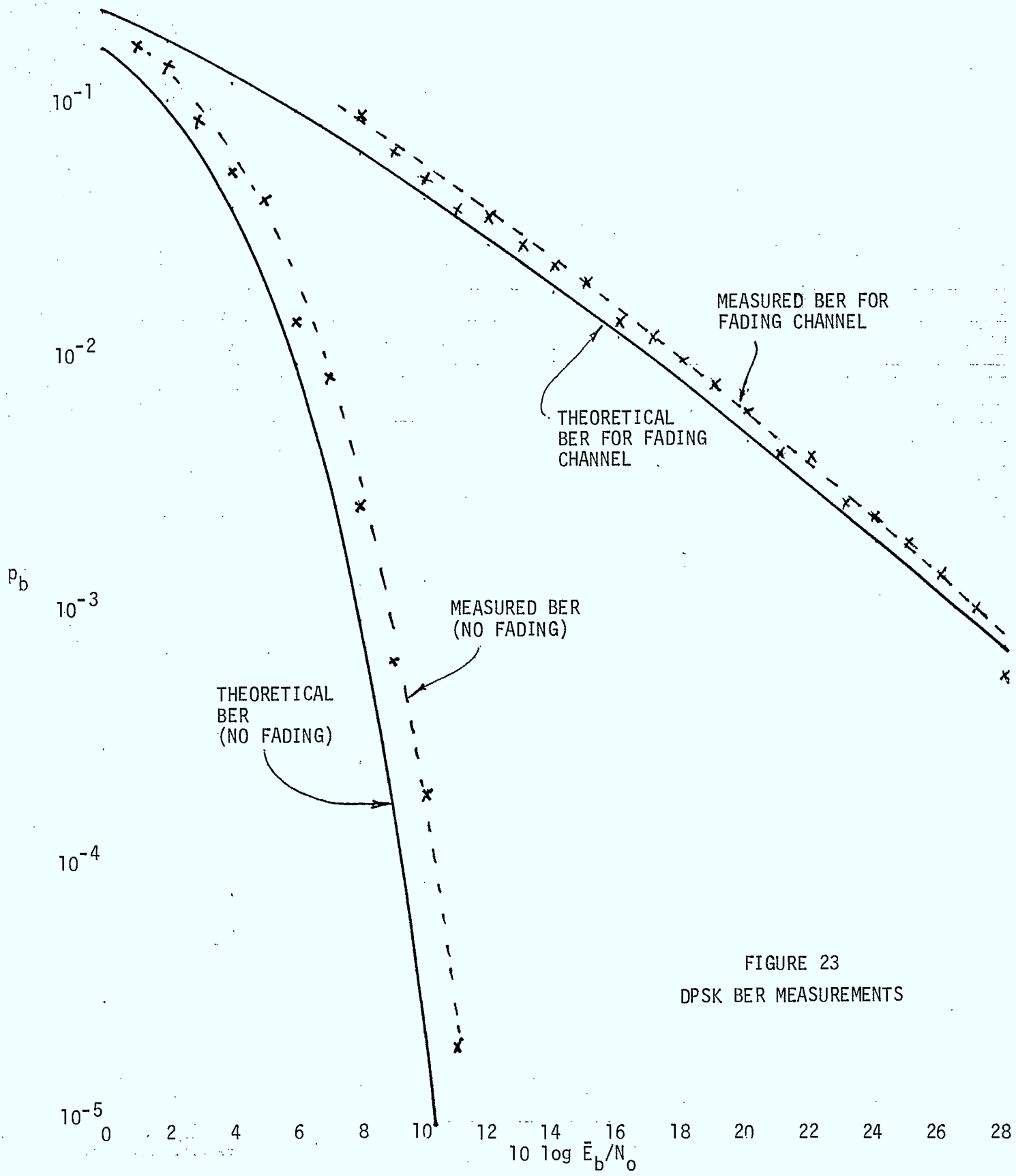


FIGURE 23

DPSK BER MEASUREMENTS

4.3 Measurements of the FFSK Modem Set

The Fast Frequency-Shift Keying (FFSK) is a coherent binary modulation technique which has the following properties [4]:

(1) it is phase coherent

(2) it has low deviation ratio, L = 0.5

(3) it occupies a band width which is typically 0.75 times the bit rate, without need for intersymbol interference correction

(4) it uses as receiver a self-synchronizing circuit and a phase detector

The bandwidth requirements for the FFSK modulation technique relative to FSK modulation techniques with modulation indices L = 1.0 and L = 0.71 is shown in Figure 25. The superiority of the FFSK modulation technique in terms of bandwidth utilization over the other two FSK modulators is apparent. This aspect indicates the suitability of the FFSK technique for mobile radio applications which require transmission of digital signals at high speeds over limited bandwidth channels.

The FFSK modulator used in the experiment reported here has been developed at the Communications Research Centre of the Federal Government [5]. The modulator has been tested in field experiments involving transmission of voice signals digitized at 16 K.bits/sec. In the experiment reported here the BER performance of the modulator is obtained under simulator fading conditions.

4.3.1 FFSK in Fading Channel

For FFSK, the bit error rate, P_e, is given by [4],

$$P_e(\rho) = Q(\sqrt{2\rho}) \qquad (\rho = \frac{E_b}{N_o})$$

where $$Q(x) = \int_x^\infty \frac{e^{-y^2/2}}{\sqrt{2\pi}}\, dy$$

$$\simeq \frac{1}{\sqrt{2\pi}x}\, e^{-x^2/2}$$

Thus $$P_e(\rho) = \frac{1}{\sqrt{4\pi\rho}}\, e^{-\rho} \qquad \text{.....(17)}$$

Let ρ_o be the signal-to-noise ratio at the receiver given by:

$$\rho_o = \frac{\bar{E}_b}{N_o}$$

where $\bar{E}_b$ is the average energy per bit at the receiver.

The probability density function of ρ when the signal is subjected to fading will be [7]:

$$f(\rho) = \frac{1}{\rho_o}\, e^{-\rho/\rho_o}$$

The BER of the received signal in the existence of fading will be given by:

$$P_b = \int_0^\infty P_e(\rho).\, f(\rho)\, d\rho$$

$$= \int_0^\infty \frac{1}{\rho_o}\, e^{-\rho/\rho_o} \quad \frac{1}{\sqrt{4\pi\rho}}\, e^{-\rho}\, dp$$

$$= \sqrt{\frac{1}{4\rho_o(1+\rho_o)}} \qquad \text{.....(18)}$$

$$\approx \frac{1}{2\,\rho_o}$$

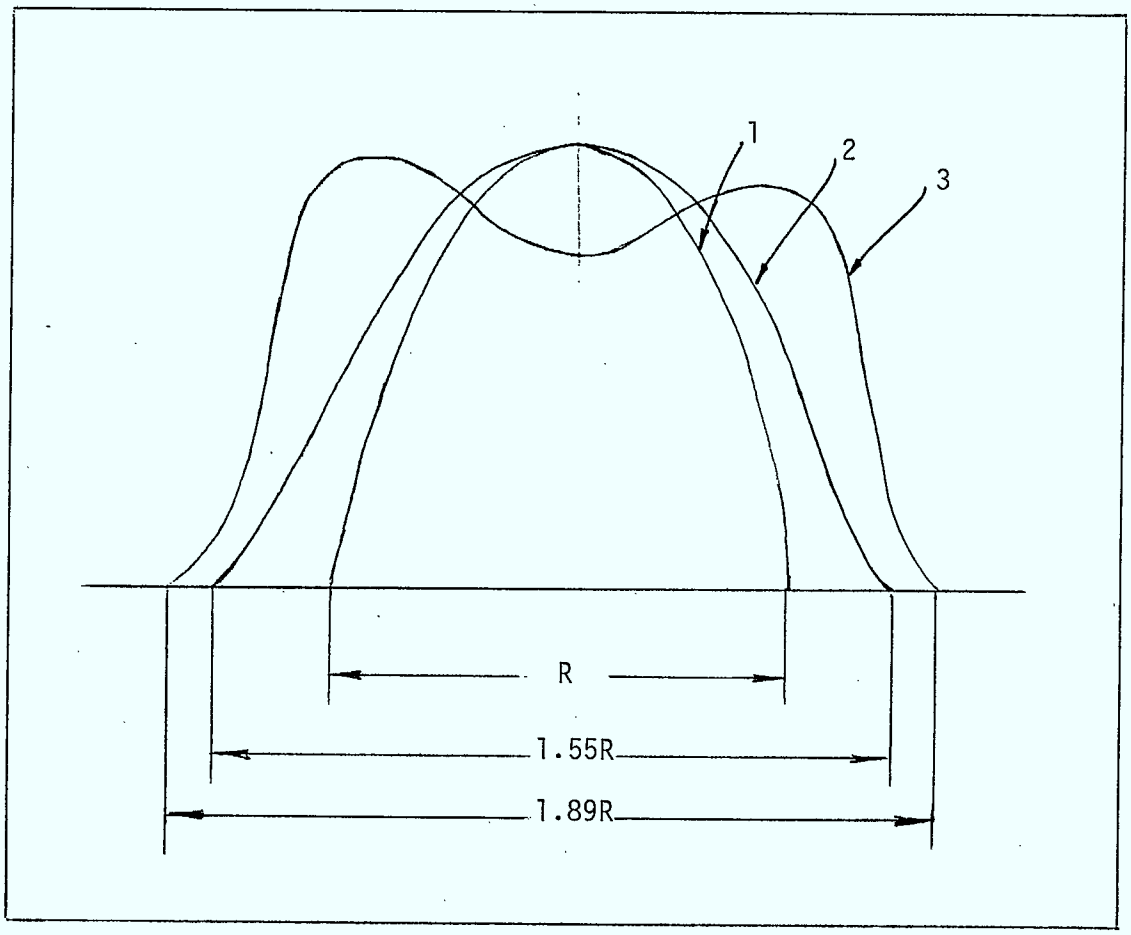


FIGURE 25

Relative Bandwidth Requirements for:

1. FFSK, $h = 0.5$
2. Coherent FSK, $h = 0.7$
3. Non-Coherent FSK, $h = 1.0$

4.3.2 Experimental Set-up

Figure 26 illustrates the experimental set-up used for measuring the performance of the FFSK modulator under simulated fading conditions. The modulator clock is used to generate an output data stream (PRBS) at 16 k.bits/second from the data generator which is fed as input data to the modulator. The modulator RF input signal has f_c = 60 MHz at +10dBm. The modulated signal thus has a carrier frequency of 60 MHz, with the RF output of the modulator at -16 dBm. This signal is down converted to a centre frequency of 455 KHz which is the IF input to the demodulator section.

The down conversion from f_c = 60 MHz to f_c' = 455 KHz is accomplished by multiplying the RF output of the modulator by a signal with frequency f_m = 60.455 MHz and then filtering out the high frequency components. To ensure that the IF frequency remains constant at 455 KHz, it is essential to maintain the difference $f_m - f_c$ equal to 455 KHz. This is achieved by using the same input signal to the modulator's R.F. section to generate f_m as shown in Figure 26.

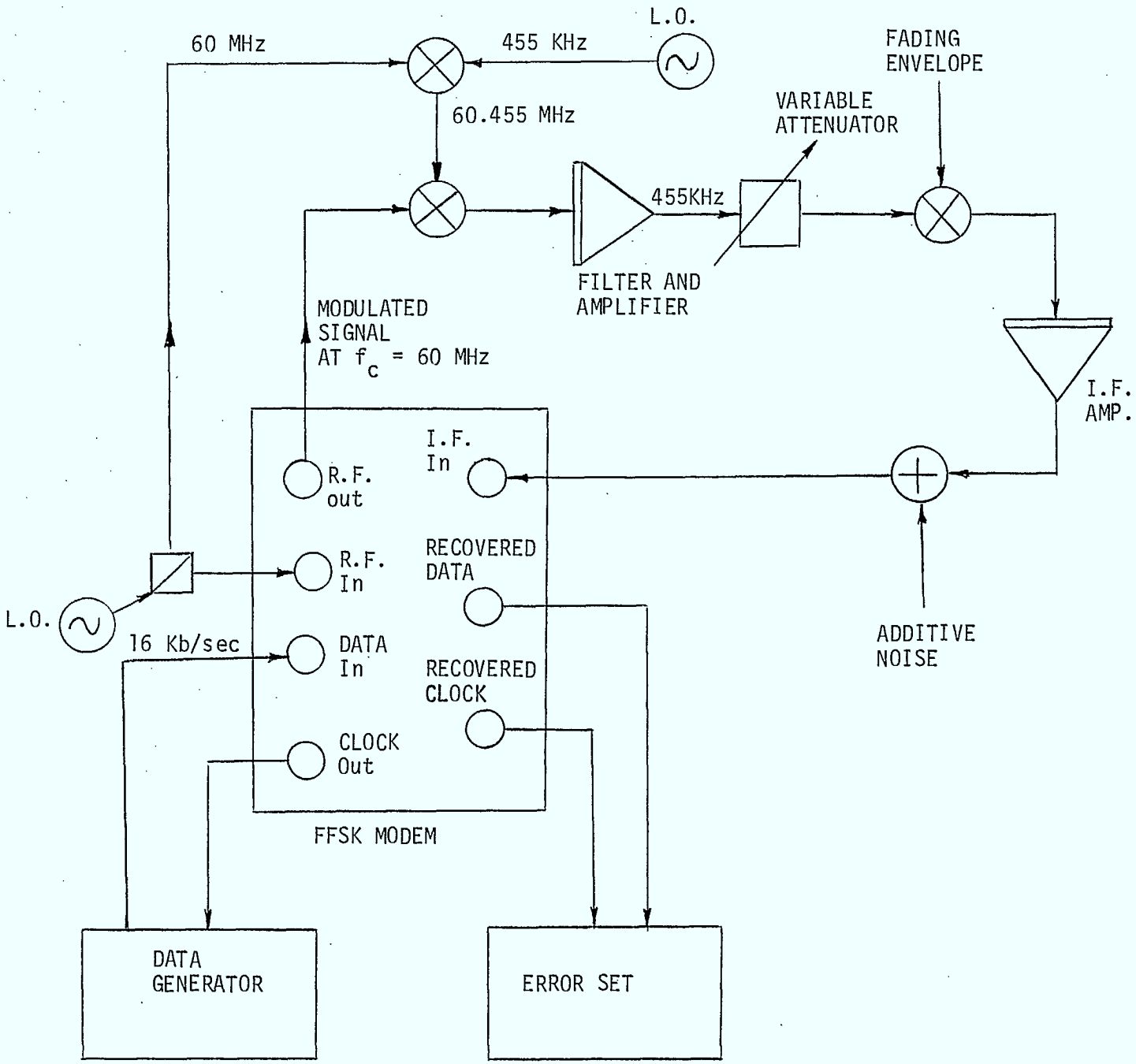


FIGURE 26: Modem Measurement Set-Up

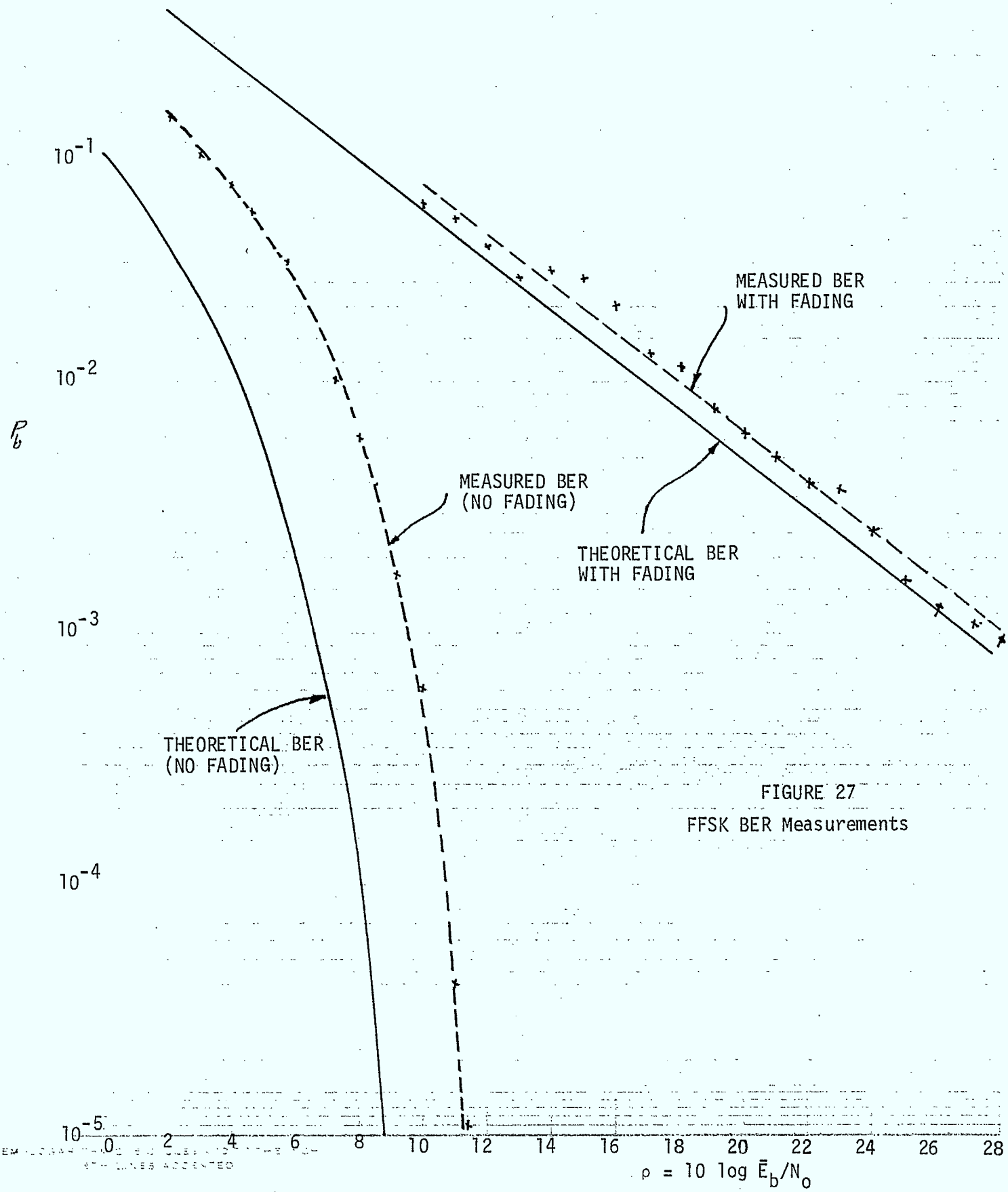


FIGURE 27

FFSK BER Measurements

4.3.3 Results

The results of the measurements conducted on the FFSK modem set are shown in Figure 26. The theoretical BER with no fading signal if based on equation (17). The measured BER for the modem falls within 2dB in SNR from the theoretical BER.

Under fading conditions, the agreement between the measured BER and the theoretical curve is extremely close; a maximum difference of at most 1 dB in SNR exists between the two curves.

The effect of fading on the performance of the FFSK modem becomes noticable at low BER. For example, to obtain a BER of 10^{-3}, it is essential to increase the SNR from approximatley 10 dB (with no fading) to 28 dB when fading conditions are taken into account.

The effect of fading on the transmission of data messages is obviously a dominant factor that must be addressed. This indicates the importance of transmitting data at higher speeds and the use of forward error corrections such as those discussed in Chapter 2.

4.4 Non-Recursive Implementation of a Tamed Frequency Modulator

Introduction

The Tamed frequency modulation (TFM) technique has the advantage of placing very little out of band radiation as compared with other constant-envelope modulation technique [6]. This modulation technique can allow data transmission at a rate of 16 K bits/sec with a radio channel spacing of 30 K Hz with less than -70 dB out of band radiation into the adjacent channels. The modulation scheme still allows orthogonal coherent detection of the modulated signal.

The code rule for TFM defines the phase function value at the sampling instants

$t = (m - 1)\,T,\ mT,\ (m + 1)T,$ ..... as follows:

$$\phi(mT + T) - \phi(mT) = \frac{\pi}{2} - \left(\frac{a_{m-1}}{4} + \frac{a_m}{2} + \frac{a_{m+1}}{4} \right) \quad \text{..... (19)}$$

with $\phi(o) = 0$ if $a_o \cdot a_1 = 1$ and $\phi(o) = \frac{\pi}{4}$ if $a_o \cdot a_1 = -1$

where a(t) is the data signal.

If the three successive bits have the same polarity the phase changes by $\frac{\pi}{2}$, and the phase remains constant for three bits of alternating polarity. The change in phase values for all different combination of data input is illustrated in Table 4.1. It should be noted that the phase values of the TFM signal at successive sampling moments are dependent. For better spectrum efficiency, the phase should vary as smoothly as possible between sampling moments.

TABLE 4.1

a_{m+1}	a_m	a_{m-1}	$\Delta\phi(m+1) = \phi(m+1) - \phi(m)$
-1	-1	-1	$-\pi/2$
-1	-1	+1	$-\pi/4$
-1	+1	-1	0
-1	+1	+1	$+\pi/4$
+1	-1	-1	$-\pi/4$
+1	-1	+1	0
+1	+1	-1	$+\pi/4$
+1	+1	+1	$+\pi/2$

4.4.1 Implementation of the Modulator Circuit

The tamed frequency modulator can be built using both recursive and non-recursive techniques [6]. However, because of instability problems of the former, the latter scheme was chosen.

A basic block diagram of a non-recursive system is shown in Figure 28. The implementation is based on a quadrature modulator. The imput data is fed to a network which puts out the sine and cosine of the phase angle according to the code rate given in equation (19). The outputs are applied to two product modulators operating in quadrative. An interpolation technique is used to ensure that the phase function changes smoothly from one sampling instant to the next.

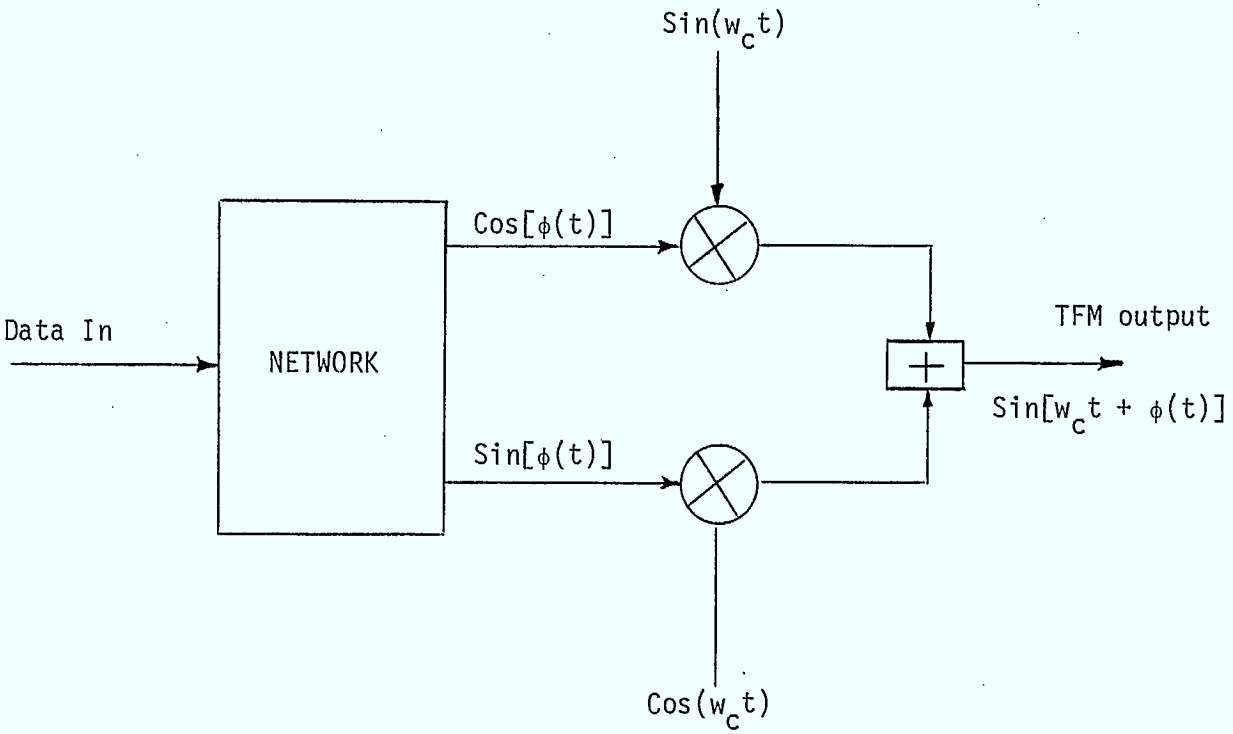
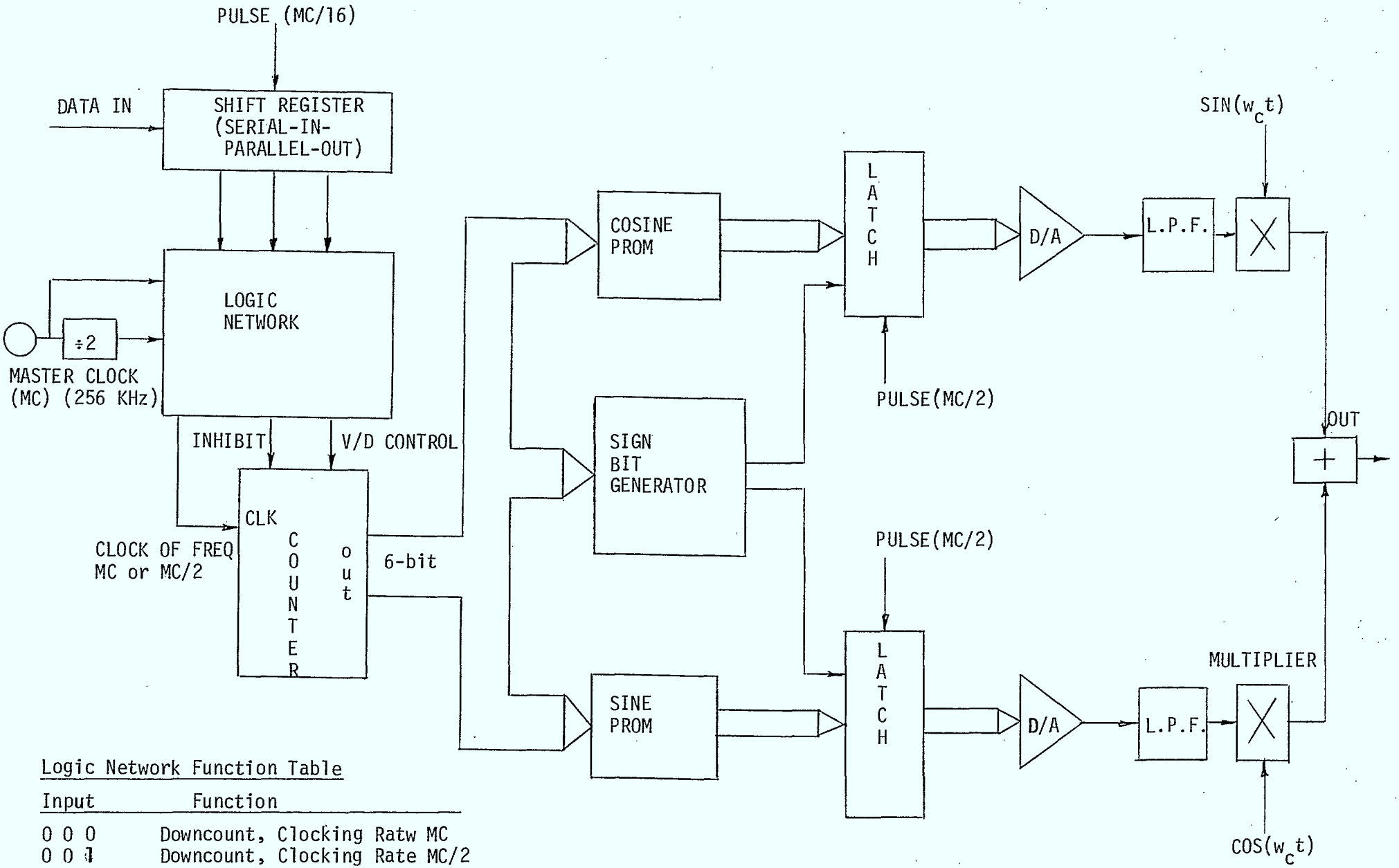


Figure 28 - Basic Block Diagram of a Tamed Frequency Modulator Circuit

A 3-bit TFM system was implemented using a linear interpolation technique. It is seen from equation (19) that at the sampling instants the phase value can only change by 0, $\pm \frac{\pi}{4}$ or $\pm \frac{\pi}{2}$. In order for the phase function to vary smoothly from one sampling instant to the next, 8 - interpolating levels were introduced between samples. Thus for a phase change of $\pm \frac{\pi}{4}$, the phase function changes in 8 steps, each step of size $\pm \frac{\pi}{32}$, and for a phase change of $\pm \frac{\pi}{2}$, the step size is $\pm \frac{\pi}{16}$. To implement this interpolation scheme two PROMS were coded with the Sine and Cosine of angles $\frac{n\pi}{32}$ for n = 0, 1 .....63, to encompass the entire 0 to 360^{0} phase circle. The address to the PROMS is changed at 8 times the sampling rate for a phase change of $\pm \frac{\pi}{4}$. For a phase change of $\pm \frac{\pi}{2}$, the address is changed at 16 times the sampling rate although the data outputs from the PROMS are still "latched" out at 8 times the sampling rate so as to provide only 8 interpolating levels.

Figure 29 shows a block diagram of a circuit used to implement the TFM system. The data enters a serial-in, parallel-out shift register at the appropriate sampling rate. (The system was designed for 16 K bit/sec data rate). The outputs from the shift register are fed to a logic network which controls the operation of a 6-bit up-down counter according to the input bit pattern. A function table for the logic network is included in Figure 29. The counter is either upcounted, down counted or inhibited depending on the input bit string. The clocking rate is doubled when the bit strong is either 0, 0, 0 or 1, 1, 1.

The counter output forms the address of two PROMS which contains the unsigned COSINE and SINE of the angle values in 8-bit digital words. The sign bit is generated externally from the address inputs. The output from the PROMS and the sign bits are latched and fed to two D/A converters



Logic Network Function Table

Input	Function
0 0 0	Downcount, Clocking Ratw MC
0 0 1	Downcount, Clocking Rate MC/2
0 1 0	Inhibit
0 1 1	Upcount, Clocking Rate MC/2
1 0 0	Downcount, Clocking Rate
1 0 1	Inhibit
1 1 0	Upcount, Clocking Rate MC/2
1 1 1	Upcount, Clocking Rate MC

FIGURE 29 - Tamed Frequency Modulator Circuit

followed by two low pass filters and two product multipliers operating in quadrature. Each low pass filter was designed to have linear phase (Bessel filter) with a cut-off frequency around 64 KHz. The output from the two multipliers are added in a summing amplifier to provide the final phase modulated output. The complete circuit details are included in Appendix D.

4.4.2 Results

A 3-bit TFM system using linear interpolation scheme was bread-boarded for initial investigations. To conserve power, the digital logic part was built using CMOS devices. Analog devices AD561 and AD534 were used as digital to analog converters and analog to analog multipliers respectively. Although 1 PROM could be multiplexed, for convenience, 2 PROMS (2716) were used for storing the Sine and Cosine code Tables. Each PROM location was coded with the respective Sine or Cosine value of angle $\frac{n\pi}{32}$ with n varying from 0 to 63. The total memory requirement is therefore 128 bytes. When the input data is such that the phase change between two successive intervals is $\pi/4$, the PROM addresses are scanned at 128 KHz i.e. 8 times the data rate (16 k bits/sec). When the phase change is $\pi/2$ the addresses are scanned at 16 times the data rate. However, only the output corresponding to every alternate address input is presented to the D/A. Figure 30(a) and (b) illustrate the situations. Figure 30(a) shows the D/A outputs from the Sine (top) and the Cosine (bottom) channels. The input data stream is continuously held at 011. Consequently, the PROM addresses are incremented at a rate of 128 KHz - thus producing a Sine and a Cosine wave output with a periodicity of 0.5 msec ($\frac{1}{128KHz} \times 64$). A continuous input of 110, 001 or 100 will provide identical results, however in the last two cases the PROM addresses will be continuously decremented.

Figure 30 (b) shows the D/A outputs from the Sine (top) and Cosine (bottom) channels for a continuous inout of 111. In this case the PROM addresses are incremented at twice the above rate and thus producing a Sine and a Cosine ware output with periodicity of 0.25 m sec. Doubling of the output step is also evident from the figire. For a continuous input of 000, the PROM addresses will be continuously decremented, however, the D/A outputs will appear identical to Figure 3(b).

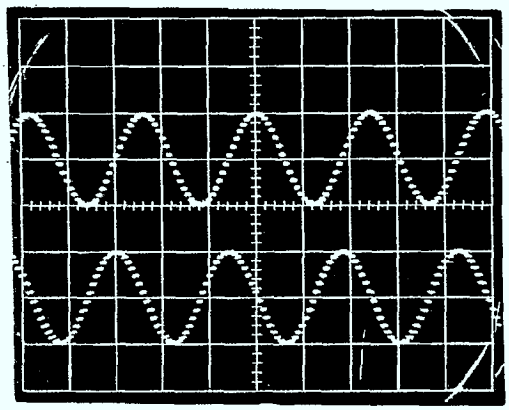
Figure 31 demonstrates the code rule that is fundamental to the TFM system. For this demonstration, the input shift register was replaced by a 3-bit counter so that all possible combinations of the input data stream are sequentially presented to the TFM system. The D/A output from the Sine (top) and the Cosine (bottom) channels are shown in the figure. When an input of 010 is presented to the system, no change in phase takes place at the output. This is seen by the Straight line portion on the left hand side of the figure. The output remains fixed until the input is changed at 011. When a phase change of $+45^{o}$ takes place in 8 equal steps. Following this the input is changed to 100. The subsequent phase changes are -45^{o}, 0^{o}, $+45^{o}$, $+90^{o}$, -90^{o} and -45^{o} until the situation repeats. In this figure, the absolute phase angle is close to 0^{o} during the time no phase change takes place i.e. between input 010 and 011. Figure 30(a) (b), and 31 only illustrate the operation of the TFM system for arbitrary inputs. In actual operation the change in input at any sampling interval is dependent on the past input.

A carrier frequency of 455 KHz was used in the present experiments. A quadrative modulation was achieved by using two square waves shifted in phase of 90^{o}. A circuit schematic for generating 90^{o} phase

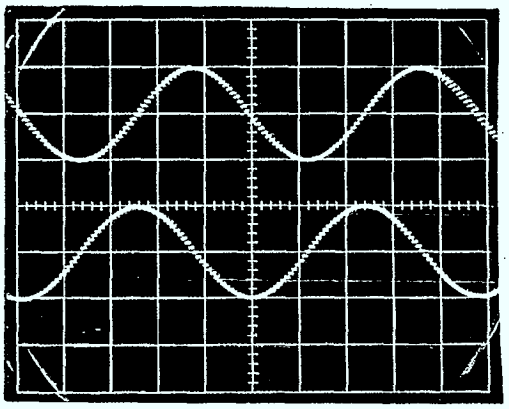
shifted square waves is shown in appendix D. Two multipliers (AD534) were used for up translation. The output from the multipliers were added in an operational amplifier summer. A band pass filter can be employed at the output of the summer network to suppress unwanted modulations around the harmonics of the carrier frequency. Using a psendo random data input, the output spectrum showed more than 45dB attenuation beyond a 16 KHz band spread as shown in Figure 32. The results were as expected for a 3-bit transation. At present, however, a demodulator circuit is yet to be built for data recovery.

4.4.3 Summary

The initial results on TFM system clearly holds promise. Detailed characterization is now underway. The circuit is also being refined. It is believed that the D-A converter and the multiplier network in each channel can be replaced by a single multiplying D to A converter (MDAC). This will reduce cost and further save power. Also, the configuration will be more amenable to integration on a single chip.



(a)



(b)

Figure 30 - D/A Outputs for an Input (a) 011; (b) 111
[Horizontal Scale - 0.1 m sec/div; Vertical
Scale - SV/div.]

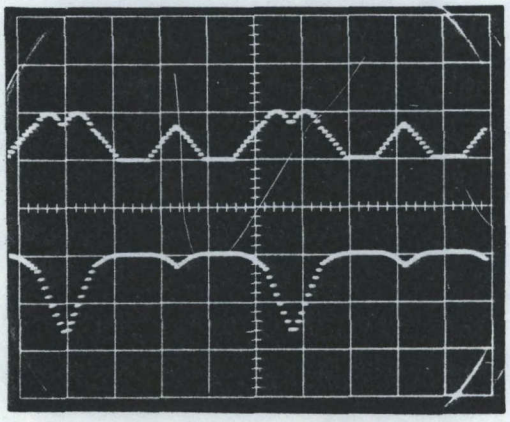


Figure 31 - D/A Outputs for Input Continuously Varying from 000 to 111 by Means of a 3-bit Counter

4.5 The Fading Signal Simulator

4.5.1 Fading Simulator Circuit

The black diagram of the fading simulator circuit is shown in Figure 33. A white gaussian noise generator is used to generate a random signal with a uniform spectrum up to about 200 KHz. This signal is then bandlimited using a narrow bandpass filter with a centre frequency of f_o = 1 KHz and sharp cutoff frequencies of approximately ($f_o \pm f_m$), f_m = 7.6 Hz. The band limited signal is then full-wave rectified after it has been amplified to raise the signal to such a level as would enable the rectifier to operate efficiently. The rectified signal is next passed through a low-pass filter (f_c = 200 Hz) to remove the 1 KHz carrier. The result is a signal whose amplitude approximates the Raleigh distribution. The resultant wave form is mixed with the IF signal using an amplitude modulator.

If the operating frequency of the system is taken to be at 170 MHz, the wavelength λ will be equal to 1.765m. The maximum doppler frequency, f_m, is given by

$$f_m = v/1.765 \text{ Hz, } v \text{ is the vehicle speed.}$$

Thus for v = 48 Km/hr, f_m = 7.6 Hz and for v = 96 km/hr, f_m = 15 Hz.

4.5.2 Fading Simulator Testing

The circuit shown in Figure 34 is used to test the fading simulator. The output signal from the fading circuit is compared to a variable d.c. reference. The voltage comparator has the following characteristics:

$$e_o = + V_z, \text{ if } e_i < e_{ref},$$

$$e_o = - V_z, \text{ if } e_i > e_{ref}$$

The resulting random square wave is then sampled at 10 Kb/sec using a clock generator and a NAND gate. The number of pulses is then recorded using a frequency counter which is activated using a gate signal (push button) for one second durations.

The percentage of time the signal level exceeded the d.c. threshold level is calculated as:

$$\% \text{ time above threshold level} = \frac{N}{f_c \cdot T_g} \times 100$$

where: f_c = frequency of clock generator = 10 Kb/sec

T_g = gate duration = 1 second

N = counter reading at the end of the gate pulse

Thus the cumulative distribution of the output signal from the fading simulator can be determined.

Figure 35 shows a plot of the percentage of time the signal level exceeds the threshold for various threshold levels. The solid line represents the theoretical curve for Raleigh distribution while the dotted line represents the result of the measurements. The range of agreement extends from about +5dB to -20dB. At each threshold level, thirty readings were taken and averaged.

Figure 36 shows a plot of the normalized level crossing rate for various threshold levels. The solid line represents the theoretical curve while the dotted line represents the experimental results. The agreement between the two curves is again very close for a range of 5 dB to -20 dB. It is concluded that the simulated circuit produces an output

which has the same characteristics as the fading signals in mobile radio channels.

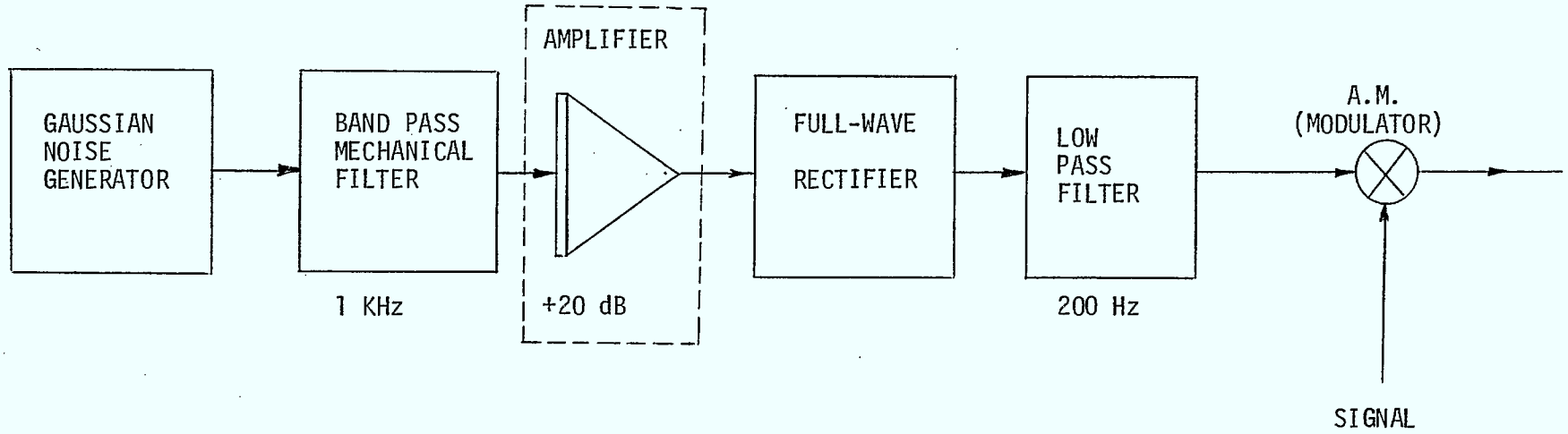


FIGURE 33: Block Diagram of Fading Simulator

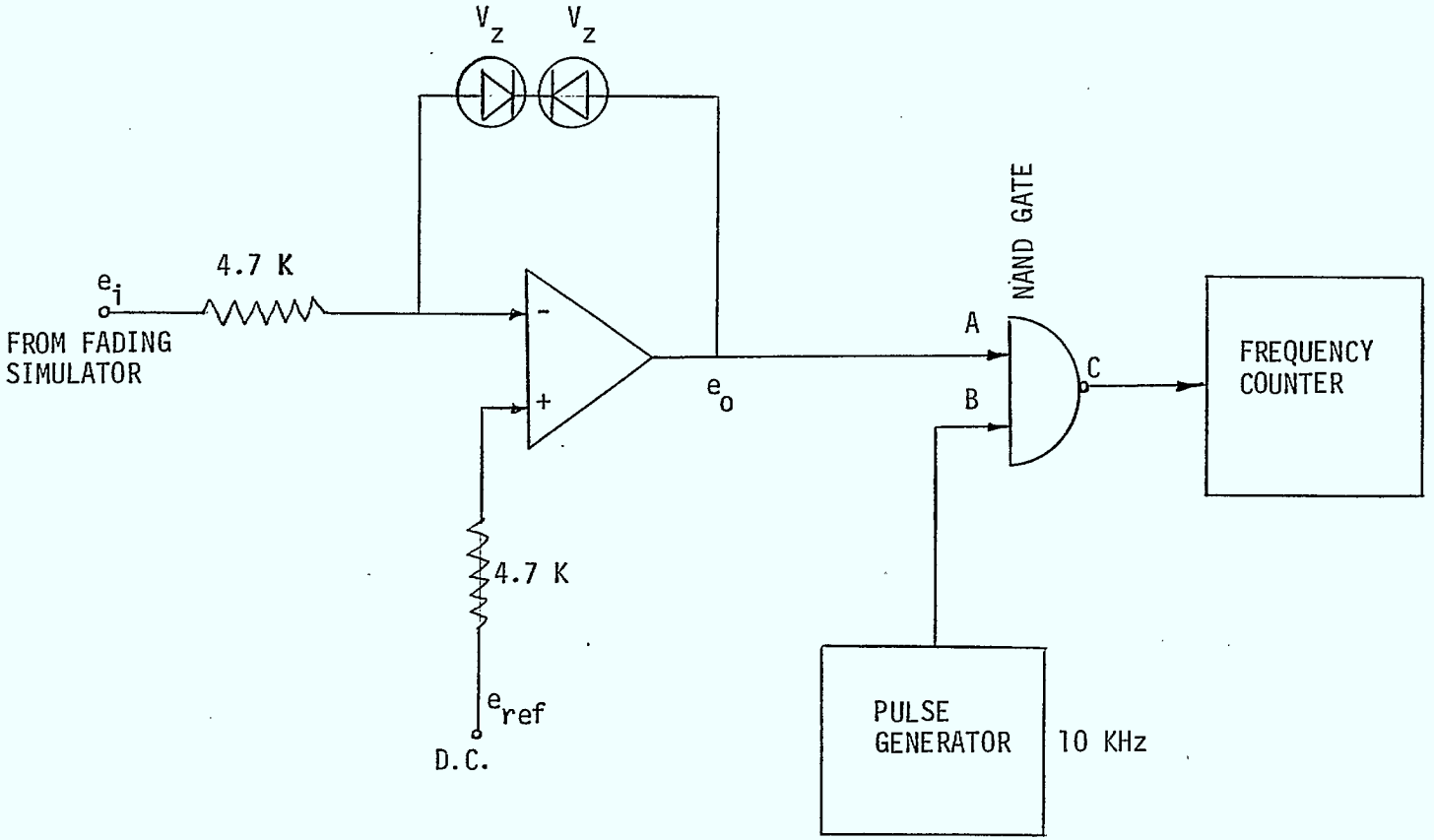


FIGURE 34: Circuit Diagram for Testing the Simulator

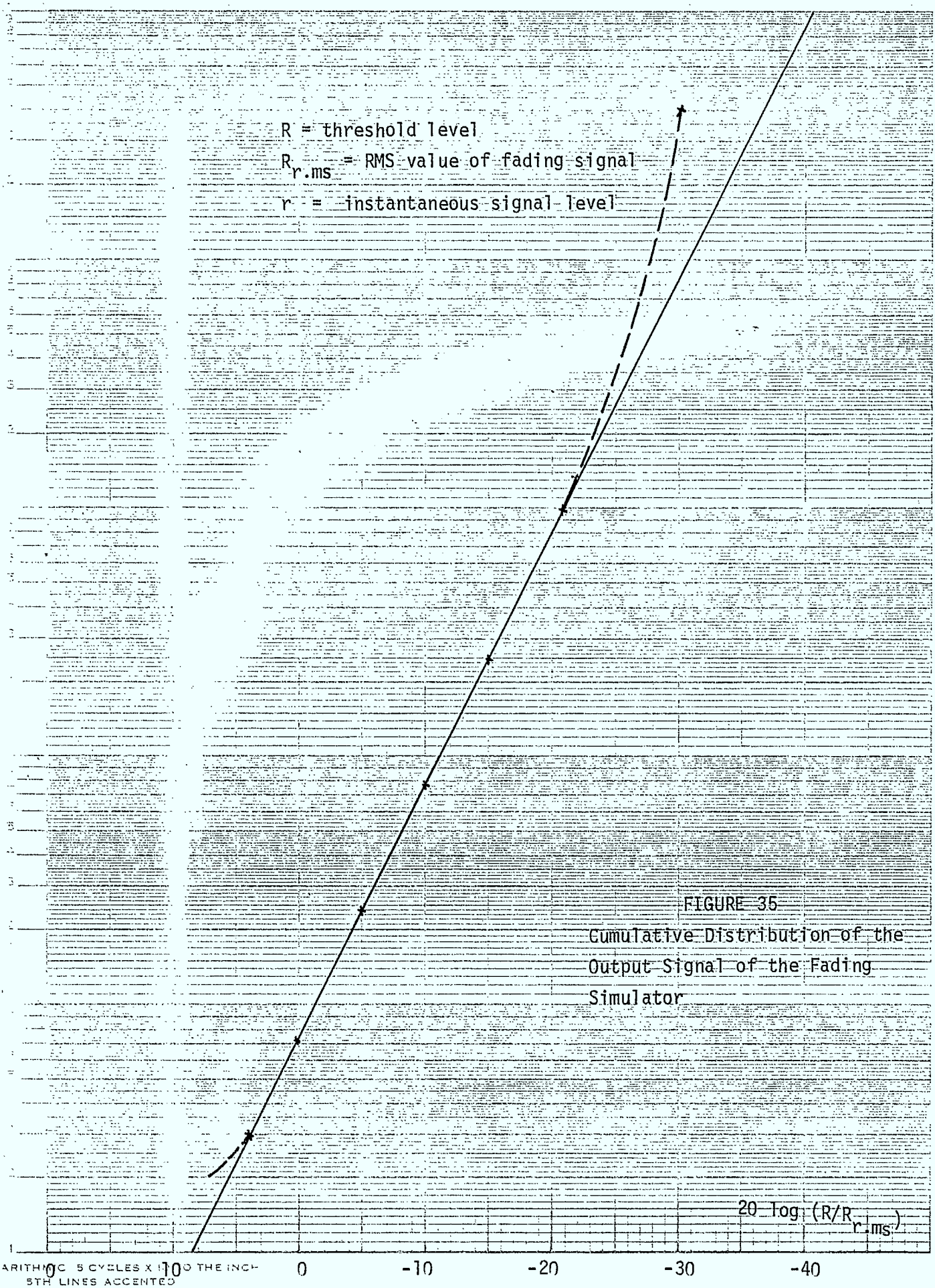


FIGURE 35
Cumulative Distribution of the Output Signal of the Fading Simulator

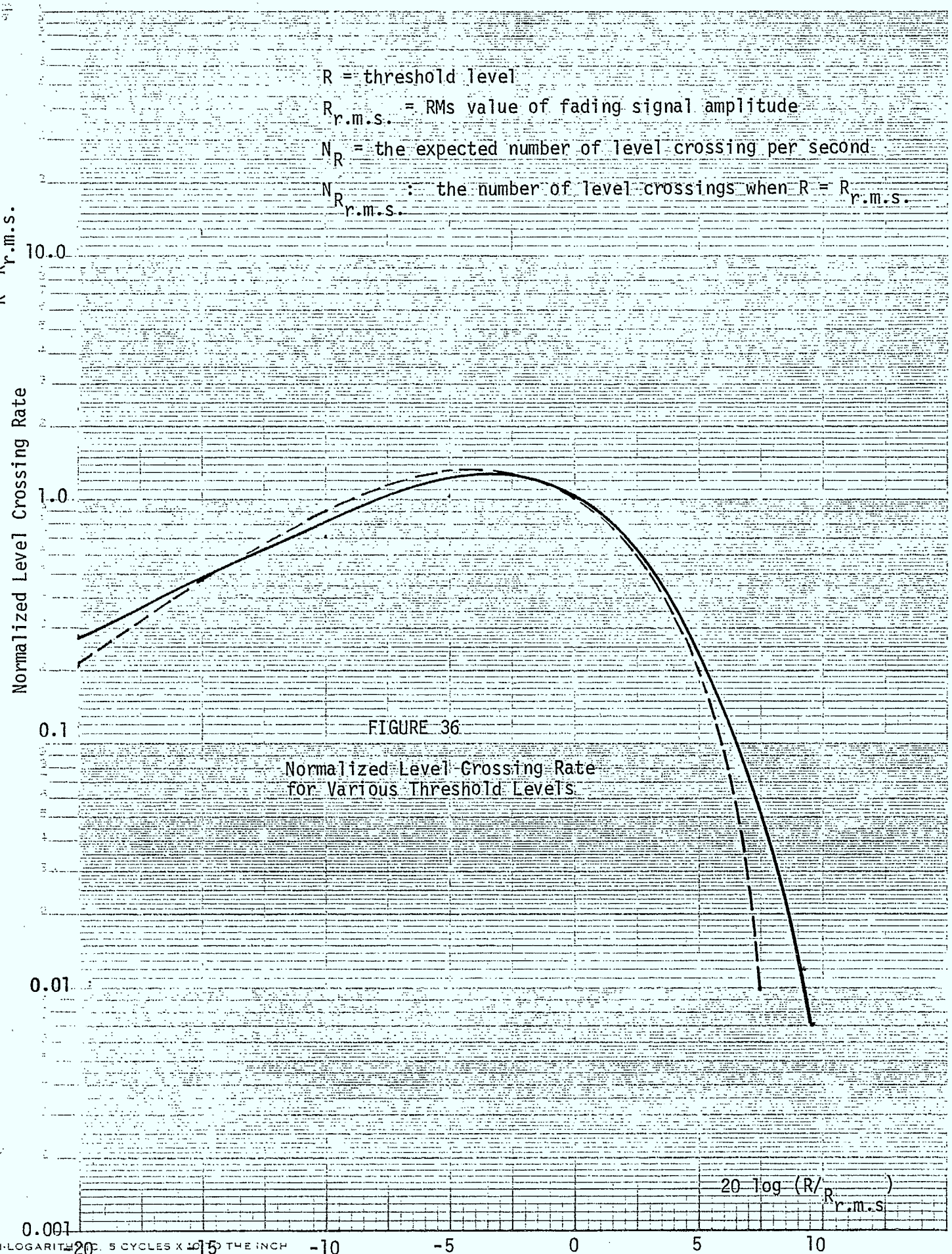


FIGURE 36

Normalized Level Crossing Rate
for Various Threshold Levels

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Chapter 5

Summary and Future Research

5.1 Summary

The following is a summary of the results of the research reported here.

1. In chapter 2, the use of forward error correction in improving the performance of a stop-and-wait ARQ scheme over random-error and Rayleigh fading channels was examined. The results show that both the mean wasted time and the mean time to successful transmission can be substantially reduced by forward error correction.

2. A low cost CMOS microprocessor board has been designed and implemented, as reported in chapter 3. The microprocessor is functionally equivalent to the Intel 8020 board with respect to the mobile terminal control requirements. However, the CMOS board's power consumption is approximately 1/30 of a functionally comparable board constructed using the I^2L technology.

3. The performance of two modulator sets (DPSK and FFSK) which have been used previously in mobile applications has been tested experimentally under simulated fading conditions. Fading effects were shown to be dominant at low BER, as substantially higher SNR at the receiver is required to obtain the same BER when no fading signals exist.

4. A non-recursive TFM modulator circuit has been designed and implemented. The output spectrum for the modulator circuit showed more that 45 db attentuation beyond a 16 kHz band spread. A demodulator circuit is planned in the immediate future to test the BER performance of TFM under fading conditions.

5.2 Future Research

As explained earlier, the results of the research reported here represent intermediate steps towards the objective of establishing the feasibility of an all digital integrated voice and data mobile communications system. As a follow up to these steps, the following research areas will be explored in the immediate future.

1. Construction of the TFM demodulator component. This will be followed by testing the TFM modem under fading conditions to compare its performance to the FFSK modem.

2. Construction of a voice digitization encoder/decoder circuit at 16 Kb/sec. The effects of modulation and fading on the quality of voice received over radio channels will be tested.

3. Construction of a suitable voice detection circuit which will be used as a carrier on/off switch in the voice circuit of the mobile terminal.

4. The implementation of forward error correcting codes will be explored with special considerations given to the trade-offs between improvement in throughput and added complexity and cost. Improvements in performance obtainable through the use of diversity transmission will also be examined. Encryption techniques will be studied so as to meet the confidentiality requirements needed in certain applications such as police communication.

APPENDIX A

A SAMPLE OF MICROPROCESSOR TEST ROUTINES

EPROM #1 (MEMORY, PARALLEL I/O, RST 5.5 TEST)

RESET	00	XMT	PORT TEST	
	00	AF	XRLA,A	
	01	d301	OUTA,XMT	
	03	2F	COMPA	
	04	C30100	JMP 01	
TRAP	24	MEMORY TEST		
	24	3ECE	MOV A, #CE	
	26	30	Sim	ENABLE
	27	FB	E1	INTERRUPTS
	28	C34000	JMP40	
START	40	AF	XRLA,A	OUTPUT TRIGGER
	41	d301	OUT A,XMT	PULSE TO
	43	2F	COMPA	TO TRANSMITTER
	44	d301	OUTA,XMT	CONTROL PORT 01
	46	2F	COMPA	
	47	d301	OUTA,XMT	
	48	2601	MOV H, #01	TEST EPROM
	4B	2E00	MOV L, #0	FROM 100_{16} to 2000_{16}
	4d	23	INC H,L	
	4e	7C	MOV A,H	
	4f	FE20	CPI #20	is Adde = 2000?
	51	CA5E00	J2,X	No continue; Yes go to RAM
	54	3EFF	MOV A, #FF	check EPROM content
	56	46	MOV B, (H,L)	iF = FF continue

	57	B8	CMP A, B	if # FF ERROR! RESTART
	58	CA4doo	JZ 4d	
	5B	C34000	JMP 40	
	5E	2630	MOV H, #3ø	SET START RAM
Y	60	23	INC H,L	TEST RAM FROM
	61	7C	MOV A,H	3,000 to 4000_{16}
	62	FE40	CPI, #40	
	64	CA 4000	JZ 40	is Addr = 4000_{16}
	67	AF	XRLA,A	YES RESTART: NO CONTINUE
	68	77	MOV (H,L),A	WRITE"ø" in RAM
	69	46	MOV B, (H,L)	READ FROM RAM
	6A	B8	CMP A,B	COMPARE
	6B	C24000	JNZ 40	IF # RESTART
	6E	3EFF	MOV A, #FF	
	70	77	MOV (H,L),A	WRITE "FF" in RAM
	71	46	MOV B, (H,L)	READ
	72	B8	COM A,B	COMPARE
	73	CA6000	JZ Y	IF = CONTINUE
	76	C34000	JMP 40	IF # RESTART

RST 5.5 ADDR 2C TEST KEYBOARD PORT

USE DIP SWITCH ASSEMBLY TO TEST KEYBOARD PORT. USE 555 TO INTERRUPT CPU AND JUMP TO KEYBOARD ROUTINE

2C	C3 7F00	JMP 7F	TEST KEYBOARD PORT
7F	FB	EI	
80	dbo2	in P02	
82	47	MOV B,A	
83	EE00	XRL A,#ø	

```
85    CA 2400     BZ 24
88    3EFF        MOV A,#FF
8A    A8          XRL A,B
8B    CA 9700     B7 XMT1
8E    3E 47       MOV A, #47
90    A8          XRL A,B
91    CA9d00      BZ XMTØ
94    C37F00      JMP 7F
97    3C          XMTI INCA
98    d301        OUT P01
9A    C37F00      JMP 7F
9d    d301        XMTO OUT P01
9F    C37F00      JMP 7F
```

EPROM #2 (UART TEST) WITH RS 232 TERMINAL

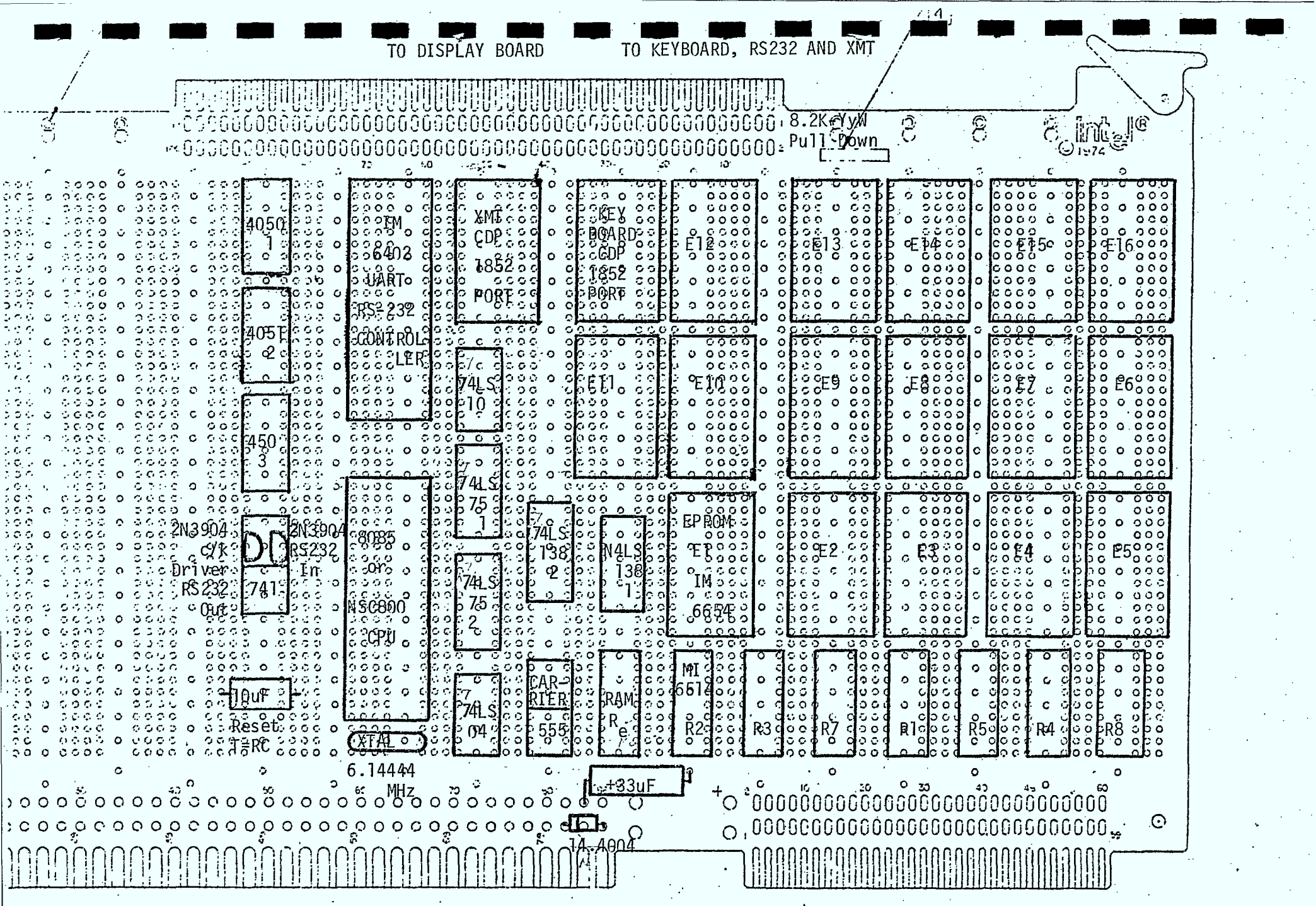
AND EXTERNAL 4.8 kHz CLK BAUD RATE 300

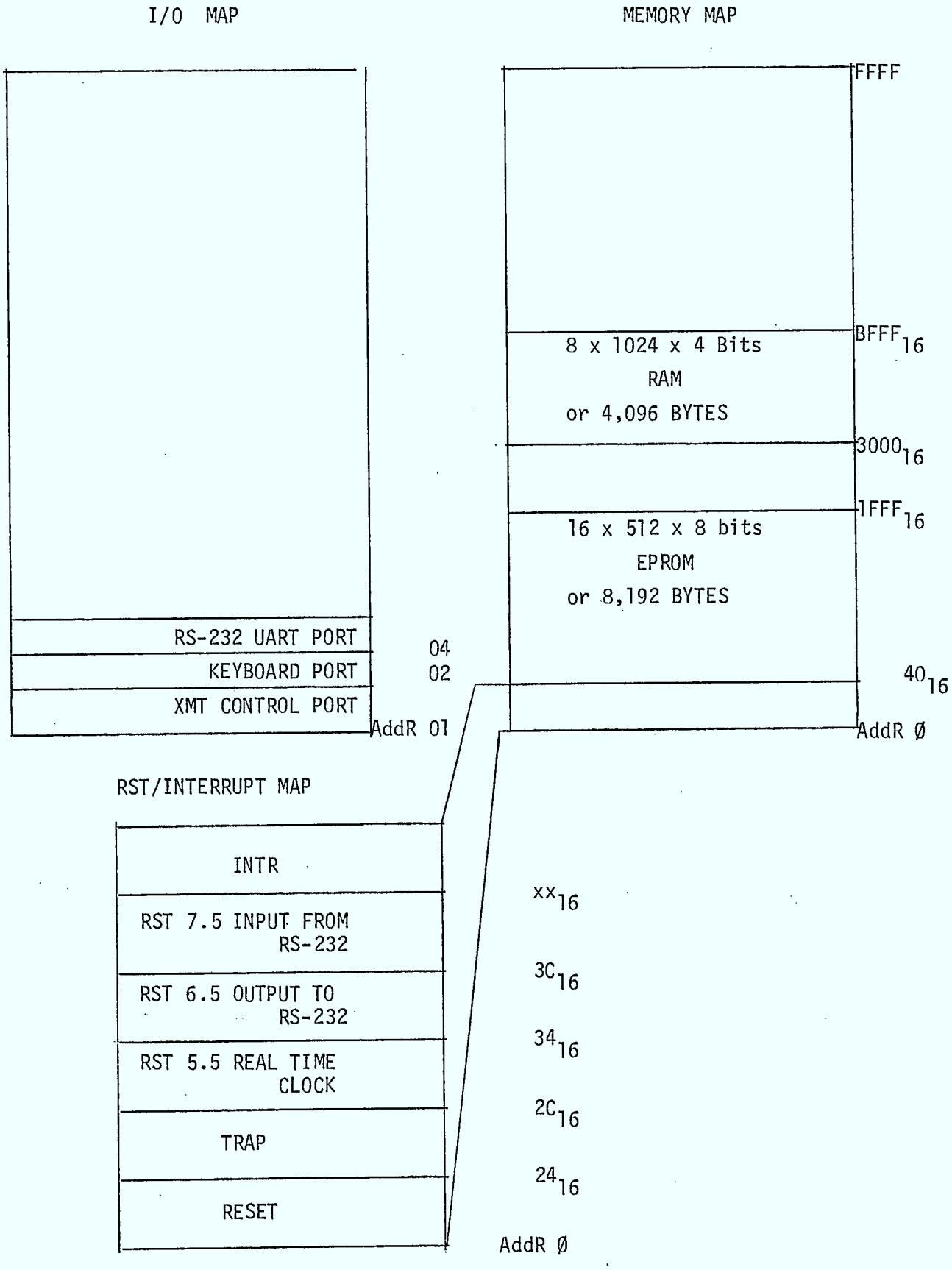
RESET	00	3E od	MOV A,#od	SET 6.5 INT
	02	30	Sim	
	04	06 00	MOV B,#Ø	CLR RB
	06	C3 AØ 00	JMP AØ	
RST 6.5	34	C3 BOOO	JMP BØ	(WRITE TO RS-232)
RST 7.5	3C	3E od	MOV A, #od	(READ FROM RS-232)
	3E	30	Sim	SET 6.5 INT
	3F	C3 C500	JMP C5	
	AØ	26 00	MOV H, #Ø	SET MESSAGE
	2	2E dd	MOV L, #dd	POINTER
	4	Fb	EI	ENABLE INT
	5	76	HALT	WAIT
	BØ	23	INC H,L	INCREMENT POINTER
	1	3E 2E	MOVA,#2E	CHECK IF MESSAGE
	3	BE	CMPA,(H,L)	IS FINISHED
	4	CA BC 00	BZ A	YES GO TO READ OUT
	7	7E	MOV A,(H,L)	NO OUTPUT
	8	d3 04	OUT P04	CHARACTER TO RS 232
	A	Fb	EI	EN INT
	B	76	HALT	AND WAIT
	C	78 A	MOV A,B	OUTPUT REG B
	d	d304	OUT P04	TO RS 232
	f	3E ob	MOV A,#0B	SET 7.5 INT
	C1	30	SIM	READ FROM RS 232

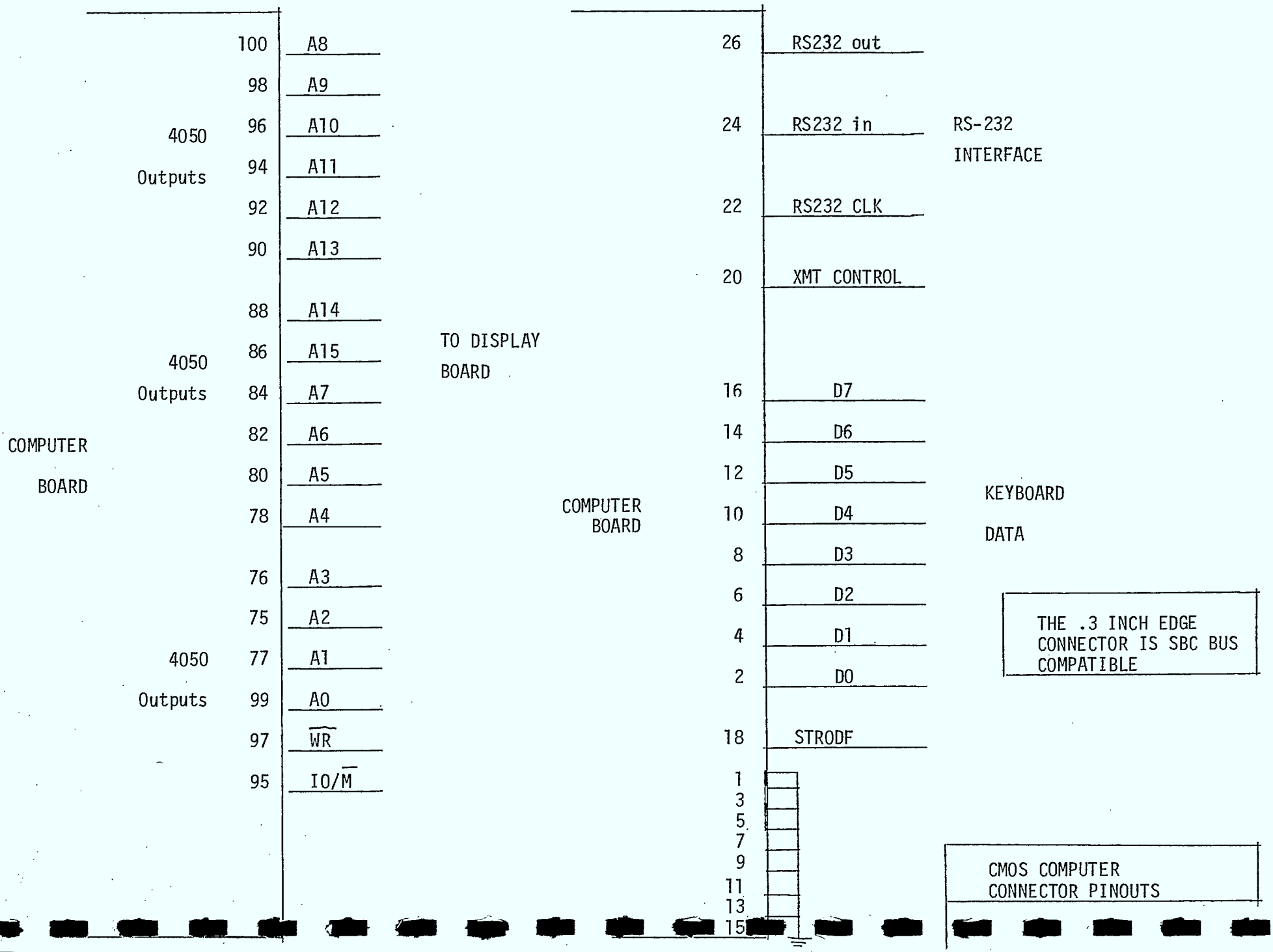
```
2       Fb          EI                  WAIT
3       76          HALT

C5      db 04       In A,P04            GET CHARACTER IRO
7       47          MOV B,A             RS 232 AND STORE
8       21 F000     MOV H,L #F000       IN REG B
b       Fb          EI                  INITIALIZE POINTER
c       76          HALT                WAIT FOR RS-232
                                        WRITE INTERRUPT
```

CHARACTER SETS IN EPROM dE to 103

dE	OA	LF	F1	OA	CR
f	od	CR	2	od	LF
E0	54	T	3	59	Y
1	59	Y	4	4F	0
2	50	P	5	55	u
3	45	E	6	20	
4	20		7	48	H
5	43	C	8	41	A
6	48	H	9	56	V
7	41	A	A	45	E
8	52	R	B	20	
9	41	A	C	54	T
A	43	C	d	59	Y
B	54	T	E	50	P
C	45	E	f	45	E
d	52	R	100	44	D
E	0A	LF	1	20	
f	od	CR	2	20	
F0	2E	.	3	2E	.


TO DISPLAY BOARD
TO KEYBOARD, RS232 AND XMT
8.2K YyW
Pull-Down
intel
©1974
4050 1
405 2
450 3
IM 6402 UART RS-232 CONTROLLER
XMT CDP 1852 PORT
KEY BOARD CDP 1852 PORT
74LS 10
74LS 75 1
74LS 75 2
74LS 04
74LS 138 2
N4LS 138 1
2N3904 C/K Driver RS232 Out
2N3904 RS232 In
741
8085 or NSC800 CPU
EPROM IM 6654
CAR-RIER 555
RAM
MI 6614
R2
R3
R7
R1
R5
R4
R8
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
10uF
Reset
RC
XTAL
6.14444 MHz
+33uF
14-A004
INTEL SBC BUS COMPATIBLE
CMOS COMPUTER PHYSICAL LAYOUT
FEB 80


I/O MAP
MEMORY MAP
FFFF
BFFF16
8 x 1024 x 4 Bits
RAM
or 4,096 BYTES
3000₁₆
1FFF₁₆
16 x 512 x 8 bits
EPROM
or 8,192 BYTES
RS-232 UART PORT
04
KEYBOARD PORT
02
XMT CONTROL PORT
40₁₆
AddR 01
AddR Ø
RST/INTERRUPT MAP
INTR
xx₁₆
RST 7.5 INPUT FROM
RS-232
3C₁₆
RST 6.5 OUTPUT TO
RS-232
34₁₆
RST 5.5 REAL TIME
CLOCK
2C₁₆
TRAP
24₁₆
RESET
AddR Ø


100 A8
98 A9
96 A10
94 A11
92 A12
90 A13
88 A14
86 A15
84 A7
82 A6
80 A5
78 A4
76 A3
75 A2
77 A1
99 A0
97 WR
95 IO/M
4050 Outputs
4050 Outputs
4050 Outputs
COMPUTER BOARD
TO DISPLAY BOARD
COMPUTER BOARD
26 RS232 out
24 RS232 in
22 RS232 CLK
20 XMT CONTROL
16 D7
14 D6
12 D5
10 D4
8 D3
6 D2
4 D1
2 D0
18 STRODF
1 3 5 7 9 11 13 15
RS-232 INTERFACE
KEYBOARD DATA
THE .3 INCH EDGE CONNECTOR IS SBC BUS COMPATIBLE
CMOS COMPUTER CONNECTOR PINOUTS

Power Requirements:

+5v @ 135 mA using the NMOS 8085 CPU and in a memory access routine

(see memory test routines on EPROM #1)

125 mA in Halt State

+12v @ 4 mA under switching operation

-12v @ 4 mA (see EPROM #2 UART Test)

RS-232 Interface

FORMAT 8 Bit

Even Parity

1 stop bit

Baud rate tested at 300 baud using a 4.8 kHz c/k and the decwriter II

APPENDIX B

MICROPROCESS BOARD COMPONENT DESCRIPTION

PART NUMBER	DESCRIPTION	PRICE
SEMICONDUCTORS		
1 x P8085	INTEL CPU	
1 x 1M 6402 CPL	UART	
2 x CDP 1852D	PARALLEL PORT	
16 x 1M 6654IJG	EPROM	
8 x MI-6514-5	RAM	
3 x CD4050AE	HEX BUFFER	
2 x 74LS138N	DECODER	
2 x 74LS75N	4 BIT LATCH	
1 x 74LS 10N	3 I/p NAND	
1 x 74LS04N	INVERTERS	
1 x LM741CN	OP-AMP	
1 x NE 555N	TIMER	
2 x 2N3904	NPN	
4 x IN4004	diode	
PASSIVE		
20 x .01 uF	PHILLIPS CAPACITORS	
20 x .02 uF	DISK CAP.	
1 x 33 uF	ELECTROLYTIC	
1 x 10 uF	ELECTROLYTIC	
1 x 100 pF	CERAMIC	
25 x 1/4 WATT	RESISTORS	
1 x 614414444 MHZ	CRYSTAL	

PART NUMBER	DESCRIPTION	PRICE
HARDWARE		
1 X 1000 402 -01	INTEL PROTOTYPE MODULE BOARD SBC 905	
8 x 8505	3/4" SPACERS	
4 x 2374	1" SPACERS	
8 x 4-40 1"	SCREWS	
2 x 40 pins	SOCKETS	
18 x 24 Pins	SOCKETS	
8 x 18 pins	SOCKETS	
9 x 16 pins	SOCKETS	
2 x 14 pins	SOCKETS	
200 FT #30	KYNAR WIRE	

CMOS COMPUTER PRICE LIST

FEB 80

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6514

1024 x 4 CMOS RAM

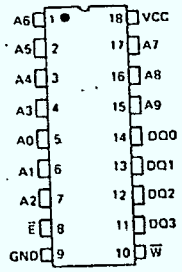
JULY 1978

Features

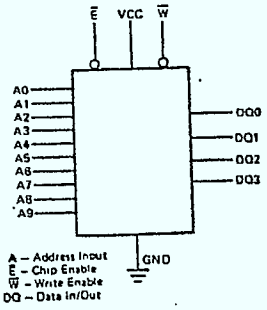
- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



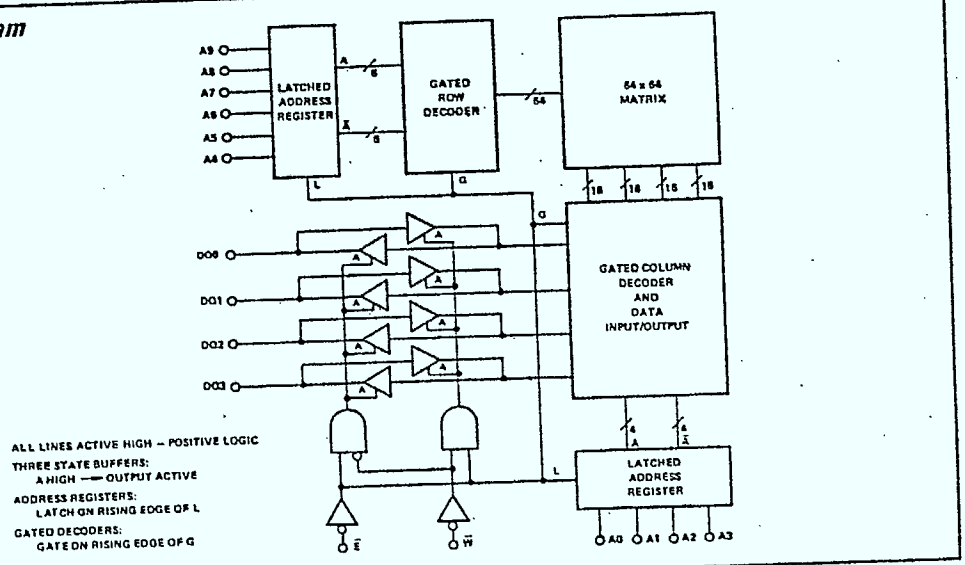
Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS	
Supply Voltage — VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	ID = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		8.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	300		240	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		240	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		240	150		ns	④
	TDVWH	Data Setup Time	200		160	100		ns	④
	TWHQZ	Data Hold Time	0		0	0		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	0		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC test conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF; All timing measured at ½ VCC.

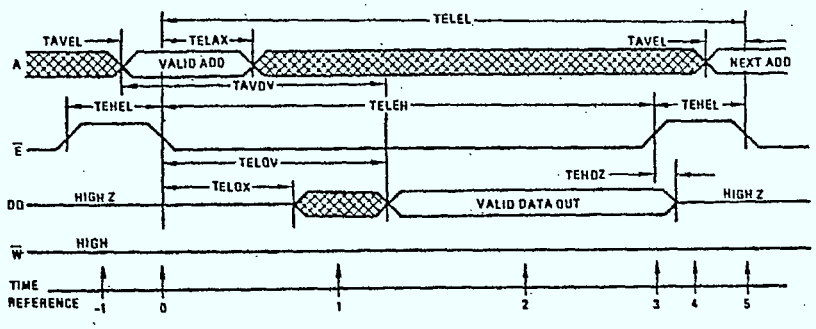
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – VCC	+8.0V	Operating Supply Voltage Commercial	4.75V to 5.25V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Operating Temperature Commercial	0°C to +75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	350		300	200		ns	④
	TELWH	Write Enable Pulse Hold Time	350		300	200		ns	④
	TDVWH	Data Setup Time	250		220	150		ns	④
	TWHDZ	Data Hold Time	0		0	0		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	0		ns	④
	TDVWL	Output Data Valid to Write Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		420	320		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

Read Cycle

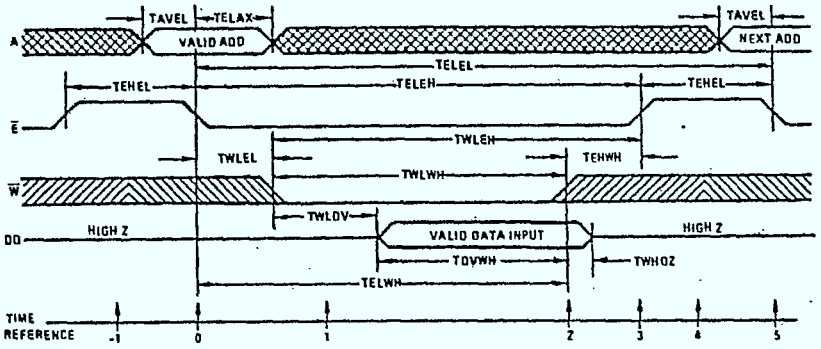


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of Ē (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). W̄ must remain high throughout the read cycle. After the data has been read Ē may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



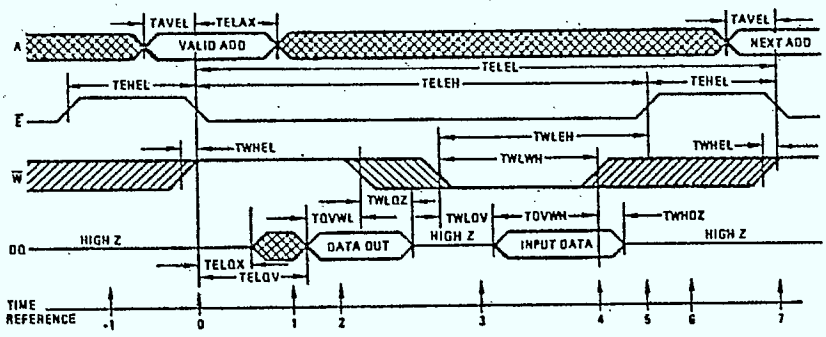
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of Ē (T = 0), which latches the address information in on chip registers. If a dedicated write cycle is to be performed and the outputs are not to become active TWLEL and TEHWH must be met. Under these conditions TWLDV is unnecessary and input data may be applied at any convenient time as long as TDVWH is still met. If TWLEL is not met then the outputs may become enabled momentarily near the beginning of the cycle and a disable time (TELQZ) must be met before the input data is applied (TWLQZ = TWLDV). Similiarly, if TEHWH is not met the outputs may enable briefly near the end of the cycle.

The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum required $\overline{E}$ high time (TEHEL) the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

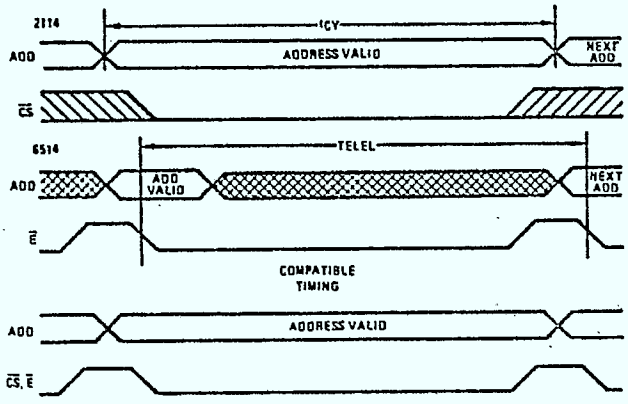
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↘	X	V	WRITE MODE, DATA IS WRITTEN
5	↘	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2114 Compatibility



2114 — Requires the Address to Remain Valid Throughout the Cycle.

6514 — Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

Battery Backup Applications

The HM-6514 is especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1.) As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2.) $\overline{E}$ must be held high at CMOS VCC. $\overline{W}$, address and data inputs should be held at either GND or CMOS VCC to minimize power dissipation.

3.) When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4.) The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75 volts).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reverse biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop, .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanuin diode yielding a VF ≈.2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the $\overline{E}$ circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

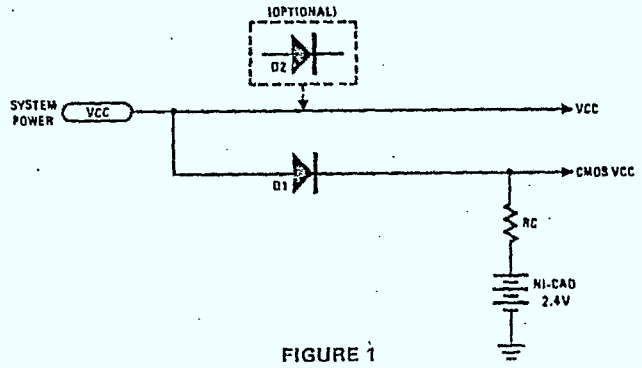


FIGURE 1

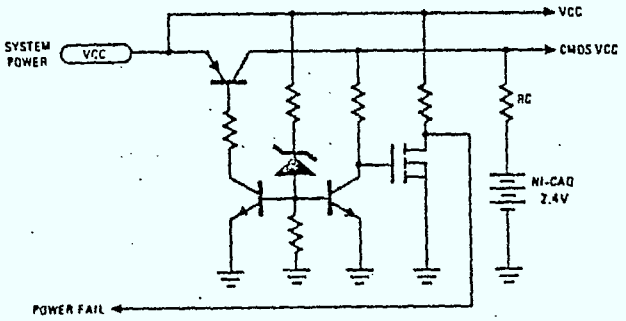


FIGURE 2

INTERSIL

IM6653/IM6654 4096 Bit CMOS UV Erasable PROM

FEATURES

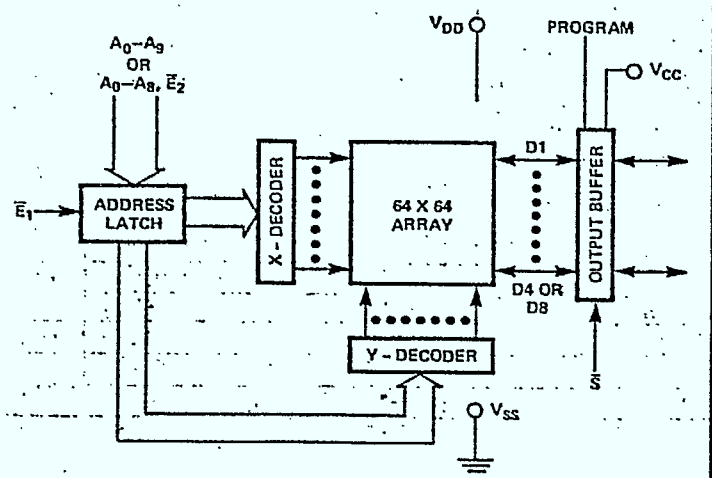
- Organization — IM6653: 1024 x 4
  IM6654: 512 x 8
- Low Power — 5μW Typical Standby
- High Speed
  — 300ns 10V Access Time for IM6653/54 AI
  — 450ns 5V Access Time for IM6653/54 -1I
- Single +5V supply operation
- UV erasable
- Synchronous operation for low power dissipation
- Three-state outputs and chip select for easy system expansion
- Full −55°C to +125°C MIL range device — IM6653/54 M

GENERAL DESCRIPTION

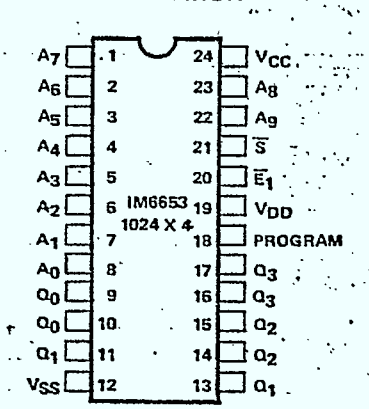
The Intersil IM6653 and IM6654 are fully decoded, 4096-bit, CMOS electrically programmable ROMs (EPROMs) fabricated using Intersil's advanced CMOS processing technology. The EPROMs are specifically designed for program development applications where rapid turn-around for program changes is required.

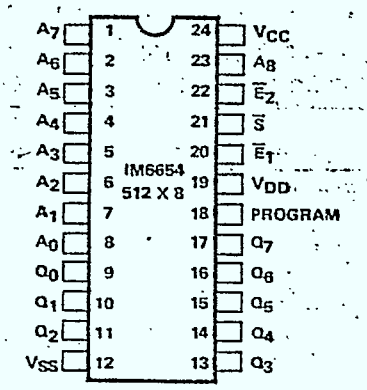
The 24 pin packages have a transparent lid to allow the user to erase the EPROM by exposing it to ultraviolet light. The EPROM may then be reprogrammed.

BLOCK DIAGRAM



PIN CONFIGURATION





ORDERING INFORMATION

24 PIN PACKAGE		SELECTION/TEMPERATURE RANGE			
		INDUSTRIAL			MILITARY
		STD 5V	HI SPEED 5V	STD 10V	STD 5V
CERDIP (FRIT SEAL)	JG	IJG	-1I JG	AIJG	MJG
CERAMIC (SIDE BRAZE)	DG	IDG	-1I DG	AIDG	MDG

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... +11.0V
- $V_{CC} = V_{DD}$ ..... +11.0V

Input or Output Voltage Supplied ..... GND −0.5V to V_{DD} +0.5V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
- Temperature
  - Industrial ..... −40°C to +85°C
  - Military ..... −55°C to +125°C
- Voltage
  - 6653/54 I, -1I 4.5-5.5
  - 6653/54 M 4.5-5.5
  - 6653/54 AI 9.5-10.5

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD}$ = Operating Voltage Range, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54I, -1I, M		IM6653/54AI		UNITS
			MIN	MAX	MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1$, $\overline{S}$	V_{DD} - 2.0		V_{DD} - 2.0		V
	V_{IH}	Address Pins	2.7		V_{DD} - 2.0		
Logical "0" Input Voltage	V_{IL}			0.8		0.8	
Input Leakage	I_I	$0V \leq V_{IN} \leq V_{DD}$	-1.0	1.0	-1.0	1.0	µA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	V_{CC} - 0.01		V_{CC} - 0.01		V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2$ mA	2.4				
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$		GND +0.01		GND +0.01	
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 2.0$ mA		0.45			
Output Leakage	I_{OZ}	$0V \leq V_O \leq V_{CC}$	-1.0	1.0	-1.0	1.0	µA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100		100	
	I_{CC}	$V_{IN} = V_{DD}$		40		40	
Operating Supply Current	I_{DDOP}	f=1 MHz		6		12	mA
Input Capacitance	C_I	Note 1		7.0		7.0	pF
Output Capacitance	C_O	Note 1		10.0		10.0	

Note: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

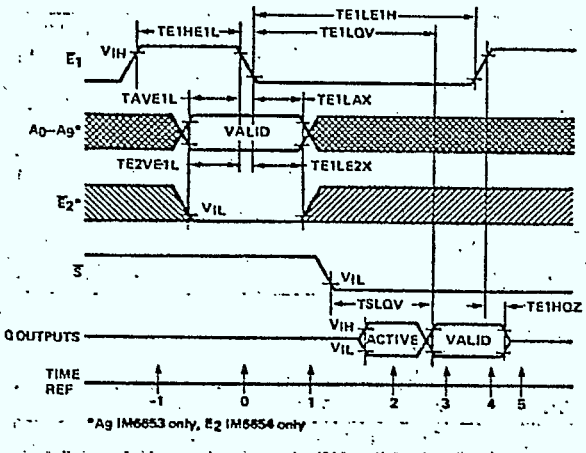
TEST CONDITIONS: $V_{CC} = V_{DD}$ = Operating Voltage Range, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6653/54-1I		IM6653/54 I		IM6653/54 M		IM6653/54 AI		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE1LQV		450		550		600		300	
Output Enable Time	TSLQV		110		140		150		60	
Output Disable Time	TE1HQZ		110		140		150		60	
$\overline{E}_1$ Pulse Width (Positive)	TE1HE1L	130		150		150		125		
$\overline{E}_1$ Pulse Width (Negative)	TE1LE1H	450		550		600		300		ns
Address Setup Time	TAVE1L	0		0		0		0		
Address Hold Time	TE1LAX		80		100		100		60	
Chip Enable Setup Time (6654)	TE2VE2L	0		0		0		0		
Chip Enable Hold Time (6654)	TE2LE2X		80		100		100		60	

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	—	Address Lines
9-11,13-17	Q_0-Q_7	—	Data lines, 6654
	Q_0-Q_3	—	Data lines, 6653
12	V_{SS}	—	GND
18	Program	—	Programming pulse input
19	V_{DD}	—	Chip +V supply, normally tied to V_{CC}
20	$\overline{E_1}$	L	Strobe line, latches both address lines and, for 6654, Chip enable E_2
21	$\overline{S}$	L	Chip select line, must be low for valid data outputs
22	A_9	—	Additional address line for 6653
	$\overline{E_2}$	L	Chip enable line, latched by strobe E_1 on 6654
24	V_{CC}	—	Output buffer +V supply

READ CYCLE TIMING



READ MODE OPERATION

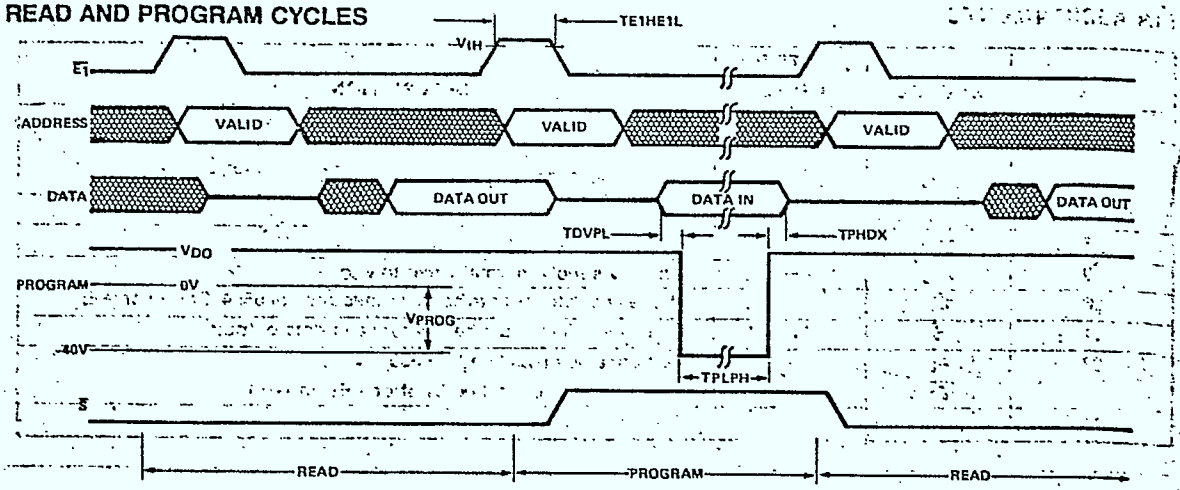
In a typical READ operation the address lines are latched by a downward edge on the strobe line, $\overline{E_1}$. The chip must then be selected by driving pin 21 ($\overline{S}$) low. If the chip has been selected the data outputs become valid an access time (TELQV) after the downward strobe edge. The data outputs remain valid until the strobe line is returned to a high level. Both $\overline{S}$ and $\overline{E_2}$ may be tied low during the READ cycle. Note that $\overline{E_2}$ is latched by the downward strobe edge, but $\overline{S}$ is not. The PROGRAM pin must be tied high to V_{DD}.

FUNCTION TABLE

TIME	INPUTS				OUTPUTS	NOTES
REF.	$\overline{E1}$	$\overline{E2}$*	$\overline{S}$	A	Q	
-1	H	X	X	X	Z	DEVICE INACTIVE
0	↓	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E2}$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF ($\overline{E1}$,$\overline{S}$)
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↑	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS -1)
0	↓	H	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E2}$ LATCHED
1	L	X	X	X	Z	OUTPUTS REMAIN HIGH-Z SINCE $\overline{E2}$ LATCHED HIGH

*$\overline{E2}$ not present on IM6653 which functions as if $\overline{E2}$ were tied LOW.

READ AND PROGRAM CYCLES



DC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pin Load Current	I_{PROG}			80	100	mA
Programming Pulse Amplitude	V_{PROG}		38	40	42	V
V_{CC} Current	I_{CC}			0.1	5	mA
V_{DD} Current	I_{DD}			40	100	
Address Input High Voltage	V_{IHA}		V_{DD} -2.0			V
Address Input Low Voltage	V_{ILA}				0.8	
Data Input High Voltage	V_{IH}		V_{DD} -2.0			
Data Input Low Voltage	V_{IL}				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pulse Width	TPLPH	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
Program Pulse Duty Cycle					75%	
Data Setup Time	TDVPL		9	10		μs
Data Hold Time	TPHDX		9	10		
Strobe Pulse Width	TE1HE1L		150			ns
Address Setup Time	TAVE1L		0			
Address Hold Time	TE1LAX				100	
Access Time	TE1LQV				1000	

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode, V_{CC} and V_{DD} are tied together to the normal operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at V_{DD}-2V minimum. Low logic levels must be set at V_{SS}+.8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E_1}$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to -40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. Pulse rise and fall times must not be faster than 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

IM6653/IM6654

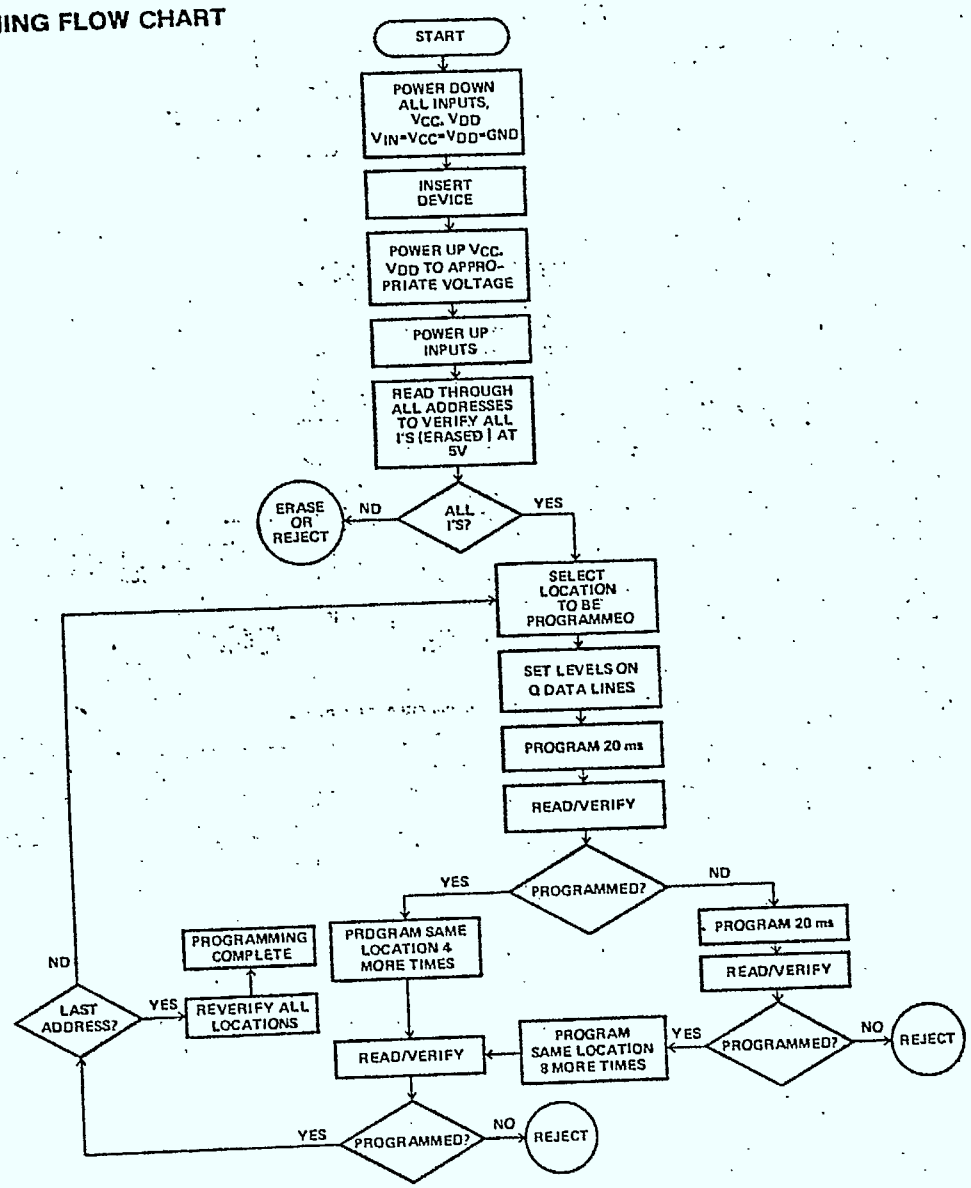
PROGRAMMING SYSTEM CHARACTERISTICS

1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40V volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied following the algorithm shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins.
4. The programming is to be done at room temperature.

ERASING PROCEDURE

The IM6653/54 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm². The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before programming.

PROGRAMMING FLOW CHART



INTERSIL

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- Low Power — Less Than 10mW Typ. at 2MHz
- Operation Up to 4MHz Clock — IM6402A
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UART's — IM6402
- On-Chip Oscillator with External Crystal — IM6403
- Operating Voltage —
  - — IM6402-1/03-1: 4-7V
  - — IM6402A/03A: 4-11V
  - — IM6402/03: 4-7V

GENERAL DESCRIPTION

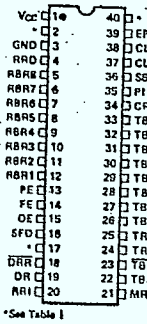
The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 7.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits operating clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 on pins 2, 17, 19, 22, and 40 as shown in Figure 5. The IM6403 utilizes pin 2 as a crystal divide control and pins 17 and 40 for an inexpensive crystal oscillator. TBREmpty and DReady are always active. All other input and output functions of the IM6402 and IM6403 are identical.

PIN CONFIGURATION



*See Table 1

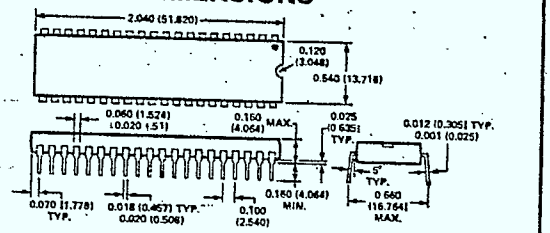
TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT CLOCK
2	N/C	DIVIDE CONTROL	DIVIDE CONTROL
17	RRC	XTAL	EXTERNAL CLOCK INPUT
40	TRC	XTAL	GND

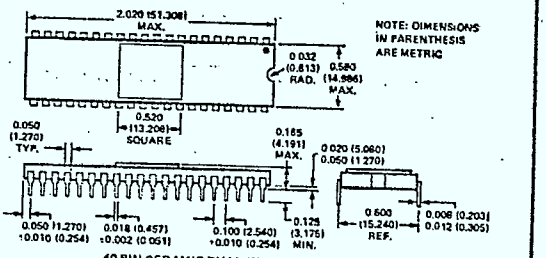
ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-IPL
CERAMIC PKG	IM6402-1/03-1IDL	IM6402/03-AIDL	—
MILITARY TEMP.	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP. WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

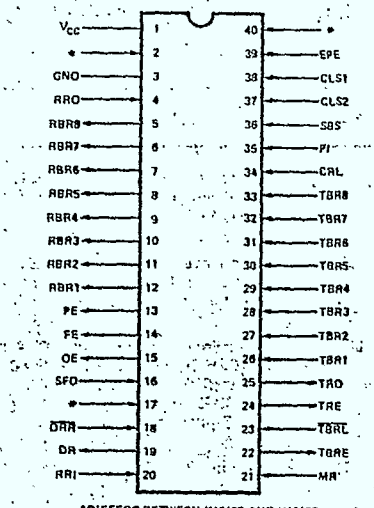
PACKAGE DIMENSIONS



40 PIN PLASTIC DUAL-IN-LINE PACKAGE (PL)



40 PIN CERAMIC DUAL-IN-LINE PACKAGE (DL)



*DIFFERS BETWEEN IM6402 AND IM6403.

FIGURE 1. Pin Configuration

IM6403 FUNCTIONAL PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$: active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE* to a high impedance state. See Figure 4 and Figure 5. *IM6402 only.
17	IM6402-RRC IM6403-XTAL or EXT CLK IN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 2.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 3.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL or GND	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TABLE 2. Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402AI/03AI ..... -40°C to +85°C
- Military IM6402AM/03AM ..... -55°C to +125°C

Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4V to 11V, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		5.0	500	µA
8	I_{CC}	Power Supply Current IM6402A Dynamic	f_C = 4MHz			9.0	mA
9	I_{CC}	Power Supply Current IM6403A Dynamic	$f_{CRYSTAL}$=3.58MHz			13.0	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_C	Clock Frequency IM6402A	See Timing Diagrams (Figures 2,3,4)	D.C.	6.0	4.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403A			8.0	6.0	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
4	t_{MR}	Pulse Width MR		400	200		ns
5	t_{DS}	Input Data Setup Time		40	0		ns
6	t_{DH}	Input Data Hold Time		30	30		ns
7	t_{EN}	Output Enable Time			40	70	ns

TIMING DIAGRAMS

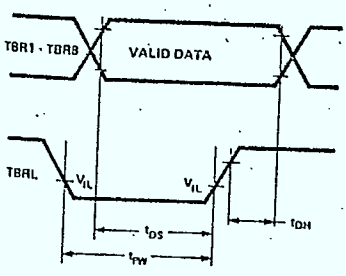


FIGURE 2. Data Input Cycle

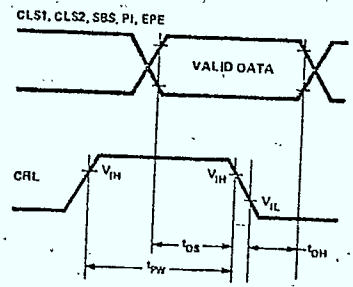


FIGURE 3. Control Register Load Cycle

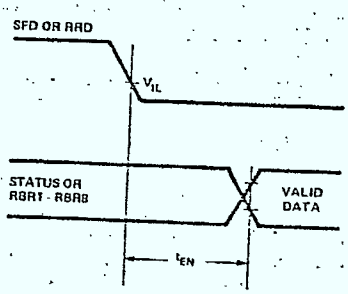


FIGURE 4. Status Flag Enable Time or Data Output Enable Time

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402-1I/03-1I ..... -40°C to +85°C
- Military IM6402-1M/03-1M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH}=-0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{DL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	100	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_C = 2MHz			1.9	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{CRYSTAL}$=3.58MHz			5.5	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_C	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.	3.0	2.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403			4.0	3.58	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
4	t_{MR}	Pulse Width MR		400	200		ns
5	t_{DS}	Input Data Setup Time		50	20		ns
6	t_{DH}	Input Data Hold Time		60	40		ns
7	t_{EN}	Output Enable Time			80	160	ns

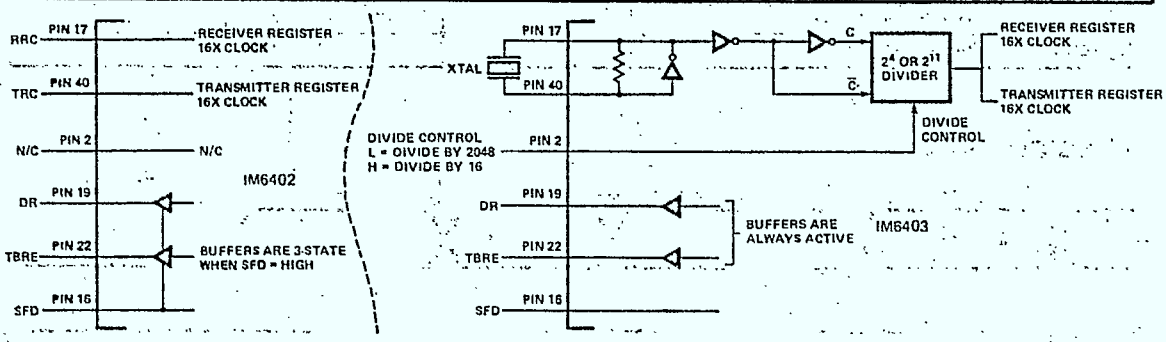


FIGURE 5. Functional Difference Between IM6402 and IM6403 UART (6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three inputs (RRC, TRC, pin 2) as shown in Figure 5. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 11). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
IM6402/03 ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0 \pm 10\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-5.0		5.0	µA
4	V_{OH}	Output Voltage High	$I_{OH} = -0.2mA$	2.4			V
5	V_{OL}	Output Voltage Low	$I_{OL} = 1.6mA$			0.45	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-5.0		5.0	µA
7	I_{CC}	Power Supply Current Standby	$V_{IN} = GND$ or V_{CC}		1.0	800	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	$f_C = 500$ KHz			1.2	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{CRYSTAL} = 2.46$MHz			3.7	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: $V_{CC} = 5V$, $T_A = 25°C$.

A.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0V \pm 10\%$, $C_L = 50pF$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_C	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.	3.0	1.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403			4.0	2.46	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
4	t_{MR}	Pulse Width MR		600	200		ns
5	t_{DS}	Input Data Setup Time		75	20		ns
6	t_{DH}	Input Data Hold Time		90	40		ns
7	t_{EN}	Output Enable Time			80	190	ns

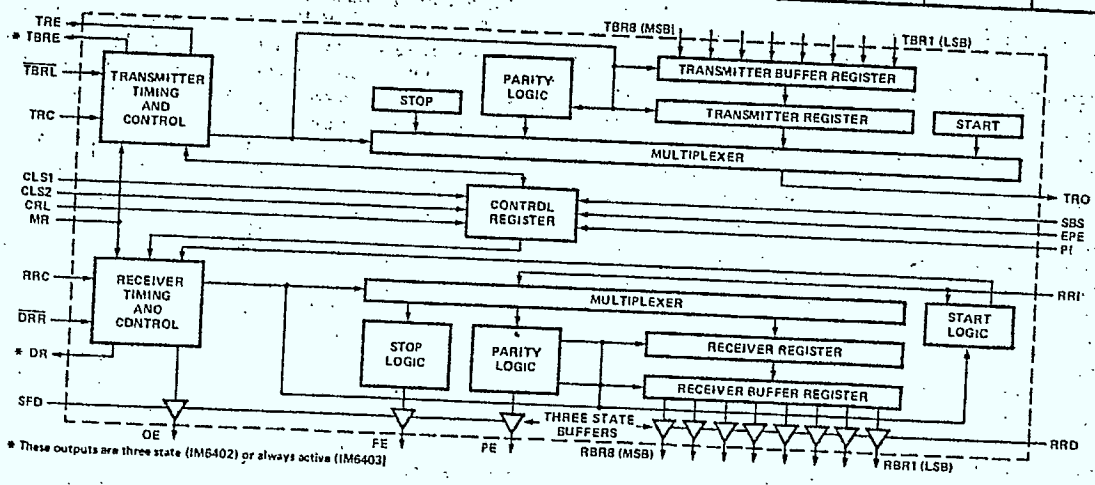


FIGURE 6. IM6402/03 Functional Block Diagram

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal.

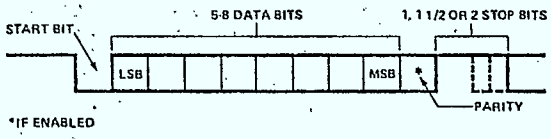


FIGURE 7. Serial Data Format

Transmitter timing is shown in Figure 8. Ⓐ Data is loaded into the transmitter buffer register from the inputs T8R1 through T8R8 by a logic low on the $\overline{\text{T8RL}}$ oad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{\text{TBRL}}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. Ⓑ The rising edge of $\overline{\text{TBRL}}$ clears TBREmpty. 0 to 1 clock cycles later data is transferred to the transmitter register and TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins.

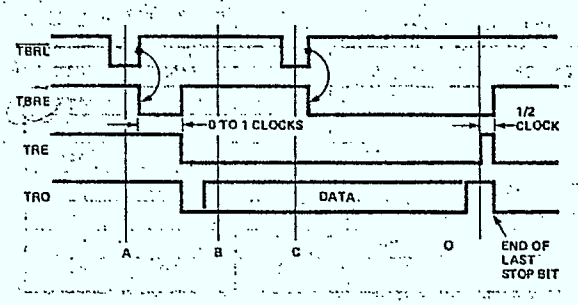


FIGURE 8. Transmitter Timing (Not to Scale)

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Receiver timing is shown in Figure 9.

Ⓐ A low level on $\overline{\text{DRR}}$eset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transfered to the RBRegister. A logic high on PError indicates a parity error. Ⓒ 1/2 clock cycle later DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

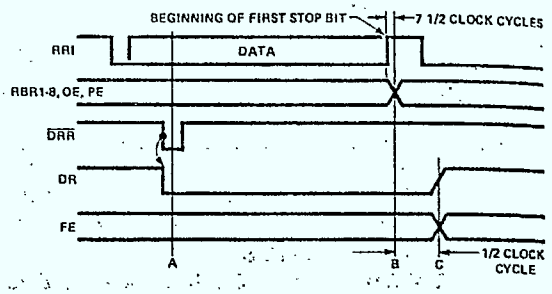


FIGURE 9. Receiver Timing (Not to Scale)

START BIT DETECTION

The receiver uses a 16X clock for timing (see Figure 10.) The start bit Ⓐ could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

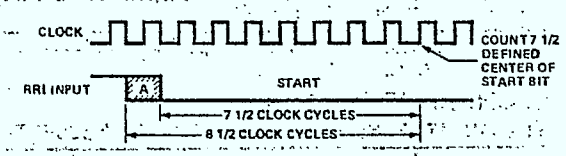


FIGURE 10. Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 11 shows how the IM6403 can be interfaced to an IM6100 microcomputer system with the aid of an IM6101 Programmable Interface Element (PIE). The PIE interprets Input/Output transfer (IOT) instructions from the processor and generates read and write pulses to the UART. The SENSE lines on the PIE are also employed to allow the processor to detect UART status. In particular, the processor must know when the Receive Buffer Register has accumulated a character (DR active), and when the Transmit Buffer Register can accept another character to be transmitted.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs should be committed.

The baud rate at which the transmitter and receiver will operate is determined by the external crystal and DIVIDE CONTROL pin on the IM6403. The internal divider can be set to reduce the crystal frequency by either 16 (PIN 2:HIGH) or 2048 (PIN 2:LOW) times. The frequency out of the internal divider

Preliminary Data

8-Bit Input/Output Port

The RCA-CDP1852D and CDP1852CD are parallel, 8-bit, mode-programmable COS/MOS input/output ports designed for use in CDP-1800 series microprocessor systems. These input/output ports are compatible and will interface directly with the CDP1802 without additional components.

The mode control is used to program the device as an input port (mode=0) or output port (mode=1). If the CDP1852 is used as an input port (mode=0), data is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request Flip-Flop ($\overline{SR}$=0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the microprocessor. When $\overline{CS1}$·CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of $\overline{CS1}$·$\overline{CS2}$ resets the Service Request Flip Flop, $\overline{SR}$=1.

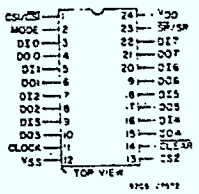
If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1}$·CS2·CLOCK=1. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1}$·CS2=1 and will be present, 1 level, until the following negative, high-to-low transition of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register and service request flip-flop.

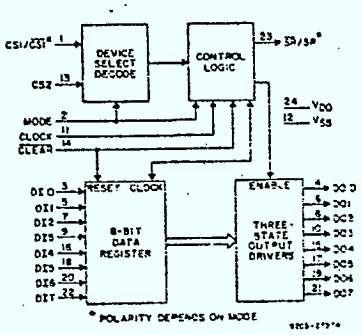
The CDP1852D is functionally identical to the CDP1852CD. The CDP1852D has a recommended operating voltage range of 3 to 12 volts, and the CDP1852CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1852D and CDP1852CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

Features:
- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Interfaces with CDP1802 microprocessor without additional components
- Single voltage supply
- Full military temperature range (−55°C to +125°C)
- Parallel 8-bit data register and buffer
- Flip-flop for service request
- Asynchronous register clear
- Low quiescent and operating power



Terminal Assignment



Functional Diagram

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1852D ..... −0.5 to +15 V
CDP1852CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor
For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1852D Min.	CDP1852D Max.	CDP1852CD Min.	CDP1852CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Strobe Pulse Width, t_{WS}		Typical		Typical		
	5	200		200		ns
	10	100		–		
Data Setup Time, t_{DS}	5	0		0		ns
	10	0		–		
Data Hold Time, t_{DH}	5	100		100		ns
	10	50		–		

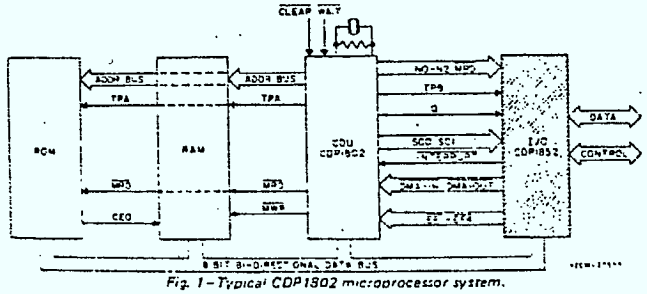
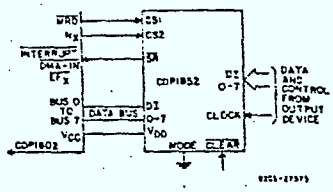


Fig. 1 – Typical CDP1802 microprocessor system.

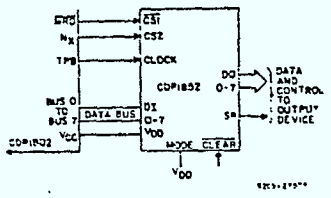
ELECTRICAL CHARACTERISTICS at T_A=25°C

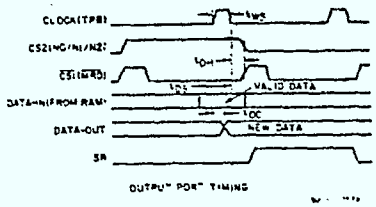
CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1852D TYPICAL VALUES	LIMITS CDP1852CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L	–	5	50	100	μA
	–	10	100	–	
	–	15	500	–	
Output Drive Current:					
N-Channel (Sink), I_DN	0.4	5	1.6	1.6	mA
	0.5	10	3.6	–	
P-Channel (Source), I_DP	4.6	5	−1.6	−1.6	
	9.5	10	−3.6	–	
Dynamic: t_r, t_f=10 ns, C_L=50 pF					
Propagation Delay Times:					
Output from CS, t_{CA}	–	5	200	200	ns
	–	10	100	–	
Data to Output, t_{OD}	–	5	200	200	
	–	10	100	–	

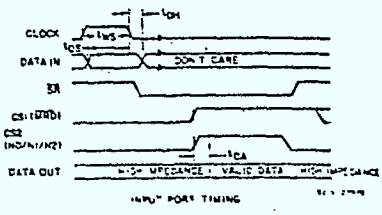


MODE = 0

CLOCK	CS1·CS2	$\overline{CLEAR}$	Data Out Equals
X	0	X	High-Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In







MODE = 1

CLOCK	$\overline{CS1}$·CS2	$\overline{CLEAR}$	Data Out Equals
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

SR = 1▲	SR = 0
$\overline{CS1}$·CS2 ↘	CLOCK ↘ Or $\overline{CLEAR}$ ↘

Fig. 2—CDP1852 output port operation.

$\overline{SR}$ = 0	$\overline{SR}$ = 1▲
CLOCK ↘	CS1·CS2 ↘ Or $\overline{CLEAR}$ ↘

Fig. 3—CDP1852 input port operation.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1852. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1852 is used as an output port with the CDP1802 microprocessor:

$$t_{WS}(TPB) = 1.0\ t_c$$

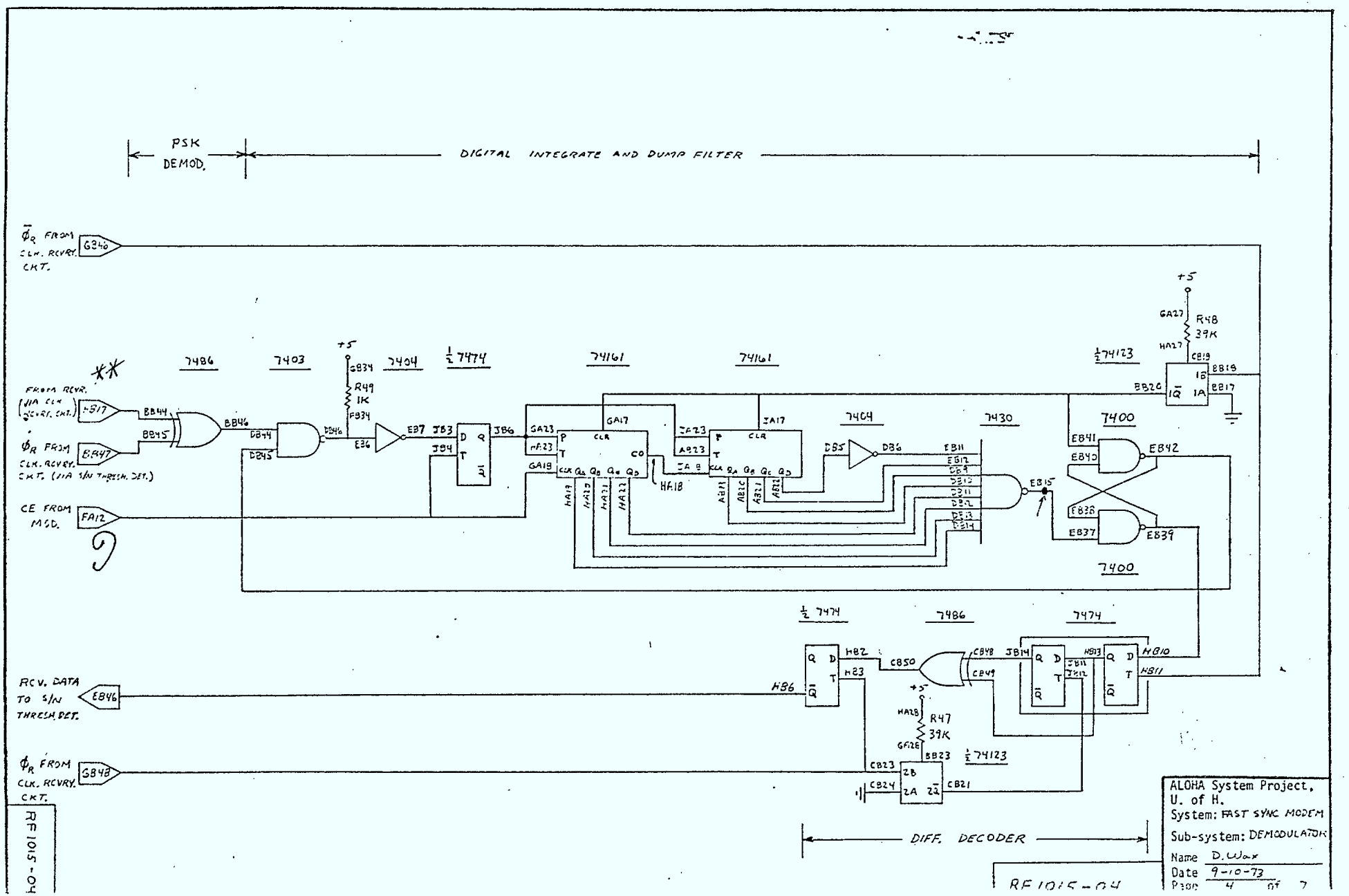
$$t_{DH} = 0.5\ t_c$$

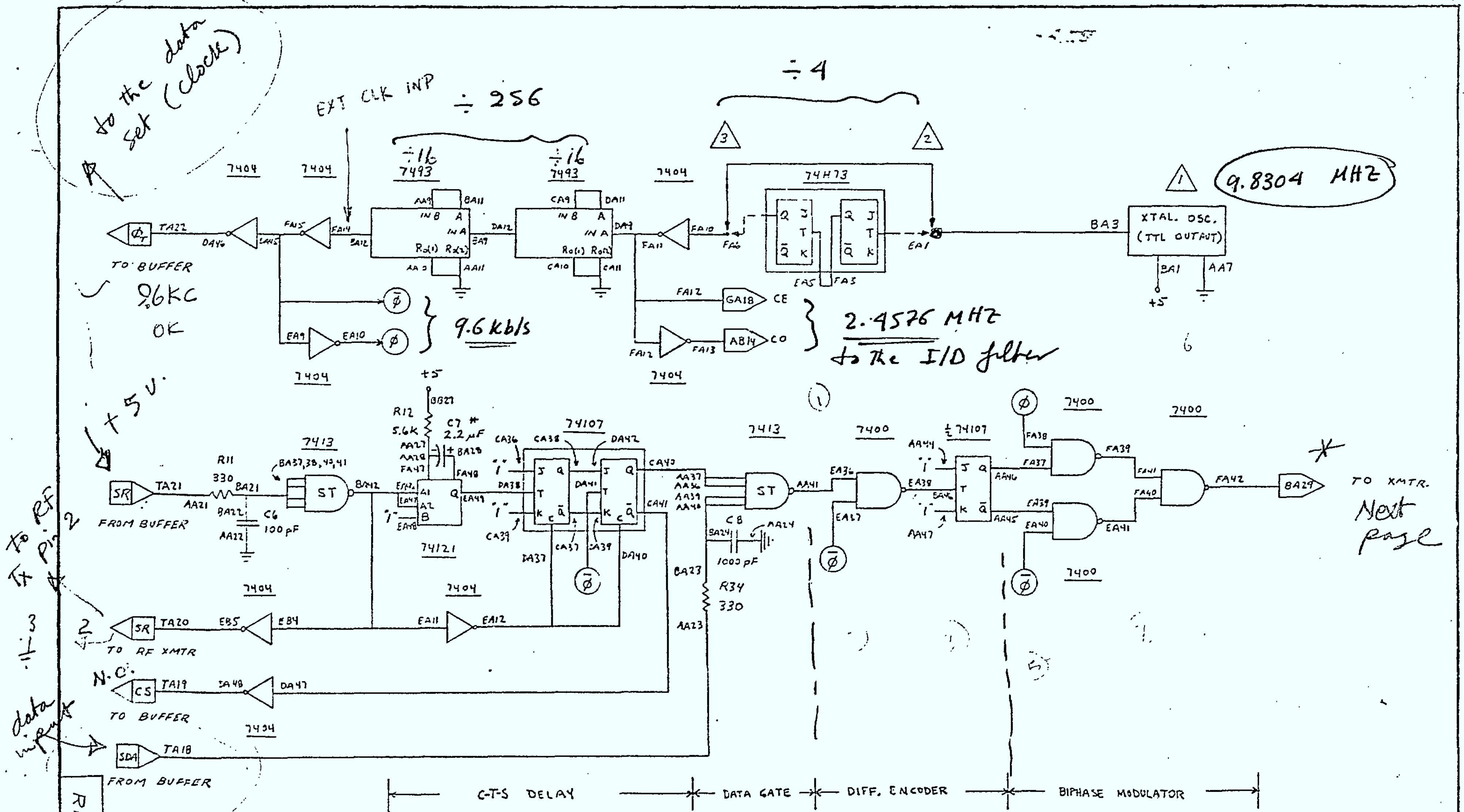
$$t_c = \frac{1}{\text{CDP1802 clock frequency}}$$

▲ The service request flip-flop is placed in the "1" state by the termination of the I/O port selection, CS1·CS2 or $\overline{CS1}$·CS2. System implementations should be avoided which cause a transient selection of the port. The termination of the signal may improperly place the service request flip-flop in the "1" state. The transition used to set and reset SR/$\overline{SR}$ may be positive or negative. The polarity will not affect circuit operation shown in Figs. 2 and 3.

APPENDIX C

DPSK Modem Circuit Diagram


PSK DEMOD.
DIGITAL INTEGRATE AND DUMP FILTER
$\bar{\phi}_R$ FROM CLK. RCVRY. CKT.
ϕ_R FROM CLK. RCVRY. CKT. (VIA S/N THRESH. DET.)
CE FROM MSD.
FROM RCVR. (VIA CLK RCVRY. CKT.)
7486
7403
7404
½ 7474
74161
74161
7404
7430
7400
½74123
7400
½ 7474
7486
7474
½74123
+5
R48 39K
R49 1K
R47 39K
RCV. DATA TO S/N THRESH. DET.
ϕ_R FROM CLK. RCVRY. CKT.
DIFF. DECODER
RF1015-04
ALOHA System Project, U. of H.
System: FAST SYNC MODEM
Sub-system: DEMODULATOR
Name D. Wax
Date 9-10-73
Page 4 of 7



△ — SEE DATA RATE OPTION TABLE

* — 10 % TOLERANCE

RF 1015-01

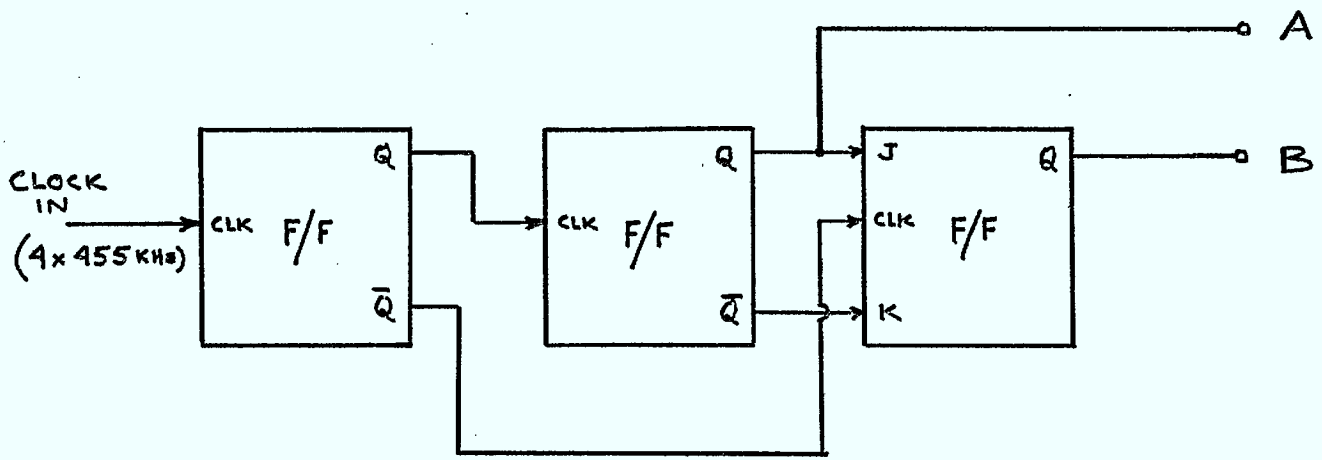
ALOHA System Project,
U. of H.
System: FAST SYNC MODEM
Sub-system: MODULATOR
Name D. Wax
Date 9-10-73
Page 1 of 7

RF 1015-01

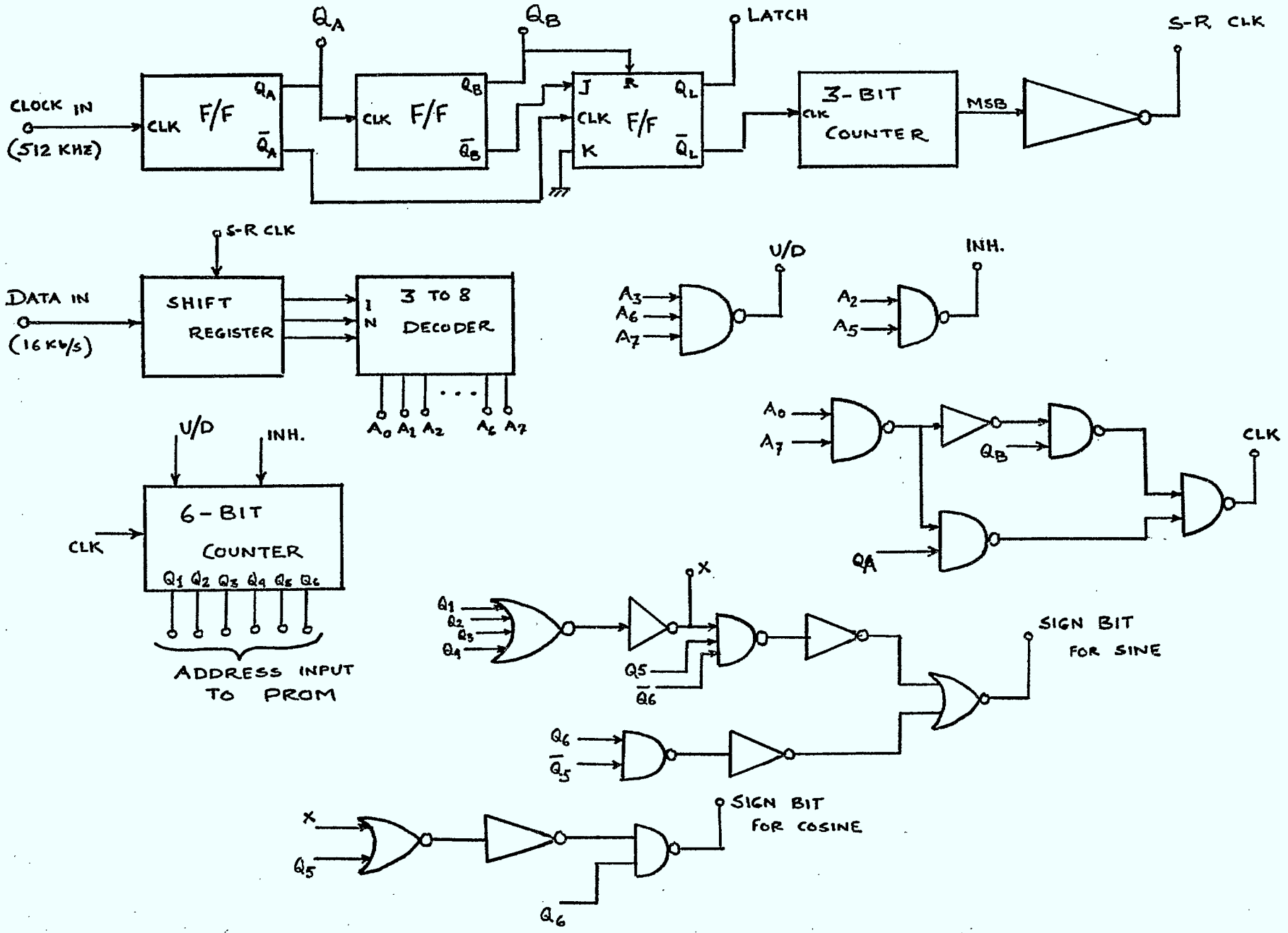
APPENDIX D

IMPORTANT CIRCUIT DETAILS

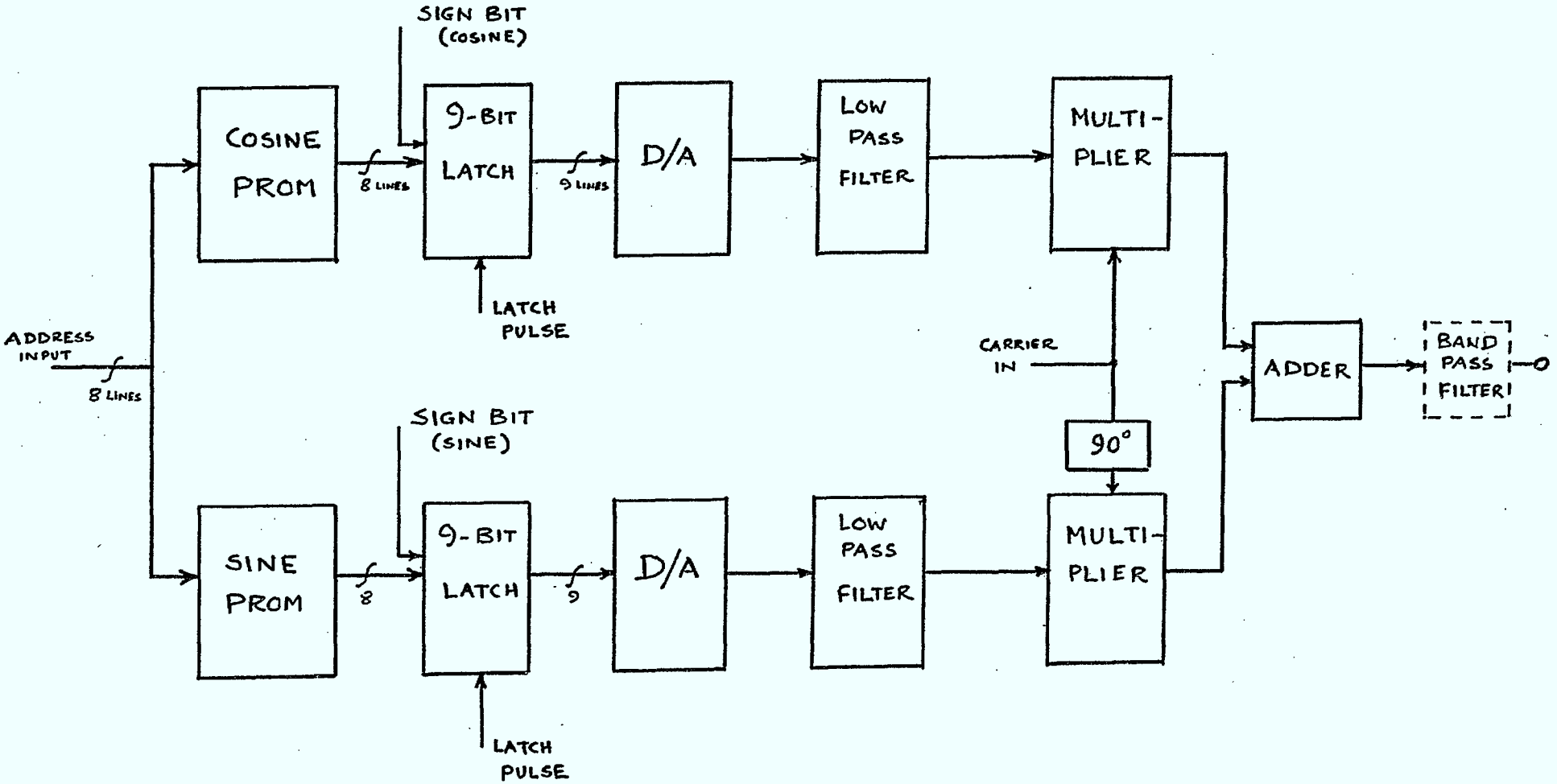
FOR TFM MODULATOR



GENERATION OF 90° PHASE SHIFTED SQUARE WAVES


CLOCK IN
(512 KHz)
CLK F/F
Q_A
$\bar{Q}_A$
CLK F/F
Q_B
$\bar{Q}_B$
J R
CLK F/F
K
Q_L
$\bar{Q}_L$
LATCH
3-BIT COUNTER
CLK
MSB
S-R CLK
DATA IN
(16 Kb/s)
SHIFT REGISTER
3 TO 8 DECODER
IN
A_0 A_1 A_2 A_6 A_7
S-R CLK
U/D
INH.
A_3
A_6
A_7
A_2
A_5
U/D
INH.
CLK
6-BIT COUNTER
Q_1 Q_2 Q_3 Q_4 Q_5 Q_6
ADDRESS INPUT TO PROM
A_0
A_7
Q_B
CLK
$\bar{Q}_A$
X
Q_1
Q_2
Q_3
Q_4
Q_5
$\bar{Q}_6$
SIGN BIT FOR SINE
Q_6
$\bar{Q}_5$
X
Q_5
Q_6
SIGN BIT FOR COSINE

LOGIC PART


SIGN BIT (COSINE)
COSINE PROM
8 LINES
9-BIT LATCH
9 LINES
D/A
LOW PASS FILTER
MULTI-PLIER
LATCH PULSE
ADDRESS INPUT
8 LINES
CARRIER IN
ADDER
BAND PASS FILTER
90°
SIGN BIT (SINE)
SINE PROM
8
9-BIT LATCH
9
D/A
LOW PASS FILTER
MULTI-PLIER
LATCH PULSE

ANALOG PART

MAHMOUD, SAMY A.
--Analysis and design of land mobile communications systems based on digital techniques: final report.