CARLETON UNIVERSITY
SYSTEMS ENGINEERING

STUDY ON "SSB MOBILE RADIO SYSTEMS"
FINAL REPORT

by

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1.0 INTRODUCTION

1.1 SCOPE

The objective of this research is to examine the feasibility of applying the SYNCOMPEX concept to SSB Mobile Communication Systems at UHF/VHF frequencies. Specifically, the research examines the following aspects:

1) Study of variable ratio companding algorithms and digital encoding of the output of these algorithms.

2) Study of suitable modulation systems for the transmission of the encoded companding ratio (control signal), and automatic frequency control circuits.

3) Study of the intermodulation effects resulting when the modulated control signal is placed out-of-band and in-band with respect to the audio (speech) signal.

4) Study of the Automatic Gain Control (AGC) System and its resultant audio signal distortion.

5) Results of these studies will then be used to examine the feasibility of a digital implementation of the base band section of the SSB System. Schematic design details of such implementation will follow the studies of the various components.

At present, two different SSB tranceivers with Pilot-Based Fading Correction circuits are available commercially. However, no standard has been adopted yet with respect to the signal characteristics, the companding method and the fading correction mechanisms. This leaves the door open for the development of new generations of SSB tranceivers with enhanced cost/performance ratio and additional features. In this context, the system investigated here has the potential of several advantages over existing systems:

1) The transmission of speech signals and data signals without the need for an external data modem, since the digital implementation includes a built-in modem for the control signal.

2) The use of signal processors (eg. NEC 7720 and TMS320) permits the implementation of other speech processing mechanisms, such as speech encryption (in the frequency demain), if required.

3) The all digital implementation of the SSB Base Band section is consistent with the current technological trends of hardware and production cost reduction.

4) Better speech quality is expected to be gained through the use of variable ratio companding algorithms.

The advantages listed above can be gained, however, only after solving several technical problems. Examples of these problems include the AGC circuit, the effect of the BER on the companding process at the receiver, the expansion of the bandwidth to accommodate the control signal, and hardware cost reduction.

This report presents a summary of research conducted to examine feasible implementation of digital SSB systems. The report includes six chapters organized as follows:

- Chapter 1. The Introduction.

- Chapter 2. This chapter presents a summary of voice companding algorithms and coding schemes for the control information. Performance estimates of various coding schemes are compared in order to select the most appropriate scheme for the digital implementation of the base-band sub-system.

- Chapter 3. This chapter investigates the basic characteristics of the modulation techniques which can be used for transmitting the companding gain information. Two modulation systems are found to meet the requirements: FSK and DPSK. The BER performance of the two techniques is investigated for the SSB channel under fading conditions. This chapter also investigates the basic structure of the AGC component and the residual signal distortion at the receiver caused by hard-limiting the correction gain signal. An AFC circuit for the receiver section is also proposed in this chapter.

- Chapter 4. This chapter investigates the intermodulation distortion which results when the modulated control signal is placed in-band and out-of-band with respect to the speech signal.

- Chapter 5. This chapter presents a preliminary schematic design for the base-band section of the SSB system based on the use of TMS 320 Signal Processor. The feasibility of implementing Hilbert Transform using the processor is also included.

- Chapter 6. This chapter presents concluding remarks and recommendations for further study.

1.2 BASIC SYSTEM CONFIGURATION

The basic system under investigation consists of a base-band section (for speech processing) and an IF/RF section for upconversion and transmission of the speech signal.

The speech signal is amplitude companded using a variable ratio companding algorithm. The value of the companding ratio, which varies with time, is encoded into a binary stream which has to be modulated and is referred to as the control signal. The spectrum of the speech signal may be inverted before the companding is applied. this sepctrum inversion is performed to reduce intermodulation effects.

A typical output signal of the base-band section will have the frequency spectrum shown in Figure 1.1. The modified Amplitude Compandored Single Side Band (ACSSB) speech signal occupies approximately 2.7 KHz. The control signal is placed beside the speech signal with an internal guard band of 0.6 KHz. External guard bands are provided to separate the SSB channel from adjacent channels.

At the receiver end, the control signal is separated from the speech signal. The envelope of the control signal is passed through an Automatic Gain Control Circuit to enable the receiver to compensate for the effects of fading on the gain of the speech signal. As well, an Automatic Frequency Control Circuit is used to

synchronize the receiver to the carrier of the in-coming signal.

It is possible to place the control signal in-band by splitting the speech signal around the mid-point frequency of the spectrum [1] and shifting the upper half to higher frequency band to make room for the control signal. This scheme has the advantage of equal group delay (due to IF filtering) for both the control signal and the speech signal. The synchronization problem between the control signal and the speech signal will be somewhat alleviated in this case. However, the in-band configuration adds complexity to the base-band processing and may adversely affect the intermodulation distortion.

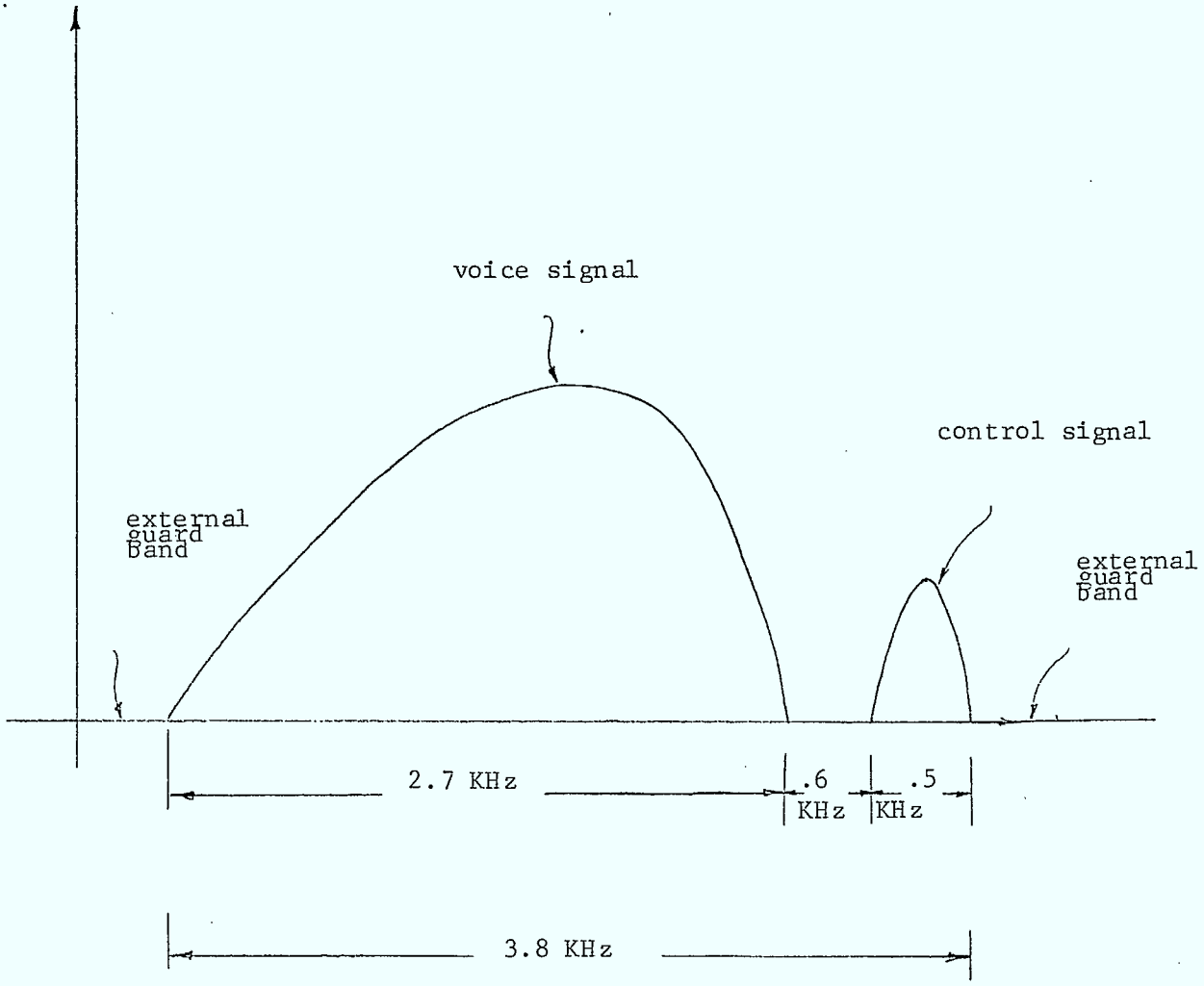


Figure 1.1
Spectrum Allocation With Out-Of-Band
Control Signal

2.0 COMPANDING ALGORITHMS AND CODING SCHEMES

2.1 COMPANDING ALGORITHMS

A brief overview of companding algorithms is presented in this section.

2.1.1 Amplitude Companding

The purpose of Amplitude Companding is to reduce the effect of noise on the quiet syllables of the voice. The basic principle is the quiet syllables are selectively amplified before transmission over the radio channel. The receiver then attenuates these syllables back to their original volume. When these syllables are attenuated, the noise from the channel is also attenuated thus making these syllables more audible.

Amplitude Companding techniques can be grouped into two catagories:

(i) Fixed Ratio: In this case the companding gain for a syllable is relative to the number of dB the syllable's volume is below maximum volume. For example in a 2:1 compander, a syllable with a relative volume of -10 dB would be amplified to -5 dB.

(ii) Variable Ratio: In this case the compander ratio is adjusted for each syllable so that all syllables are transmitted with the same volume.

The advantage of Fixed Ratio Companding is that it can be readily implemented with off-the-shelf linear IC's. The present technical limit is a 4:1 compander (two 2:1 compander chips in series) which would transmit a -40 dB syllable at -10 dB. A Variable Ratio compander, on the other hand attempts to transmit the -40 dB syllable at as close to 0 dB as possible. Thus Variable Ratio Companding is more effective at reducing the effects of channels noise on quiet syllables.

A Variable Ratio Compander also requires a Control Channel. Over this channel the actual companding ratio is transmitted to the receiver so that it will know by how much to attenuate the received voice signal. The Control Channel can be combined for transmission with the companded voice signal in two ways:

(i) Frequency Division Multiplexing: A separate frequency band within the mobile channel is dedicated to the control channel.

(ii) Time Division Multiplexing: Also know as Time Compression, blocks of the speech are compressed in time so that time slots are available for the transmission of control information.

2.1.2 Frequency Companding

The purpose of Frequency companding is to reduce the bandwidth of the voice signal. Before transmission the frequency components of voice are mapped into a smaller band of frequencies. The receiver then performs the inverse mapping and thus restores the voice signal to its original frequencies.

2.1.3 Summary

Both Frequency and Amplitude Companding could potentially be combined into the same ACSSB design. However, by switching from FM (20-30 KHz bandwidth) to ACSSB (4-6 KHz bandwidth) most of the possible spectrum efficiency improvement has already been achieved. Thus, in order to keep the cost down, it is recommended to use only Amplitude Companding since it will improve voice quality with the same transmitter power or use less transmitter power for the same voice quality.

The aim of the rest of this report is to examine the design issues for the Variable Ratio Amplitude Companding alternative with Frequency Division Multiplexing for the Control Channel. In a Fixed Ratio design, a control tone is needed for Automative Frequency Control and Automatic Gain Control at the receiver. If this pilot tone is also digitally modulated then it can carry the Control Channel information which is needed for a Variable Ratio Companding system. The Time Division Multiplexing alternative for adding the Control Channel has not been considered further because of the problems of time slot syncronization.

2.2 CODING SCHEMES

Several schemes for digitally encoding amplitude companding information are discussed in this chapter. Their performance at two different bit rates are compared against objectives for several criteria. Some overall conclusions for selection are then drawn in the summary.

2.1.1 Performance Criteria and Objectives

The performance characteristics of the coding scheme have a direct effect on the overall performance of amplitude compander/expander system. The encoding characteristics of the coding scheme limit the compander's ability to quickly and accurately adjust the compander gain to changes in the speech level within the constraint of the transmission bit rate. The decoding properties of the coding scheme largely determines how the expander reacts to transmission errors in the radio channel.

The performance criteria, employed in this chapter, provide an objective first approximation of how the choice of coding scheme affects the performance of the compander/expander system. The evaluation of speech processing systems, however, is basically a "subjective science"; thus the performance numbers (objectives and calculations) only give an approximate estimate of the overall performance of the resulting system. Each criteria and a design objective for it are described below:

(i) Dynamic Range

Definition: The maximum possible variation in the compander gain.

Design Objective: At least 40 dB.

(ii) Attack Time

Definition: The time to lower the compander gain, the full dynamic range, at the beginning of a spoken word.

Design Objective: Less than 50 ms.

(iii) Tracking Time

Definition: The time to raise or lower the gain 24 dB during a spoken word or phrase.

Design Objective: Less than 50 ms.

(iv) Steady State Precision

Definition: How close the compander gain can be adjusted to an arbitrary level.

Design Objective: Within 3 dB.

(v) Transmission Error Effects

Definition: The effect transmission errors have on the resulting expander gain.

Design Objective: Sudden large errors or continuously large errors in the expander gain should be unlikely results from transmission errors. Errors in the expander gains are considered tolerable if they do not substantially degrade the intelligibility of the speech or create objectional sounds for the listener.

The Attack and Tracking Times described above, are intended to be benchmarks for comparing the performance of various schemes and the effect of the transmission data rate constraint. The following formula is used to calculate these times:

Attack Time	=	Average latency before transmission + the time to transmit the bits required to encode a gain drop over the entire dynamic range.
Tracking Time	=	Average latency before transmission + the average time to transmit the bits required to encode a gain change of 24 dB in the middle of the dynamic range.

2.2.2 3-Bit PCM

The 3-Bit PCM scheme which was considered for an HF Syncompex System in reference [2] is evaluated in this section. Three bits of each code word select 1 out of 8 possible gain levels (0 dB, 6 dB, 12 dB, ..., 42 dB) and a fourth bit establishes word synchronization. Performance estimates for 100 and 150 bps. Transmission rates are listed in Figure 2.1.

Advantages

The 3-Bit PCM scheme adequately meets the design objectives for Dynamic Range, Attack Time, Tracking time, and Steady-State Precision at both 100 and 150 bps. Transmission errors in the 3 "gain bits" of the code word only cause an expander gain error in the one or two speech blocks affected by the code word. The expander gain will correct itself after receiving a correct code word.

Disadvantages

Single bit errors in the gain bits can cause sudden large errors in the expander gain. Bit slip or other errors which can cause incorrect word synchronization can produce extended periods of large erratic expander errors which are very annoying to the listener. Loss of word synchronization, however, is usually detectable by continuously monitoring the "sync" bit. Thus the receiver could react to loss of word synchronization by holding the expander gain at a safe level until synchronization is re-established.

2.2.3 3-Bit Delta Modulation

There are many possible 3-bit Delta Modulation schemes; thus to keep the analysis simple only one scheme whose performance is believed to be representative, is evaluated in this section. The scheme is taken from reference [2] and the coding is shown below:

Code	Gain Step
010	set to 8
111	+2 steps
101	0 "
001	-1 "
100	-2 "
000	-3 "

This code achieves word synchronization with unique self-synchronizing words. There are 8 compander gain levels .pa and a 6 dB step size. Performance estimates for 100 and 150 bps are listed in figure 2.1.

Advantages

At 150 bps, the 3-Bit Delta Modulation scheme meets the design objectives for Dynamic Range, Tracking Time, and Steady-State Precision, while the Attack Time is only slightly poorer than the objective. However, when the transmission speed is lowered to 100 bps the Attack and Tracking Time objectives are no longer met. So long as word synchronization is maintained, a transmission error in one code word will not cause a prolonged error in expander gain.

Disadvantages

Single bit errors can cause sudden large errors in the expander gain. Bit slips or other errors which cause incorrect word synchronizatin can produce extended periods of large erratic expander gain errors which are very annoying to the listener. Because word synchronization is achieved with unique code words, it may take a long time to detect a loss of word synchronization. Thus it will be difficult for the expander to take compensating action during periods of incorrect synchronization.

2.2.4 2-Bit Delta Modulation

The 2-Bit Delta Modulation scheme which was considered for H.F. Syncompex in reference [2] is evaluated in this section. There are 8 compander gain levels, each separated by a 6 dB step size. The coding is shown below:

Code	Gain Step
11	+4 steps
01	0
00	-1

Word synchronization is achieved using unique self synchronizing words. Performance estimates for 100 and 150 bps are shown in figure 2.1.

Advantages

The design objectives for Dynamic Range, Tracking Time and Steady-State precision are adequately met at both 100 and 150 bps. So long as word synchronizatin is maintained, a transmission error in one code word will not cause a prolonged error in the expander gain.

Disadvantages

To meet the design objective for Attack Time a transmission data rate of about 300 bps would be required. Single bit errors can cause sudden large errors in the gain. Loss of word synchronization can produce extended periods of large erratic gain errors which will be difficult for the expander to detect.

2.2.5 1-Bit Simple Delta Modulation

In 1-Bit Simple Delta Modulation the only two codes (0 and 1) mean either raise or lower the gain by one step. Eight compander gain levels, spaced at 6 dB intervals are sufficient to achieve a 42 dB Dynamic Range and an acceptable Steady State Precision. In calculating the Steady State Precision it was assumed that the gain changes linearly during a block period rather than discontinuously at the beginning of each Block Period. In practice, discontinuous gain caused a significant distortion of the voices; thus the gain must be changed smoothly from one step to another.

The Attack Time can be improved by employing a larger step size at the beginning of each spoken word. When the compander gain changes from decreasing to increasing the step size returns to normal (Tracking) size. Performance calculations for 100 and 150 bps, and for Attacking Step Sizes of 6 and 12 dB are listed in figure 2.1. When the Attacking Step Size is 12 dB, the Dynamic Range can be increased to 48 dB (a multiple of 12 dB) without affecting the other performance measures.

Advantages

All four alternatives meet the design objectives for Dynamic Range, Attack and Tracking Time, and Steady State Precision; except for the 100 bps alternative with a 6 dB step size which has a poor Attack Time. The 150 bps alternative with a 12 dB attacking Step Size has exceptionally good Attack and Tracking Times, and a good Dynamic Range.

There are no word synchronization problems, only bit synchronization is needed. Where transmission errors do occur, they usually cause a constant error in the expander gain until either of the maximum or minimum limits are reached, at which time accummulated errors are corrected. When transmission errors occur close together there is almost a 50% probability that they will cancel each other.

Disadvantages

The worst case Steady State Precision of 6 dB is undesirable. Once there is an error in the expander gain, it will likely remain until the next end of a spoken word, at which time the expander will reach a Dynamic Range limit.

2.2.6 1-Bit Enhanced Delta Modulation

The 1-Bit Enhanced Delta Modulation scheme differs from the previous one by providing a "no change" possibility. The coding is as follows:

Code	Step Change
1 following a 1	+1 step
0 following a 1	0 "
1 following a 0	0 "
0 following a 0	-1 step

The step sizes and number of steps examined in this section, are the same as the 1-Bit Simple Delta Modulation scheme with the addition of two alternatives with 8 dB step sizes and 6 levels. The performance calculations are listed in Figure 2.1.

Advantages

All six alternatives meet the design objectives for Dynamic Range, Attack and Tracking Times, and Steady State Precision; except for the 100 bps alternative with a 6 dB step size. The 150 bps alternative with a 12 dB step has exceptionally good Attack and Tracking Times, as well as a good Dynamic Range and Steady State Precision. The 1-Bit Enhanced Delta Modulation scheme has essentially the same transmission error performance characteristics as the 1-Bit Simple Delta Modulation scheme.

Disadvantages

Once there is an error in the expander gain, it will likely remain until the end of the next spoken word. The 100 bps alternative with a 6 dB step size has a poorer Attack Time.

2.2.7 Summary

In order to rank the alternative coding schemes, the following ratings are used:

Excellent	-	Meets all design objectives and is significantly better in the overall performance.
Good	-	Clearly meets all design objectives.
Adequate	-	Meets or almost meets all design objectives.
Poor	-	does not meet all design objectives but does not have any intolerable flaws.
Unacceptable	-	Has at least one intolerable flaw.

An assessment of the various coding schemes using the above ratings, are listed in Figure 2.2. The ratings shown in this figure are only intended as an initial guideline for selecting a companding algorithm and its parameters. Because of the subjective nature of voice performance, a final design can only be arrived at after considerable experimentation and fine tuning.

Many other alternatives, with different Bit Coding Schemes, could have been considered for the 2 and 3-Bit Delta Modulation techniques. However, by changing the bit coding, one performance factor will be lowered in order to improve another. Thus further investigation of these is unlikely to yield an overall improvement which would make the 2 and 3 Delta Modulation schemes competitive with the other schemes.

	Data Rate (bps)	Block Length (ms)	Step - Size Attack (dB)	Step - Size Track (dB)	Dynamic Range (dB)	Attack Time (ms)	Track Time (ms)	Steady State Precision Average (dB)	Steady State Precision Worst Case (dB)
3 - Bit PCM	100	40	6	6	42	60	60	1.5	3.0
	150	26.7	6	6	42	40	40	1.5	3.0
3 - Bit Delta Mod.	100	33.3	6	6	42	116	83	1.5	3.0
	150	20	6	6	42	70	50	1.5	3.0
2 - Bit Delta Mod.	100	20	6	6	42	150	60	1.5	3.0
	150	13.3	6	6	42	100	40	1.5	3.0
1 - Bit Simple Delta Mod.	100	10	6	6	42	75	45	2.5	6.0
	150	6.7	6	6	42	50	30	2.5	6.0
	100	10	12	6	48	45	45	2.5	6.0
	150	6.7	12	6	48	30	30	2.5	6.0
1 - Bit Enhanced Delta Mod.	100	10	6	6	42	75	50	1.5	3.0
	150	6.7	6	6	42	50	33	1.5	3.0
	100	10	12	6	48	45	50	1.5	3.0
	150	6.7	12	6	48	30	33	1.5	3.0
	100	10	8	8	40	55	40	2.0	4.0
	150	6.7	8	8	40	37	27	2.0	4.0
Design Objectives →					40	50	50	3.0	

FIGURE 2.1 PERFORMANCE ESTIMATES FOR VARIOUS DIGITAL CODING SCHEMES

(A) Data Rate = 100 bps

GOOD:	1-Bit Simple Delta Modulation with a 12 dB Attacking Step Size
	1-Bit Enhanced Delta Modulation with a 12 dB Attacking Step Size
ADEQUATE:	3-Bit PCM
	1-Bit Enhanced Delta Modulation with 8 dB Step Sizes.
POOR:	1-Bit Simple Delta Modulation with a 6 dB Attacking Step Size
	1-Bit Enhanced Delta Modulation with a 6 dB Attacking Step Size
UNACCEPTABLE:	3-Bit Delta Modulation
	2-Bit Delta Modulation

(B) Data Rate = 150 bps

EXCELLENT:	1-Bit Enhanced Delta Modulation with a 12 dB Attacking Step Size
GOOD:	3-Bit PCM
	1-Bit Simple Delta Modulation with a 12 dB Attacking Step Size
	1-Bit Enhanced Delta Modulation with a 6 dB Attacking Step Size
	1-Bit Enhanced Delta Modulation with 8 dB Step Sizes
ADEQUATE:	1-Bit Simple Delta Modulation with a 6 dB Attacking Step Size
POOR:	3-Bit Delta Modulation
UNACCEPTABLE:	2-Bit Delta Modulation

FIGURE 2-2 ASSESSMENT OF CODING SCHEMES

3.0 MODULATION SYSTEMS AND AUTOMATIC GAIN CONTROL

Transmission of the control signal will require the use of a modulator with the following general requirements:

1. Constant amplitude modulated signal to reduce sensitivity to fading effects in the SSB-UHF/VHF channel,

2. Transmission of data rate of 150 bits/sec within an IF bandwidth limited to 0.5 kHz in order to fit the IF signal spectrum shown in Figure 1.1,

3. Non-coherent demodulation; due to the near impossibility of establishing a coherent reference at the receiver under fading channel conditions,

4. Relative implementation simplicity (i.e. circuit simplicity),

5. Acceptable BER performance (10^{-3} - 10^{-4}) under fading channel conditions.

Two modulation techniques appear to satisfy the above general requirements: non-coherehent FSK and DPSK. The former technique is simpler to implement but is less efficient in terms of spectrum utilization and BER performance. However, both techniques have constant amplitude IF signals and can be used for automatic gain compensation when RF linear amplifiers are used, as is the case in SSB tranceivers.

Section 3.1 examines the residual distortion which results when the envelope of the control signal is detected and used as a reference for Automatic Gain Control (AGC). Following the distortion analysis, an expression for the BER in the fading channel environment is obtained in Section 3.2 for non-coherent FSK and DPSK as a function of the signal-to-noise ratio. Section 3.3 presents an AFC Circuit suitable for correcting the frequency offset at the receiver for low signal-to-noise ratio.

3.1 AUTOMATIC GAIN CORRECTION (AGC) DISTORTION

Figure 3.1 illustrates the basic components of the SSB receiver. The IF signal is down-converted to base-band with a local oscillator carrier $\omega_c + \Delta\omega_c$, where $\Delta\omega_c$ is the frequency offset due to carrier stability. The voice and control signals are separated by band-pass filters. These filters are delay-matched and qualized across the respective bandwidths. The control signal is demodulated by a frequency descriminator technique (Section 3.3) which generates $\Delta\omega_c$ and the bit stream of the control signal. The speech signal is corrected by $\Delta\omega_c$ to remove the frequency offset first. This is followed by a "Limited" gain correction to compensate for fading. The gain correction signal, S_2, is the output of the envelope detector of the Control Signal.

The dynamic range of the gain correction has a limited value of $\frac{1}{\sigma r_c}$, where r_c is the RMS of the fading signal and $\frac{1}{\sigma}$ is the maximum available correction gain. The "limited" dynamic range of the correction gain introduces residual distortion which is a function of $\frac{1}{\sigma}$. An expression of the ratio of the speech signal to this residual distortion is obtained in the following:

Assumptions: Derivation of the residual distortion is based on the following assumptions with respect to the components of Figure 3.1.

(1) The voice BPF is delay equalized across its bandwidth [3].

(2) The absolute delays in the paths of the voice and control signal are matched to allow timely AGC and AFC.

(3) Fading is non-selective (i.e. flat fading across the spectrum of the channel).

(4) Slow AGC is used prior to filtering to remove slow shadow fading [4].

$$S_3 = S_1 \min\left(\frac{1}{S_2}, \frac{1}{\sigma_{16}}\right)$$

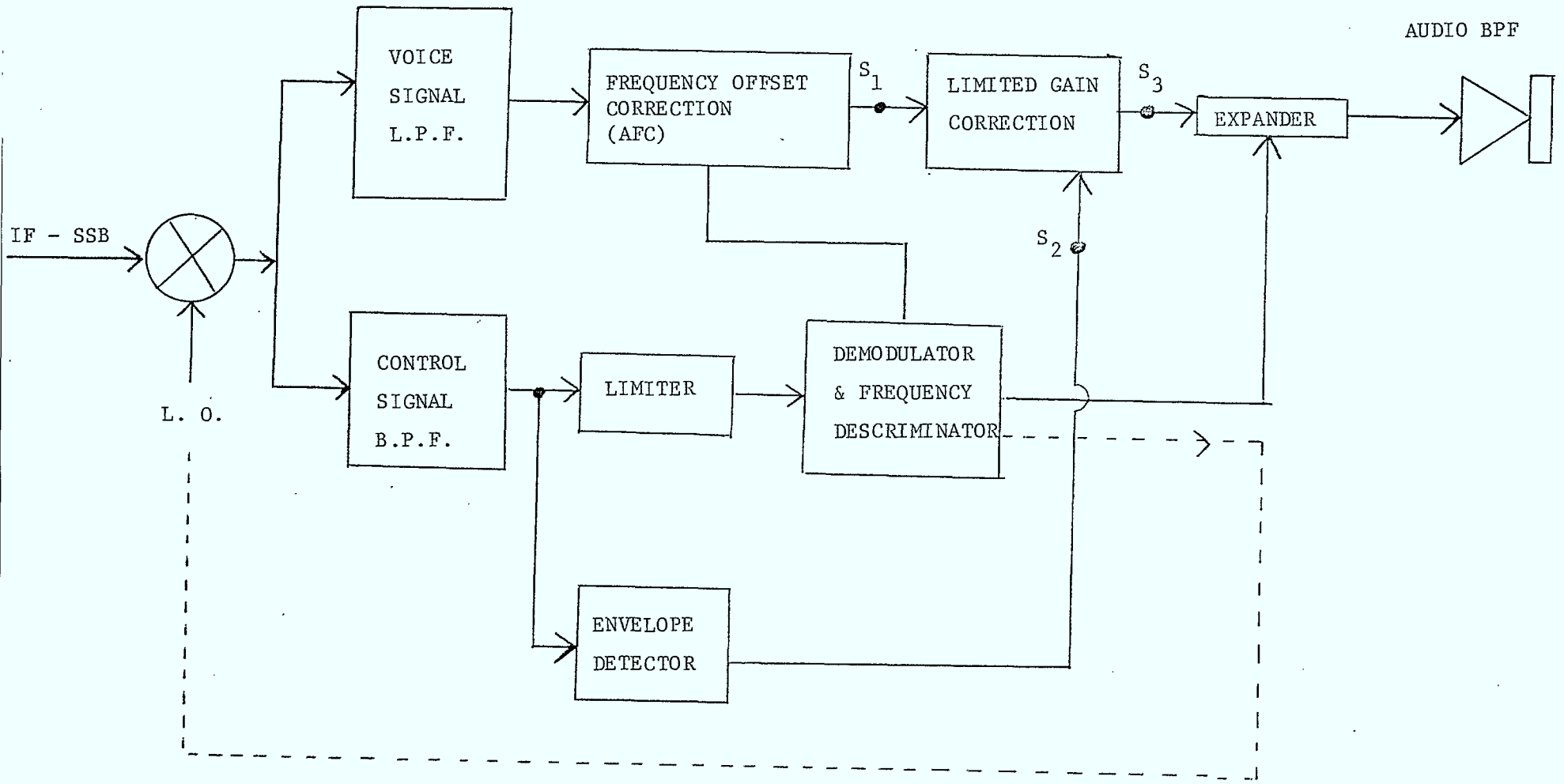


FIGURE 3.1

AGC FOR SPEECH SIGNAL USING FSK MODULATION

(5) Ergodicity is assumed for signals and channels; thus ensemble average is interchangeable with time average.

The generated base-band voice signal can be expressed as:

$$S(t) = v(t)\, e^{j\theta(t)} \qquad \text{.....(1)}$$

while the modulated data control signal is given by:

$$d(t) = e^{j\beta(t)} \qquad \text{.....(2)}$$

where is the audio envelope, $\theta(t)$ and $\beta(t)$ are the audio and control phase functions. After SSB modulation and combining, the transmitted signal will be:

$$S_t(t) = v(t)\, e^{j(\omega_c t + \theta(t))} + e^{j(\omega_c t + \beta(t))} \qquad \text{.....(3)}$$

Let $r(t)\, e^{j\phi(t)}$ be the complex fading signal caused by vehicle motion. The input to the receiver will be given by (ignoring $\phi(t)$):

$$S_r'(t) = r(t)\, v(t)\, e^{j(\omega_c t + \theta(t))} + r(t)\, e^{j(\omega_c t + \beta(t))} \qquad \text{.....(4)}$$

If we assume that the down conversion will lead to a frequency offset error $\Delta\omega_c$, the output of the voice BPF will be:

$$S_{rv}'(t) = v(t)\, r(t)\, e^{j[(\omega_c \pm \Delta\omega_c)t + \theta(t)]} \qquad \text{.....(5)}$$

and the output of the control BPF will be,

$$S_{rc}'(t) = r(t)\, e^{j[(\omega_c \pm \Delta\omega_c) + \theta(t)]} \qquad \text{.....(6)}$$

The descriminator output, $(\Delta\omega_c)$, can be used to correct the frequency offset in the speech signal. The envelope detector output will be inverted in the time domain and used to correct the

gain in the speech signal. Thus only gains as deep as will be corrected where r_o is the RMS value of r(t). Thus the corrected speech signal will be given by:

$$S_d(t) = r(t)\ \min\left(\frac{1}{r(t)}, \frac{1}{\sigma r_o}\right) v(t)\, e^{j\theta(t)} \qquad \text{.....(7)}$$

If we define the signal-to-distortion ration, R, as:

$$\mathcal{R} = \frac{\overline{S^2(t)}}{\overline{[S_d(t) - S(t)]^2}} \qquad \text{.....(8)}$$

it will be possible to calculate R using the probability distribution function of r(t), given by:

$$f(r) = \frac{2r}{r_o^2} \cdot e^{-\left(r^2/r_o^2\right)}, \qquad r(t) \geq 0 \qquad \text{.....(9)}$$

substituting from (1), (7), and (9) into (8), we obtain:

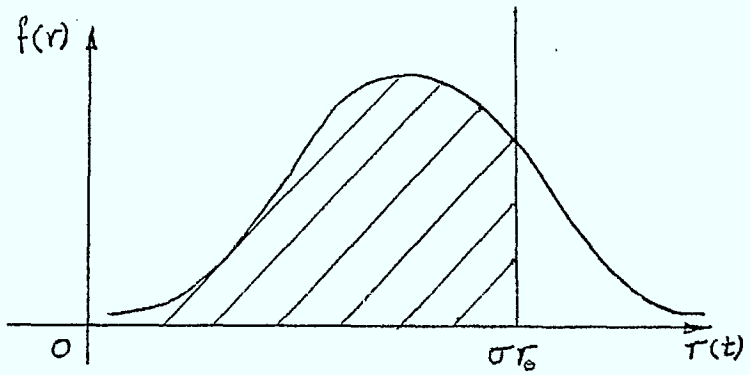
$$\mathcal{R} = \left(\bar{\beta}\right)^{-1} \qquad \text{.....(10)}$$

where:

$$\beta = \left(r(t)\ \min\left(\frac{1}{r(t)}, \frac{1}{\sigma r_o}\right) - 1\right)^2 \qquad \text{.....(11)}$$

thus $\bar{\beta}$ will be given by:

$$\bar{\beta} = \int_0^\infty \left[r(t)\ \min\left(\frac{1}{r(t)}, \frac{1}{\sigma r_o}\right) - 1\right]^2 \cdot \frac{2r}{r_o} e^{-\left(r^2/r_o^2\right)}\, dr$$



The above intergrand has a zero value for $r(t) \geq \sigma r_0$, and for $r(t) \leq \sigma r_0$ we have $\frac{1}{r(t)} \geq \frac{1}{\sigma r_0}$, thus:

$$\bar{\beta} = \int_0^{\infty} \left(\frac{r(t)}{\sigma r_0} - 1 \right)^2 \frac{2r}{r_0^2} e^{-r^2/r_0^2} dr$$

from the integration table, $\bar{\beta}$ is given by:

$$\bar{\beta} \cong \sigma^{-2} (1 - e^{-\sigma^2}) + 1$$

thus:

$$\mathcal{R} \cong \frac{1}{\sigma^{-2}(1 - e^{-\sigma^2}) + 1} \qquad \text{.....(12)}$$

Figure 3.2 gives a plot of the signal/distortion ratio as a function of the correction gain. It is clear that as the dynamic range of the hardlimiter increases, the residual distortion due to deep fades decreases. This distortion effect can be further reducted through the use of diversity techniques [3].

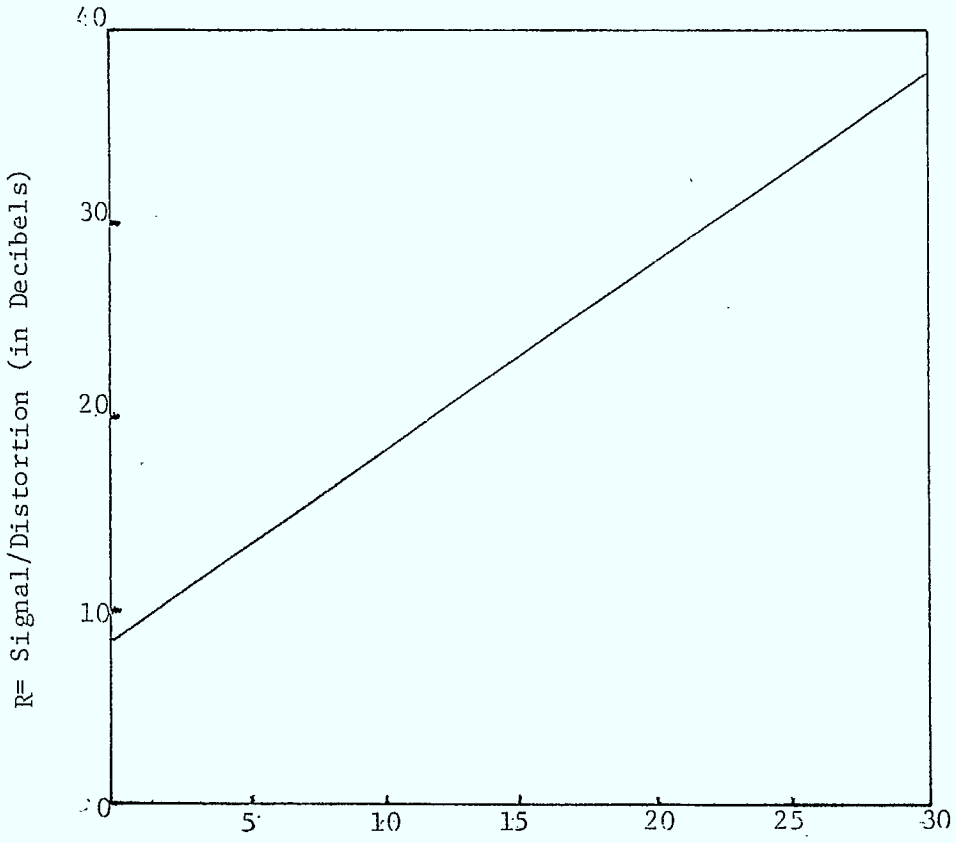


Figure 3.2

Signal/Distorion Vs. Correction Gain

3.2 BER UNDER FADING FOR NON-COHERENT FSK AND DPSK

The probability of error, P_e, for non-coherent FSK is given by ([6] and [7]):

$$P_e = 1/2 \exp \{-A^2/4No\} \quad \ldots\ldots(13)$$

(The filter bandwidth is usualy of the order of $2/T_b$.)

where:

$A^2/2$ = signal power, $No = 2\eta/T_b$ and noise power is equal to η multiplied by the filter bandwidth. T_b is equal to $1/r_b$, r_b is the bit rate.

It follows that the signal-to-noise ratio S/N will be given by:

$$S/N = A^2/4\ \eta\ r_b$$
$$= A^2/2No$$

If we define ρ = S/N, it follows that:

$$P_e = 1/2 \exp \{-\rho/2\} \quad \ldots\ldots(14)$$

The error rate due to the fading envelope can be obtained by averaging the error rate of the steady state signal over the fading envelope [5].

Since the fading is Rayleigh distributed, the probability density function of ρ is:

$$f(\rho) = \begin{cases} \frac{1}{\rho_o} e^{-\rho/\rho_o} & ; \ \rho \geq 0 \\ 0 & ; \ \text{otherwise} \end{cases} \quad \ldots\ldots(15)$$

where ρ_o is the average carrier-to-noise ratio averaged over the Rayleigh-fading,

$$P_e(\rho_0) = \int_0^\infty P_e(\rho)\, f(\rho)\, d\rho \qquad \text{.....(16)}$$

$$= \int_0^\infty \frac{1}{2} e^{-\rho/2} \frac{1}{\rho_0} e^{-\rho/\rho_0}\, d\rho$$

The above integral reduces to:

$$P_e(\rho) = \frac{1}{2+\rho} \qquad \text{.....(17)}$$

The probability of error for the DPSK modem is given by [6]:

$$P_e(\rho) = \frac{1}{2} e^{-\rho}$$

substituting in equation (16) and carrying out the integration we obtain the following expression for the probability of error in DPSK under fading conditions:

$$P_e(\rho) = \frac{1}{2(1+\rho)} \qquad \text{.....(18)}$$

The probability of error, with and without fading, for non-coherent FSK and DPSK is shown in Figures 3.3 and 3.4 respectively. The effect of fading on the BER is considerable in both cases. For example, to retain a BER of 10^{-3} when FSK is used under fading conditions, the S/N ratio has to increase from 12 (db) (under no fading) to 28 db. To do the same thing when DPSK is used, the S/N ratio has to increase from 8 db to 26 db. The plots of Figures 3.3 and 3.4 will assist in determining the minimum required S/N ratio for the control signal to maintain an acceptable BER level with respect to the speech companding algorithm.

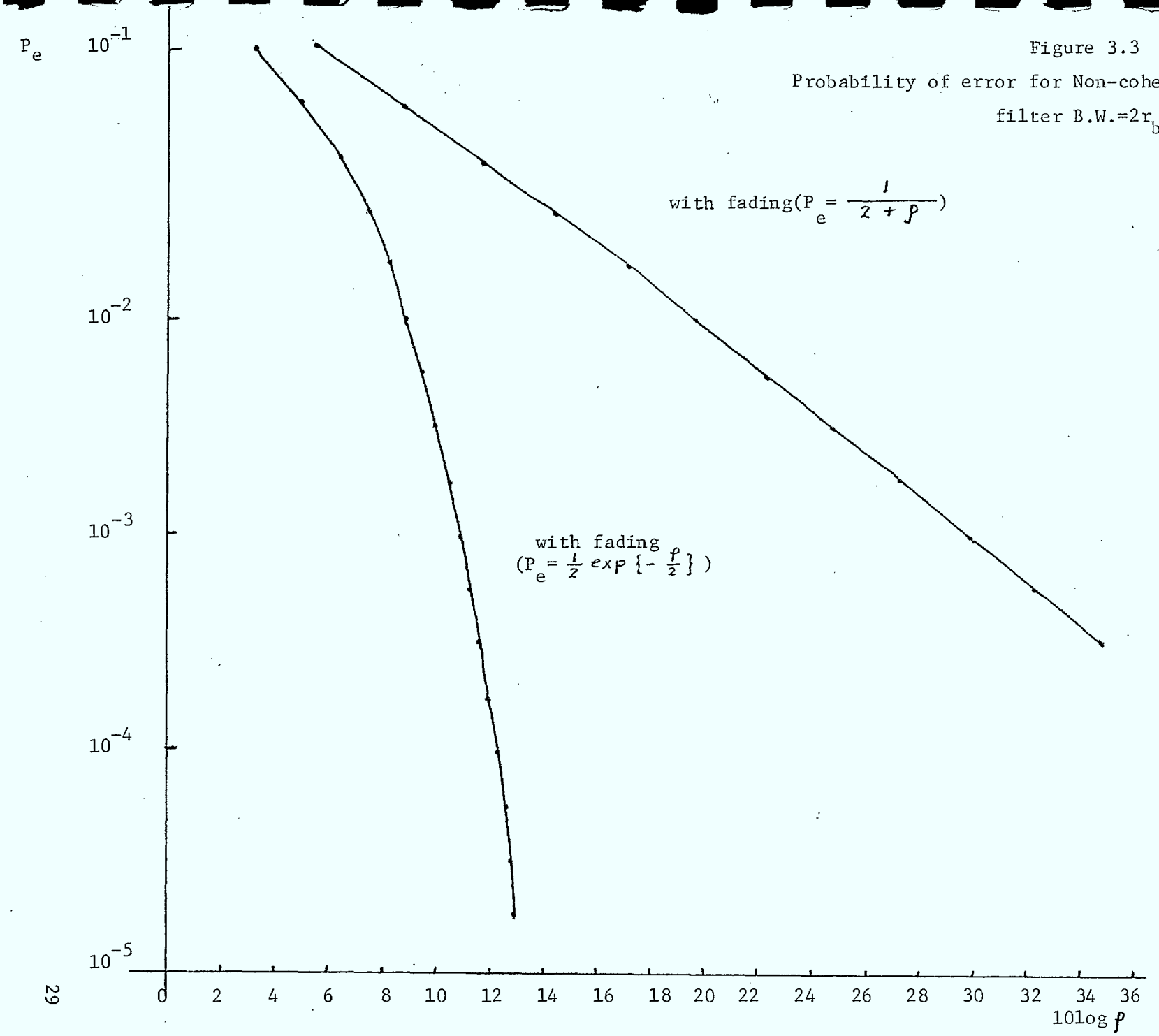


Figure 3.3

Probability of error for Non-coherent FSK with filter B.W.=$2r_b$

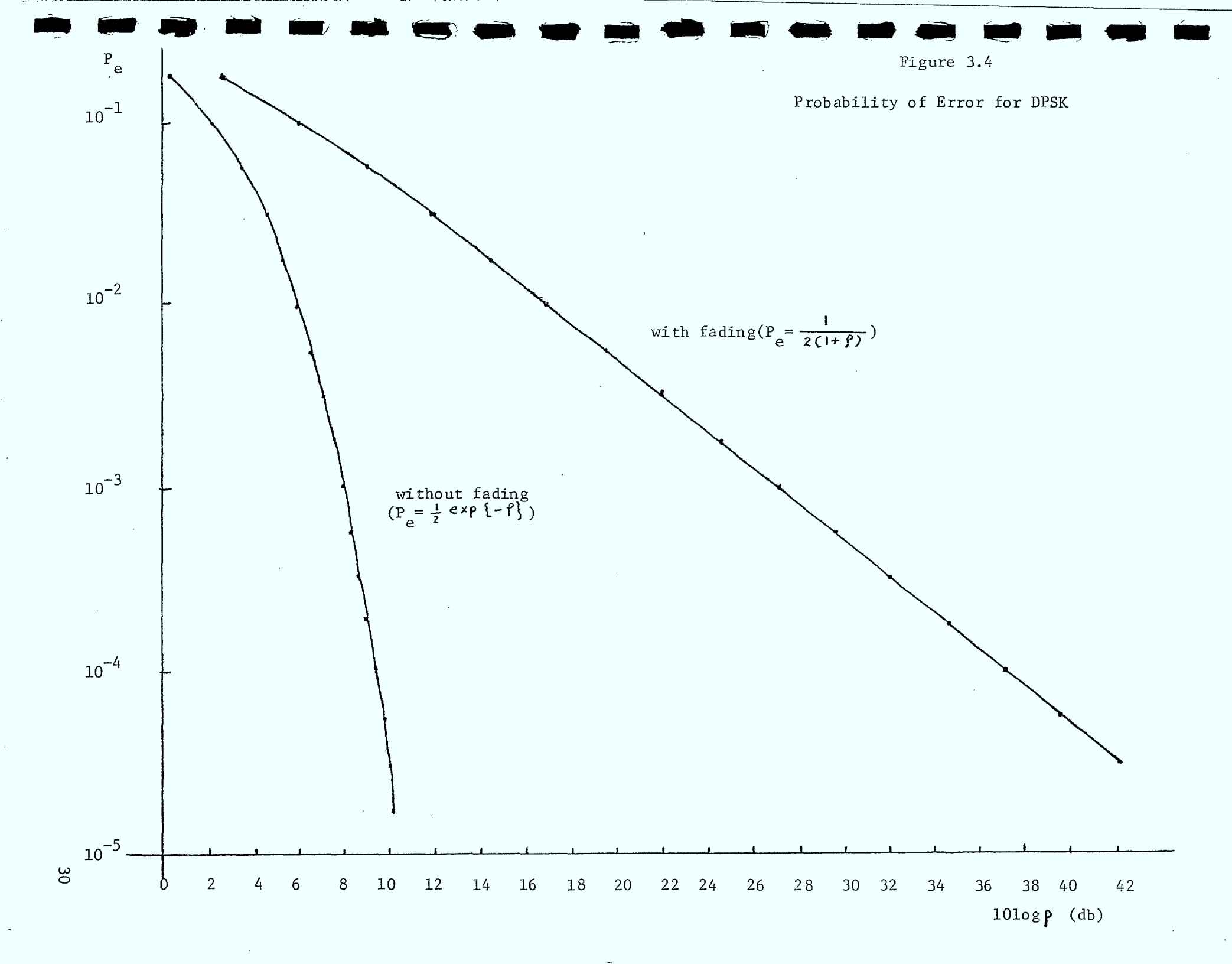


Figure 3.4
Probability of Error for DPSK
P_e
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
with fading ($P_e = \frac{1}{2(1+\rho)}$)
without fading
($P_e = \frac{1}{2} \exp\{-\rho\}$)
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42
10log ρ (db)

3.3 A PROPOSED AFC CIRCUIT

Conventional demodulation of non-coherent FSK is based on a descriminator concept in which the signal is passed through two bandpass filters ($f_c + f_d$ and $f_c - f_d$). For a data rate of 150 bps, f_d will be in the range of 75 to 100 Hz and the distance between $+f_d$ and $-f_d$ will be in the range of 150 to 200 Hz. In the VHF/UHF band the frequency offset range can be as high as 400 Hz. Clearly, it is impossible to bandpass the two components $f_c + f_d$ and $f_c - f_d$ separately without compensating for the frequency offset. The frequency offset can be detected at the beginning of the call session between the two end tranceivers. Communications can proceed once the receiver has locked onto the incoming carrier. It is also essential to continuously monitor all frequency shifts (due to doppler effects) and compensate the speech signal accordingly.

It is thus essential to include an Automatic Frequency Correction Circuit in the receiver. In this section, an AFC circuit is proposed which does not require signal normalization.

The circuit has been proposed and analysed in [8], and has been shown to be superior to the ideal detector below zero to 10 dB input S/N. In this section we review the basic concept underlying this detector and examine its applicability to the SSB system under study.

Figure 3.5 shows the basic configuration of the proposed AFC circuit. The IF signal (voice + control signal) is hardlimited first to remove the fluctuations in amplitude caused by fading. The hardlimited signal is multiplied by a local carrier to generate the I and Q components. The I and Q components are bandpass

filtered to remove the high frequency components. Thus the output of the bandpass filters will be given by:

$$S_a = \cos [K d(t) \pm \Delta\omega_c t]$$

and:

$$S_b = \sin [K d(t) \pm \Delta\omega t]$$

where S_a is the signal at point a and S_b is the signal at point b in Figure 3.5. The term kd(t) represents the information carried by the FSK signal plus the phase shift due to fading.

The derivative of S_a is then multiplied by S_b and the derivative of S_b is multiplied by S_a. The outputs of the two multipliers are added:

$$X(t) = \dot{S}_b S_a + \dot{S}_a S_b = (K d'(t) \pm \Delta\omega_c)[\cos^2(\ ) + \sin^2(\ )]$$

$$= K d'(t) \pm \Delta\omega_c$$

In binary non-coherent FSK, d(t) will be given by:

$$d(t) = \pm \omega_d t + \phi(t)$$

where $\phi(t)$ is the phase shift due to fading. Thus:

$$d'(t) = \pm \omega_d + \phi'(t)$$

which suggests the possibility of obtaining the frequency offset from X(t) by passing X(t) through a lowpass filter and extracting the D.C. component.

The above circuit lends itself readily to digital implementation since all components following the two IF mixers can be easily implemented using the digital signal processor.

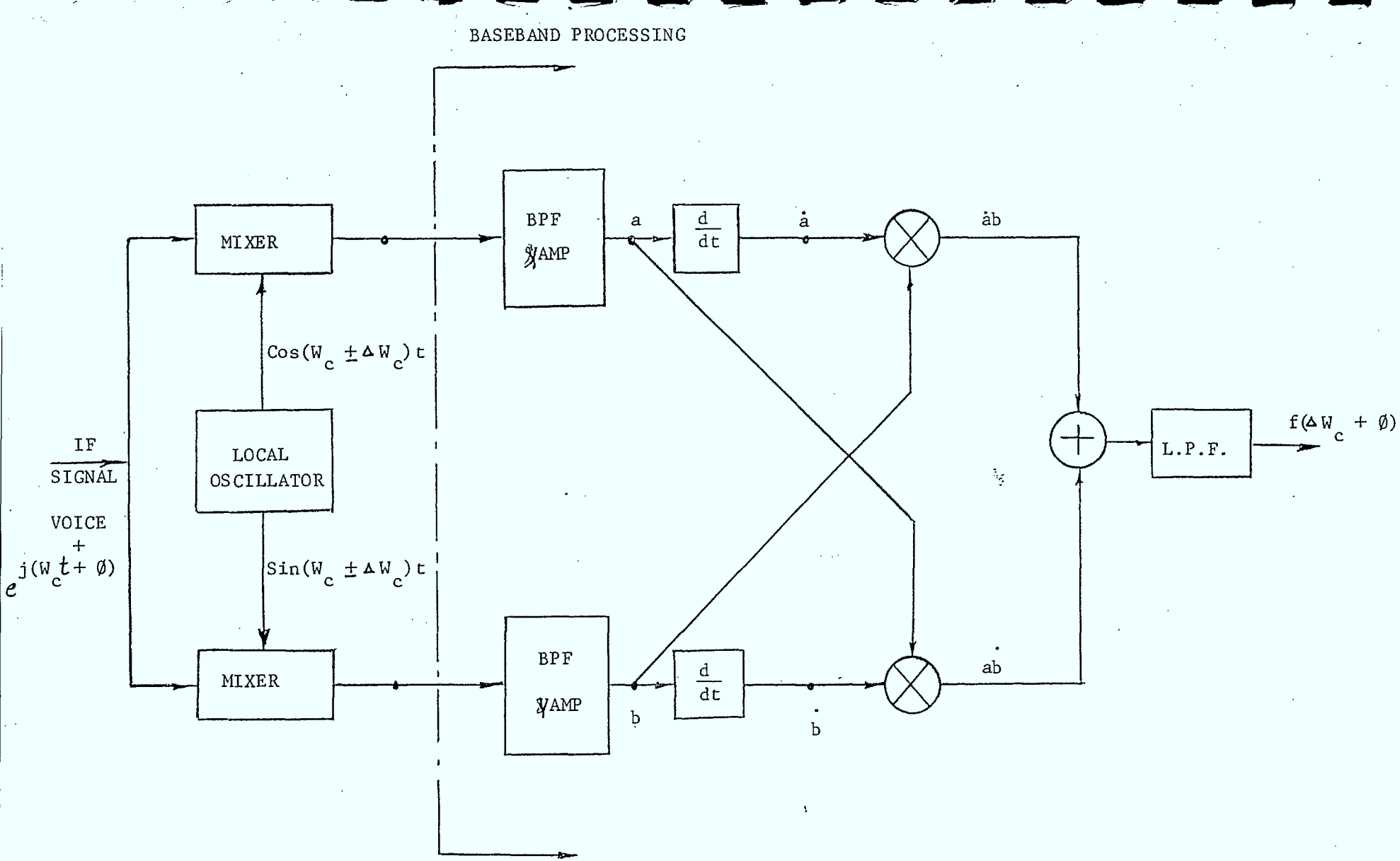


FIGURE 3.5

PROPOSED AFC CIRCUIT

4.0 INTERMODULATION EFFECTS

4.1 INTRODUCTION

The evaluation of IM in-band distortion of the ACSSB channel is considered in this Section. The focus is on evaluating the intermodulation distortion when the signal goes through a non-linear amplifier. We consider the forms of spectrum allocation and compare the in-band intermodulation distortion caused by each. These two forms of spectrum allocation within the SSB channel are:

1. The Control Signal (FSK modulated binary signal) is placed out-of-band with respect to the voice signal (Figure 4.1).

2. The Control Signal (FSK modulated binary signal) is placed in-band by splitting the voice signal and shifting the upper half of the spectrum to higher frequencies (Figure 4.2). This scheme is described in reference [1].

For each of the above two schemes, we obtain results for the 3rd and 5th order IM components and their magnitudes as a function of the frequency (around the RF reference) and in relation to the fundamental harmonic component (i.e. the desired signal).

Section 4.2 provides some background on intermodulation definitions, notations and computational procedures. Section 4.3 presents computational results for each of the two spectrum allocation schemes mentioned above.

4.2 MODELLING OF IM DISTORTION

The analysis in this Section follows closely the analysis used in reference [13] which considered IM distortion in a single SSB channel with speech signal and out-of-band pilot tone.

We consider the general case where the input signal, $e_i(t)$, (speech plus modulated control signal) to the non-linear amplifier

is a sum of m narrowband bandpass signals:

$$e_i(t) = \mathcal{R}e\left\{ p(t)\ e^{j\omega_o t + j\theta(t)} \right\} \quad \ldots\ldots(4.1)$$

The non-linear amplifier is represented by the single-tone response characteristic:

$$g(A)\ e^{jf(A)} \quad \ldots\ldots(4.2)$$

which means the output of the amplifier, $y_i(t)$, when the input is a sinusoidal signal, $x_i(t)$, will be given by:

$$y_i(t) = \mathcal{R}e\left\{ g(A)\ e^{j\omega_o t + jf(A)} \right\} \quad \ldots\ldots(4.3)$$

where:

$$x_i(t) = \mathcal{R}e\left\{ A\ e^{j\omega_o t} \right\}$$

We assume that the amplifier characteristics is frequency independent, i.e. its frequency response is flat over the range of interest. This assumption is valid since the bandwidth of the channel (less than 10 kHz) is much smaller than the RF frequency (150 MHz and up).

Thus for the multi-tone input given by equation (4.1), the output will be:

$$e_o(t) = \mathcal{R}e\left\{ g(p[t])\ e^{j(\omega_o t + f[p(t)] + \theta(t))} \right\} \quad \ldots\ldots(4.4)$$

In [12], equation 4.4 hs been shown to be equivalent to:

$$e_o(t) = \mathcal{R}e\left\{ [\ e^{j\omega_o t}\ ] \cdot \sum_{K_1+K_2+\cdots K_m=1}^{\infty} e^{j\sum_{i=1}^{m} K_i\theta_i(t)} \cdot M(K_1, K_2, \ldots K_m) \right\} \quad \ldots\ldots(4.4)$$

where $M(K_1, \ldots K_m)$ is the complex amplitude of the IM product;

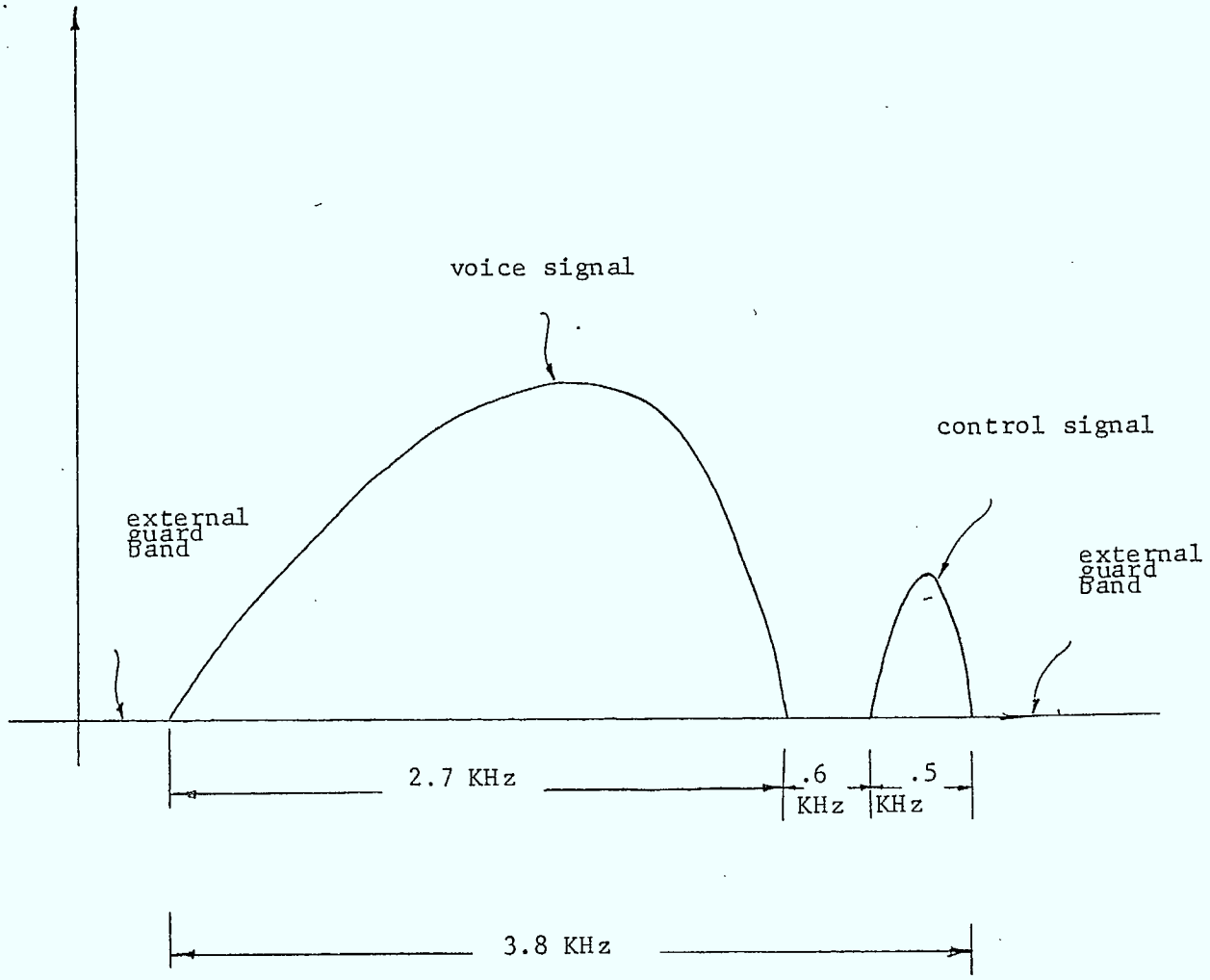


Figure 4.1
Spectrum Allocation With Out-Of-Band
Control Signal

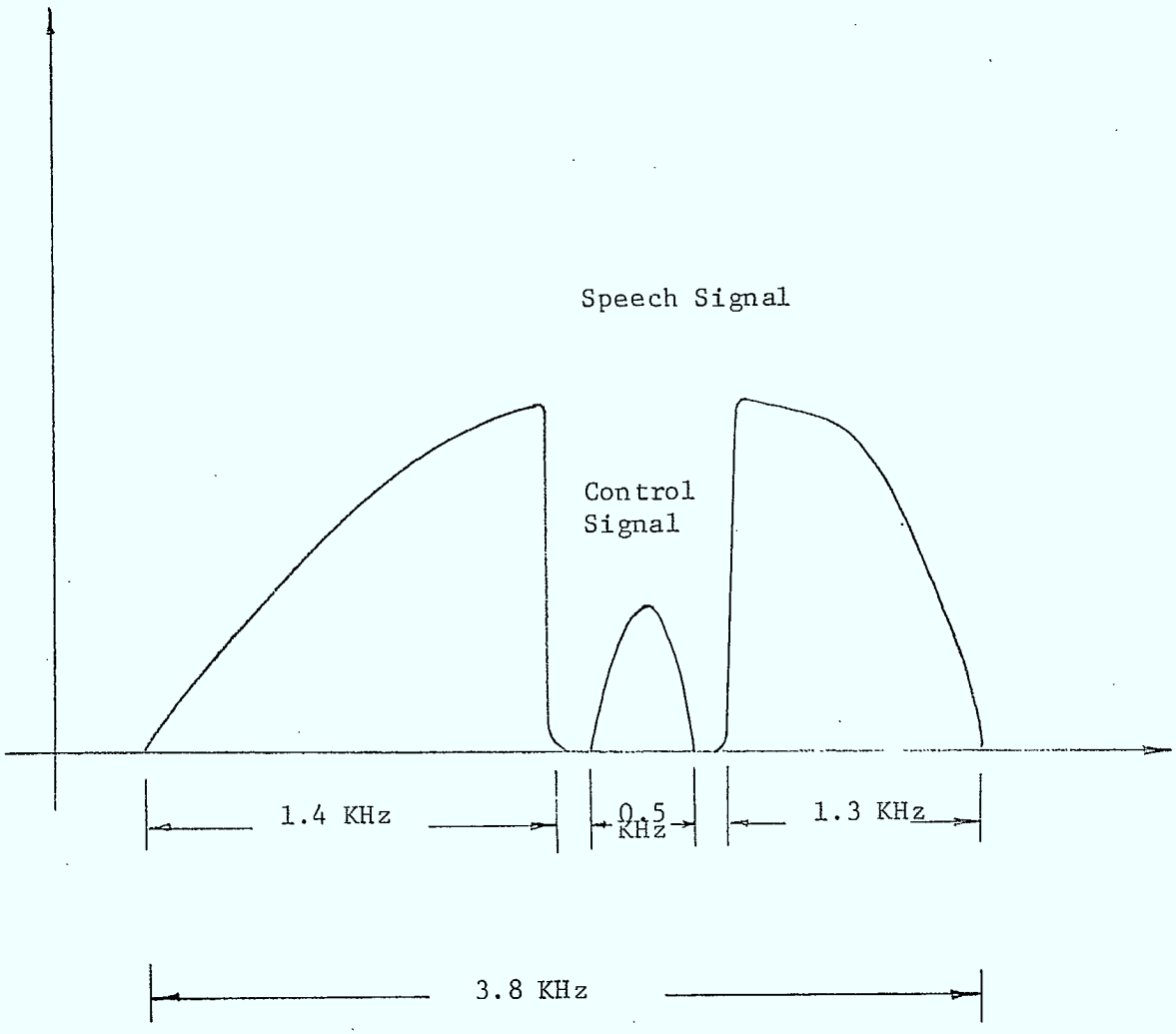


Figure 4 .2

Spectrum Allocation With in-band Control Signal

K_i is an integer.

The output signal given by equation (4.5) is composed of a number of pure tones, each tone frequency characterized by the vector $\bar{K} = (K_1, K_2, \ldots, K_m)$. Thus $\omega_t = K_1\omega_1 + K_2\omega_2 + \cdots\cdots K_m\omega_m$.

Equation 4.5 indicates that there are m "fundamental" output tones (the same frequencies as the incoming tones), defined by the vectors $\bar{K}_j$:

$$\bar{K}_j = (K_1, K_2, \cdots\cdots K_m), \quad \text{where} \quad K_i = \begin{cases} 1 & \text{if } i=j \\ 0 & \text{if } i \neq j \end{cases}$$

for $j = 1, 2, \ldots\ldots, m$.

All the other possible combinations allowed give rise to the intermodulation products. However, we consider only those products described by the vectors satisfying the condition:

$$\sum_{i=1}^{m} K_i = 1 \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.6)$$

The IM products allowed by equation (4.5) are classified according to the sum of the absolute values of the components of the vector K. Thus,

$$\text{order of IM product} = \sum_{i=1}^{m} |K_i|$$

As an example, products of the type (1,1,-1,0 . . .,0) or (2,-1,0, . . .0) are called 3rd order and they represent IM distortion components falling on the frequencies given by:

$$\omega = \omega_c + \omega_1 + \omega_2 - \omega_3 ,$$

and $$\omega = \omega_c + 2\omega_1 - \omega_2$$

The overall computational model of the problem and the evaluations to be made for a single channel IM distortion can be summarized as follows:

(i) The Amplifier

The amplifier is modelled by the following equation:

$$g(p)\, e^{jf(p)} = \sum_{s=1}^{L} b_s J_1(\alpha s p) \quad \text{.....(4.7)}$$

α is constant [0 or 1]; b_s are complex co-efficients

(ii) The Input Signal

Consists of N equally spaced, equal amplitude tones at a specified input power level representing speech, and M equally spaced tones representing the control signal. The control signal tones are 13 dB below the voice tones. Two configurations are considered: out-of-band control signal (Figure 4.3) and in-band control signal (Figure 4.4). The flat spectrum assumption represents some kind of a "worst case" situation in terms of IM generation ([10], [11], [12], [13]).

(iii) COMPUTER OUTPUT IM DISTORTION

Each fundamental and IM product is evaluated via the following equation [13]:

$$M(K_1, K_2, \ldots K_m) = \sum_{s=1}^{L} b_s \prod_{i=1}^{m} J_{K_i}(\alpha s A_i(t)) \ldots \quad (4.8)$$

The proof of the above equation is given in [12].

Where:

L: number of co-efficients in the expansion
M: number of input signals
b_s: complex co-efficients
J_n: Bessel functions of the first type

$A_i(t)$: amplitude of its signal

By sorting all the IM products of interest, we obtain a spectral description of the output signal (N tones + M tones + a number of IM components).

4.3 COMPUTATIONAL RESULTS

Figure 4.5 shows the power spectral density of the output signal when 12 tones are input to the system together with 3 in-band control tones. The plot shows the position of the adjacent channels. The spectrum of the SSB channel falls in the range of 9.0 to 11 kHz above the carrier frequency (the frequency of the suppressed carrier). The following channel parameters are used:

channel bandwidth = 3.8 kHz

frequency separation = 6.3 kHz

guard band (GB) = 0.66 kHz

The IM power for the third and fifth order IM are shown in relation to the (desired) fundamental component.

Figure 4.6 shows the power spectral density for the fundamental, 3rd and 5th order IM when the control signal tones are placed in-band. In comparison with the out-of-band signal case (Figure 4.5), it is clear that both the in-band and adjacent channel IM distortion is higher for the in-band control signal. To illustrate this difference, the IM distortion due to the 3rd and 5th order components are combined and plotted for both cases in Figure 4.7. The in-band control signal case introduces IM distortion, both in-band and in adjacent channel, which is approximately 20 db higher than the case with the control signal placed out-of-band.

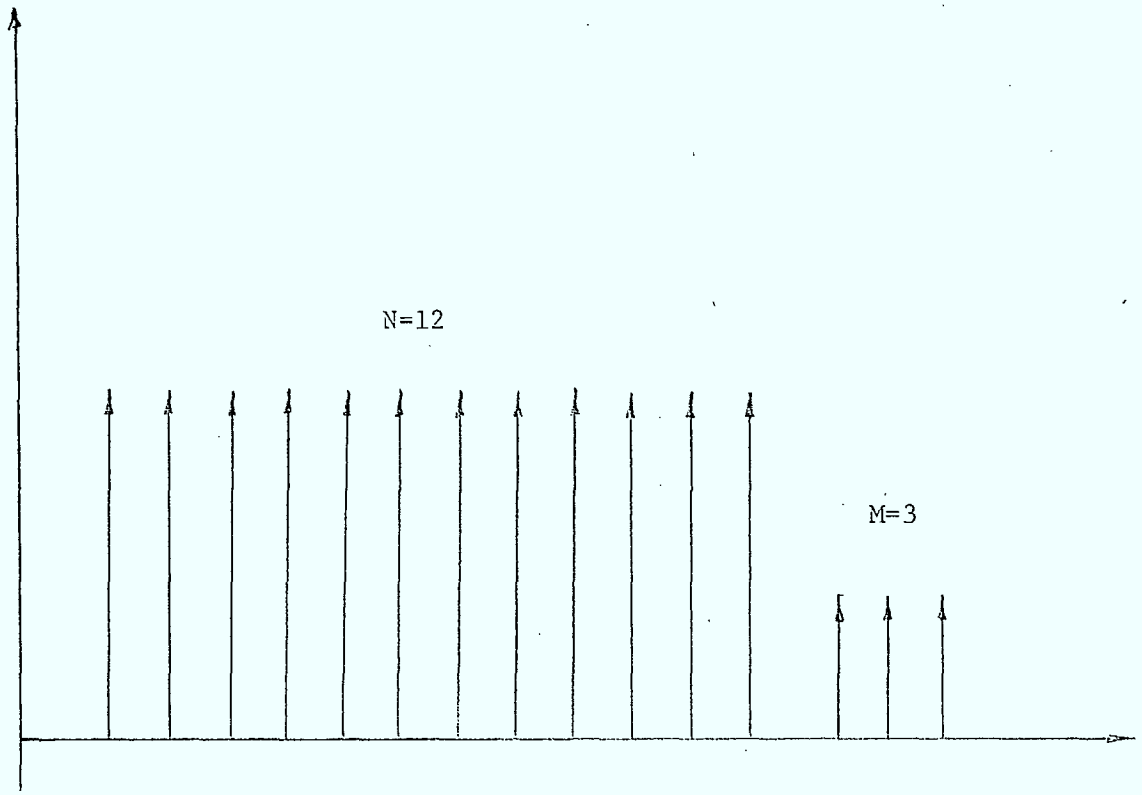


Figure 4.3

Input Signal to Amplifier
(Out-of-band Control Signal)

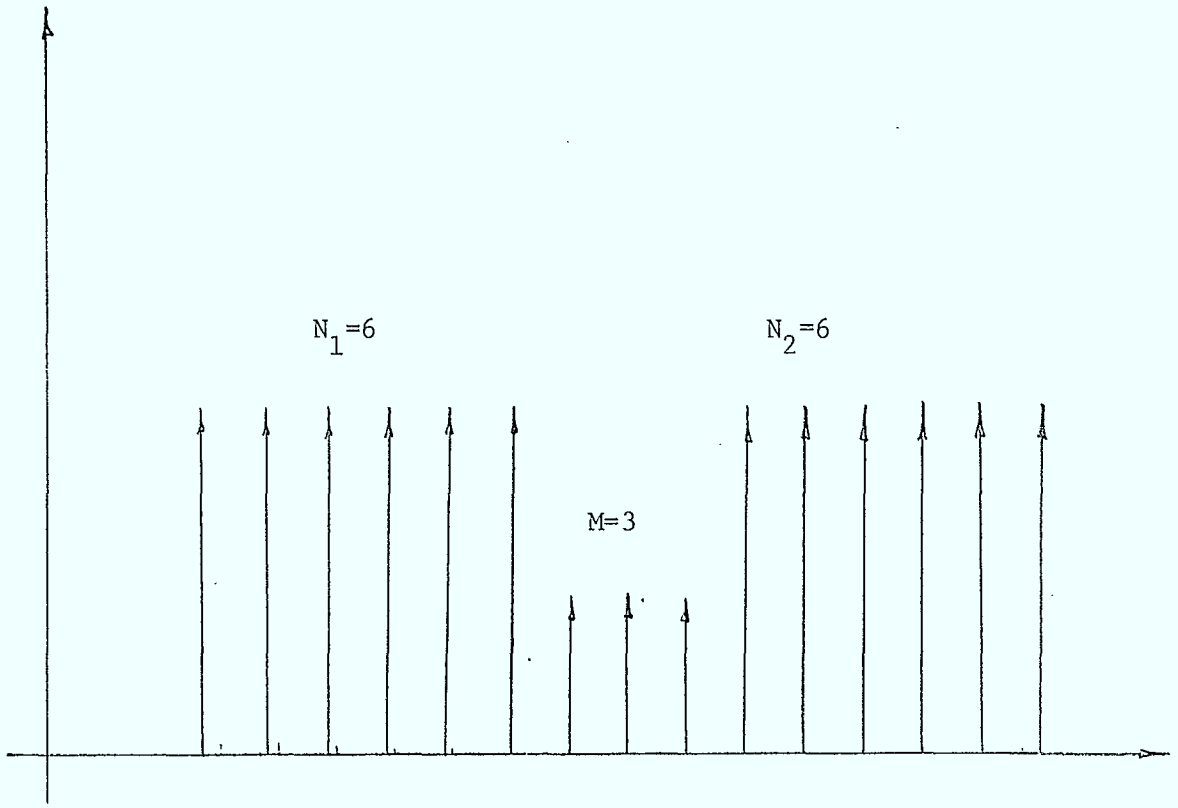


Figure 4.4

Input Signal to Amplifier
(Out-of-band Control Signal)

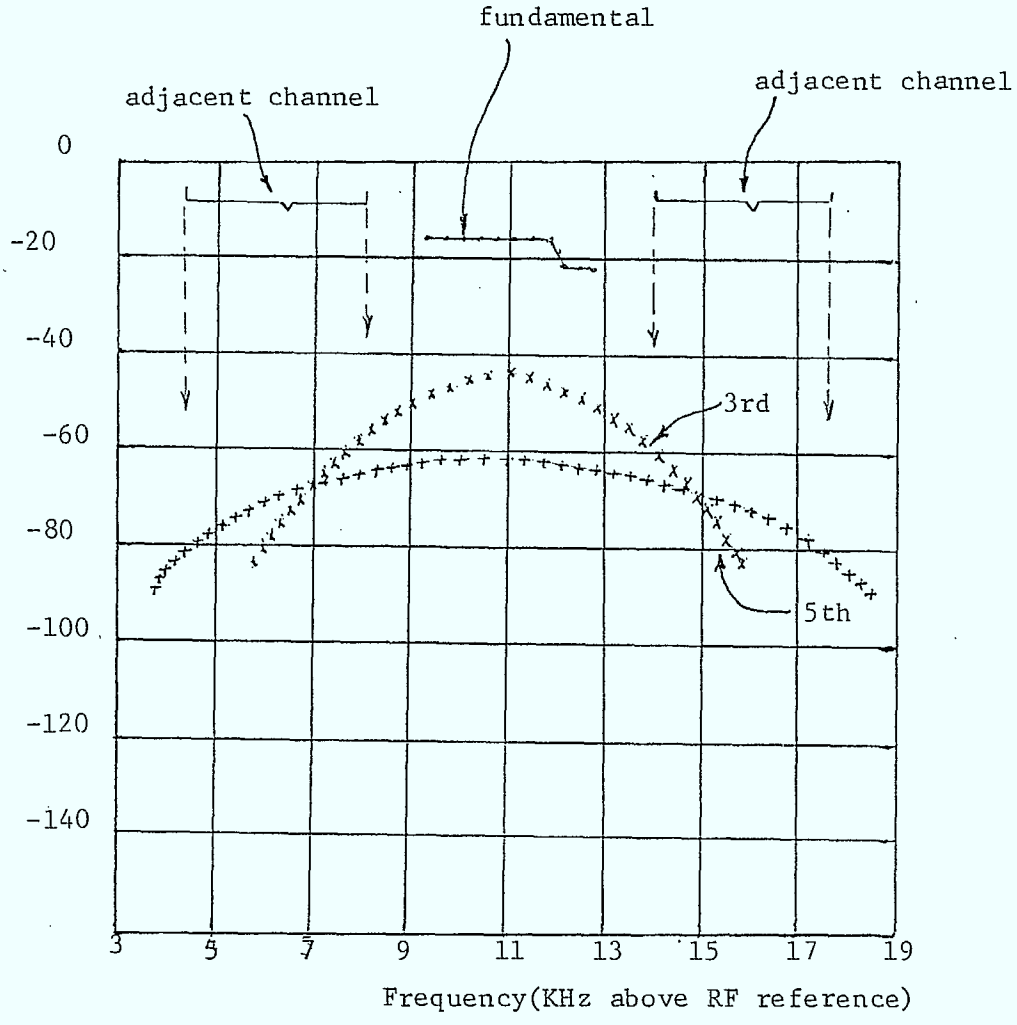


Figure 4.5

(3rd and 5th Order IM Components of Output Spectrum)

N=12

M=3

(out-of-band Control Signal)

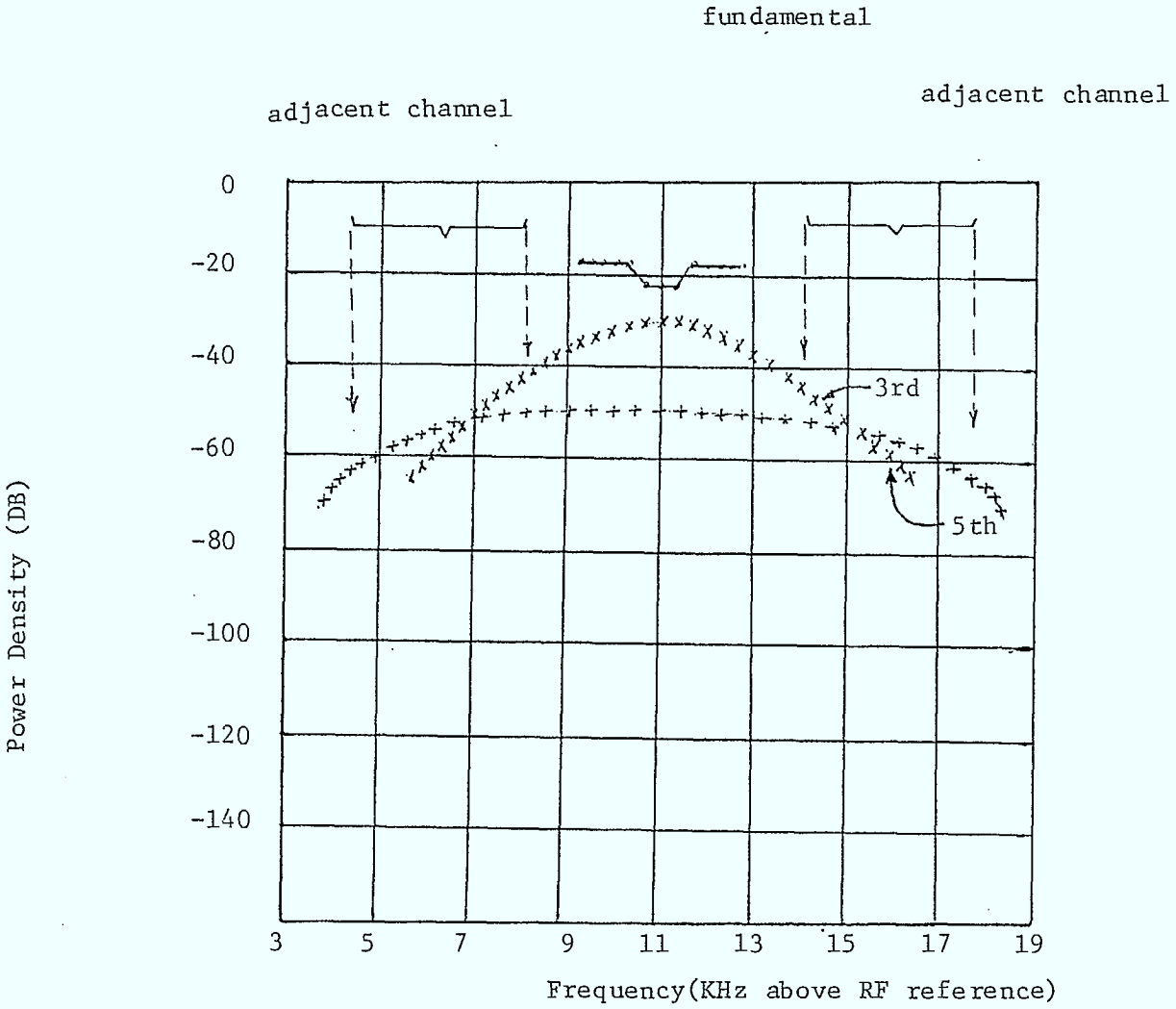


Figure 4.6

(3rd and 5th Order IM Components of Output Spectrum)
N=12
M=3
(In-band Control Signal)

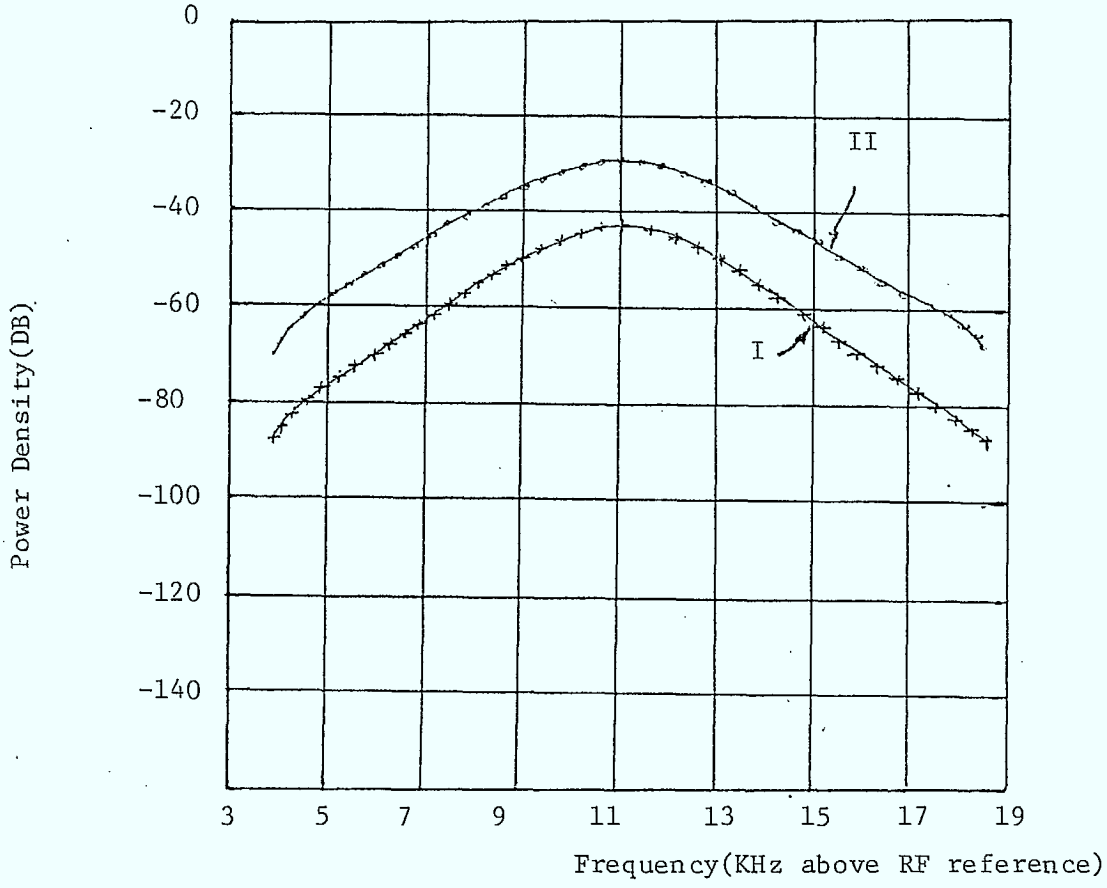


Figure 4.7

Combined 3rd and 5th order IM Components

(I----Control Signal out-of-band)
(II---Control Signal in-band)

5.0 IMPLEMENTATION CONSIDERATIONS

In this section, we evaluate the feasibility of implementing the ACSSB baseband section of both transmitter and receiver using digital signal processors.

After discussing the advantages of basing the implementation on digital processor components in Section 5.1, we evaluate two signal microprocessors (Nippon 7720 and TM5 320) for the purpose of selecting the one deemed most suitable for the current application (Section 5.2).

Section 5.3 examines the signal flow in the transmitter and the receiver and identifies the processing functions applied to the signal during its flow.

Section 5.4 proposes three different hardware architectures which use different combinations of analog and digital circuitry to implement the transmitter and the receiver functions.

Section 5.5 examines processor and data transfer timing considerations in relation to the sampling rate and the total processing requirements associated with each set of speech samples.

5.1 ADVANTAGES OF DIGITAL IMPLEMENTATION

The recent advances being made in the field of digital component technology are having profound effects on all aspects of digital systems design.

Modern component technology has recently opened a floodgate of high performance components that have dramatically altered the cost/performance criteria for all digital systems. The new generation of high performance microprocessors and microcomputers such as the TMS 320 family has made digital signal processing an

affordable alternative to analog design for processing voice signals.

Digital signal processing offers several advantages over analog signal processing:

1. Flexibility

   The programmability of D.S.P. systems permits a vastly greater flexibility for modifications, imporvements and adding of new features. Due to this flexibility, new approaches could be investigated and tested easily and rapidly. Different algorithms could be compared and evaluated without major hardware re-design.

2. Stability

   In D.S.P. there is no performance degradation over time and temperature; so there is no drift in filter characteristics or other signal processing parameters.

3. Self Diagnostic

   Microcomputers can perform extensive self diagnostic tests with little additional cost compared to analog circuits.

4. Predictability

   In analog design, discrete component tolerances prohibit exact matching of multi-pole filters. This restriction is eliminated because digital realizations are not subjected to such tolerences.

5. Repeatability

   In analog design the production-lot variations affect the circuit performance while in digital design the performance is identical from one device to another.

6. Reliability

   Digital systems require less manual tuning, less maintenance of equipment and are more stable and predictable.

7. Future Cost

   Digital Systems are in general very simple. They eliminate the need of costly precision components; they also eliminate the production re-tuning so often required in analog systems integration. The rapid and continuous decrease in the cost of VLSI chips will make the digital alternative more economical in the near future.
   In D.S.P. systems the same hardware provides a wider range of

options at reduced cost, size, weight and maintenance.

5.2 THE SIGNAL PROCESSOR

5.2.1 Candidate Selection

Recently a new generation of high performance microprocessors and microcomputers, aimed at D.S.P. applications, has been announced. This new generation includes the Intel 2920, the N.E.C. 7720, the Texas Instruments TMS 320 and the Hitachi (which is not available yet).

The Intel 2920 appeared first. It has on-board program memory, scratchpad memory, D/A circuitry, A/D circuitry, digital processor and I/O circuitry; therefore it is called analog signal processor. Its EPROM section contains 192 words of 24 bits each; its RAM section contains 40 words of 25 bits for the storage array and 16 words of 25 bits for the constant array. The Intel 2920 has a no-branch instruction set. Its speed is relatively slow compared to the other candidates due to the lack of hardwired arrary multiplier.

The NEC 7720 has a program ROM of 512 X 23 bits, a data/coefficient ROM of 510 X 13 bits and a data RAM of 128 X 16 bits. It has an instruction execution cycle of 250 n sec. The chip includes a 16 X 16 bits parallel multiplier with a 32-bit result. It also has a serial input/output port.

The Texas Instruments TMS320 has a program ROM of 1536 X 16 bits, expandable to 4096 X 16 bits by an external memory, a data RAM of 144 X 16 bits. It has an instruction execution cycle of 200 ns. The chip includes a 16 X 16 bits parallel multiplier with a 32-bit result, a 0-15-bit barrel shifter. It has a very simple and

effective architecture which makes it the best available candidate.

Table 5.1 shows the performance benchmarks for both the NEC 7720 and the Texas Instruments TMS 320. It is clear from this comparison that although the TMS 320 has an instruction execution cycle 1.25 times faster than the NEC 7720, the TMS 320 performs an F.F.T. more than 2.75 times faster than the NEC 7720. This shows that the matching between the hardware architecture of the system and the algorithms that have to be executed is not a simple matter since the instruction execution cycle is only one factor in assessing the speed of the processor when executing relatively sophisticated algorithms (e.g. Hilbert Transfor, F.F.T.) The superiority of the TMS 320 processor in terms of its data RAM and its ROM space expandability and processing speed makes it a more suitable processor for implementing the ACSSB System than the Nippon 7720 (see next section). A summary of the comparitive features of four chips. (TMS 320, NEC 7720, AMI S2B11 AND INTEL 2920) is provided in Table 5.2 [14].

	NEC 7720	TI TMS 320
SECOND ORDER DIGITAL FILTER (BIQUAD)	2.25 micro-sec	2.0 micro-sec
SINE/COS OF ANGLES	5.25 micro-sec	4.8 micro-sec
b/A LAW TO LINEAR CONVERSION	0.5 micro-sec	0.8 micro-sec
FFT 32-POINT COMPLEX	0.7 micro-sec	0.254 micro-sec
FFT 64-POINT COMPLEX	1.6 micro-sec	0.580 micro-sec

TABLE 5.1

D.S.P. PERFORMANCE BENCHMARKS

COMPETITIVE SUMMARY

FEATURE	TI TMS32010	NEC μPD7720	AMI S2811	INTEL 2920
DATA-WORD SIZE (BITS)	16	16	16	25
COEFFICIENT SIZE (BITS)	16	13	16	(1)
ACCUMULATOR WIDTH (BITS)	32	16	16	28
SATURATION ARITHMETIC	HARDWARE	SOFTWARE	HARDWARE	HARDWARE
BOOLEAN LOGIC OPERATION?	YES	YES	NO	YES
MULTIPLIER IMPLEMENTATION	HARDWARE	HARDWARE	HARDWARE	SOFTWARE
MULTIPLIER PRECISION (IN × IN = OUT)	16 × 16 = 32	16 × 16 = 32	12 × 12 = 16	12 × 25 = 28
MULTIPLICATION TIME (NS) (WORST CASE)	200	250	300	4800
PARALLEL I/O (BITS)	16	8	8	4 IN/8 OUT
INSTRUCTION WORD (BITS)	16	23	17	24
INSTRUCTION CYCLE (NS)	200	250	300	400
SUBROUTINE LEVELS	50	4	1	NONE
INTERATION (LOOP) COUNTER?	YES	NO	YES	NO
CONDITIONAL JUMPS?	YES	YES	YES	NO
FULL-SPEED EXTERNAL MEMORY EXPANSION	YES	NO	NO	NO
INSTRUCTION ROM (BITS)	1536 × 16	512 × 23	256 × 17	192 × 24
COEFFICIENT ROM (BITS)		512 × 13	120 × 16	N/A
DATA RAM (BITS)	144 × 16	128 × 16	128 × 16	40 × 25
Z^{-1} FUNCTION?	YES	YES	YES	NO
LOOK-UP TABLES?	YES	YES	YES	NO
INTERRUPTS – HARDWARE	YES	YES	NO	NO
– SOFTWARE	YES	NO	NO	NO

TABLE 5.2

5.2.2 The TI TMS 320

a) Architecture

The TMS 320 architecture is a single accumulator Harvard type architecture modified to allow crossovers between the separate program and data memories. Figure 5.1 shows a block diagram of its internal architecture.

High performance is achieved by the 32-bit ALU, the 16 X 16-bit parallel multiplier, the 0-15-bit barrel shifter and the 32-bit accumulator. the TMS 320 has eight input/output ports and a single-level interrupt.

Two modes of operation are available on the TMS 320: a microcomputer mode which can expand its 1.5k X 16-bit words of on-chip ROM to 4k total words; and a microprocessor mode where all 4k words of program memory are external. The TMS 320 has an on-chip data RAM of 144 X 16-bit words.

The chip also includes a 12-bit program counter, 4 X 12-bit stack registers, 2 X 16 bit auxiliary registers during multiply operations. It includes also two single-bit register, the auxiliary register pointer, containing the address of the current auxiliary register, and the data memory page register containing the page of data RAM.

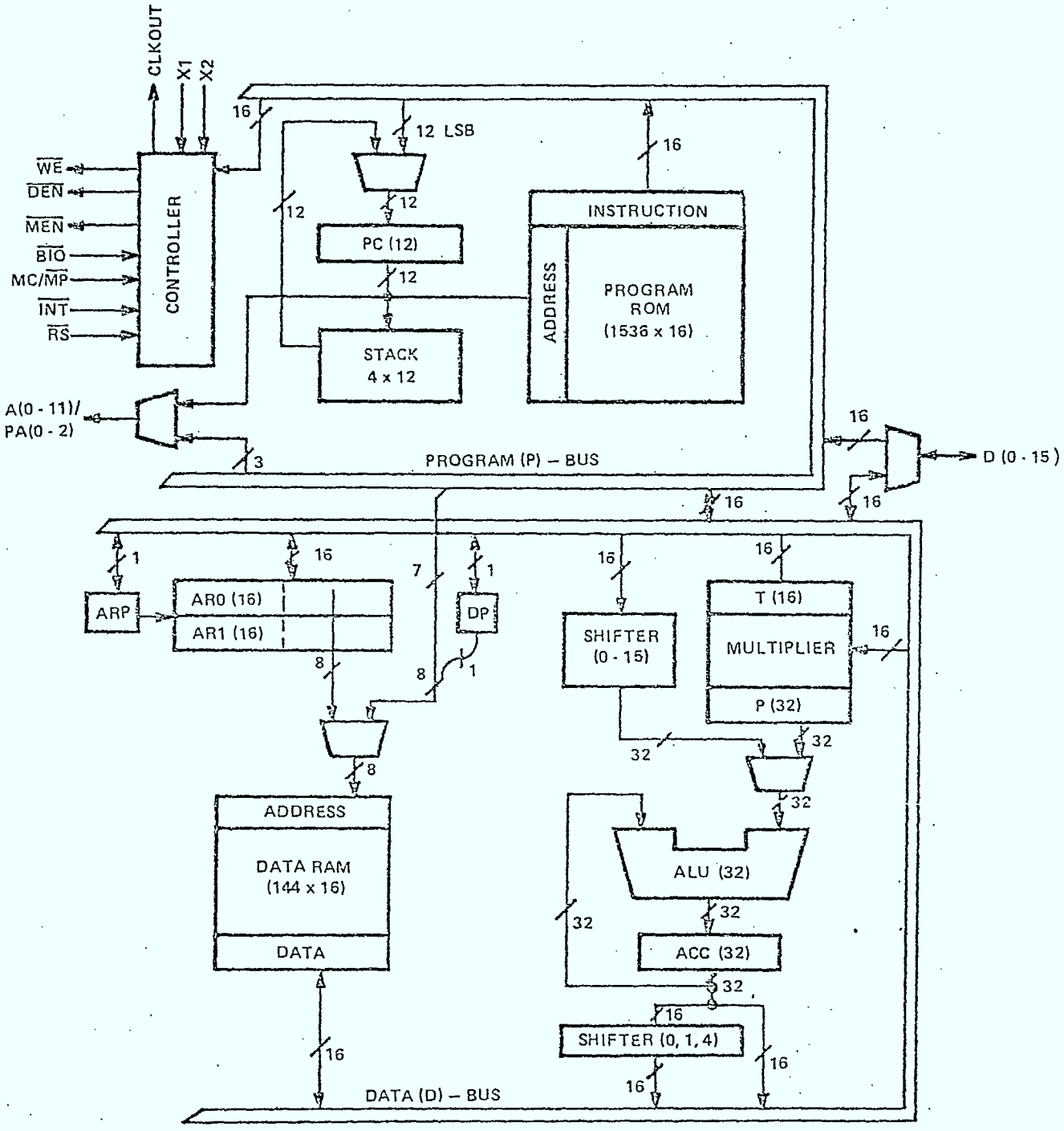


FIGURE 5.1
Basic TMS-320 Architecture

b) Data RAM Expansion

The data RAM could be extended in two different ways. Data can reside within the program space so that a system designer can make trade-offs between the amount of table and program space needed for a specific application. This is done by the table read (TBLR A) and the table write (TBLW A) instructions. These are three-cycle instructions. TBLR uses the twelve LOW order bits of the accumulator as an address for a word in program memory and transfers that word to a Location in data memory specified by a field of the instruction word. The reverse operation is done by using the TBLW instruction; a word in data memory is transfered to the program memory.

The main disadvantage of using this method is the transfer speed. In order to load the accumulator by a data residing in the data RAM only one cycle is needed (200 ns); nevertheless, if the data resides in the program space, a "table read" instruction is needed to transfer the data to the data RAM, then a "load accumulator" instruction is needed to transfer the data to the accumulator, which takes a total of four cycles (800 ns). The accumulator has to be previously loaded by the source address which makes the total transfer time 1 micro-second.

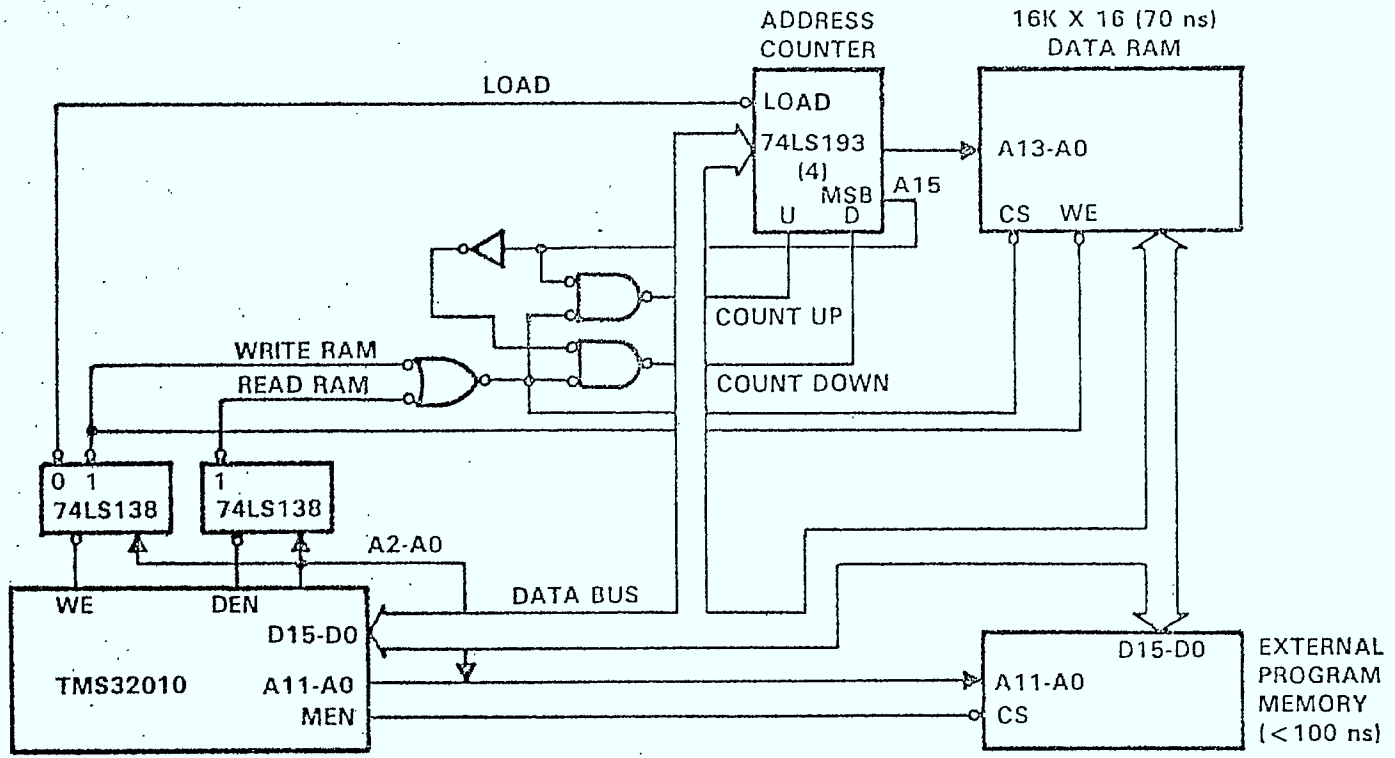
The other alternative for extending the data RAM is building a special hardware interface. The external data memory is addressed as one input/output peripheral. This configuration is used for sequentially accessing large data store.

The external data memory is viewed by the processor as a very large stack; the stack is fully controlled by the hardware

interface. The circuit diagram of a possible interface circuit is shown in Figure 5.2.

The main advantage of this configuration is that the size of the added external memory could be expanded without limit. In order to transfer data from the external memory to the accumulator, an "input" instruction followed by a "load accumulator" instruction has to be used. The transfer to the internal data RAM by the "Input" instruction takes two cycles (400 ns) and the transfer to the accumulator takes one cycle (200 ns); which makes a total transfer time of 600 ns. The main disadvantage of the configuration is that the external memory cannot be accessed in a random manner; it is accessed only sequentially.

EXTENDED EXTERNAL PROGRAM AND DATA INTERFACE



- USED FOR SEQUENTIALLY ACCESSING LARGE DATA STORE
- EXTERNAL DATA RAM ADDRESSED AS I/O PERIPHERAL

FIGURE 5.2

c) Addressing Modes

There are two basic modes of addressing the data memory: direct and indirect memory addressing. In the direct memory addressing, the data word is derived from the data memory address defined by a field in the instruction word.

In the indirect memory addressing, the data word is derived from the data memory address specified by the contents of one of the auxiliary registers (the one specified by the auxiliary register pointer).

The instruction set includes also some load immediate instructions where a portion of the instruction word is dedicated for data. The immediate instructions are unusual in a Harvard architecture since the program and memory busses are independent. This was possible on the TMS 320 due to the connection between the two busses.

d) Additional TMS 320 Features

The barrel shifter performs a bit shift of 0-15 places left. Left-shifted data is zero filled and the high order bit is sign-extended during shift operations. The data word from memory is always passed through the shifter. Thus the data operand may be shifted any number of bits with zero extra time and zero extra instuctions.

The 320 provides for "free" accumulation of successive products via the LTA instruction.

A special instruction "data move" (DMOV), is provided to enable the user to move the contents of a given location to the next higher location in one machine cycle; which is very useful in many

applications such as convolution.

The I/O branch control (BIO) is an external pin which allows the user to interrogate the condition of external peripherals. A zero level on BIO will cause a branch when sampled by the BIOZ instruction.

e) Future Versions of the TMS 320

The TMS 320 architecture allows the addition of new features in the next generations of the chip. The page addressing dield in the "load data page immediate" instruction allows the existence of up to 27 pages of data memory . The future versions of the TMS will thus have larger data memory space.

All the instructions dealing with the auxiliary register pointer: "store auxiliary register", "load auxiliary register" and "load auxiliary register immediate" have a register address field of 3 bits; which supports the existence of 8 auxiliary registers.

In the present chip, the shifter, at the output of the accumulator allows only a left shift of 0, 1 or 4 bits of the high order accumulator bits while storing it. The left shift for the "store accumulator low" instruction is not implemented. The next generation will include more flexibility in this respect.

The next generations of the TMS 320 may also include, according to Texas Instuments, serial ports and A/D, D/A coverters.

5.3 TRANSMITTER/RECEIVER FUNCTIONS

5.3.1 Transmission Functions

Figure 5.3 shows the data flow in the transmitter. The voice signal from the microphone is pre-amplified. The frequency spectrum of this signal may be inverted to reduce the intermodulation distortion.

The amplitude of the frequency inverted voice signal is then raised to a nearly constant level, resulting in the companded voice signal. This amplitude change is digitally encoded onto the compander data stream which is digitally modulated, forming the control signal. The total audio signal is formed by summing the control signal and the companded voice. The audio signal is then modulated to give the IF SSB signal.

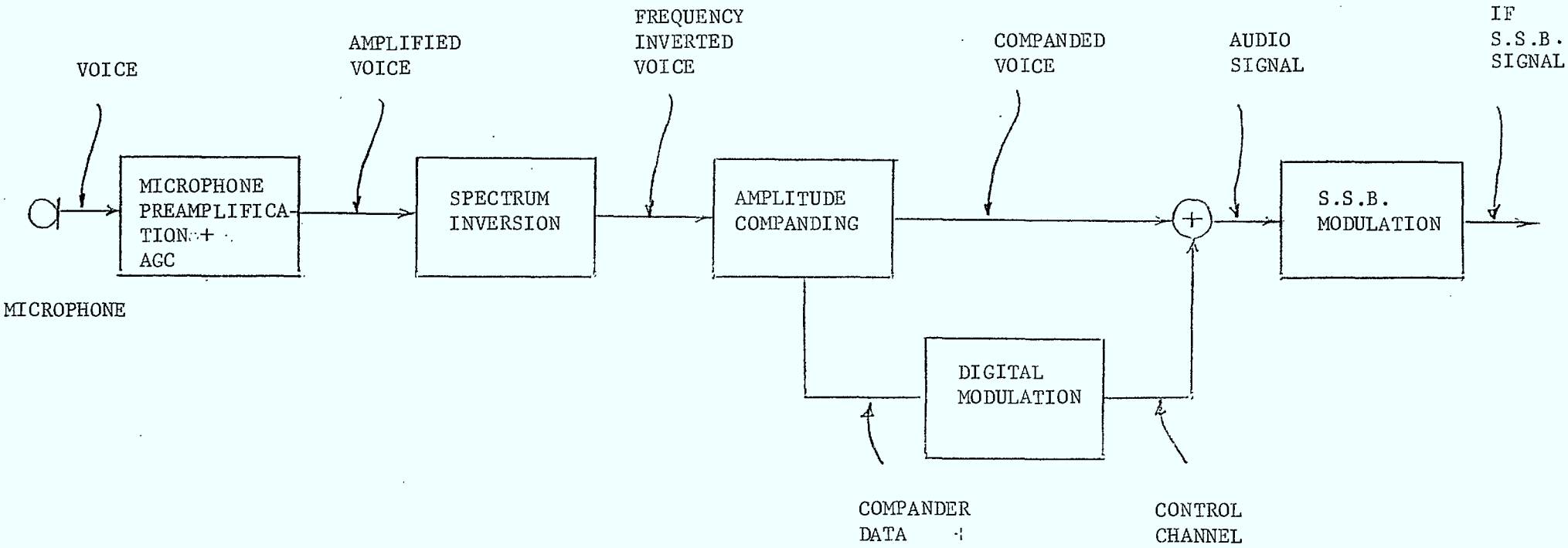


FIGURE 5.3

TRANSMISSION FUNCTIONS :

(data flow)

Setting of the Compander Gain

This function is performed after a whole block is entered; i.e. every 4ms. The compander gain is initially set to one while the samples are entered. The largest sample in the block is stored.

If the maximum input multiplied by the compander gain is larger than the maximum possible integer, the compander data is set to zero. The compander gain is adjusted according to the previous and the actual compander data: (0, 1) same gain, (0,0) lower gain.

If the maximum input multiplied by the compander gain is smaller than or equal to the maximum possible integer, the previous compander data is checked. If it is a zero, it is restored to one and the gain remains the same. If it is a one, the possibility of having the next higher compander gain without overflow is checked. If this is possible, the compander gain is incremented to its next higher value; otherwise the compander data is set to zero and the compander is unchanged. Figure 5.4 shows a flow chart for the algorithm used in setting the compander gain.

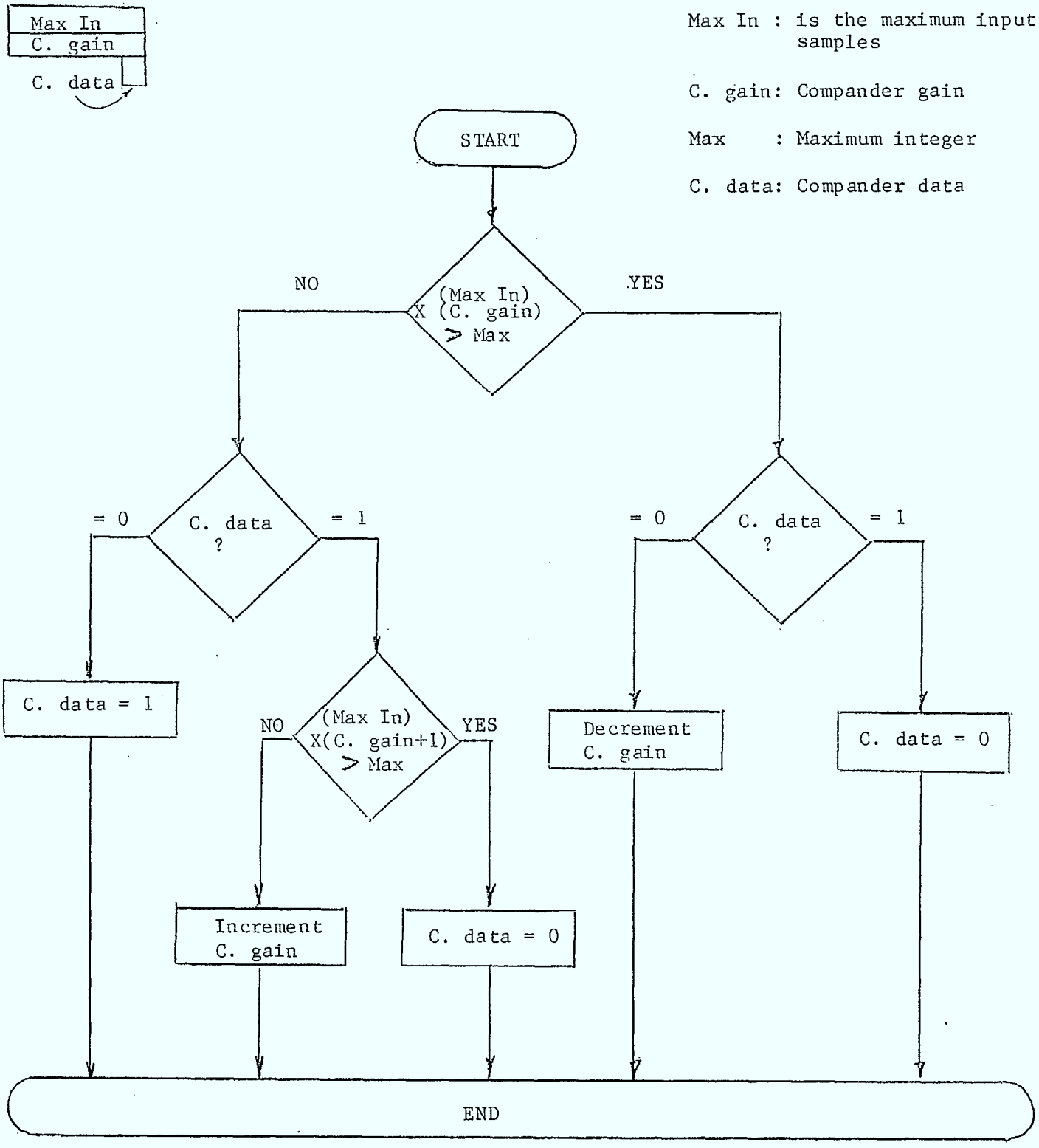


FIGURE 5.4

COMPANDER GAIN SETTING

5.3.2 Reception Functions

Figure 5.5 shows the IF signal and data flows in the receiver. The IF SSB signal is demodulated to give the Base Band signal. The frequency offset is estimated and fed back to the "IF to Base Band down coverter". The purpose of the Audio A.G.C. stage is to compensate for channel fading. This is done by amplifying the Base Band signal such that the control channel portion of the received audio signal is held constant.

The companded voice signal is then extracted by the coice channel filter. The control channel is obtained from the control channel filter and is demodulated to give the compander data. The amplitude expander is then able to employ the compander data to restore the frequency inverted voice. The correct voice spectrum is then obtained by inverting the spectrum of the previous signal. An AFC circuit is used to detect the carrier and correct for the frequency offset as explained in Section 3.

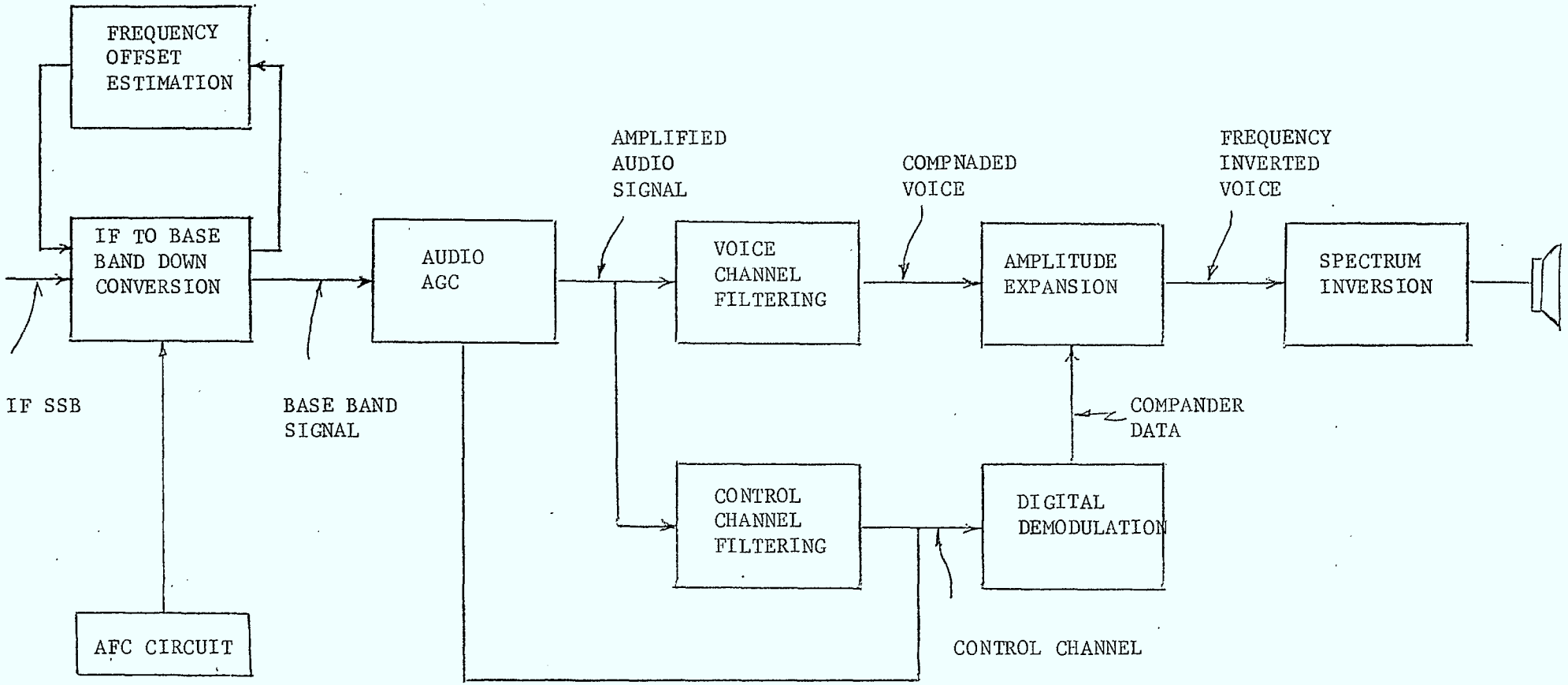


FIGURE 5.5

RECEPTION FUNCTIONS :

(data flow)

5.4 HARDWARE ARCHITECTURE

The R.F. and I.F. processing has to be implemented analog-wise; no digital circuits available now or in the near future, can handle such huge amounts of computation in real time. The baseband processing could be performed wholly or partially by the TMS 320 digital signal processor.

The digital processing is performed by sampling the analog signal, encoding the analog samples into digital and feeding the digital samples to the digital signal processor. Since the bandwidth of the baseband signal is 4 kHz, the Nyquist frequency is 8 kHz. In order to eliminate the aliasing noise, the sampling rate has to be at least 8 kHz. For some implementation considerations concerning the anti-aliasing filter and the reconstruction filter, it is suggested to use a sampling rate of 12 kHz.

The main constraint in the design procedure is the real time consideration. All the digital operations acting on a sample has to be accomplished before the arrival of the next sample. This constraint implies the partition of the baseband processing between some analog circuits and the D.S.P., depending on the architecture used.

Simple Architecture

Figure 5.6 shows a hardware configuration of the system using a unibus single processor architecture. The programmable interval timer generates the sampling clock and the block starting clock. Depending on the radio control selector, either the transmitting or the receiving functions are performed.

In the transmission mode, at every sampling clock, the amplified voice signal is sampled and encoder into a digital sample by the A/D converter. This sample is fed into the TMS 320 digital signal processor, where the spectrum inversion, the amplitude companding and the digital modulation functions are performed. The resulting audio signal is converted into the analog form by the D/A Converter, and is modulated using a S.S.B. modulator, into an IF SSB signal.

In the reception mode, the IF signal is converted into base band. A frequency offset estimation is fed back to the local oscillator in order to improve the tracking of the carrier frequency. The base band signal is then sampled, converted into the digital form and fed to the TMS 320. The base band digital signal processing includes the audio A.G.C., the voice filtering, the control channel filtering, the digital demodulation, the amplitude expansion and the spectrum inversion. The recovered voice channel is then converted into the analog form, amplified, and fed to the speaker.

The decision as to whether the transmitting or the receiving functions are to be performed is taken by the processor. Using the I/O branch control facility in the TMS 320 (explained in the previous chapter). The start of the sample cycle processing is determined either by an interrupt from the A/D converter or by using the test and skip method. The processor recoginzes the start of a new block period either by an interrupt from the timer or by testing an external flag. Figure 5.7 shows a flow chart of the TMS 320 software.

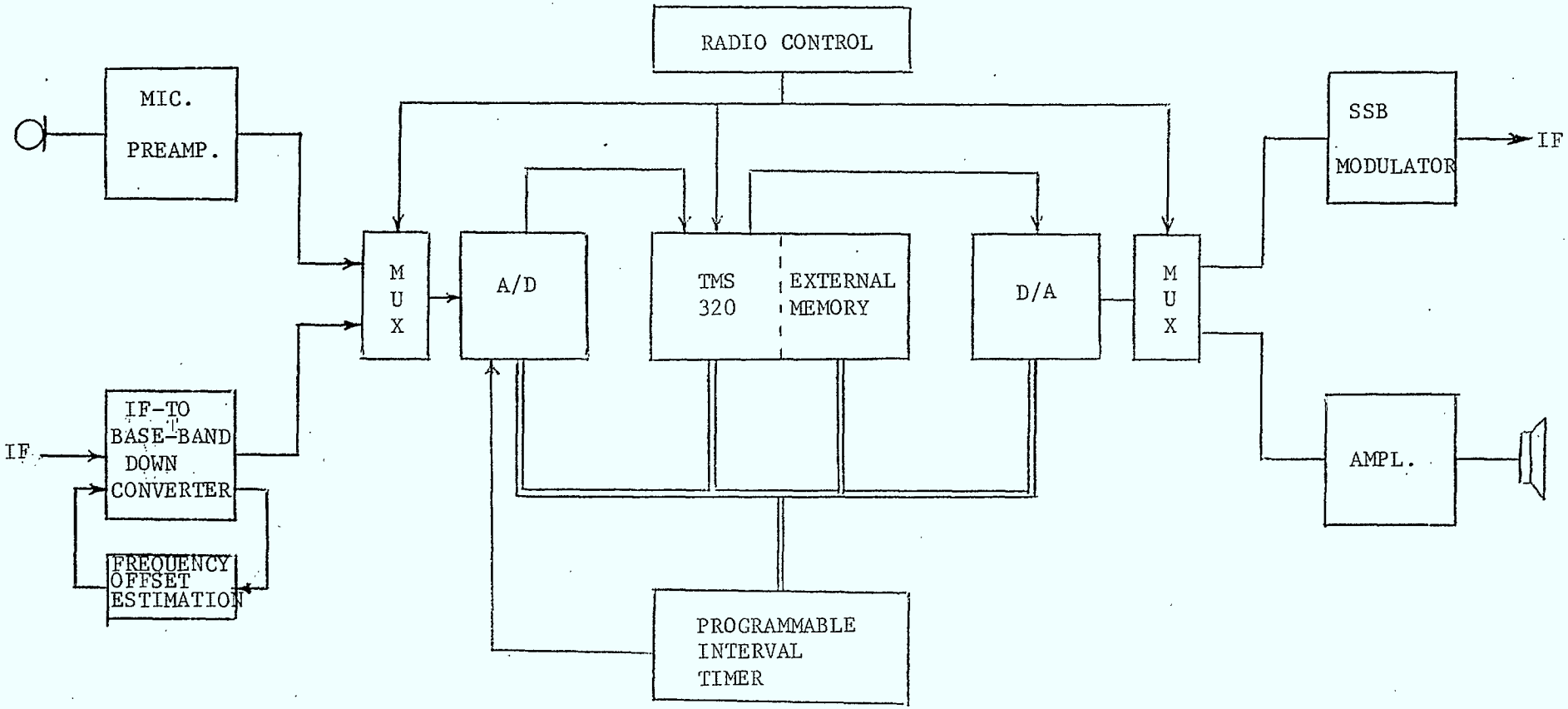


FIGURE 5.6

SINGLE PROCESSOR ARCHITECTURES

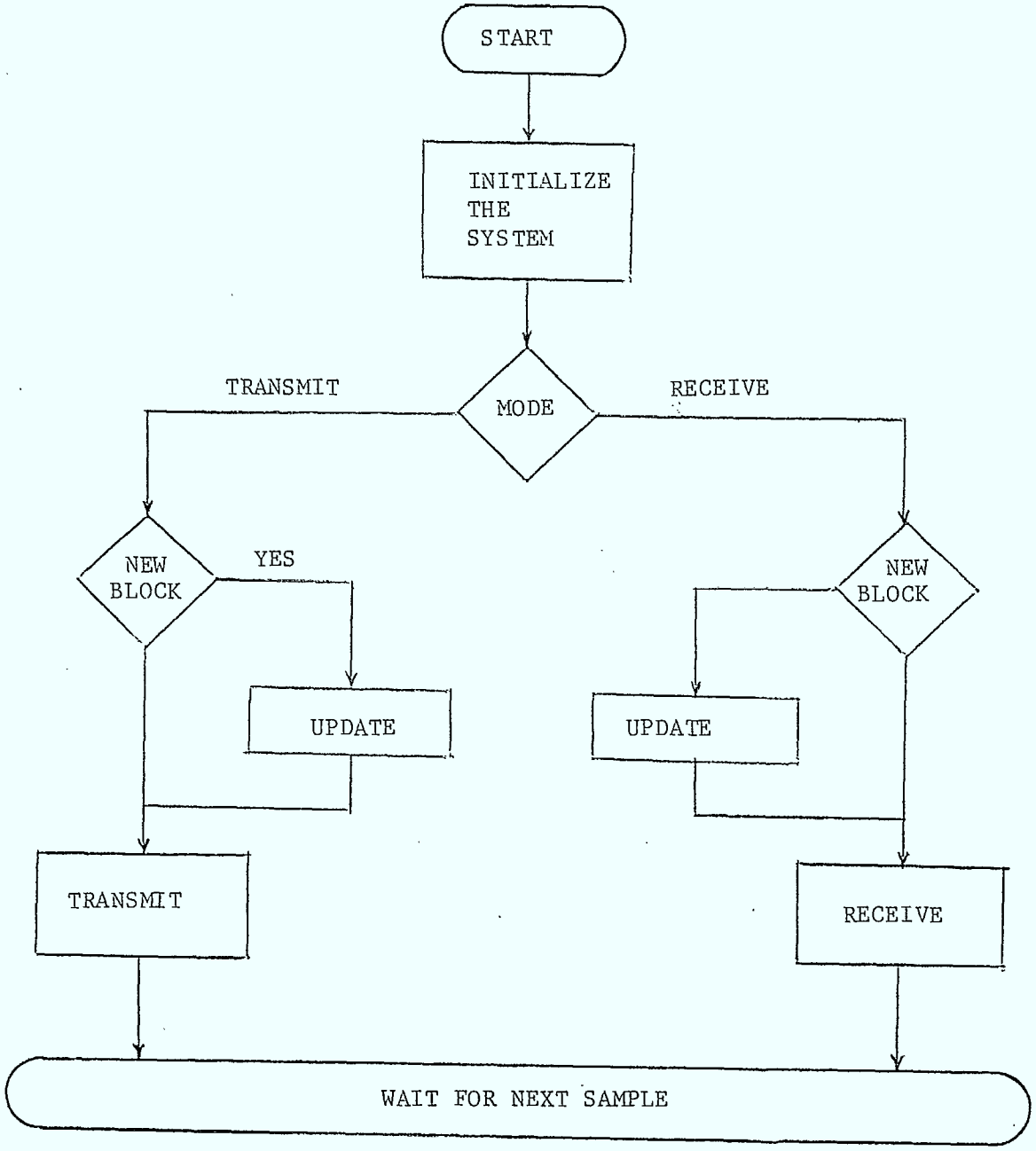


FIGURE 5.7

SOFTWARE CONTROL BRANCHING IN
THE SINGLE PROCESSOR ARCHITECTURE

If the companding gain is set to 2 per bit, it will substantially reduce the number of necessary computations per sample. A multiplication by 2, or a division by 2 could be done within any operation using the 2 shifters available at the input and output of the ALU of the TMS 320. This will allow some other functions, such as the frequency offset estimation in the receiver and the generation of the signals of the I and Q channels using the Hilber transform, to be performed digitally.

Multi-Processor Architectures

The projected price of the TMS 320 for 1985 is of the order of $15. Therefore, any enhancement in the system performance which require the use of multiple processors will be economically feasible in the future.

The use of several processors will increase and speed up the computational power of the system, it will also increase its memory size for both the data RAM and the program ROM. This will allow almost all the base band operations to be processed digitally. As well it will allow the use of higher order digital filters, which will enhance the total system performance.

a) Classical Parallel Architecture. In the simple architecture shown in Figure 5.7 the TMS 320 DSP could be replaced by the circuit shown in Figure 5.8. The different tasks are partitioned between the two processors. The logical circuit determines the bus access right for the processors. this configuration increases the system throughput by 80%. Its drawback is its control complexity. This architecture makes

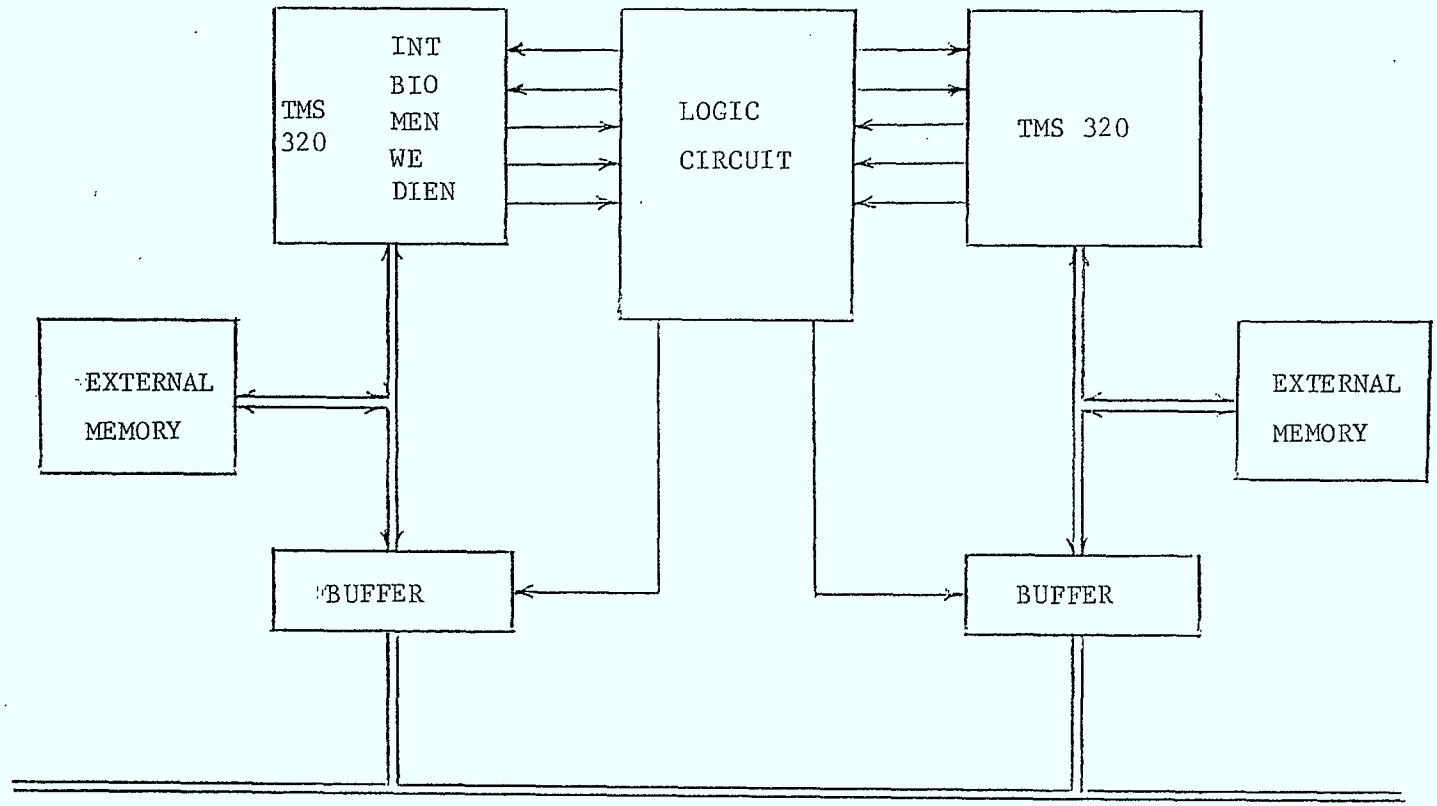


FIGURE 5.8

TWO PROCESSOR ARCHITECTURE

use of the I/O control branch facility of the TMS 320 which is required by the system.

b) Pipeline Architecture. A pipline system consists of a sequence of processing units through which a data stream passes. Partial processing is performed by each segment, and a final result is obtained after the data has passed through all the segments of the pipeline. A pipeline system could be viewed as a multiple instruction single data stream (MISD) system.

The system configuration using a pipeline architecture is shown in Figure 5.9. A two segements pipeline is proposed. Each segment consists of a TMS 320 D.S.P., having its own bus and its own peripherals. The communication between the 2 segments is achieved through a FIFO buffer. The FIFO buffer is implemented in the data RAM of the first processor; and the word to be transferred is stored by the processor in an external buffer. The second processor considers the buffer and input port.

The first processor is dedicated to the input process and to the house-keeping operations. It performs the transmission functions (while storing the amplified voice samples), sets the compander gain and generates the compander data (which are passed later to the second processor).

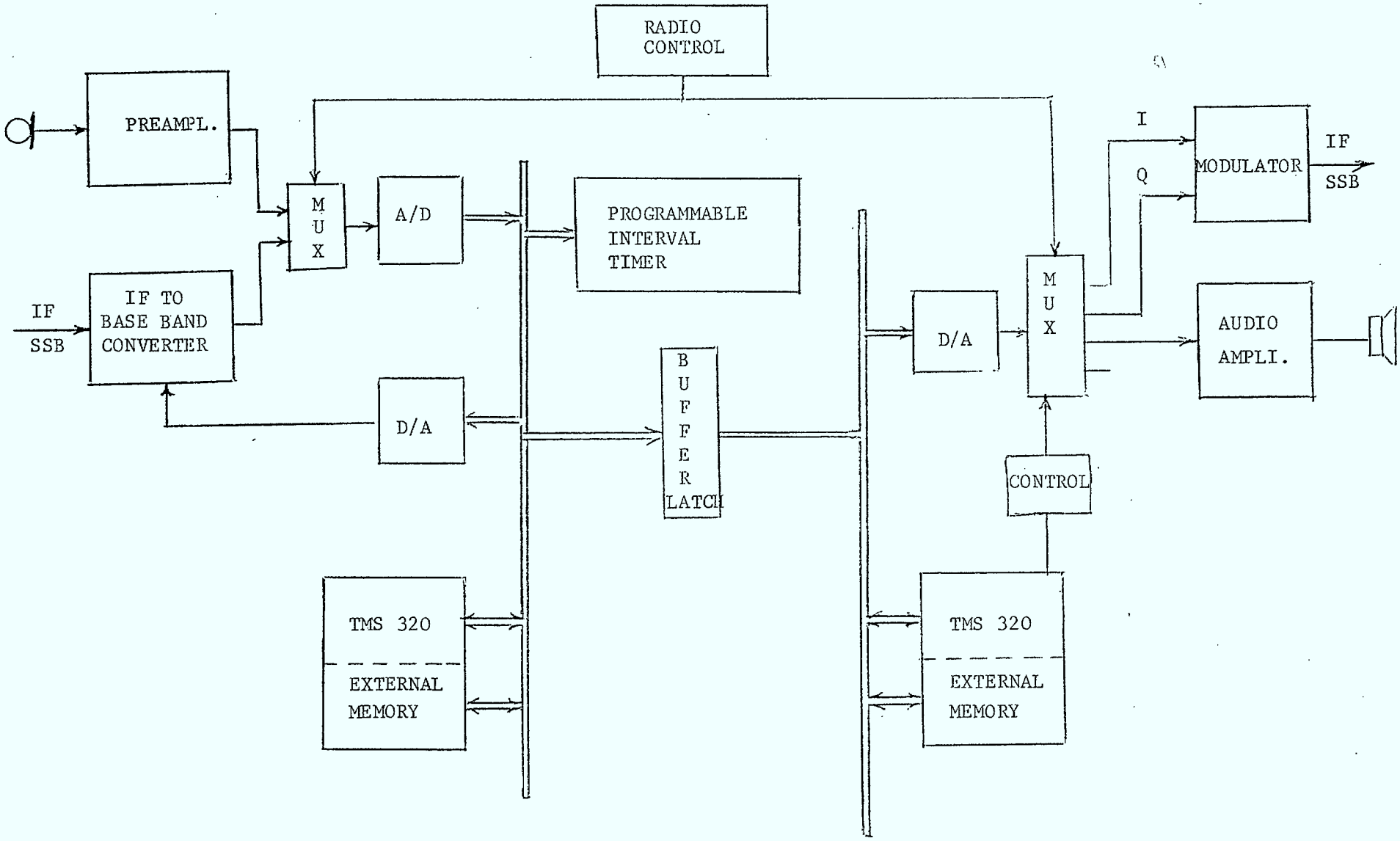


FIGURE 5.9

PIPELINE ARCHITECTURE

When the reception functions are performed, it inputs the samples and performs the frequency offset estimation.

The second processor is dedicated to the digital filtering operations, the amplitude expanding and companding algorithms and to the output operation.

The proposed architecture offers all the advantages of any multiprocessor system previously mentioned. In addition, the interconnection between the processors is very simple.

In the single processor architectures, a complete block of samples has to be stored before any processing in order to calculate the compander gain. This restricts the scratchpad memory in the single processor architecture. This restriction is removed in the proposed pipeline architecture since the main computations are done in the second processor while the samples are stored in the first one. The proposed architecture also removes the bottleneck that may happen at the beginning of every block period in the simple architecture.

5.5 TIMING CONSIDERATIONS

If the sampling rate is 12 kHz, the samples are separated by 83.3 micro-seconds. This means that for the system to be feasible, all the operations acting on a sample has to be accomplished in less than 83.3 micro-seconds. Most of the 320 instructions are one-cycle instructions (200 ns); except the input/output and the branch instructions which are two cycle instructions and the table read and write which are three-cycle instructions. This means that an average of 400 instructions per sample could be performed in real time, using the in-line programming technique.

The divide operation takes about 25 micro-seconds on the TMS 320. Therefore, a proper choice of the companding gain is a major factor in the feasibility of the system. As an example let us consider the case of companding gains of 2,4,8... . The multiplication or division by 2 in the 320 could be done using the barrel shifter at no extra cost; time-wise and instruction-wise, which means that a major part of companding-expanding algorithm could be performed without delay.

On the other hand, if the gains are choosen such that the division operation could be done by few shifts and adds, the companding-expanding algorithm would be executed in a reasonable time (few micro-seconds).

The TMS 320 can perform a second order biquad filter in 2 micro-seconds. Several units of such section could be cascaded to form a higher order filter. A 320 program that performs a one stage second order biquad filter is shown in Figure 5.10.

Figure 5.11 shows the implementation of a phase-locked loop, used sometimes in AFC circuit realization. The time required to process the loop is 2.6 micro-second. Finally, Figure 12 shows a routine for calculating the sine/cosine of an angle. The sine/cosine routine requires 4.8 micro-second. Figure 5.10, 5.11 and 5.12 are taken from reference [14].

Discrete Hilbert Transfer

In order to study the feasibility of implementing a discrete Hilbert transform using the TMS 320, a stringent design in terms of overall system trade-offs is examined.

The following parameters are chosen:

(i) a symetrical frequency response

(ii) a peak error of less than 0.1%

(iii) F= 0.02 (meaning 96% of the Nyquist bandwidth is within the peak specifications).

(iv) a 12 kHz sampling rate

Then from [15] an FIR filter implementation would require that 95 samples be stored and 24 multiplications be performed ever 83.3 micro-seconds.

The TMS 320 can store up to 144 samples in its internal data RAM and can perform 416 multiplications every 83.3 micro-seconds.

Based on these assumptions the utilization of the TMS 320 resources will be:

(i) 66% of the data RAM

(ii) 5.8% of the multiplier

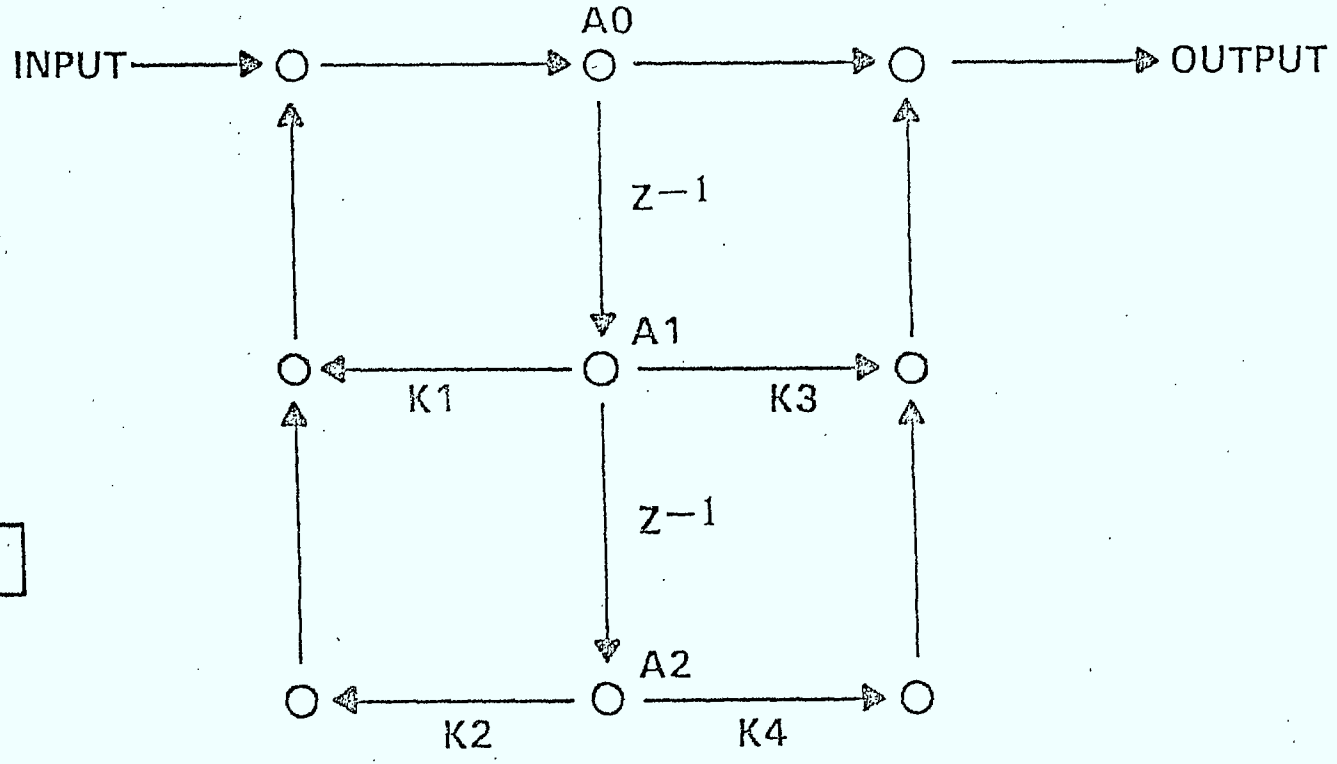
However, the data RAM space is not a limited resource; more data could be stored in the program space. If the space is still not enough, a special interface could be built to extend the data RAM.

In order to accomplish one multiplication, the instruction set of the TMS 320 forces some extra overhead in storing one of the operands in the T register and restoring the result. If we assume that the data is available in the data RAM; the Hilbert transform will require approximately 40% of the TMS 320 processing resources.

If more stringent design parameters are required, a third TMS 320 chip could be added to the system. This chip will be dedicated to the Hilbert transform implementation.

TMS32010: SECOND ORDER BIQUAD FILTER

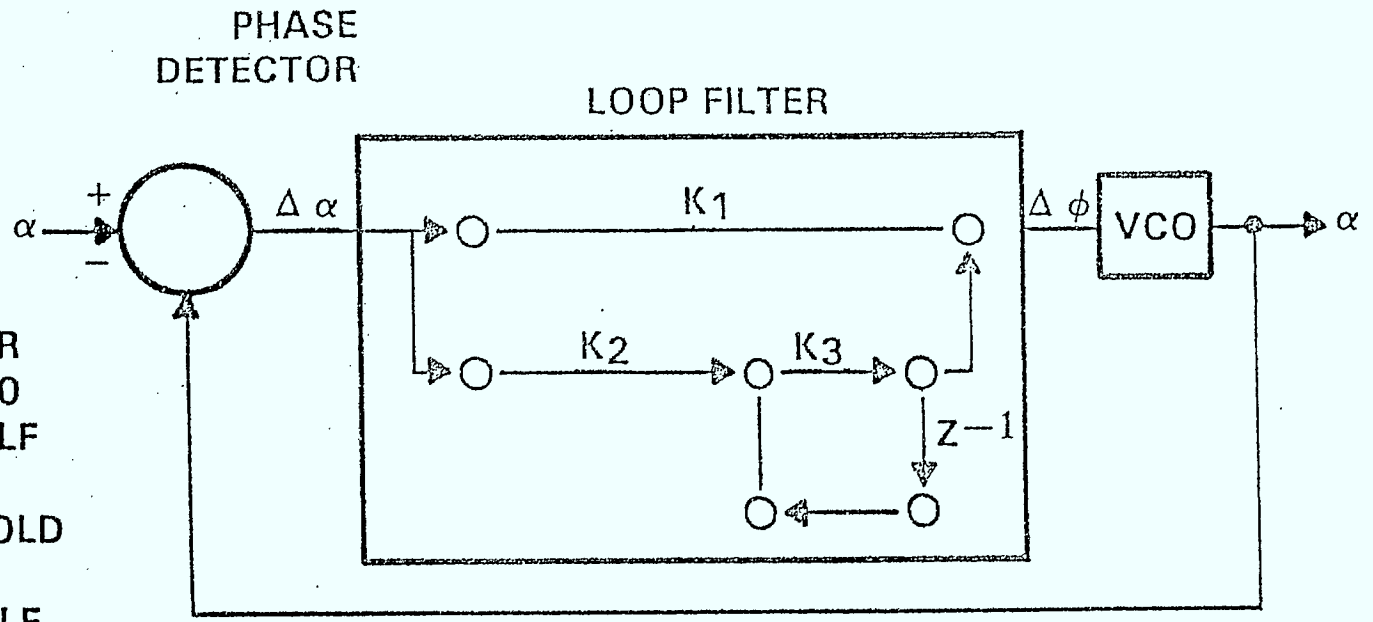
LT	A1
MPY	K1
LTA	A2
MPY	K2
APAC	
SACH	A0
MPY	K4
LTD	A1
MPY	K3
LTD	A0
TOTAL:	2.0 μs



$$Y_n = (X_n + K_3X_{n-1} + K_4X_{n-2}) + K_1Y_{n-1} + K_2Y_{n-2}$$

FIGURE 5.10

TMS32010: DIGITAL PHASE-LOCK LOOP



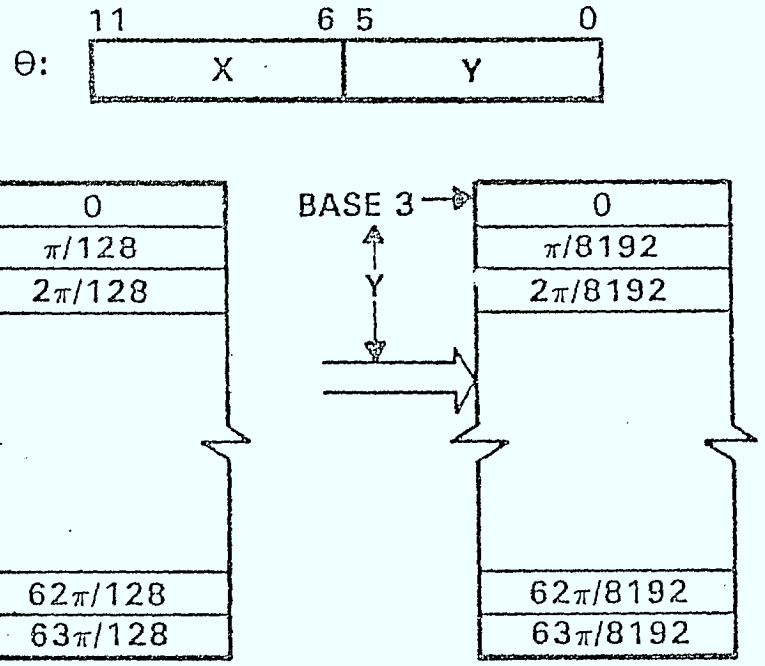
LAC	ALFAR
SUB	ALFA0
SACL	DELALF
ZAC	
LT	SUMOLD
MPY	K3
LTA	DELALF
MPY	K2
LTA	DELALF
SACL	SUMNEW
MPY	K1
LTD	SUMNEW
SACL	DELPHI
TOTAL:	2.6 μs

FIGURE 5.11

TMS32010: SINE/COSINE OF ANGLE θ

```
LAC     THETA, 10
SACH    X
LAC     X
ADD     BASE 1
TBLR    SINX
LAC     BASE 2
SUB     X
TBLR    COSX
LAC     THETA
SUB     X,6
ADD     BASE 3
TBLR    SINY
LT      SINY
MPY     COSX
PAC
SACH    X,1
LAC     X
ADD     SINX
```

TOTAL:	4.8 μs



$$\text{Sin}\theta = \text{Sin}(x+y) \cong \text{Sin}x + \text{Sin}y\ \text{cos}x$$

FIGURE 5.12

6.0 CONCLUDING REMARKS AND RECOMMENDATIONS FOR FURTHER STUDIES

6.1 CONCLUDING REMARKS

This study has examined the application of the SINCOMPEX concept to SSB Mobile Communication Systems in the VHF/UHF frequency bands. The study focused on the sub-systems (components) comprising the base-band sections of the transmitter and the receiver, with the aim of implementing most of these components using the newly introduced family of digital signal microprocessors. Specifically, the study investigated the following aspects:

- Variable ratio companding algorithms and methods for encoding the companding gain variable were surveyed and evaluated based on a number of performance criteria (dynamic range, attack time, tracking time, steady state precision and sensitivity to transmission errors). Based on these performance criteria, two encoding shcemes were recommended: (1) 1-bit Enhanced Delta Modulation with a 12 dB Attacking Step Size with data rate of 100 bit/second, and (2) the same sheme with data rate of 150 bit/second.

- Two modulation techniques were identified as suitable for transmitting the control signals: non-coherent FSK and DPSK. The bit error in each technique were computed under fading conditions and found to be within the acceptable limits of the sensitivity of the encoding scheme with respect to transmission errors. Both modulation system can be implemented easily using the digital microprocessor.

- The residual distortion resulting from the use of the hard limiter in the AGC circuit was analysed. The results suggest that improvements can be attained using space diversity techniques.

- An Automatic Frequency Control (AFC) circuit was proposed to augument the mini-coherent FSK demodulator. The circuit is particularly suitable for low S/N ratio, which is the case of the control signal in the land/mobile channel.

- In-band and adjacent SSB channel distortion resulting from the IM products were analysed and computed for two signal configurations: (1) the control signal is placed out-of-band with respect to the speech signal, and (2) the control signal is placed in-band, by splitting the speech spectrum and shifting the upper frequency component 1.1 kHz to the right.

The IM distortion due to the 3rd and 5th harmonics was found to be approximately 20 dB higher in configuration (2) than in configuration (1).

- Implementation of the complete base-band section using the TMS 320 (Texas Instrument) was investigated. Three architectures were proposed; the utility of each architecture depends on the number of components to be implemented digitally. In the simplest architecture, one processor is used where the companding algorithm, speech processing and control signal modulation are implemented digitally while the AFC circuit and the SSB signal generator are implemented separately. In the most advanced architecture, three processors are used to implement the entire set of subcomponents, including the Hilbert Transform which is used to generate the SSB signal.

- Implementation of the signal configuration in which the control signal is placed in-band, as described in reference [1] will require a dedicated TMS 320 chip to perform the speech processing with this configuration. Thus placing the control signal in-band has one advantage (protection against the group delay introduced by the IF filter) and two disadvantages (complexity of implementation and higher IM distortion).

6.2 RECOMMENDATIONS FOR FURTHER STUDIES

The study reported here was intended to serve as a prelude to the iplementation of the SIMCOMPEX concept, if found feasible, using digital processing hardware (signal processors) in the UHF/VHF band. Several research aspects remain as candidates for further investigation.

- Implementation of the proposed AFC circuit and testing it under simulated fading conditions for frequency offset range of $\pm$ 0.5 kHz.

- Implementation of the AGC circuit and using it to test the BER performance of the modem (non-coherent FSK and DPSK) under simulated fading conditions.

- Study of the use of space diversity techniques to reduce the residual distortion in the speech signal due to AGC hardlimiting under severe fading conditions.

- Finally testing the performance of the entire base-band/IF sections under simulated fading conditions using formal subjective speech evaluation methods.

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