# INVESTIGATION OF

# PCM - DELTA CODE CONVERSION

FINAL REPORT

MARCH 31, 1980

D.E. DODDS

DSS Contract #0SU79-00111

## 1. Introduction

The transmission of digitized voice is most frequently achieved using PCM coding of the signal. In applications where the bit rate is low or where a noisy channel introduces frequent bit errors, the voice signal is often coded using delta modulation. Both coding formats are now employed in existing systems. Conversion must be done by decoding to an analog voice signal then recoding in the other format. The objective of this work is to research and recommend a totally digital solution to the interfacing of PCM and Delta Modulation systems. Specifically, it is intended to interface standard CVSD with telephone standard CPCM with newly developed EVSD. The contract defines two tasks: first a literature survey and evaluation and second a proposal for system partitioning and analysis of the proposal. A brief report on each topic follows:

## 2. Literature Survey

Computerized literature searches were conducted on 3 data bases: INSPEC, NTIS and DSIS. These are respective abbreviations for National Technical Information Service (USA Government), Canadian Defence Scientific Information Service. The INSPEC search was done from the data base at Lockheed in Palo Alto, California. Publications of interest are listed in the attached references. The following table illustrates the contributions of each search.

| | Number of Citations | Number Applicable | Reference |
|---|---|---|---|
| NTIS | 25 | 1 | (3) |
| DSIS (A) | 10 | 2 | (1) , (2) |
| (B) | 50 | 1 | (3) |
| INSPEC 1969-1977 | 109 | 18 | (4) - (26) |
| 1978-1979 | 13 | 5 | |

The literature search turned up several good papers which are directly applicable to this project. A paper by Eggermonth et al (6) appearing in the Philips Technical review, had significant impact on the system partitioning. Papers by Villeret (16) support the IIR filtering approach. Papers with performance measurements such as references (2) and (16) illustrate poor SNR vs dynamic range performance. This is due in part to the low quality CVSD codecs which were used and, according to personal discussions, due to imperfect grounding in the large digital conversion system.

## 3. Proposed Topology For Code Conversion

### 3.1 Interfacing Format

In order to digitally convert between coding formats such as CVSD, EVSD, CPCM and possible DPCM and ADPCM it is necessary to select a suitable standard interface format. Initially it was suggested that the interface be high sample rate LPCM however further investigation revealed merit in using high sample rate DPCM. The original concept was to accumulate approximate signal increments to get a digital (LPCM) equivalent of the approximate signal $\tilde{x}(t)$. In CPCM conversion the LPCM signal would then be filtered before subsampling (decimation). To allow for the gain in the digital filter, processing word length must be increased from 15 to 20 bits. With the new technique, the signal increments are digitally filtered before accumulation. The signal processing effect is the same, however, the required filter word length is reduced. A 15 bit filter word length will handle the 10 bit signal increment (step size) information. Interfacing with high sample rate DPCM also reduces EVSD - CVSD conversion since this sign plus step size magnitude signal is already available from the EVSD codec.

Figure 1 illustrates possible code conversion combinations. Shaded portions are interfacing circuits required to produce the high sampling rate DPCM. Figure 2 illustrates the summing circuits which are used in the interconnections.

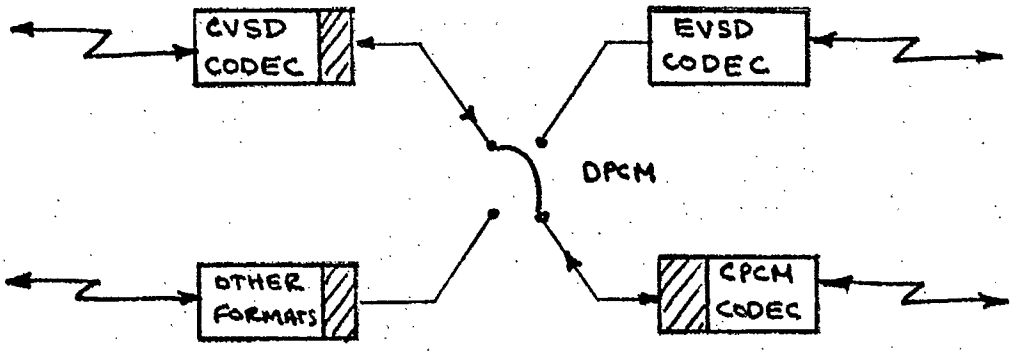



Figure 1 Block diagram illustrating conversion between any two codes.

### 3.2 Interfacing CVSD and EVSD

An EVSD decoder may be used with CVSD data (or vice versa) to give moderate quality decoded voice. At high amplitudes the adapting rate for CVSD and EVSD will be about the same. The decoded signal will not be significantly distorted because there is little step size change per cycle. At lower amplitudes the first problem is a large error in decoded level. With CVSD coding the probability of consecutive identical bits decreases rapidly with decreasing signal level. Because there is less change with EVSD coding, a moderate level CVSD signal will be interpreted as a very low level signal by an EVSD decoder. If the codecs are reversed, an EVSD coder and a CVSD decoder will cause compression of the dynamic range.

Code conversion requires the alteration of an incoming EVSD bit stream to form an outgoing CVSD bit stream. This can be done by decoding to an analog signal then recoding in the other format. It is also possible to use an accumulator creating a numeric equivalent of the analog signal. The digital CVSD encoder would then use a numeric comparator and a numeric approximate signal in the feedback loop. The proposed scheme simplifies the latter hardware by replacing the incoming accumulator, the feedback accumulator and the digital comparator with a single accumulator. Incoming increments are added, feedback increments are subtracted and the resulting sign becomes the outgoing CVSD bit.

When converting between CVSD and EVSD it is desirable to create equal step sizes on the encoding and decoding capacitors. This is the location of the approximate signals $\hat{x}(t)$ and $\hat{\hat{x}}(t)$. A digital equivalent of the analog step size is obtained from both the EVSD and CVSD codecs. A digital accumulator is then used to add incoming step sizes and subtract outgoing step sizes. If the contents of the accumulator remain nearly zero, the decoder approximate signal $\hat{\hat{x}}(t)$ will closely match the encoder approximate signal $\hat{x}(t)$. The proposed accumulator uses serial adders.

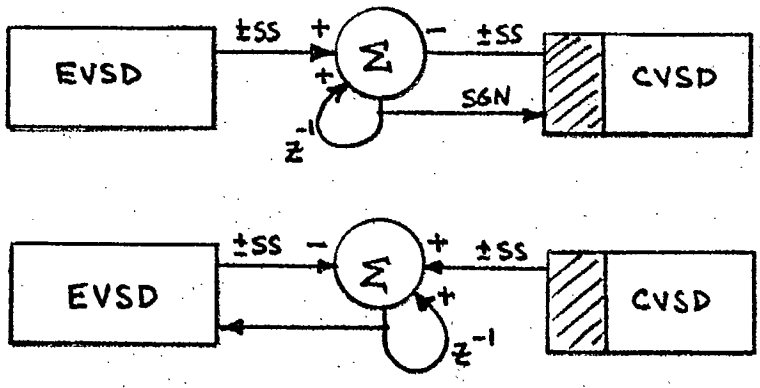
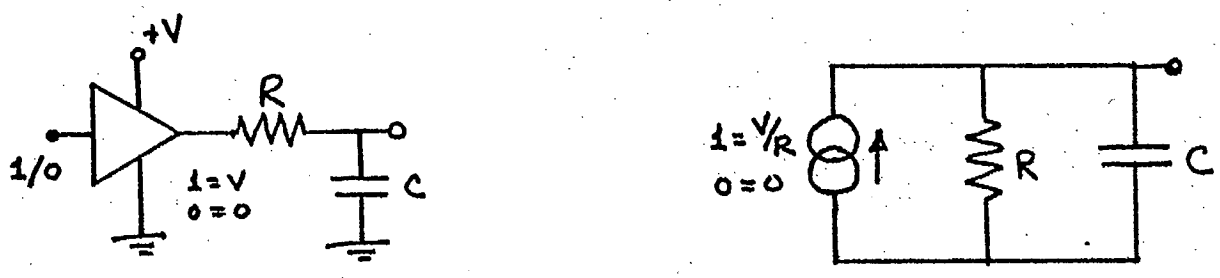



Figure 2. Signal flow diagram of EVSD - CVSD conversion.

The generator of the digital step size magnitude for the CVSD codec requires a simple digital filter to model the codec RC adaption circuit. The operation of the digital filter may be represented by the Norton equivalent of the RC adaption circuit.




(a) Actual Circuit (b) Norton equivalent circuit

Figure 3. Representation of CVSD adaption circuit.

The digital filter will have a transfer function of the form: $H(z) = \frac{1}{1 - \alpha Z^{-1}}$

A detailed development may be found in example A1 of Appendix A.

| $f_s$ | $\alpha$ | $\tau$ |
|---|---|---|
| 16 KB | 1-1/64 | 4mS |
| 32 KB | 1-1/64 | 2mS |
| 32 KB | 1-1/128 | 4mS |

The time constant, $\tau$, of the digital filter will vary directly with the sampling period. Some examples are given in the proceeding table.

The digital filter may be implemented with serial adders. A signal flow diagram is illustrated in figure 4.

Quantization error will become significant at small step sizes and this will be a source of noise. CVSD performance is quite poor at low signal levels and this quantization will cause a small amount of further degradation. The dynamic range of CVSD coding is approximately 35 dB (Ref. 29) and would require a step size range of 6 bits. It is proposed to use a 9 bit register for step size which limits the worst case quantization error to 12%.

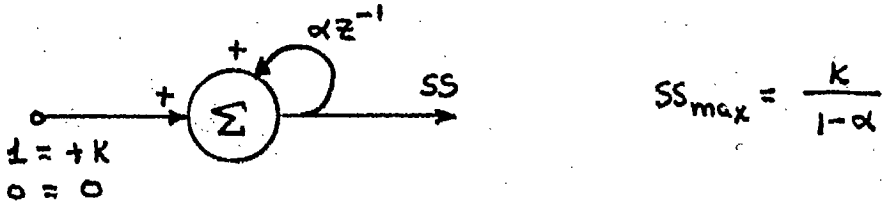



Figure 4. Signal flow diagram of CVSD adaptive step size.

## 3.3 Interfacing to CPCM

Conversion to standard companded PCM requires (1) accumulation (2) filtering (3) subsampling (decimation) and (4) companding. The reverse process requires (5) expansion (6) interpolation (7) filtering and (8) differentiation. As discussed in section 3.1, a more efficient implementation may be achieved by reversing parts (1) and (2) and also parts (7) and (8). The functions of the two filters will be discussed separately. It should be added that these filters should be approximately flat in response. There should be little change in channel response when the PCM conversion is not used.

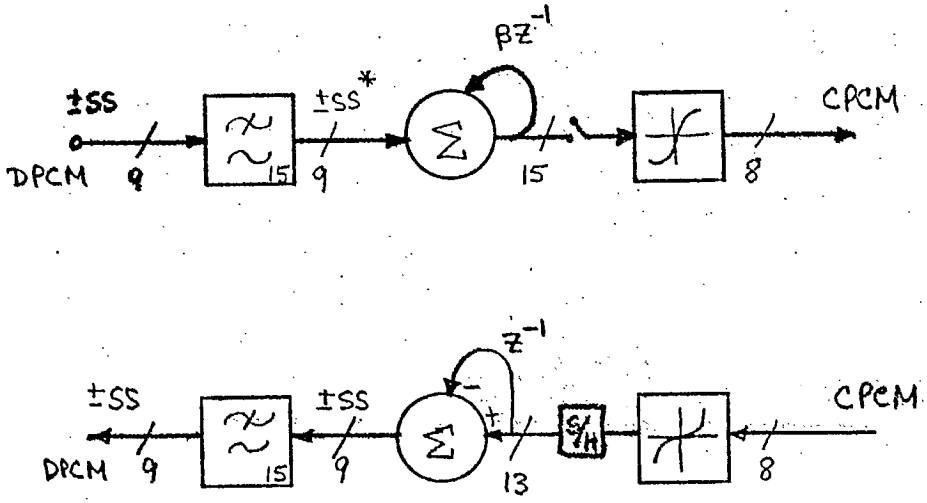



Figure 5. Signal flow diagram of CPCM conversion.

3.3.1 Quantizing Noise Filter (2) This digital filter is used prior to the accumulation and decimation during the ΔM-PCM conversion. Samples are filtered at the delta coding rate (16 KB, 32 KB or 40 KB). Prior to filtering the equivalent accumulated signal spectrum has voice spectral power below 3 KHz, quantizing nosie at intermediate frequencies followed by voice spectral power centered about the sampling frequency. This filter helps avoid signal aliasing, however, its main function is to reduce the quantizing noise power at intermediate frequencies before it is aliased into the voice band during the decimation process. Wihout this filter, quantizing noise would increase by 3 dB or 6 dB for 16 KB and 32 KB ΔM respectively. If the filter stopband gain is merely -10 dB the inband quantizing noise will increase by only .5 dB for 16 KB ΔM. An illustration of the filtering decimation and noise aliasing has been reproduced from reference 28.

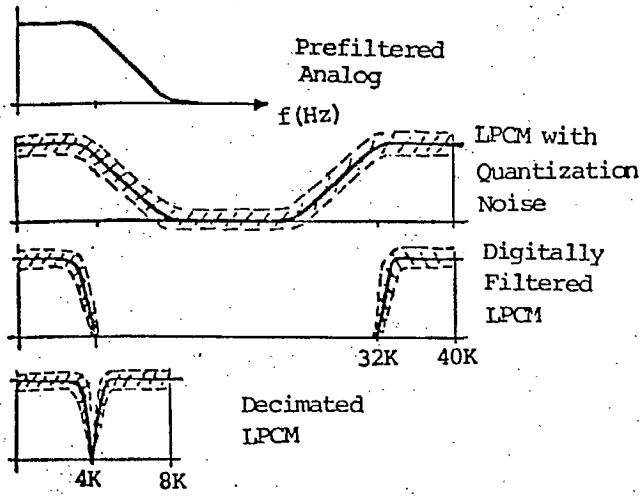



Figure 6.

3.3.2 Interpolation Filter (7) In the coversion from CPCM the samples are first expanded to LPCM then differentiated to obtain DPCM. The DPCM samples occur at an 8 KHz rate. Intermediate samples at 16, 32 or 40 KHz if the delta codec is to operate satisfactorily. Images of the voice spectrum are centered about 0, 8, 16, 24 KHz (etc.). The interpolation filter severely attenuages all frequencies except those near zero. Image components "worry" the delta codec making its step size larger than need be. The delta codec's frequency characteristics make it especially sensitive to these images. An attenuation exceeding 30 dB is recommended for frequencies 6 KHz and higher. This filter must have larger attenuation and sharper cut off than the previous quantizing noise filter. Figure 7 illustrates the function of the interpolation filter.

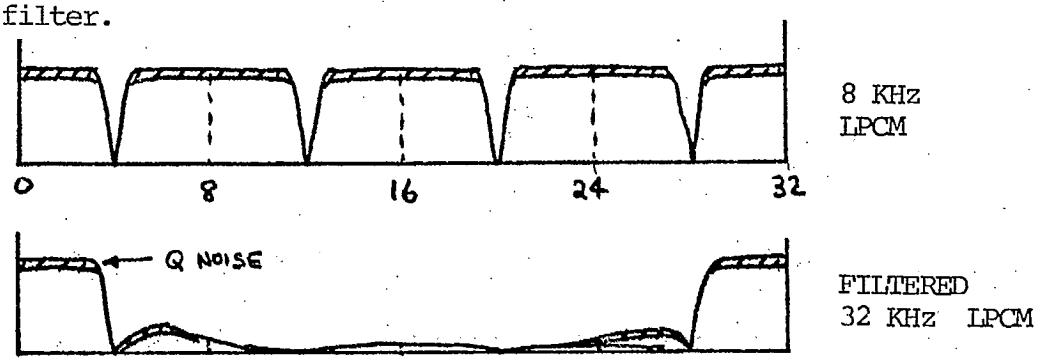
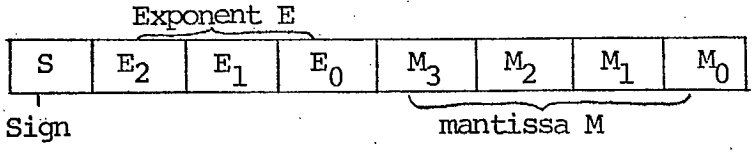



Figure 7. Signal and Noise Spectrum during conversion from CPCM.

3.3.3 Companding In an effort to reduce the transmitted bit rate PCM is transmitted in a compressed form. Linear PCM samples with 13 bit resolution are converted to an 8 bit "floating point" format with a sign-exponent-mantissa format. (Reference 30) The mantissa is effectively 5 bits with the most significant bit always logic 1. Only the lower 4 bits are transmitted. The 3 exponentbits are used to multiply the mantissa by powers of 2. The 15 segment U law is formed when the 3 exponent bits define 8 positive coding segments and 8 negative coding segments. The smallest postive and negative segments form a single segment passing through the origin.

CPCM FORMAT




Encoder threshold = $2^E$ (16 + M) - 16.5

Decoder magnitude = $2^E$ (16.5 + M) - 16.5

No proposals have yet been made for implementation of the compression and expansion required for companded PCM. Possible methods include table look up in ROM, serial computation, combinational steering networks and computation by microprocessor. The exact format will be influenced by the CPCM interface requirements.

## 4.0 Conclusion

There appears to be no theoretical barrier to all digital code conversion. The digital technique proposed closely models the "convert back to analog" approach which is known to work. The available literature is consistent, in general, with the approach taken here.

Further work on this project will include specification of the companding hardware followed by detailed design and testing of the functional blocks outlined in this report.

D.E. Dodds

References


1. Betts, W.L.; Kim U.S.; Greene, R.T. "Delta Modulation to pulse code modulation Digital Code Converter". Quarterly report Feb. 1974, 24 pages. U.S. Army Electronics Command, Fort Monmouth, N.J.

*2. Betts, W.L.; Greene, R.T. "Delta Modulation to Pulse Code Modulation Digital Code Converter". Final R&D report, June 1975, 59 pages. Electronic Communications Inc. to U.S. Army Electronics Command, Fort Monmouth, N.J.

3. Betts, W.L.; Zabanycz, P. "Digital Communications/Interoperability Techniques". Feb. 1978 final report, 30 pages. From E-Systems Inc. to Communications Research and development command, Fort Monmouth, N.J.

*4. Ghosh, S. "Code Conversion Techniques for Digital Transmission". Computer Design, Vol. 17, No. 8, pp. 103-111. Aug. 1978.

*5. Ghosh, S. "Converting Delta Modulation into PCM". Canadian Communications and Power Conference, October 1978.

*6. Eggermont, L.D.J.; Hofelt, M.H.H.; Salters, R.H.W. "Delta Modulation to PCM Converter" Philips Tech. Rev. Vol. 37, No. 11, 1977.

*7. LoCicero, J.L.; Schilling, D.L. "Non-Parametric PCM to ADM Conversion". National Telecommunication Conference, Dec. 1977.

8. LoCicero, J.L.; Schilling, D.L. "An all-digital technique for ADM to PCM Conversion". National Telecommunication Conference (NTC), Dec. 1976.

9. LoCicero, J.L.; Schilling, D.L.; Ikeda, Y. "PCM to ADM Conversion, An All-Digital Technique and an analysis of its performance". International Symposium on Information Theory, June 1976.

10. Song, D.C. "Adaptive Delta Modulation for Companded PCM Coding and Decoding". IEEE Transactions on Communications, pp. 557-561, May 1977.

*11. Villeret, M. "Numerical Conversion of PCM to Delta Modulation and Vice Versa" (in French). M.Sc. Thesis, University of Sherbrooke, April 1977.

12. Villeret, M.; Stephenne, H.; Deschenes, P.A.; Benoit, R.C.; Gitlin, J. "Continuously variable slope Delta Modulation to PCM Code Converter". European Conference on Electrotechnics (EUROCON) April 1974.

13. Deschenes, P.A.; Villeret, M. "Converter from PCM to Delta Modulation". USA Patent 3,772,678 Nov./73, Can. Patent 9 38738 Dec./73.

14. Deschenes, P.A.; Villeret, M. "Converter from Delta Modulation to PCM". USA Patent 3,707,712, Dec./72, Can. Patent 930083, July/73.

15. Villeret, M.; Deschenes, P.A.; Stephenne, H. "A new Digital Technique for implementation of any Continuous PCM companding Law". International Communications Conference (ICC), June 1973.

16. Deschenes, P.A.; Villeret, M., "Numerical Converters from PCM to Delta Mod. and Vice Versa". Canadian Symposium on Communications, Nov. 1970.

17. Goodman, D.J. "Digital Filters for the Conversion of Delta Modulation Signals to PCM". IEEE Int. Conf. Communications (ICC), June 1969.

18. Goodman, D.J.; Greenstein, L.J. "Quantizing Noise of DM/PCM Encoders". BSTJ, pp. 183-204, Feb. 1973.

19. Miller, J.H. "Digital to Digital Conversion between an Adaptive Delta Modulation Format and Companded PCM". Bell Labs. International Conference on Communication (ICC), June 1976.

20. Candy, J.C.; Ching, Y.C.; Alexander, D.S. "Using Triangularly Weighted Interpolation to get 13-Bit PCM from a Sigma-Delta Modulator". Bell Labs. IEEE Transactions on Commun., pp. 1268-75, Nov. 1976.

21. Ishiguro, T.; Kaneko, H. "A nonlinear DPCM Codec Based on DM/DPCM Code Conversion with Digital Filter". Int. Conf. Communication (ICC) June 1971.

22. Ohno, T.; Kuwahara, H.; Miyata, M.; Imai, K. "Voiceband Analog - PCM Conversion using Delta Modulation". Int. Conf. Communications (ICC) June 1976.

23. Jones, P.C. "Digital Code Conversion for Telephony". Austrailian Telecommunication Research, Vol. 9, No. 2, pp. 30-43, 1975.

24. Alahuhta, M; Vuori, J. "The application of Delta Modulation to Primary PCM Multiplex Equipment". Saehkoe (Finland), Vol. 50, No. 7, pp. 233-236, July 1977.

25. Pennington, H.; Steele, R. "A-Law PCM by a DM technique". Electronic Letters, pp. 171-173, 3/May/1973.

26. Castellino, P.; Scagliola, C. "On Optimum FIR Interpolators for Sampled Signals". CSELT RAPP. TEC. (Italy), Vol. 3, No. 3, pp. 3-9, Sept. 1975.

27. Dodds, D.E.; Sendyk, A.M. and Wohlberg, D.B., "Error Tolerant Adaptive Algorithms for Delta Coding", International Conference on Communications, pp. 8.3.1 to 8.3.5, June 1978.

28. Dodds, D.E.; Rothery, R., "Delta Modulation To PCM Conversion IEECE", Toronto, Canada, October 1979, Paper No. 79182.

29. Dodds, D.E., "Adaption Techniques for CVSD Coding", Paper 04.1 National Telecommunications Conference, Washington, D.C., November 1979.

30. CCITT Orange Book Volume III.

31. Motorola Semiconductor Products, "McMOS Handbook", Pages 10-6 to 10-20.

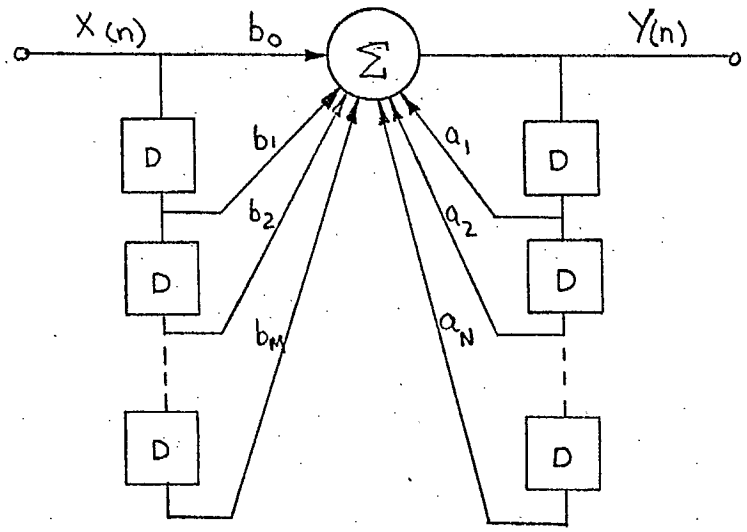
32. Kaneko, H., "A Unified Formulation of Segment Companding Laws and Synthesis of Codecs and Digital Companders", BSTI, September 1970 pp. 1555 - 1588.

## Appendix A

## Digital Filter Theory

Discrete time filters combine delay elements with signal summation to create a network response which varies with the frequency of the input signal. Although delay elements for continuous signals (transmission lines or surface acoustic wave devices) may be used, it is most common to use sampling and clocked delay circuits (charge coupled devices) to delay the analog signal. If the signal is both sampled and quantized, digital logic circuits may then be used for the delay and numeric summation. Parallel or serial arithmetic units may be used depending on the application. It should be added that each delayed signal is added to the output with a different weighting. For analog signals this can be accomplished with different resistances in a summing network. Quantized numeric signals, however, require a relatively complex digital multiplier for each delayed signal.

All the above implementations may be represented by the block diagram below. The blocks marked D indicate a unit delay. For sampled signals the unit delay is typically one sample period. Delayed samples of the input are added with multiplying coefficients $b_0$, $b_1$ ... $b_M$. At some frequencies the added signals will cancel and the output will remain at zero. The delayed input signals contribute zeros to the transfer function. Delayed samples of the output are fed back and summed to form a new output signal. At certain frequencies, the delayed output signals add in phase resulting in positive feedback and output which is larger than the input. Delayed output signals contribute poles to the transfer function.




$$Y_{(n)} = \sum_{k=1}^{N} a_k \, y_{(n-k)} + \sum_{k=0}^{M} b_k \, x_{(n-k)}$$

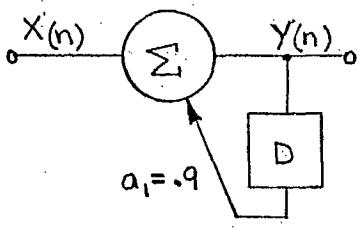
We can determine the following transfer function using the Z transforms shown below.

$$H_{(Z)} = \frac{Y_{(Z)}}{X_{(Z)}} = \frac{\sum_{k=0}^{M} b_k Z^{-k}}{1 - \sum_{k=1}^{N} a_k Z^{-k}}$$

$$Y_{(M)} \longrightarrow Y_{(Z)}$$

$$Y_{(n-k)} \longrightarrow Y_{(Z)} \cdot Z^{-k}$$

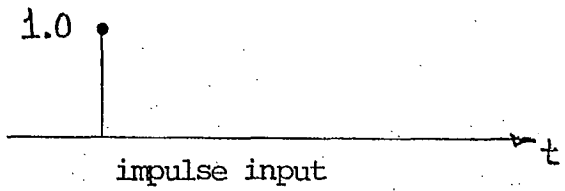
Example A1 In this example the output signal is fed back after one unit delay. A fraction of this signal is used to form the next output sample.

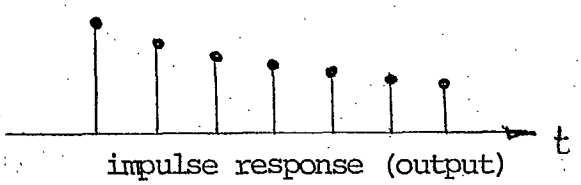


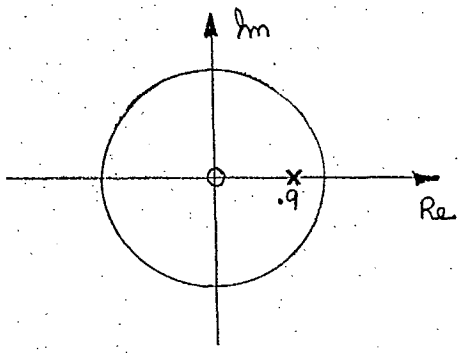

$$Y_{(n)} = X_{(n)} + a_1 Y_{(n-1)}$$

$$H_{(Z)} = \frac{1}{1 - a_1 Z^{-1}}$$

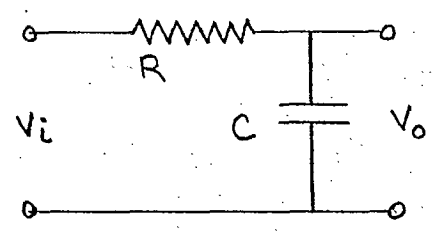
The transfer function, $H_{(Z)}$, becomes infinite when the digital frequency variable $Z = a_1$



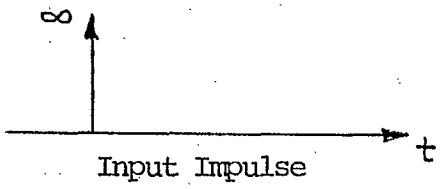

An equivalent circuit for continuous signals is a simple RC network.

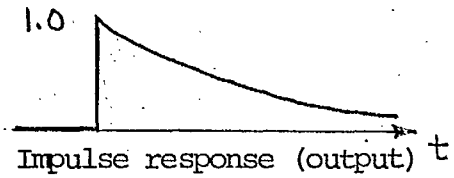


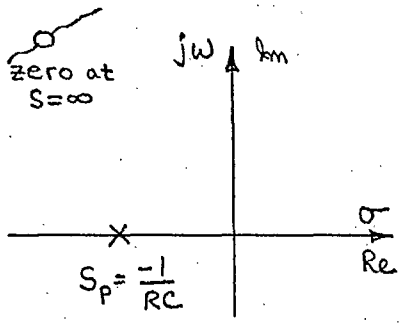

$$N_o = \frac{1}{c} \int i dt = \frac{1}{c} \int \frac{V_o - V_{in}}{R} dt$$

$$H_{(s)} = \frac{V_o(s)}{V_{in}(s)} = \frac{1/sc}{R+1/sc} = \frac{1}{SCR+1}$$

Transfer function $H_{(s)}$ becomes infinite when frequency variable $S = -1/RC$




We can compare the discrete time and continuous time filters as follows

Digital $\quad y_n = y_o\, a_1^{\,n}$

Analog $\quad y_{nT} = y_o\, e^{S_p nT}$

$\Big\}\quad a_1 = e^{S_p T}$

The analog decay time constant $\tau = RC = \frac{-1}{\sigma} = \frac{-1}{S_p}$

The time constant of the digital filter may be developed as follows

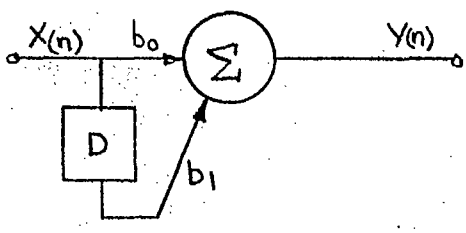
$$S_p = \frac{1}{T} \ln a_1$$

$$\tau = \frac{-1}{S_p} = \frac{-T}{\ln a_1}$$

$$\tau \simeq \frac{T}{1-a_1} \quad \text{if } a_1 \longrightarrow 1 \qquad \text{i.e.: for } a = .9$$

$$\ln a = -.105$$

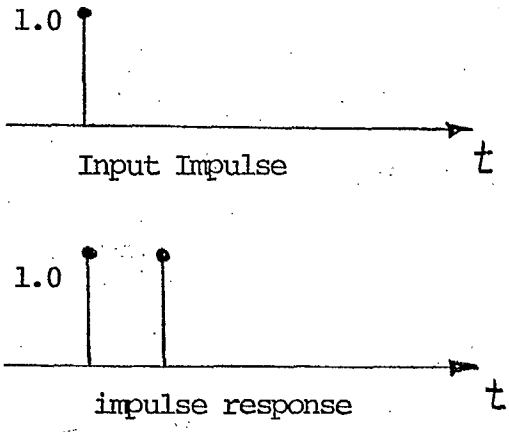
Example A2 The input signal is delayed and added with the new input to form an output.

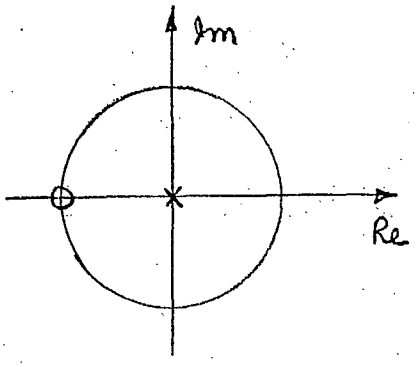



$$Y_{(n)} = b_o x_n + b_1 x_{(n-1)}$$

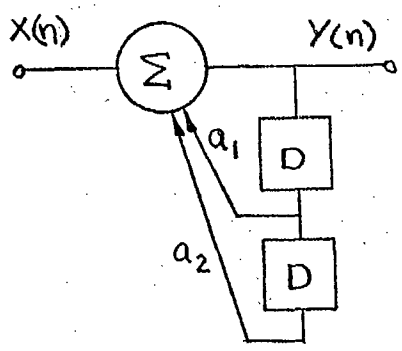
$$H_{(Z)} = 1 + Z^{-1}$$

The transfer function $H_{(Z)}$ becomes zero when the digital frequency variable $Z = -1$. There is a pole at $Z = 0$.




Example A3 Complex poles may be created by using two delays in the output signal.




$$Y_{(n)} = x_n + a_1 Y_{(n-1)} + a_2 Y_{(n-2)}$$

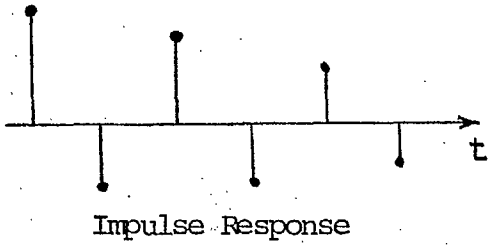
$$X_{(Z)} = Y_{(Z)} \ (1 - a_1 Z^{-1} - a_2 Z^{-2})$$

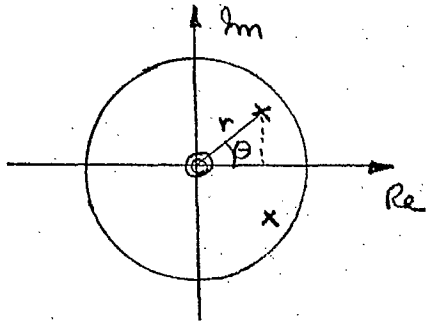
$$H_{(Z)} = \frac{1}{1-a_1 Z^{-1} - a_2 Z^{-2}}$$

Denominator is zero for poles

i.e. $Z = \frac{+a_1}{2} +_{-} \frac{1}{2} \sqrt{a_1^2 + 4a_2}$

For complex poles $a_2$ negative and $|a_2| > (\frac{a_1}{2})^2$



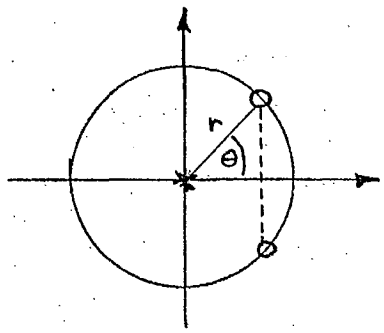

pole at $r/\theta$

where $a_2 = -r^2$

$$a_1 = 2r \cos\theta$$

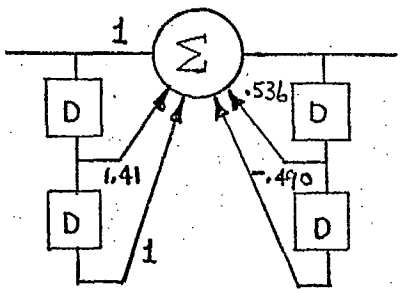
NOTE Complex zeros may be generated by delaying the input then summing.

$$H_{(Z)} = b_o + b_1 Z^{-1} + b_2 Z^{-2}$$




If $b_o = 1$ $\begin{cases} b_2 = r^2 \\ b_1 = -2r\,\text{Cos}\theta \end{cases}$ Then

Example A4 The following section may be used to generate 2 poles and 2 zeros.




Design zeros at 6 $KH_Z$ on the unit circle $\theta = 180^o \pm 45^o$

$r = 1$

pole locations at $-.707 \pm .707$

$a_2 = r^2 = 1$

$a_1 = -2r\text{Cos}\theta = +1.41$

Design poles at 3$KH_Z$ and assume 16 $KH_Z$ sampling $\theta = \frac{3}{16} \times 360^o = 67.5^o$

Let radius vector to pole be .7 to give a pole with moderate Q.

Pole locations, design values are $.268 \pm j.646$

$a_2 = -r^2 = -.49$

$a_1 = 2r\text{Cos}\theta = (1.4)(.382) = .536$

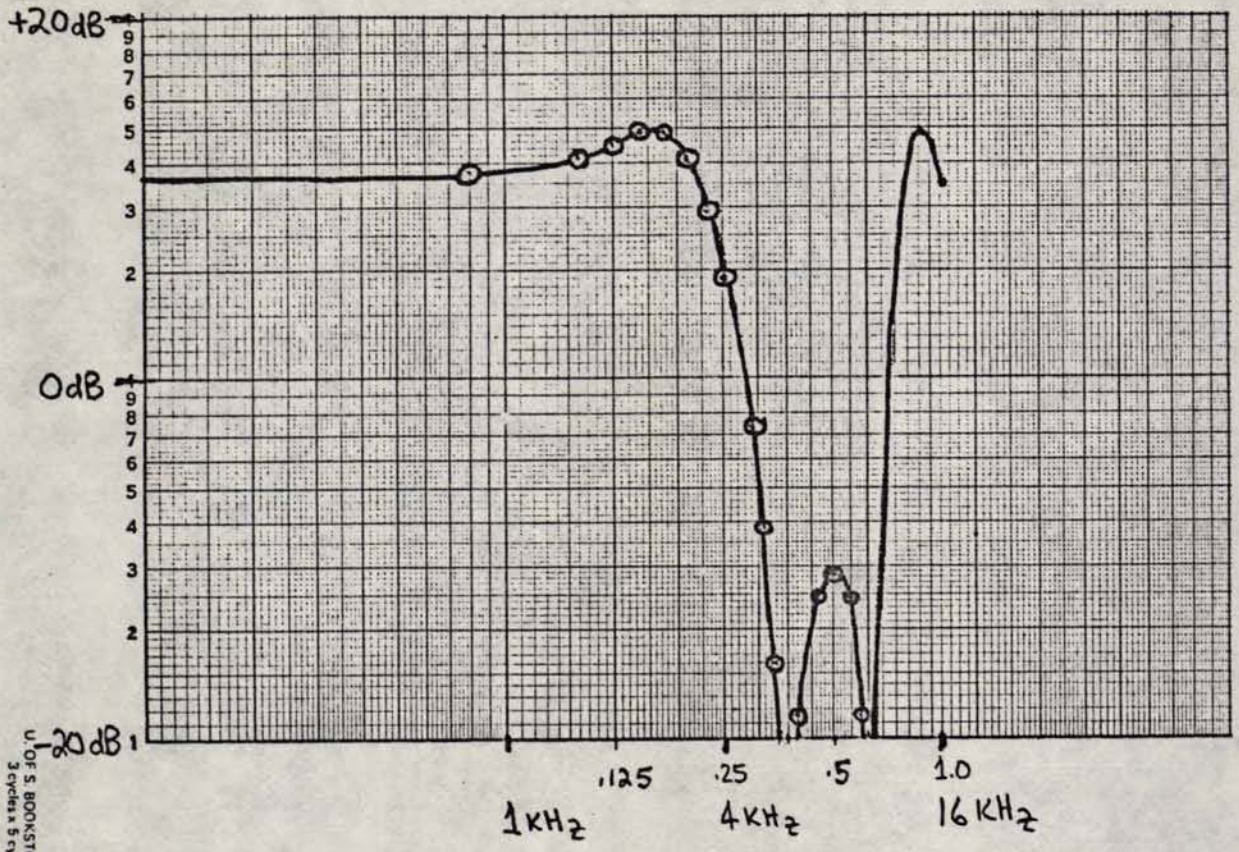
# APPENDIX B

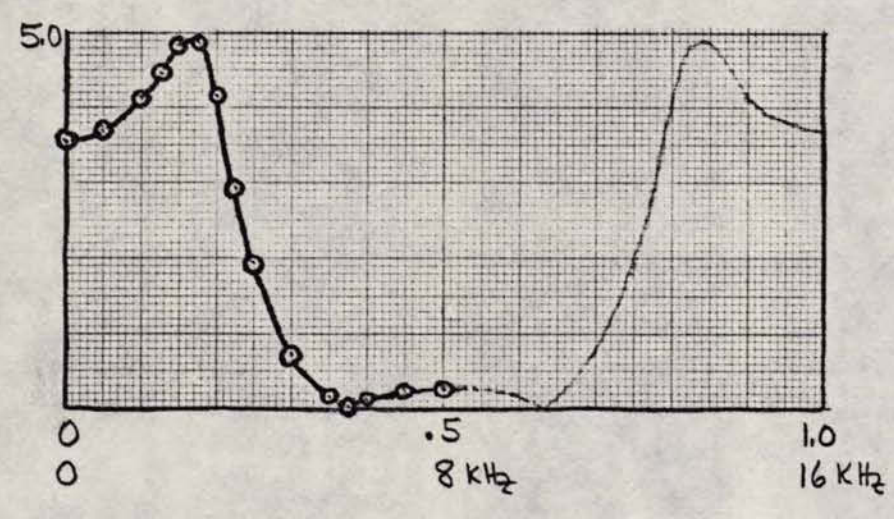
## Computation of Filter Response

The following BASIC program has been written to calculate the response of digital filters. The response in Example A4 has been calculated and graphs have been prepared.

POLE2

```
5 PRINT "ENTER TWO POLES"
10 INPUT P1,P2
25 PRINT "ENTER TWO ZEROS"
30 INPUT Z1,Z2
42 FOR N=1 TO 5
45 PRINT "ENTER NORMALIZED FREQUENCY"
50 INPUT F
60 F1=COS(F*2*π)
70 F2=SIN(F*2*π)
80 PRINT "RE=";F1,"IM=;F2
82 V1=1
84 V2=0
90 A1=P1
95 A2=P2
100 GOSUB 1000
140 A2=-P2
150 GOSUB 1000
160 A1=Z1
170 A2=Z2
180 GOSUB 1100
200 A2=-Z2
210 GOSUB 1100
220 PRINT V1,V2
230 NEXT N
240 END
1000 V1=V1/((F1=A1)↑2+(F2-A2)↑2)↑.5
1010 V2=V2-ATN((F2-A2)/(F1-A1))
1020 RETURN
1100 V1=V1*((F1-A1)↑2+(F2-A2)↑2)↑.5
1110 V2=V2+ATN((V2-A2)/(F1-A1))
1120 RETURN
```


+20dB
0dB
-20dB
.125
.25
.5
1.0
1KHz
4KHz
16KHz
U. OF S. BOOKSTORE
3 cycles x 5 cycle


5.0
0
0
.5
8 KHz
1.0
16 KHz

# INVESTIGATION OF PCM-DELTA CODE CONVERSION

## INTERIM REPORT

July 30, 1980

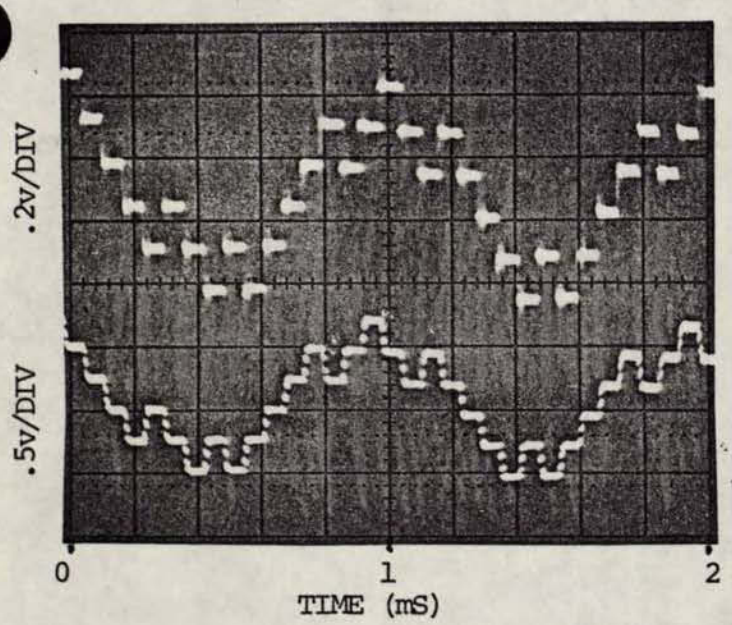
## 1. Introduction

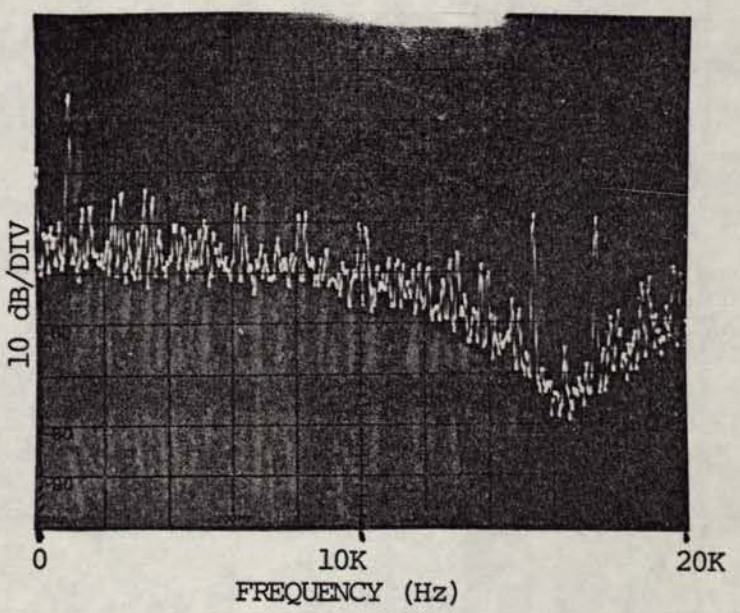
The high noise immunity of digital signals and the low cost of digital circuits promote the transmission of voice in digital form. Pulse code modulation (PCM) is most frequently used to digitize the voice signal. In applications where the bit rate is low or where a noisy channel introduces frequent bit errors an alternate coding scheme known as Delta modulation is often used. Both coding formats are now employed in existing systems. When a system using PCM coding is interfaced to a second system using Delta coding, code conversion is accomplished by decoding to an analog voice signal and re-coding to the other format. The objective of the current work is to develop a totally digital method for interfacing PCM and Delta modulation systems. In particular, it is intended to interface standard CVSD systems with telephone standard CPCM systems. An interface will also be developed for the newly developed EVSD code. The contract defines two tasks: first, a filter implementation study which will define the filter requirements and develop a structure which can be implemented with relative ease; and second, a code converter prototype development which includes filters, accumulators, companders and a PCM interface. The final report is due on March 31, 1981.

## 2. Progress

A two pole, two zero digital filter section has been built in CMOS using serial arthimetic. For the initial measurements the tap coefficients closely approximated those given in example A4 of the OSU 79-00111 Final Report dated March 31, 1980. Spectral analysis of the operating filter shows a frequency response very close to the theorectical prediction. After minor changes in the tap gains, the operation of the filter at 32 KB was verified with spectral and waveform measurements. The following photographs illustrate the filter performance as measured after the serial accumulator. A dual filter section which can be used in the code converter prototype is being constructed on a wire wrap module. Approximately 20 MSI CMOS packages will be used in this dual filter section.

(a) The two following photographs illustrate the unfiltered accumulator output signal with 16 KB sampling and a 1 KHz modulation signal x(t). The lower waveform shows the analog approximate signal $\hat{x}(t)$. The frequency spectrum shows the 1 KHz component at -15 dB and an approximately flat noise spectrum which has a null at the sampling rate of 16 KHz.



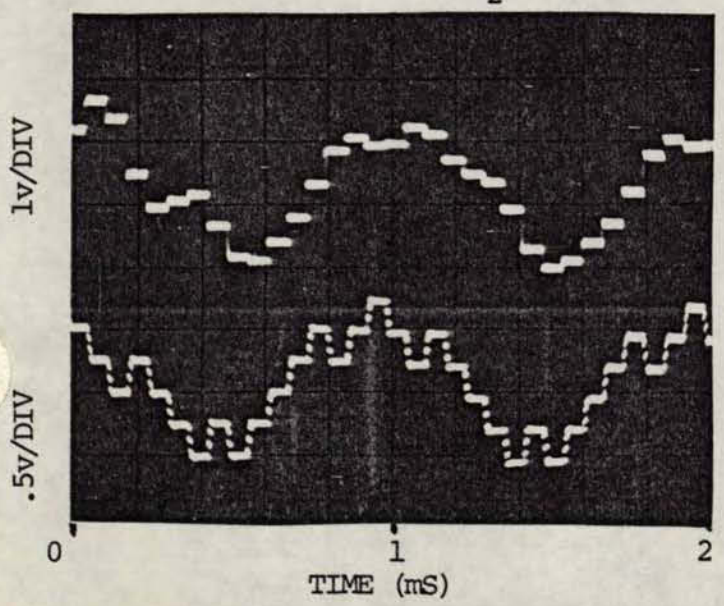



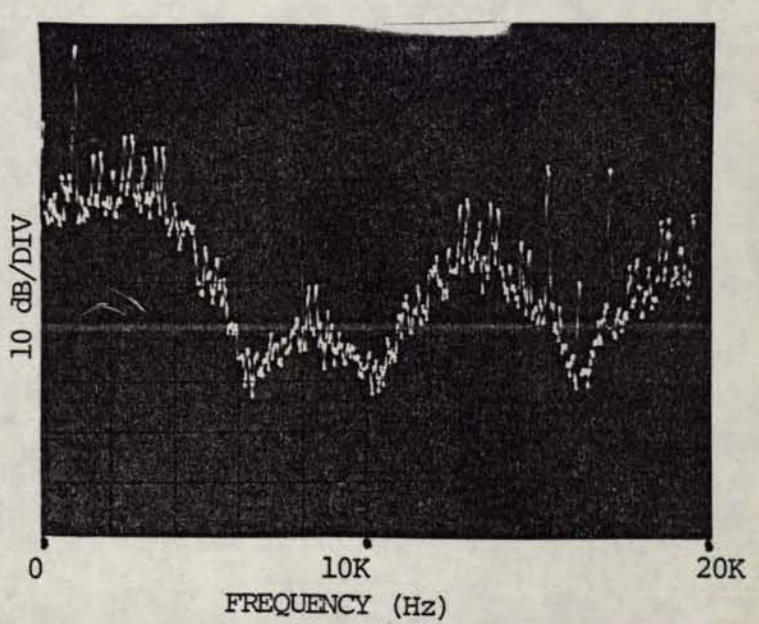

(b) The two photographs below illustrate the accumulator output with digital filtering. The modulation signal and the sampling rate remain at 1 KHz and 16 KHz respectively. The filter has a pole frequency at 6 KHz. The pole has a radius of .707 in the Z plane. The frequency spectrum shows the 1 KHz component at -4 dB, peaking in the noise spectrum at approximately 3 KHz and a null in the noise spectrum at 6 KHz. The filler coefficients are as follows:

$a_1 = +.5$ $\quad b_0 = 1.0$

$a_2 = -.5$ $\quad b_1 = 1.5$

$\quad\quad\quad\quad b_2 = 1.0$



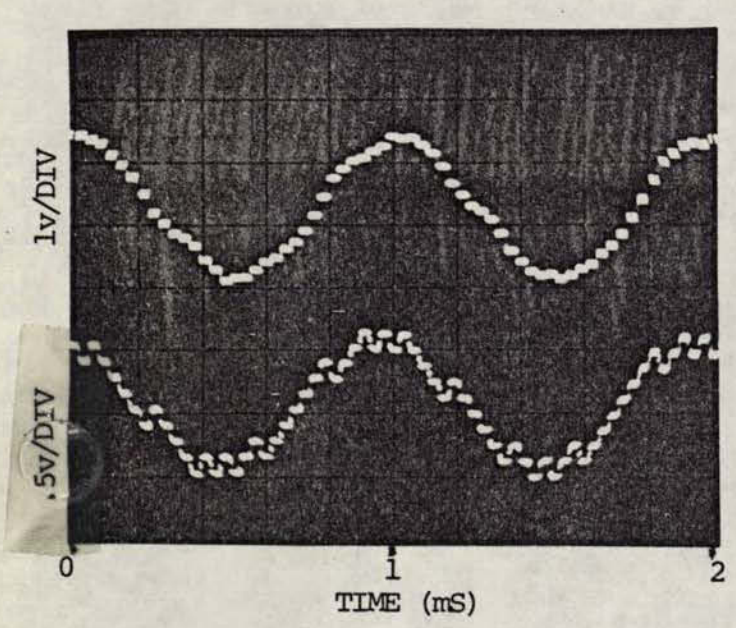



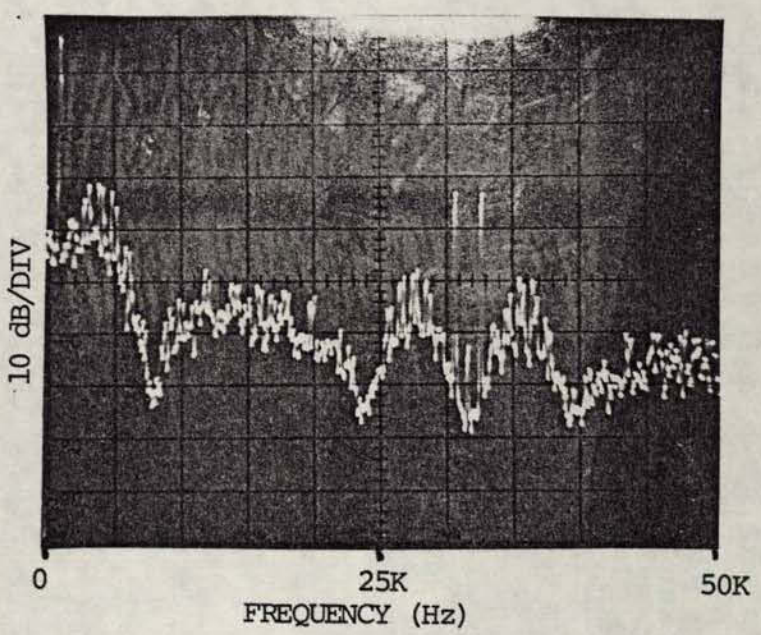
(c) The digital filter was operated at 32 KB and the tap coefficients were changed to provide a pole at 4 KHz and a zero at 8 KHz. Waveforms and output frequency spectrum are shown below. Note the frequency scale has been changed to 5 KHz/division. The filter coefficients are as follows:

$a_1 = 1.0$ $\quad b_0 = 1.0$

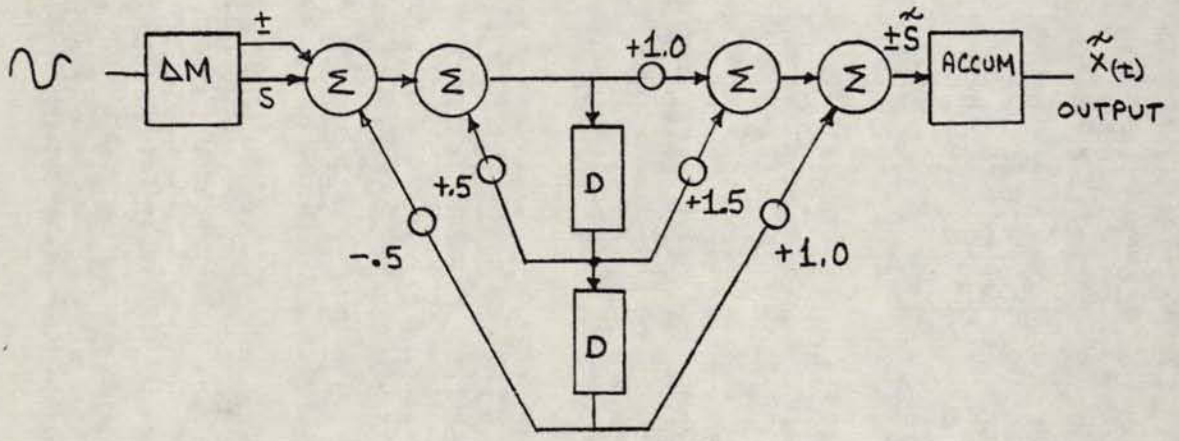
$a_2 = .5$ $\quad b_1 = 0$

$\quad\quad\quad\quad b_2 = 1.0$

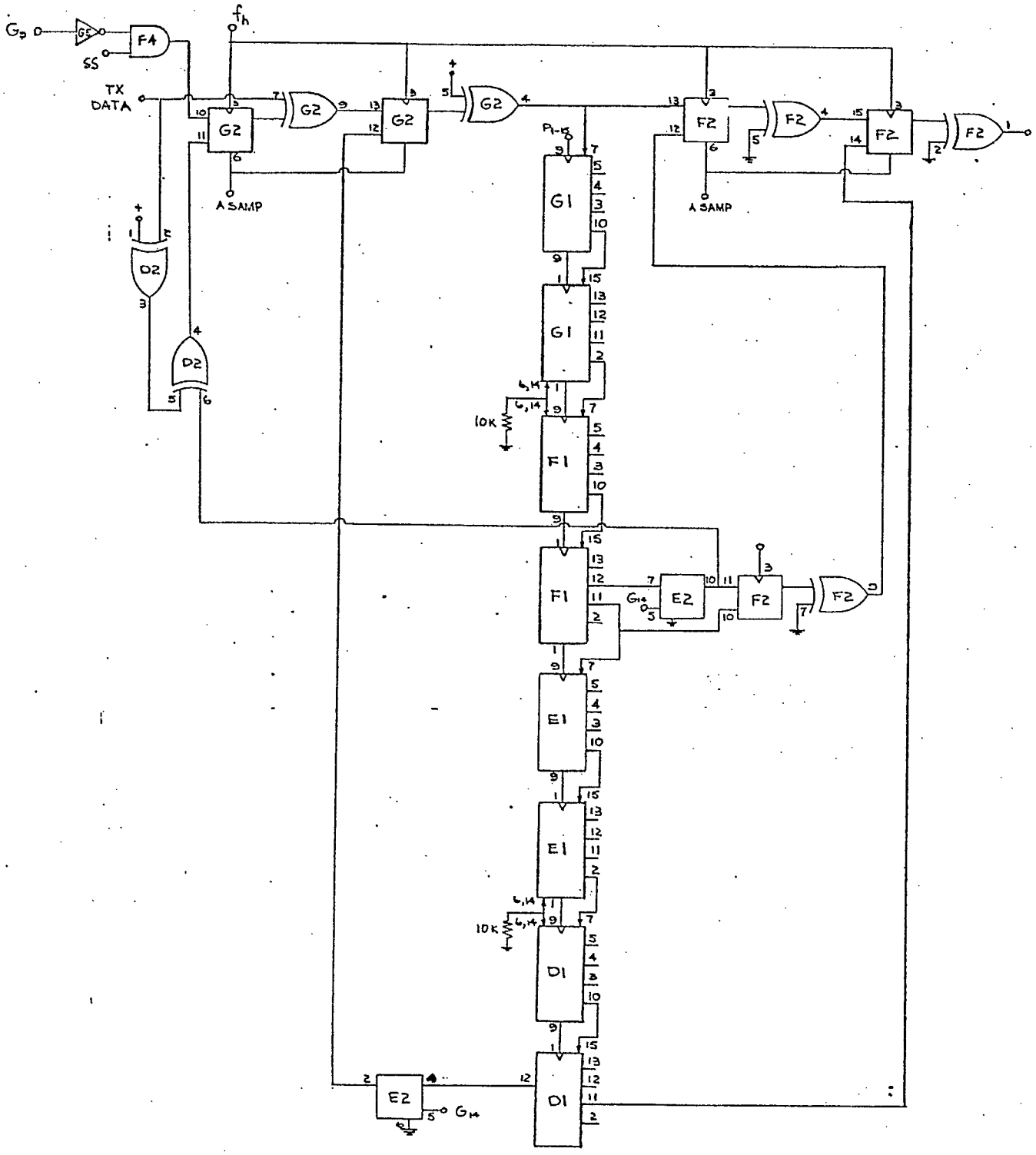


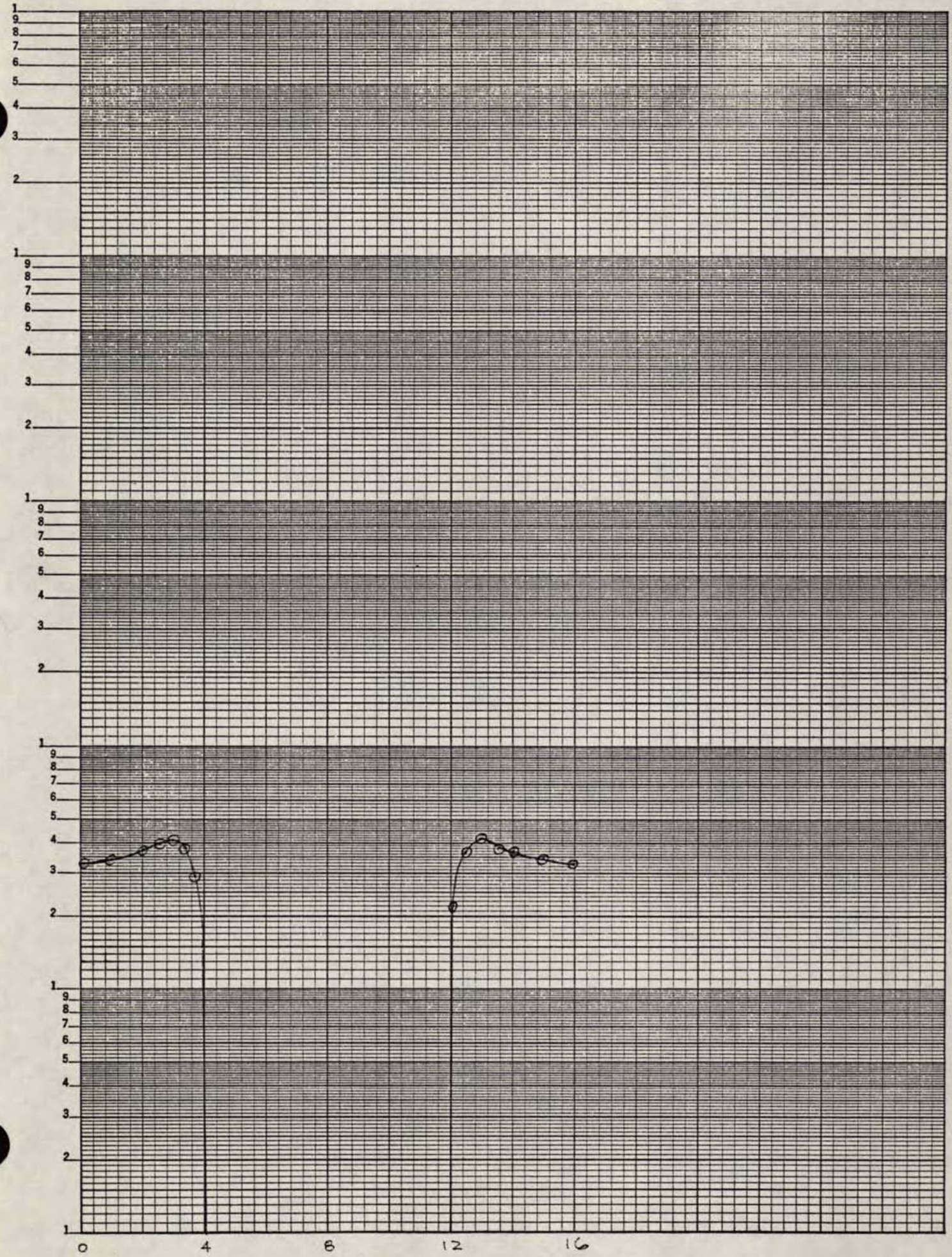




(d) A block diagram of the filter structure is shown below followed by a logic diagram of the filter.



## Logic Diagram of Single Filter Section.




0
4
8
12
16

## 3. Work in Progress

A motorola MC14407 PCM codec has been selected as the interfacing device for PCM. This codec was ordered in early May and should arrive by mid-summer. Several companding circuits are under study, no clear choice is evident at this time.

## 4. Conclusion

Substantial progress has been made achieving the contract goals. A second interim report will be issued in mid-September.