A FIBRE-OPTIC DEVELOPMENT FOR A CANADIAN LAND TACTICAL ENVIRONMENT

D.S.S. FILE NO. 12ST.3200313

CONTRACT SERIAL NO. 2ST81-00032

F.I. REFERENCE NO. 810113

Submitted To: Scientific Authority
Dr. D.C. Johnson
Communications Research Centre
Shirley Bay, Ontario 596-9230

Submitted: April 1983.

FOUNDATION ELECTRONIC INSTRUMENTS INC.
OTTAWA, ONTARIO

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DP 4619480
DL 4619499

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LIST OF ILLUSTRATIONS

EXECUTIVE SUMMARY

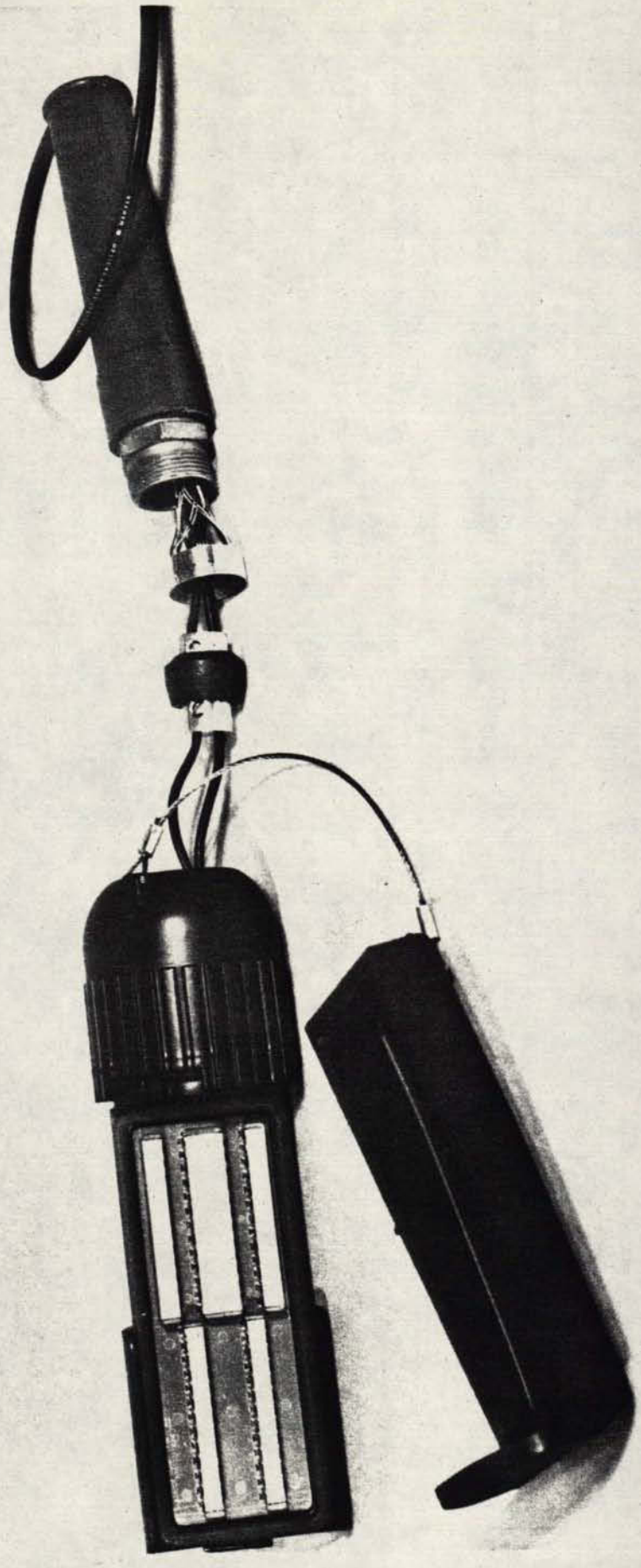
As part of the contracted deliverables, this Final Report containing drawings and equipment documentation is submitted. Environmental and mechanical test results are excluded as they form part of the LETE generated final acceptance report.

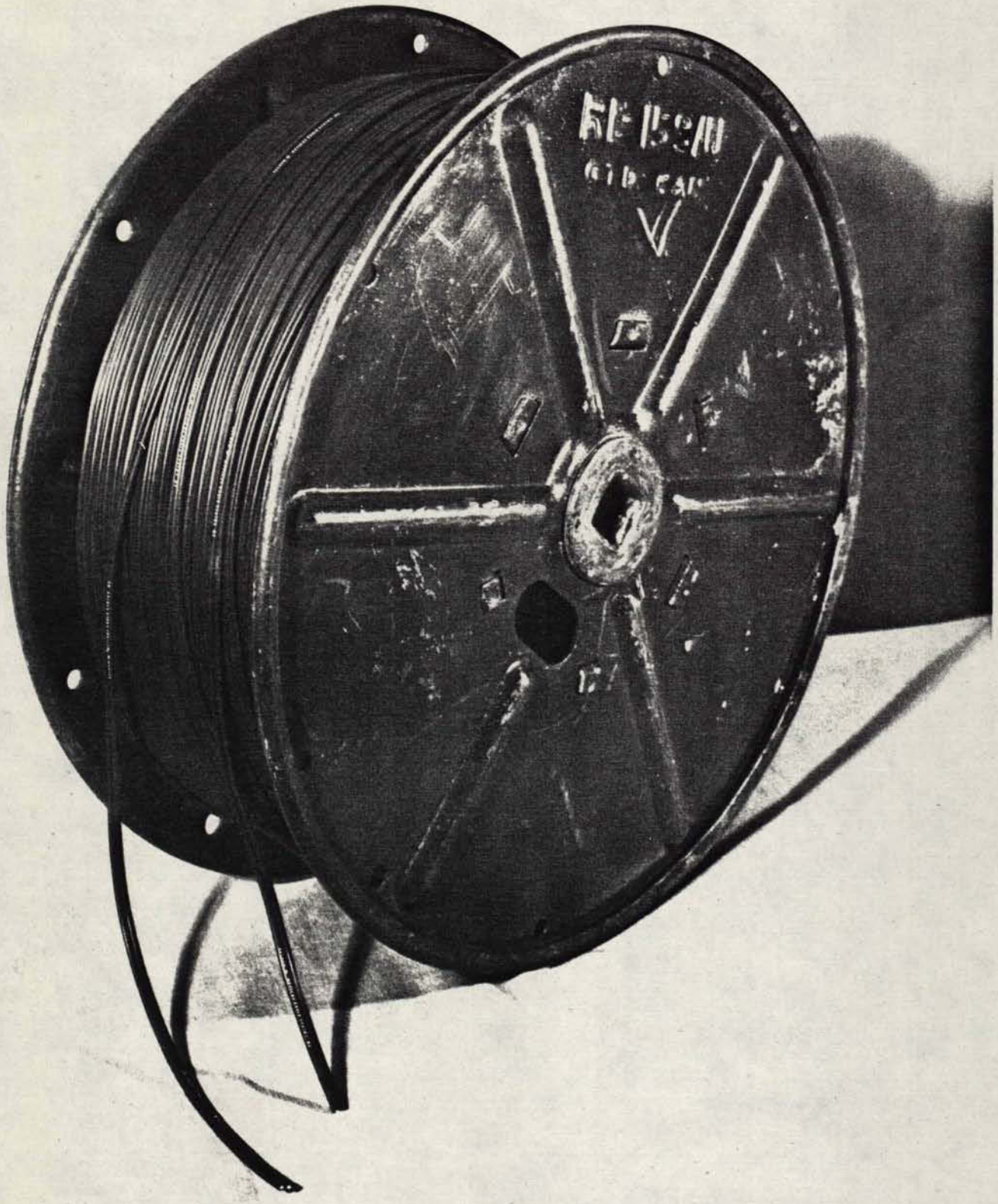
The following CEE article reprint is included as part of the executive summary.

FIBRE OPTICS IN A CANADIAN MILITARY LAND TACTICAL ENVIRONMENT

by P.C. Wheeler and R.J. McCauley

The Canadian Department of National Defence (D.N.D.) recognizes that the introduction of fibre-optic technology in land tactical communications can overcome several practical difficulties which exist with the present system. The effectiveness of the Land Tactical Area Communications System (LTACS) is limited by the interconnecting metallic cables. These cables, in addition to being heavy and bulky, are susceptible to Electro-Magnetic Interference (EMI), ground loop problems and Electro-Magnetic Pulse (EMP). Conversely, fibre-optic cables which are thinner, lighter and more flexible than their copper equivalents, are unaffected by electrical interference and can be made immune to nuclear radiation effects. In addition, optical fibres have wide bandwidths and low loss, thus allowing for greater spans of communications without the need for repeaters.





To evaluate the tactical fibre-optic capability, Foundation Instruments of Ottawa was contracted by D.N.D. to supply a prototype fibre optic system which would replace the existing weight and distance limited CX-4566 A/G 26-pair copper cable assembly. The resulting development is a 2 fibre cable without repeaters coupled with the electronic and opto-electronic circuitry necessary to interface with the operational LTACS equipment.

The existing cable assembly consists of a 26-pair copper cable (WM-130A/G), with each end of the cable terminated by a U-185 B/G electrical connector. Externally located on the telecommunication equipment shelters are signal input panels to which the electrical connectors mate. This configuration allows for the simultaneous transmission of twelve 4-wire data or voice channels. The effective fibre optic replacement for this existing parallel transmission scheme involves a parallel to serial conversion of the electrical signals. The conversion results in two time division multiplexed data channels operating one in each direction through the two-fibre cable. Such a conversion is implemented by first sampling then multiplexing the input signals. The resulting multiplexer output is a digital data stream at a data rate of 4.0 Megabits. To demonstrate the wide bandwidth of the fibre channels, a two way video link is provided. The data stream is combined with the video signal then applied to the modulator. The modulator output is a Phase Shift Keyed 12 Megahertz data carrier which is located above the baseband video frequency signal. The modulator in conjunction with the optical source converts the electrical signal to an optical signal which is applied to the fibre link. At the receiving end the optical signal is detected and converted to an electrical signal by the photodetector and demodulator. The demodulated signal is separated into the video signal and the data stream. The data stream is demultiplexed into the separate output channels. The multiplexer modulator/demodulator demultiplexer (muldem) is a custom design located in the confined space of the signal input panel.

The system is symmetrical. The muldems permit the bi-directional operation of combinations of up to twenty-four digital and analog signals in conjunction with the television channels. The digital signals are of the Military Standard 188C format up to a maximum input data rate of 19.2 kilobits/sec. The analog signals are bandwidth limited to four kilohertz and digitized with delta codecs. The baseband video channel, which employs automatic gain control (AGC), meets the transmission criteria of Broadcast Practice 23.

Because of the difficulties involved in the use of optical connectors in dirty and wet field conditions, external optical interconnects are avoided. The adapted approach employs an internally modified U-185 B/G housing to mount the optical transmitter and optical receiver circuitry. As a result, the connection between the signal input panel on the communications vehicle and the connectorized fibre cable is electrical. The present electrical contacts are used to interface the combined information signals and to feed power to the light emitting diode transmitter and p.i.n. diode receiver. The present design uses the signal input panel to enclose the power supplies and electronic circuit cards which comprise the muldems and delta codec interfaces. According to Attila J. Szanto, President of Foundation Instruments, "A muldem assembly, based on the U-185 B/G connector, yet powered externally from the equipment shelter, is under development. The assembly is contained in a custom packaged connector housing and designed for full military mechanical and environmental durability. This development will allow the co-existence of the old copper wire investment with the new glass fibre technology."

The Belden "Bitlite" fibre cable supplied by White Radio meets the mechanical requirements imposed by the system design. Each fibre in the cable is individually reinforced and jacketed together into a parallel duplex construction. The outer diameter of the flame retardant polyurethane

jacket is 3.0 millimeters by 6.2 millimeters. The RL79 cable reels which accommodate 76 meters of 26-pair copper cable now hold 1000 meters of the Bitlite fibre cable. This drastic size reduction requires a build-out plug at the connector attachment to maintain the hermetic seal. The acrylate composite coated fibres in a tight buffer cable design are suitable for the field conditions encountered during deployment and recovery. Although complete military durability is not expected for this evaluation, the Bitlite has a documented performance consistent with the intended use.

The first generation system is part of a continuing development effort of both industry and the military working closely together to achieve reliable and efficient tactical fibre optic communications.

1.0 INTRODUCTION

This document contains the theory of operation and set-up procedures required to evaluate the "Fibre-Optic Development for a Land Tactical Environment". This document is the final report required under contract deliverables.

REVISIONS		
REV	DATE	DESCRIPTIONS
E	83-03-16	DESIGN CHANGE W.O. # 2417

DATA INPUT FROM MULTIPLEXER

DATA IN GND

VIDEO COMMON

VIDEO IN SIGNAL (75Ω)

TRANSMITTER D.C. MONITOR SIGNAL INPUT

+12V REGULATED (ANALOG)

-12V REGULATED (ANALOG)

+12V GND (ANALOG)

+5V REGULATED (DIGITAL)

-12V REGULATED (DIGITAL)

+5V GND (DIGITAL)

CLOCK OUTPUT TO MULTIPLEXER

MULTIPLEXER CLOCK GND

OUTPUT SIGNAL TO TX

OUTPUT SIGNAL GND

NOTE

1) L1, L2, L3, L4, L10, L11, L22 ARE FERROXCUBE #VK200-20/4B

2) EDGE CONNECTOR CONTACTS 79, 76, 81, 82 ARE CONNECTED TO DIGITAL GND (G3)

3) EDGE CONNECTOR CONTACTS 11, 12, G3, G4 ARE CONNECTED TO ANALOG GND (G1)

4) R44 REMOVED FOR NORMAL OPERATION

LAST NO. USED	
IC6	
R82	
RV7	
C78	
Q8	
Z2	
Y1	
L23	VR2
TP44	M1

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES
MATERIAL:
FINISH:

FOUNDATION INSTRUMENTS OTTAWA

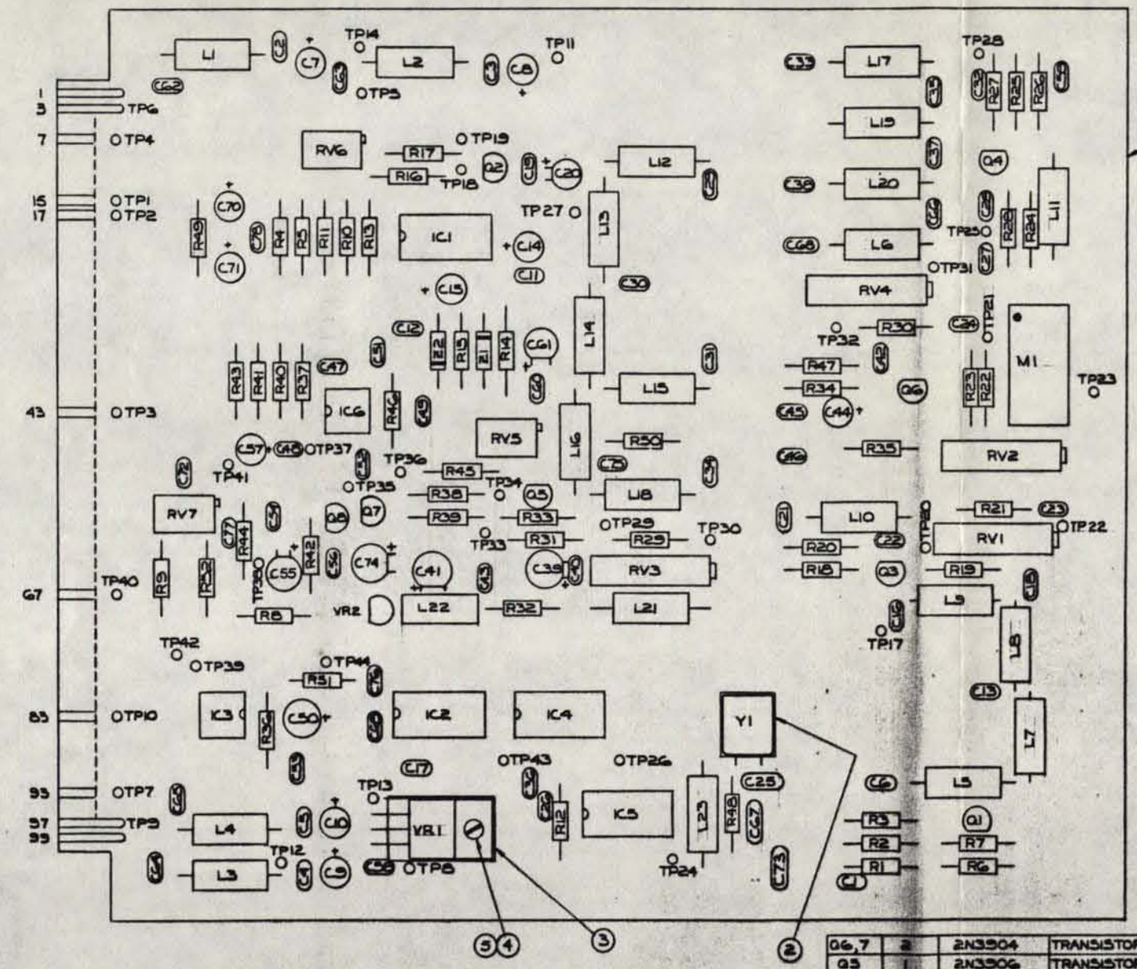
DATE: 82-04-27 | PROJ. NO: 810113 | DRAWN BY: J.WHITEMAN

LAND TACTICAL DATA & VIDEO TX - SCHEMATIC

SCALE: | SHEET OF

APPROVAL: | DWG NO: # D2201

REV	DATE	DESCRIPTIONS
A	83-03-16	DESIGN CHANGE W.O # 2417



NOTE: C65, C74, C41, C39, C61, C20 & Y1 TO BE MOUNTED FLAT ON P.C.B.

ITEM	QTY	PART NO.	DESCRIPTION	
TP1-44	44	2137-D	TEST POINT	VERO
Y1	1	183025	CRYSTAL, 12.000 MHZ	CTS OF CANADA
L23	1	1537-20	COIL 2.2μH	DELEVAN
L21	1	1537-12	1μH	DELEVAN
L19	1	1537-34	8.2μH	
L15	1	1537-26	3.9μH	
L14	1	1537-52	33μH	
L13,16	2	1537-48	27μH	
L12,18	2	1537-42	18μH	
L7,8,20	3	1537-36	10μH	
L6,17	2	1537-44	22μH	
L5,9	2	1537-32	COIL 6.8μH	DELEVAN
L10,11,22 L2,3,4	7	W200-20/48	WIDE BAND CHOKE	FERROXCUBE
5	1	HU-5001	NUT, SCREW, HEX. MACHINE, 4-40	SP-NR.
4	1	MS-5007	SCREW MACH., NYLON, 4-40 x 3/8	SP-NR.
3	A/R		MICA WASHER	
E1,2	2	IN5233	ZENER DIODE	

ITEM	QTY	PART NO.	DESCRIPTION	
Q6,7	2	2N3904	TRANSISTOR	
Q5	1	2N3906	TRANSISTOR	
Q4,8 Q1,2,3	5	2N5770	TRANSISTOR	
C26	1	CKO5BX331K	CAPACITOR, 330pF, NPO CERAMIC	AVX
C78	1	638-10829	CAPACITOR, 82pF, CERAMIC	PHILIPS
C73	1	CKO5BX121K	120pF, NPO CERAMIC	AVX
C72	1	630-03331	330pF, CERAMIC	PHILIPS
C69	1	630-03102	1000pF, CERAMIC	PHILIPS
C57	1	TAP6.8M16	6.8μF, 16WVDC, TANTALUM	ITT
C52	1	3439-050E-103M	.01μF, CERAMIC, 50V	AVX
C48	1	SR305C684KAA	0.68μF, CERAMIC	AVX
C47	1	630-03181	180pF, CERAMIC	PHILIPS
C38	1	638-34151	150pF, CERAMIC	PHILIPS
C35,37	2	638-10188	18pF, CERAMIC	PHILIPS
C33, 68	2	638-10479	47pF, CERAMIC	PHILIPS
C31,77	2	638-10689	68pF, CERAMIC	PHILIPS
C28,34,66	3	638-10229	22pF, CERAMIC	PHILIPS
C41,61,74	3	TAP100M16	100μF, 16WVDC, TANTALUM	ITT
C20,39,55	3	TAP100M10	CAPACITOR, 100μF, 10WVDC, TANTALUM	ITT

ITEM	QTY	PART NO.	DESCRIPTION	
C67	1	CKO5BX470K	CAPACITOR, 47pF, NPO CERAMIC	AVX
C13	1	638-10399	CAPACITOR, 39pF, CERAMIC	PHILIPS
C70,71 C44,50 C10,14,15 C7,8,9	10	TAP10M16	10μF, 16WVDC, TANTALUM	ITT
C6,16	2	638-10129	12pF, CERAMIC	PHILIPS
C76,72 C65,75 C62,63,66 C58,59,60 C53,54,56 C46,49,51 C42,43,45 C32,36,40 C26,27,28 C22,23,24 C18,19,21 C11,12,17 C1,2,3,4,5	39	3439-050E-104M	CAPACITOR, 0.1μF, 50V, CERAMIC	AVX
RV7	1	3299P-1-203	VARIABLE RESISTOR, 20KΩ	BOURNS
RV6	1	3299P-1-101	100Ω	BOURNS
RV5	1	3299P-1-501	500Ω	BOURNS
RV3,4	2	3006P-1-202	2KΩ	BOURNS
RV2	1	3006P-1-203	20KΩ	BOURNS
RV1	1	3006P-1-101	VARIABLE RESISTOR, 100Ω	BOURNS
R50	1		RESISTOR, 180Ω, 1/4W, ±5%	
R49	1		75Ω	
R48	1		390Ω	
R43,45 R37,41	4		100KΩ	
R9 R34,47	3		4.7KΩ	
R33,42	2		100Ω	
R17	1		330Ω	
R31	1		3.3KΩ	
R28,39	2		120Ω	
R25	1		3.9KΩ	
R24	1		51Ω	
R20	1		270Ω	
R18	1		1.8KΩ	
R21 R14,15	3		150Ω	
R3	1		2.2KΩ	
R10,6,27	3		680Ω	
R12	1		10Ω	
R26,40 R10,11,13	5		1KΩ	
R23,36 R22	5		220Ω	
R8,35,38	3		470Ω	
R6,7,1	3		560Ω	
R4,5,46 R32	4		10KΩ	
R2,44,51,52	4		2.7KΩ	
R29,30	2		RESISTOR, 1.2KΩ, 1/4W, ±5%	
VR2	1	78L10	VOLTAGE REGULATOR, +10V	
VR1	1	7905	VOLTAGE REGULATOR, -5V	
M1	1	MCL5RA-1	DOUBLE BALANCED MIXER	MINI-CIRCUITS
IC6	1	CA3140	INTEGRATED CIRCUIT	
IC4	1	74LS73		
IC3	1	75451		
IC2,5	2	74LS00		
IC1	1	733	INTEGRATED CIRCUIT	
2	A/R		DOUBLE SIDED MOUNTING TAPE	
1	1	#2202	INTEGRATED CIRCUIT	FI

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: XX ±.010
.XXX ±.005
ANGLES 1/2°
SURFACES:
REMOVE BURRS | SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

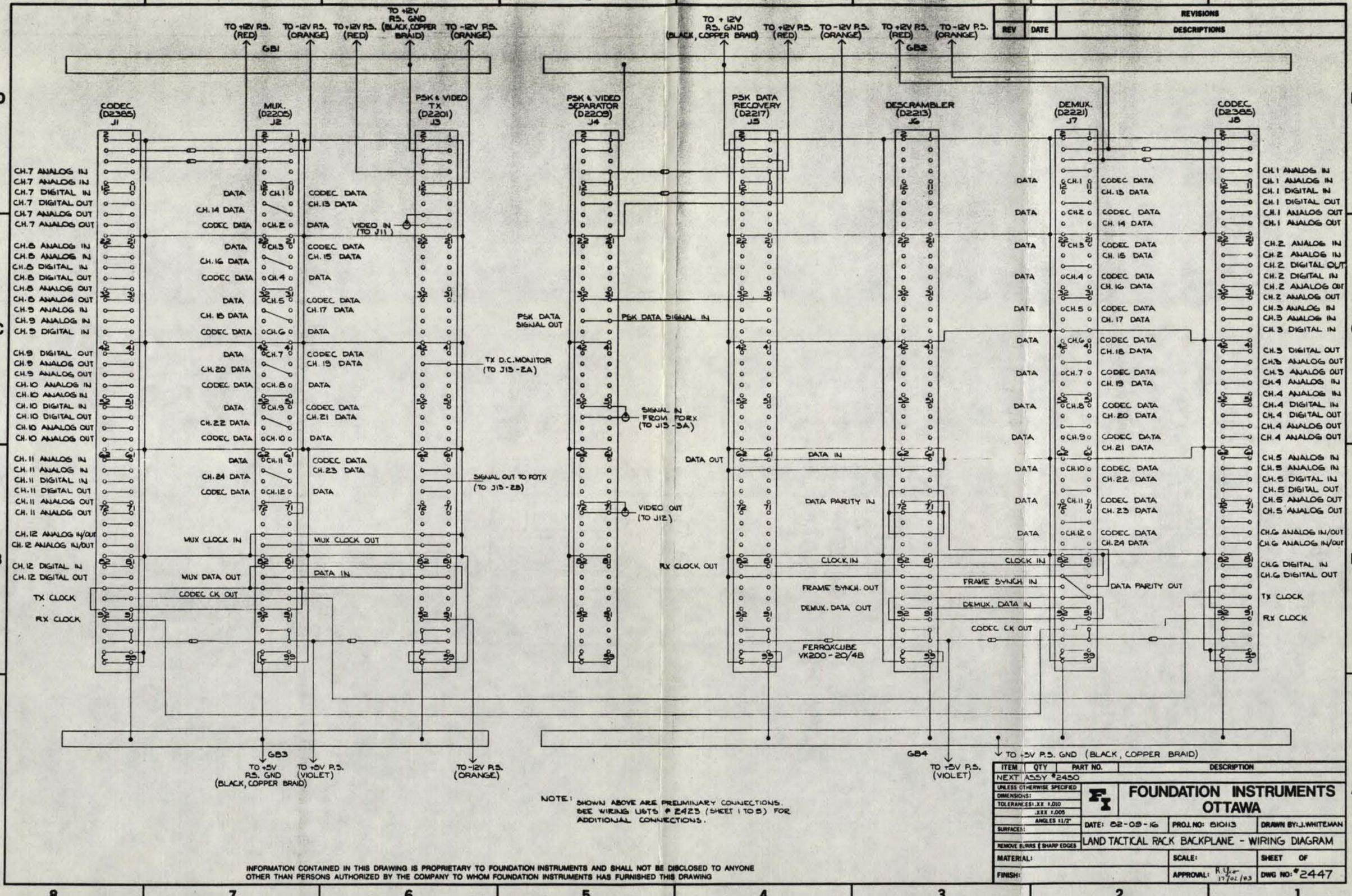
DATE: 82-09-21 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

LAND TACTICAL DATA & VIDEO TX-COMP. LAYOUT

MATERIAL: | SCALE: 2/1 | SHEET OF

FINISH: | APPROVAL: R. Ure 04/02/83 | DWG NO: #2203

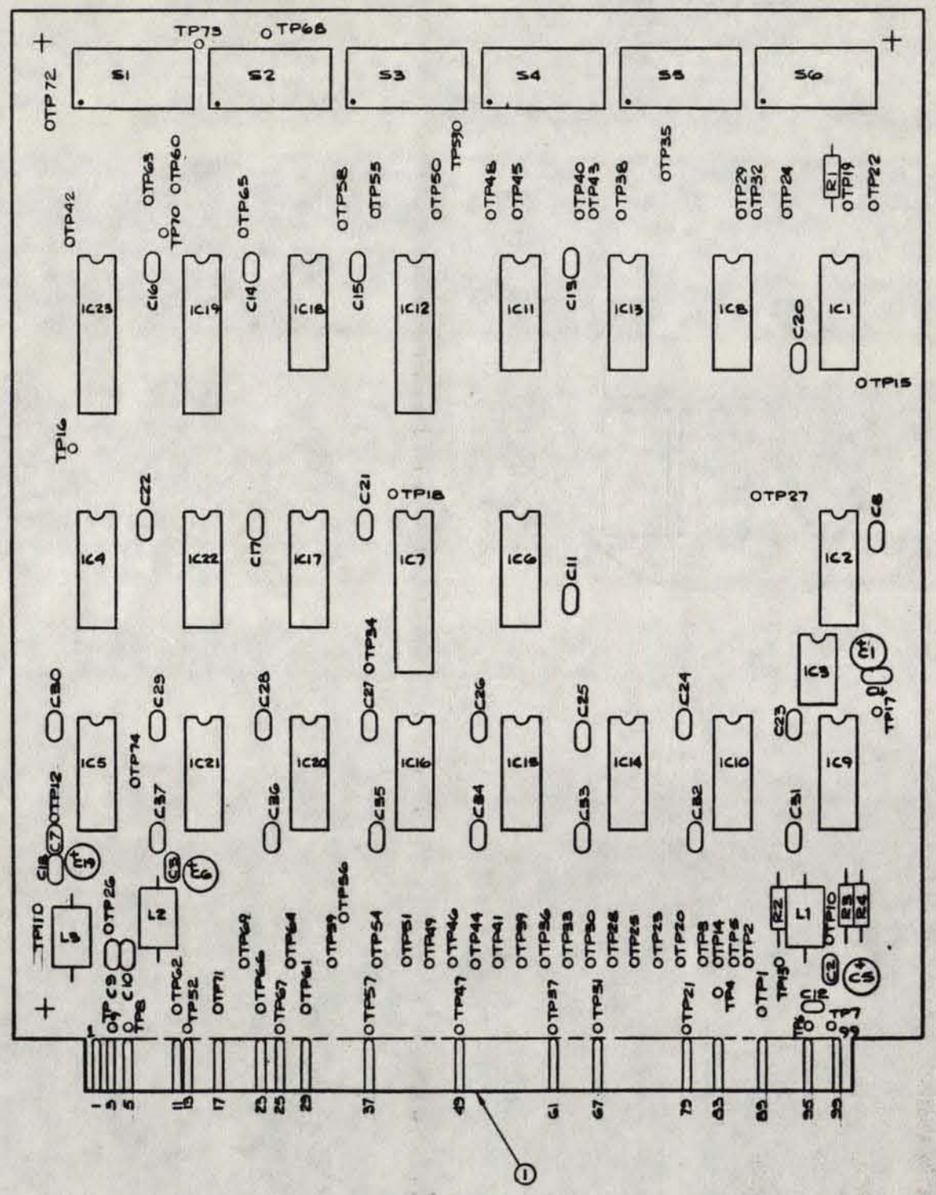
REV	DATE	REVISIONS / DESCRIPTIONS



NOTE: SHOWN ABOVE ARE PRELIMINARY CONNECTIONS. SEE WIRING LISTS # 2423 (SHEET 1 TO 5) FOR ADDITIONAL CONNECTIONS.

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY # 2450			

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010, .XXX ±.005, ANGLES ±1/2°	FOUNDATION INSTRUMENTS OTTAWA		
SURFACES:	DATE: 82-09-16	PROJ. NO: 810113	DRAWN BY: J. WHITEMAN
REMOVE BURRS & SHARP EDGES	LAND TACTICAL RACK BACKPLANE - WIRING DIAGRAM		
MATERIAL:	SCALE:		SHEET OF
FINISH:	APPROVAL: R Uzer 17/01/83		DWG NO: # 2447



REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-09-30	DOCUMENTATION CHANGED W.O.# 2311
B	82-10-26	DESIGN CHANGE W.O.# 2340

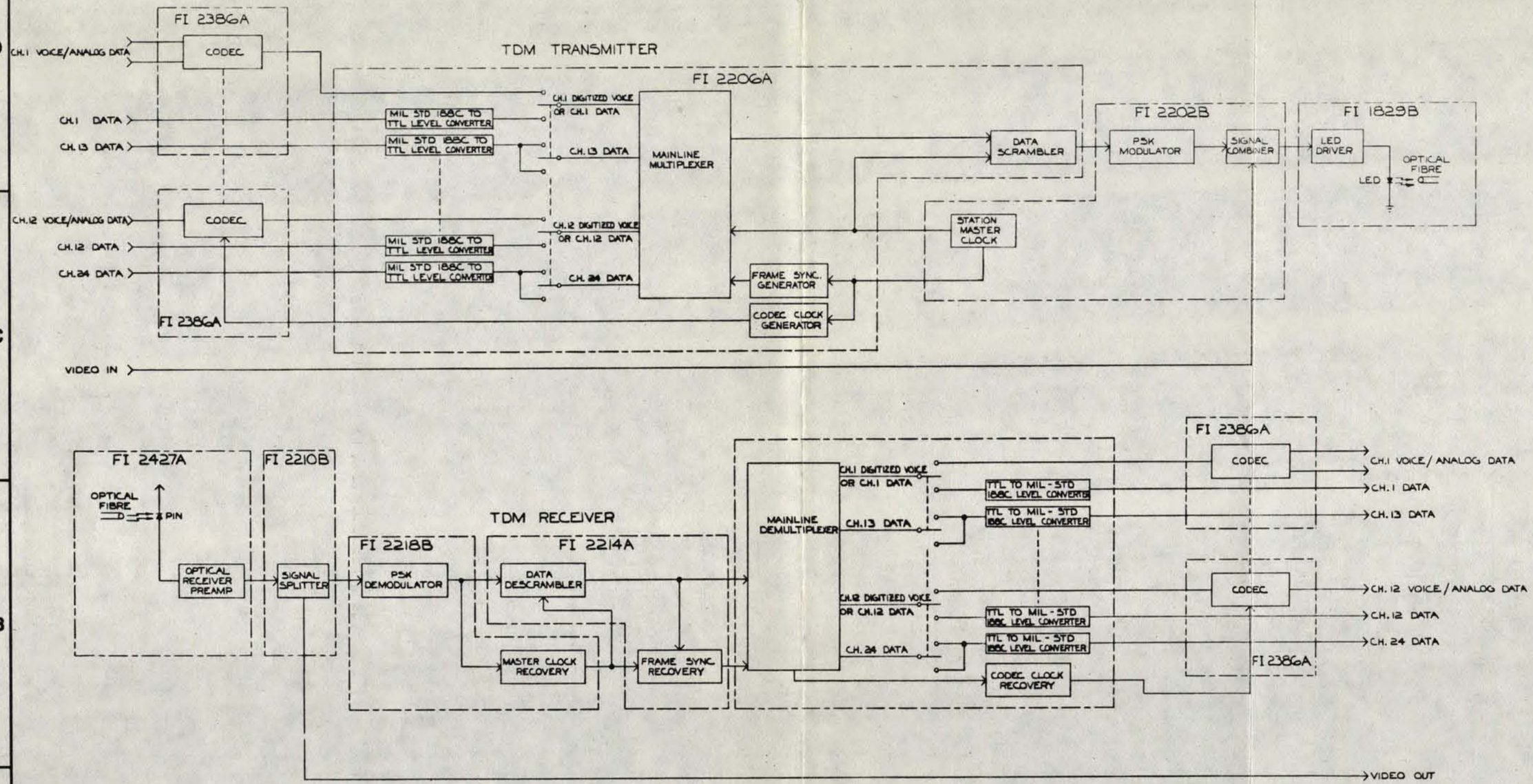
ITEM	QTY	PART NO.	DESCRIPTION	
TP1-74	74	20-2137D	TEST POINT	VERO
S4,5,6 S1,2,3	6	76STD02	SWITCH, DIP, TOGGLE, DPDT	GRAYHILL
L1,2,3	3	VK200-20/4B	COIL	FERROXCUBE
C9,10 C7,12 C35,36,37 C32,33,34 C29,30,31 C26,27,28 C23,24,25 C20,21,22 C16,17,18 C13,14,15 C8,11 C2,3,4	39	3439-050E-104M	CAPACITOR, 0.1μF, 50V, CERAMIC	AVX
C19 C1,5,6	4	TAP10M16	CAPACITOR, 10μF, 16V, TANTALUM	ITT
R4 R1,2,3	4		RESISTOR, 220Ω, 1/4W, ±5%	
IC21,5 IC15,16,20 IC9,10,14	8	9616	INTEGRATED CIRCUIT	
IC17,4 IC8,13	4	74LS04		
IC19,23 IC7,12	4	74LS377		
IC18,22 IC6,11	4	74LS164		
IC3	1	75451		
IC2	1	74LS74		
IC1	1	7400	INTEGRATED CIRCUIT	
1	1	*2222	PRINTED CIRCUIT BOARD	FI

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-09-07	PROJ. NO: 810113	DRAWN BY: L.WHITEMAN
	LAND TACTICAL DATA DEMULTIPLEXER - COMP. LAYOUT		
MATERIAL:		SCALE: 2/1	SHEET OF
FINISH:		APPROVAL: K. Uhr 09/02/83	DWG NO: *D2223

DATA LIST	FI	FOUNDATION INSTRUMENTS OTTAWA			DWG NO. 2425	REV.
APPROVAL	CONTRACT NO.	CONTRACT CANADIAN LAND TACTICAL			SHEET 3 OF 3	DATE

CODE IDENT.	DWG. SIZE	DWG NO.	SHEET NO	REV.	TITLE	DESCRIPTION	RELEASE DATE
	C	2388			DUPLEX TX VOICE CIRCUIT	MASTER	
	D	2389			FO/RX SHIELD	MECH.	
	A	2423			WIRING (PARTIAL)	LIST	
	A	2425			CDN LAND TACTICAL	DATA LIST	
	A	2426			F/O RX MODULE	SCHEMATIC	
		2427		A	F/O RX MODULE	ARTWORK	
	C	2428			F/O RX MODULE	COMP. LAY.	
	C	2429			F/O RX MODULE	MASTER	
		2431			AUDIO INTERFACE - 4 WIRE	ARTWORK	
	C	2432			AUDIO INTERFACE - 4 WIRE	COMP. LAY.	
	C	2433			AUDIO INTERFACE - 4 WIRE	MASTER	
		2435			AUDIO INTERFACE - 2 WIRE	ARTWORK	
	C	2436			AUDIO INTERFACE - 2 WIRE	COMP. LAY.	
	C	2437			AUDIO INTERFACE - 2 WIRE	MASTER	
	D	2447			BACK PLANE WIRING	DIAGRAM	
OBSOLETE	C	2515		B	CDN LAND TACTICAL TX/RX	SCHEMATIC	
OBSOLETE	C	2516			CDN LAND TACTICAL TX/RX	ARTWORK	
OBSOLETE	C	2518			CDN LAND TACTICAL TX/RX	MASTER	
	C	2588			POWER SUPPLY	SCHEMATIC	
	C	2589			POWER SUPPLY	PARTS LIST	
	D	1710		A	SYSTEM DIAGRAM	DIAGRAM	

REVISIONS		
REV	DATE	DESCRIPTIONS
A	83-01-13	DESIGN CHANGE



NOTES
1) NUMBERS REFER TO PRINTED CIRCUIT BOARD ARTWORKS.
2) CODEC BOARDS FI 2386A HAVE 6 CHANNELS EACH. CHANNELS 6 & 12 HAVE TWO-WIRE INPUTS AND OUTPUTS ALL OTHER CHANNELS HAVE FOUR-WIRE INPUTS AND OUTPUTS.

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FI **FOUNDATION INSTRUMENTS OTTAWA**

DATE: 82-08-04 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

CANADIAN LAND TACTICAL ENVIRONMENT - SYSTEM DIA

MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: | DWG NO: 1710

REV	DATE	REVISIONS / DESCRIPTIONS

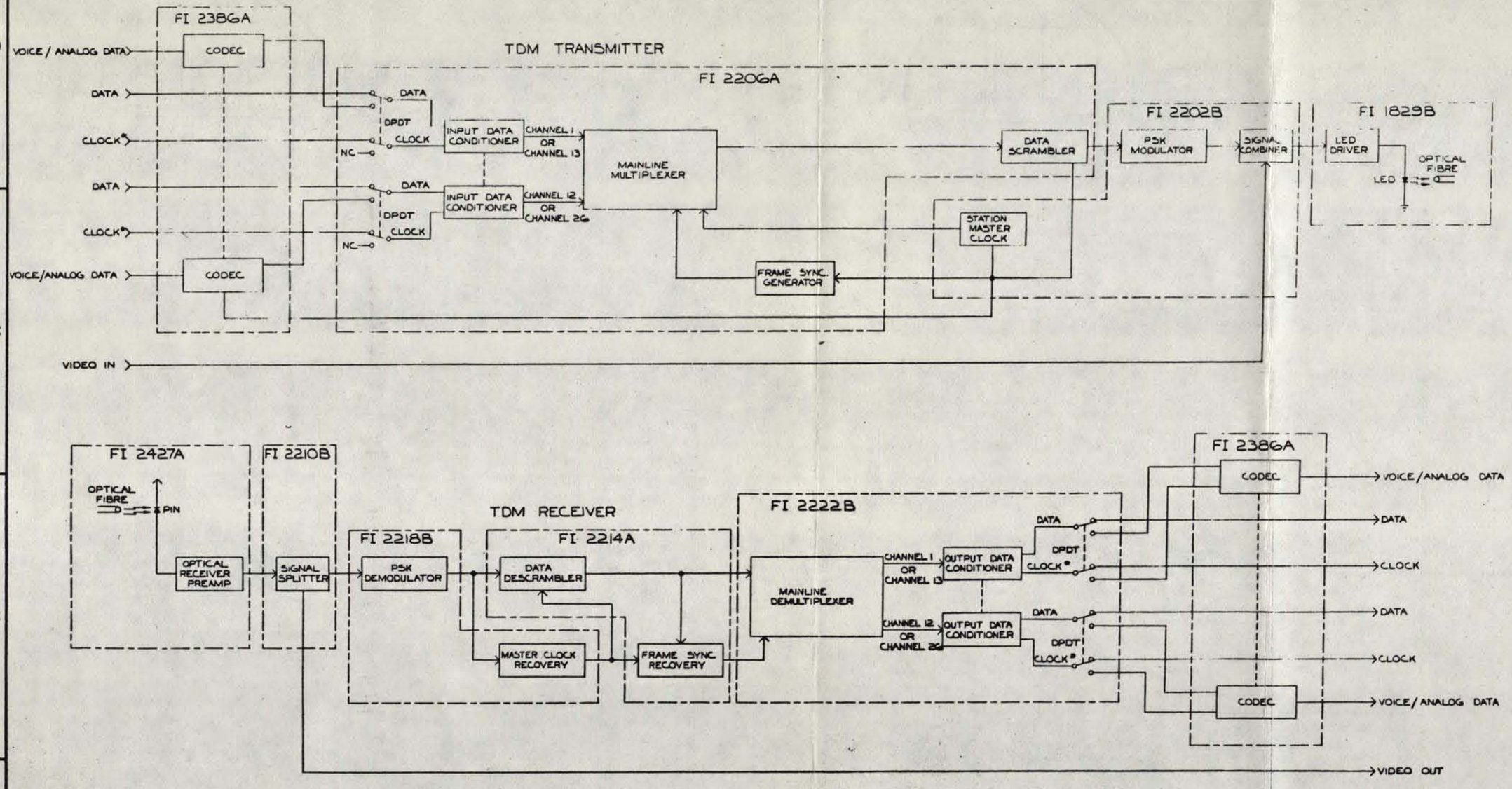


Figure 1

NOTES
1) INPUT DATA CONDITIONING MAY BE REQUIRED DEPENDING ON RECEIVER OUTPUT DATA CLOCK REQUIREMENTS (SEE TEXT)
2) * CLOCK ONLY REQUIRED FOR SYNCHRONOUS DATA
3) NUMBERS REFER TO PRINTED CIRCUIT BOARD ARTWORKS

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-08-04 | PROJ NO: 8101.3 | DRAWN BY: J. WHITEMAN

CANADIAN LAND TACTICAL ENVIRONMENT - SYSTEM DIA.

MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: | DWG NO: #1710

2.0 SYSTEM OVERVIEW

The Land Tactical system is an optical fibre system designed to replace a 26 pair copper wire cable with 2 single optical fibres.

The system shown as a block diagram in Figure 1 is one-half of the bi-directional transmission scheme. The system consists of 24 transmission ports which can be configured thus:

24 asynchronous data channels or 12 synchronous data channels (data & clock) or 12 analog frequency channels (delta-modulated data & clock) or a combination of asynchronous, synchronous and analog channels.

In addition to the 24 data channels, a baseband video channel is provided. The data channels are time division multiplexed then phase shift key (PSK) modulated onto a 12 Megahertz carrier. The PSK signal and baseband video signal are combined then applied to the light source modulator which intensity modulates (IM) the light emitting diode (LED).

The IM optical signal is launched into the fibred cable and received at the PIN photodetector. The combined electrical (video, data) signal is filtered. The PSK demodulator extracts the clock timing for demultiplexer synchronization. The demultiplexer outputs the signals to the 24 ports.

3.0 TECHNICAL SUMMARY

3.1 Fibre Optic Cable Selection

To demonstrate the advantage of optical links over conventional wire systems in deployment and recovery, two link lengths of one kilometer and two link lengths of five hundred meters are provided. As the fibre cable is accommodated on an RL-79 cable holder, the cross sectional diameter of the cable is restricted to 7 mm. To maximize the amount of launched light, and to minimize the cable loss due to a possible field splice, a fibre with a 100 micron core is utilized.

The cable selection was initiated by sending the following telex to the attached list of companies.

The fibre cable selection was based on the price and availability of the responsive cable designs. The supporting literature for the Belden 226102 selected cable is included in Appendix 1.

3.2 U-185 B/G Electrical Connector

The U-185 B/G connector is modified to accept the optical transmitter and optical receiver. The Elco Corporation hermaphrodite electrical connector mounts the transmitter and receiver board. To accommodate the reduced fibre cable size, a build-out plug is employed (see Figure 2). The assembly of the fibre cable and connector is described in Appendix 2. The modified U-185 B/G (see Figure 3) connects to the mating connector mounted on the signal input panel (see Figure 4). A simulated installation is shown in Figure 5.

414187920+
418792-0 SM D+
FOUND INST OTT

JULY 3/81 MSG 255

ATTN FIBRE OPTIC MARKETING MGR

I HAVE AN IMMEDIATE APPLICATION FOR 3500 METERS OF A TWO FIBRE RUGGEDIZED FIBRE OPTIC CABLE TO BE USED IN A TACTICAL FIELD ENVIRONMENT TRIAL. CABLE SHOULD CONTAIN NO STEEL ARMOUR TAPE NOR STEEL STRENGTH MEMBER

DESIRED PROPERTIES

OPERATING TEMP -40 DEG TO +40 DEG CELCIUS
CORE DIA 100 MICRON
MIN BANDWIDTH 35 MEGAHZ
MAX ATTENUATION 7DB/KM AT 820 NM
MAX NUMERICAL APPERTURE 0.25
MAX CABLE OUTSIDE DIA 7 MILLIMETER
STRUCTURAL CABLE TENSILE STRENGTH 4000 NEWTONS
POWDER OR GEL FILLED TO KEEP OUT WATER

TOLERANCES CAN BE RELAXED BASED ON YOUR RESPONSE

PLS TELEX QUOTE PRICE AND DEL ON YOUR MOST APPLICABLE CABLE AND SEND INFO OR HAVE SALES REP CALL

REGARDS

PC WHEELER
FOUNDATION ELEC INSTRU INC
1794 COURTWOOD CRES
OTTAWA ONT CANADA
K2C 2B5
TEL (613)226-4000
TELEX 053-4153
418792-0 SM DV

Belden Corp., 2000 S. Batavia Ave., Geneva, IL 60134
BICC Telecommunications Cable, P.O. Box 1, Prescot, Merseyside L34 55Z, U.K.
Boston Insulated Wire & Cable, 118 Shaw St., Hamilton, Ont.
Brand-Rex Co., P.O. Box 498, Willimantic, CT 06226
Kaytronics Ltd., 375 Rue Norman St., Ville St. Pierre, Quebec H8R 1A3.
Canstar Communications, 1240 Ellesmere Rd., Scarborough, Ont. M1P 2X4.
Centronic, 1101 Bristol Rd., Mountainside, NJ 07092
Corning Glass Works, Houghton Park A-2, Corning, NY 14830
DuPont Company, Fibre Optics Div., D-13020, Wilmington, DE 19898
Earling Beck Ltd., Greycaine Rd., Watford WD2 4PW, United Kingdom
Ensign Bickford Indus. Inc., 660 Hopmeadow St., Simsbury, CT 06070
Thomas and Betts, 920 Route 202, Raritan, NJ 08869
Fujikura Cable Works Ltd., 5-1, kiba 1-chome, Koto-Ku, Tokyo, 135 Japan
Galileo Electro Optics Corp., Galileo Park, Sturbridge, MA 01518
Galite Inc., 2 Tower Dr., Wallingford, CT 06492
General Cable Co., Div of GK Technologies Inc.,One Woodbridge Center, Woodbridge NJ
Hewlett-Packard, Optoelectronics Div., 640 Page Mill Rd., Palo Alto, CA 94304
Hitachi Ltd., Central Research Lab, New Marunouchi, Bldg 5-1, Marunouchi 1-chome Chiyoda-ku, Tokyo 100 Japan
ITT Components Group, Edinburgh Way, Harlow, Esses CM20 2DE, United Kingdom
Jenaer Glaswerk Schott & Gen., Hattenberg strabe Strasse 10, 6500 Mainz, Federal Republic of Germany
LTT Lignes Telegraphiques et Telephoniques, Div. Thomson - CSF, 78702 Conflans-ste-Honorine, B.P. 5 France
London Electric Wire, Optical Fibres Div., 210 Church Rd., Leyton, London, Engl
3M, Electronic Products Div., 34 Center, Bldg 225-45-02 St. Paul, MN 55144
Mitsubishi Corp., Marunouchi 2-chome, Chiyoda-ku, Tokyo 100 Japan
Nippon Sheet Glass Co. Ltd., 8-3, Shimbashi 1-chome, Minato-Ku, Tokyo Japan
N.K.F. Kabel Telecommunication Cable Systems, 85,2740 AB, Waddinxveen, The Netherlands
Northern Telecom Canada Ltd., P.O. Box 807, Saskatoon, Saskatchewan S7K 3L7.
OKI Electric Industry Co. Ltd., 10, Shiba-Kotohira-cho, Minato-ku Tokyo, Japan
Opticord, 11 Avenue d'Iena, 75116, Paris, France
N.V. Philips, M.I.G. Allied Ind/Glass, Bldg OA1, Eindhoven, The Netherlands
Pilkington P.E. Ltd., Glasscoed RD. St., Asaph Clwyd LL17 OLL, United Kingdom
TASSO Inc., 5175 de Maisonneuve W., Montreal, PQ H4A 1Z3.
Quartz Products Corp., 688 Somerset St., P.O. Box 1347, Plainfield, NJ 07061
Raychem Corp., 300 Constitution Dr., Menlo Park, CA 94025
RMP, 18, rue d'Arras, 9200 Nanterre, France
Siecor Optical Cables Inc., P.O. Box 489, Hickory, NC 28601

SAT, Societe Anonyme de Telecommunications, 41 rue Cantagrel, 75624 Paris, Fran

Standard Telephones & Cables Ltd., 3 West Rd., Harlow, Essex, United Kingdom

Sumitomo Electric U.S.A., Inc., 345 Park Ave., New York, NY 10154

Teijin Advanced Products Corp., 1-1, Uchisaiwai-cho, 2-chome, Chiyoda-ku, Tokyo 100 Japan

Telephone Cables Ltd., Chequers Lane, Dagenham RM9 6QA, United Kingdom

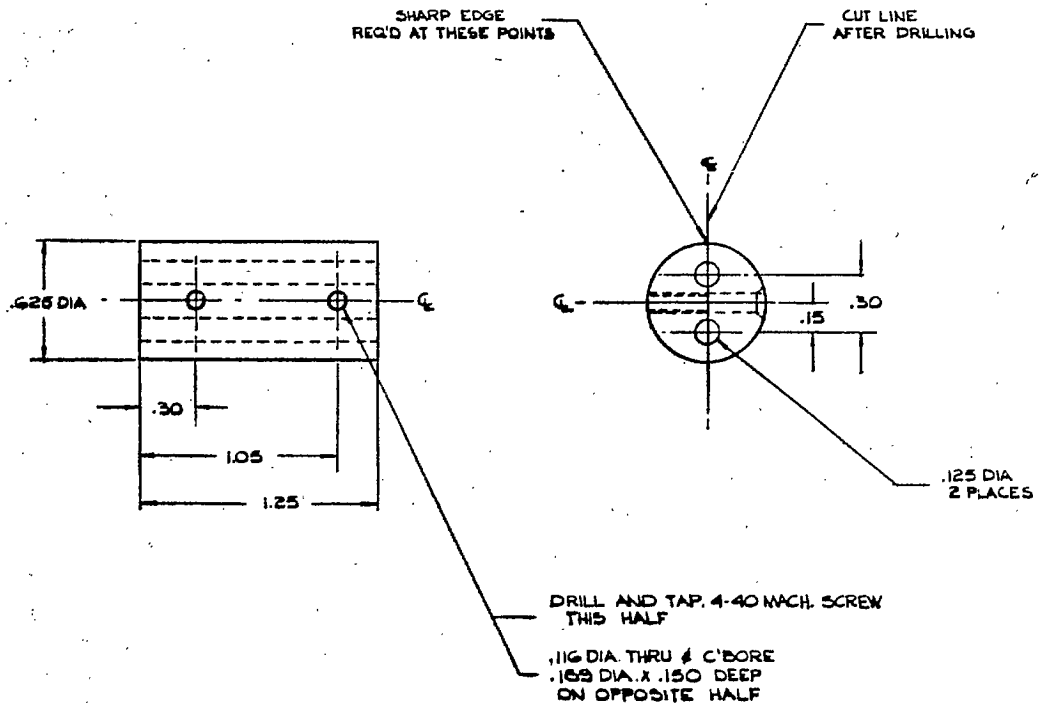
Thomas Brandt, Cables Isoles Div., 10 rue J.P. Timbaud, 92400 Courbevoie France

Tech Rep Electronics Ltd., 274 Dorval Ave., Suite No 201, Dorval, Que. H9S 3H3

Cossor Electronics Ltd., The Pinnacles, Elezabeth Way, Harlow, Essex England

REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-01-29	DESIGN CHANGED

Figure 2



ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-01-29 | PROJ. NO: 810113 | DRAWN BY: P.G.

BELDEN 226102 FIBER CABLE WATERPROOF BUSHING

MATERIAL: ALUMINUM | SCALE: 2/1 | SHEET OF

FINISH: CLEAR ANODIZE | APPROVAL: R Yee 82/01/29 | DWG NO: 1833

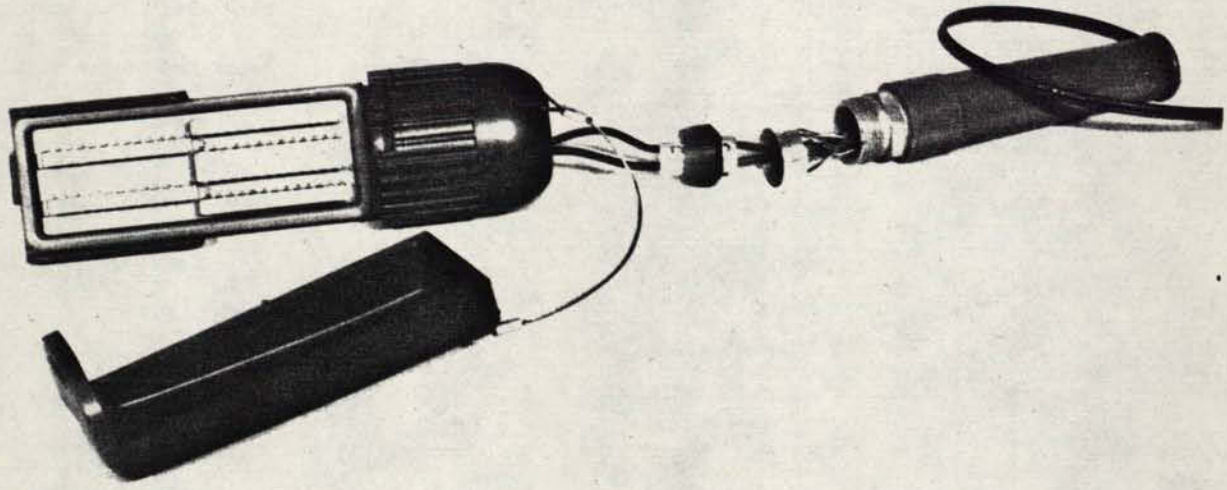


FIGURE 3

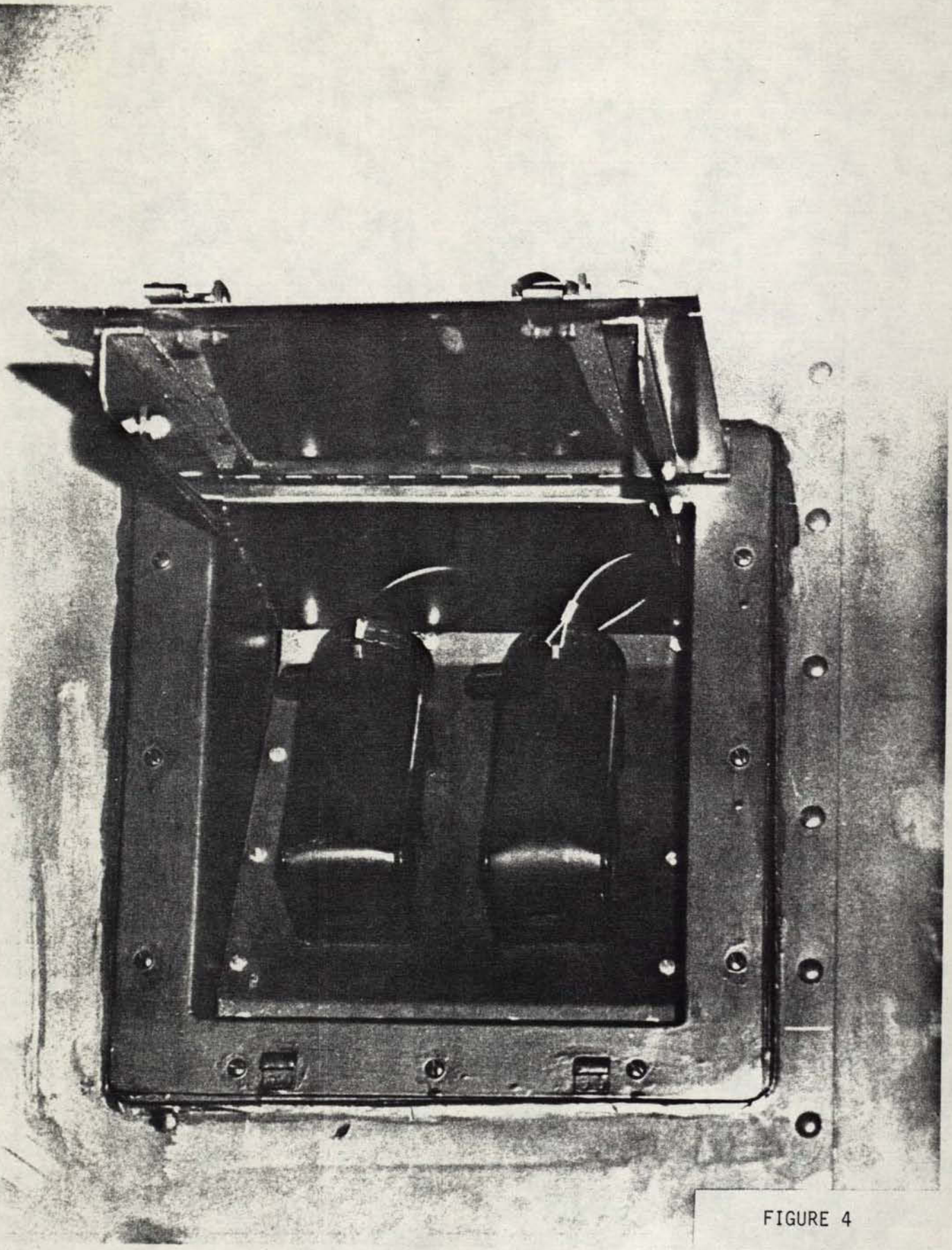


FIGURE 4

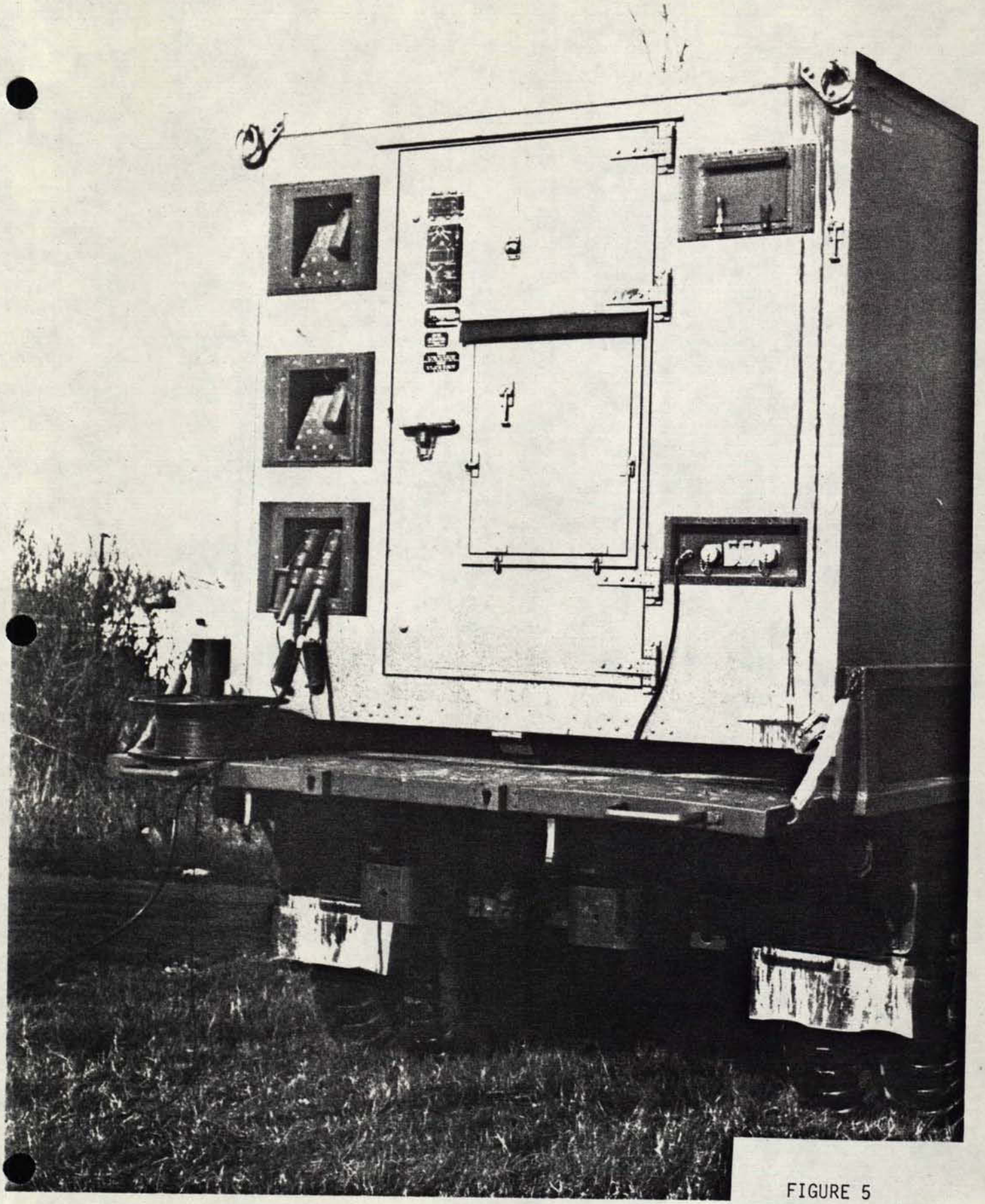


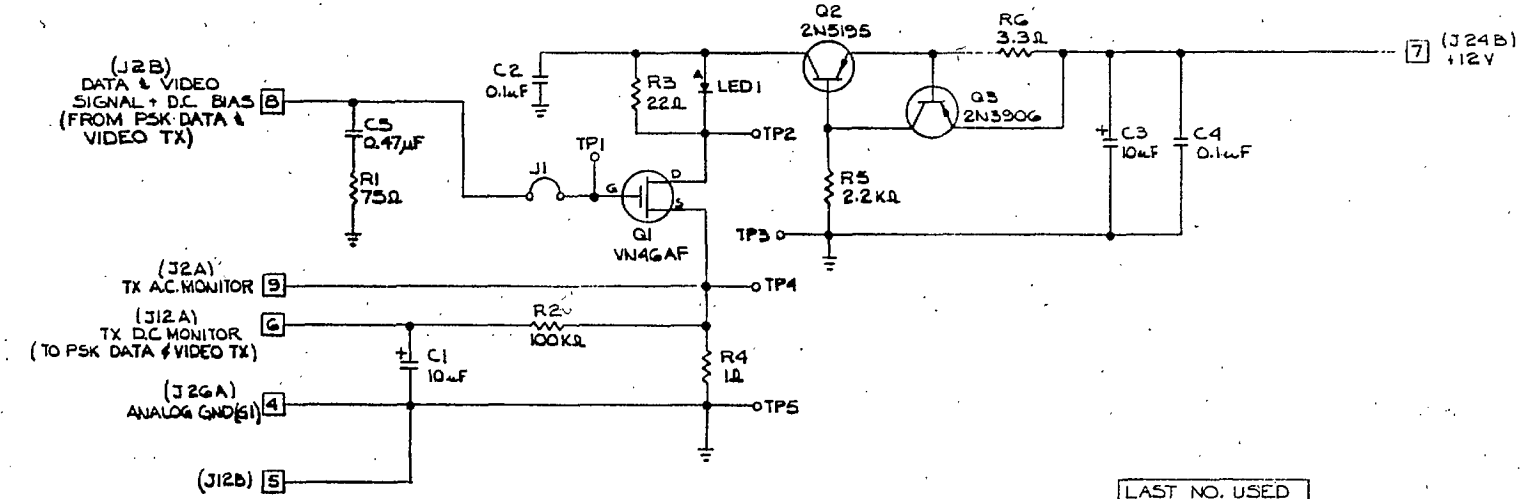
FIGURE 5

3.3 Optical Transmitter

This section describes the electrical (see Figure 6) and mechanical (see Figure 7 and Figure 8) optical transmitter assembly. The Spectronix SE3352-004 is a high radiance GaA/As infrared light emitting diode which is current modulated (and light intensity modulated) by the Siliconix VN46AF VMOS field effect transistor.

REVISIONS		
REV	DATE	DESCRIPTIONS

FIGURE 6



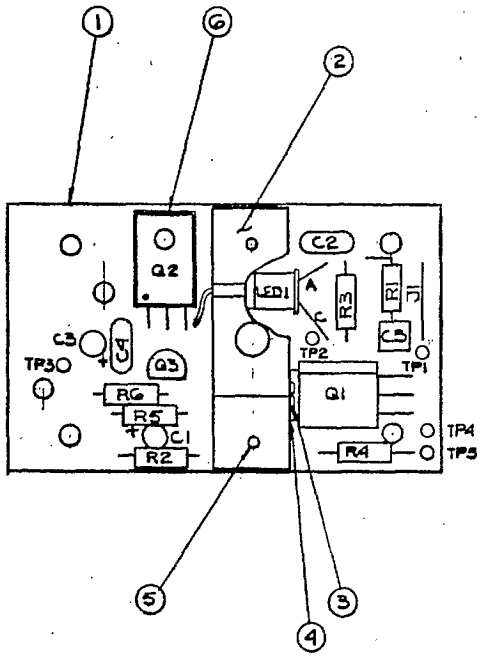
LAST NO. USED
R6
C5
Q3
J1
TP5
LED1

NOTE:
1) NUMERS IN PARENTHESES REFER TO JUMPERS FROM PCB TO DESIGNATED LUGS ON ELCO CORP. CONT. ASSY. ELECT. MX 3227/G.
2) R3 REDUCED TO 15Ω ON SOME TRANSMITTERS

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-09-15	PROJ. NO: 810113	DRAWN BY: RE.
	F/O TX MODULE - SCHEMATIC		
MATERIAL:		SCALE:	SHEET OF
FINISH:		APPROVAL: R. Yee 09/02/83	DWG NO: 1828

FIGURE 7



REV	DATE	REVISIONS DESCRIPTIONS

ITEM	QTY	PART NO.	DESCRIPTION
J1	1		JUMPER, COPPER, SOLID, INSULATED, #22 AWG
TP1-5	5	20-2137D	TEST POINT VERO
LED1	1	SE 3352-004	LIGHT EMITTING DIODE SPECTRONICS
Q3	1	2N3906	TRANSISTOR.
Q2	1	2N5195	TRANSISTOR
Q1	1	VN46AF	POWER FET SILICONIX
C5	1	3439-050E-474M	CAPACITOR, 0.47μF, CERAMIC, 50 VDC AVX
C2,4	2	3439-050E-104M	CAPACITOR, 0.1 μF, CERAMIC, 50 VDC AVX
C1,3	2	TAP10 MIG	CAPACITOR, 10μF, TANTALUM, 16WVDC ITT
R6	1		RESISTOR, 3.3Ω, 1/4W, 5%
R5	1		2.2KΩ
R4	1		1Ω
R3	1		22Ω
R2	1		100KΩ
R1	1		RESISTOR, 75Ω, 1/4W, 5%
G	A/R		DOUBLE SIDED MOUNTING TAPE
5	2	MS-109	SCREW MACH. 4-40 x 1/4, BDNG. HD.
4	1	4673	PLASTIC CASE MICA INSULATOR SP-NR
3	1	445-028	SCREW. MACH. NYLON. BDNG. HD. 4-40-3/8 SP-NR.
2	1	1861	HEAT SINK FI
1	1	1829	PRINTED CIRCUIT BOARD FI
NEXT ASSY.		DWG. # 2424	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

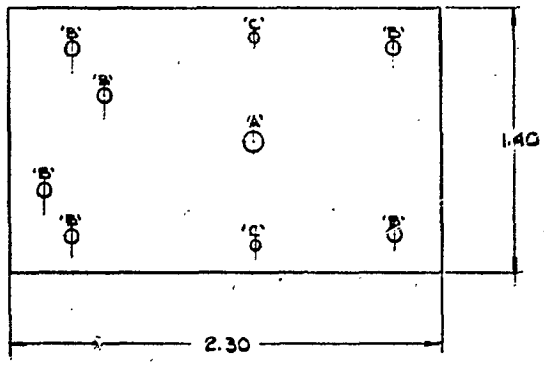
DATE: 82-09-16 | PROJ. NO: 810113 | DRAWN BY: RG.

F/O TX MODULE - COMP. LAY.

MATERIAL: | SCALE: 2/1 | SHEET OF

FINISH: | APPROVAL: R. Yee 09/02/83 | DWG NO: 1830

FIGURE 8



HOLE DATA		
SYM	DESCRIPTION	QTY
'A'	0.201 DIA	1
'B'	0.128 DIA	6
'C'	0.093 DIA	2
OTHER	0.037 DIA	

NOTE:
1) ALL HOLES TO BE DIMENSIONED AFTER PLATING.
2) ALL HOLES TO BE DRILLED ON PAD CENTERS.

REV	DATE	REVISIONS / DESCRIPTIONS

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY		DWG.# 1830	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-09-13 | PROJ. NO: 810113 | DRAWN BY: P.G.

CDN LAND TACTICAL F/O TX-- MASTER

MATERIAL: G10, .062 THK GLASS EPOXY 1OZ. COPPER EACH SIDE | SCALE: 2/1 | SHEET OF

FINISH: TIN LEAD PLATE .0002/.0003 THK | APPROVAL: [signature] 01/02/83 | DWG NO: 1831

3.4 Optical Receiver

This section describes the electrical (see Figure 9) and mechanical (see Figure 10 and Figure 11) optical receiver assembly. The Motorola MFOD100 is a p.i.n. photodiode reverse biased with a 100 Kohm load resistor. Photon generated signals are AC coupled to the bootstrapped amplifier.

REVISIONS		
REV	DATE	DESCRIPTIONS

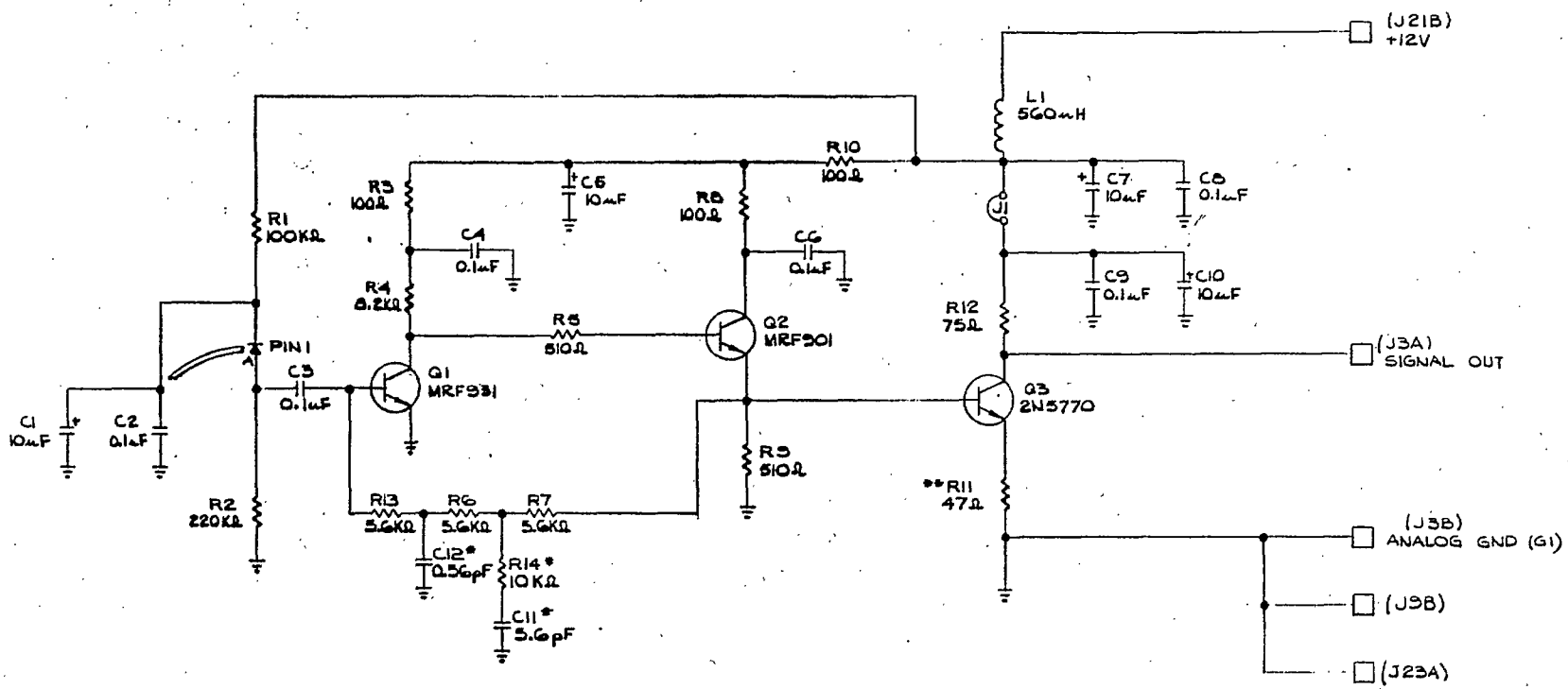


FIGURE 9

NOTE:
1) NUMBERS IN PARENTHESES REFER TO JUMPERS FROM RX PCB TO DESIGNATED LUGS ON ELCO CORP. CONT. ASSY. ELEC. MX 3227/G.
*2) THE VALUES OF R14, C11, C12 ARE ADJUSTED DURING TESTING TO GET A FLAT FREQUENCY RESPONSE.
**3) R11 IS ADJUSTED IN EACH RECEIVER TO COMPENSATE FOR OPTICAL POWER DIFFERENCES BETWEEN LINKS

LAST NO. USED
R14
C12
Q3
L1
J1
PIN1

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

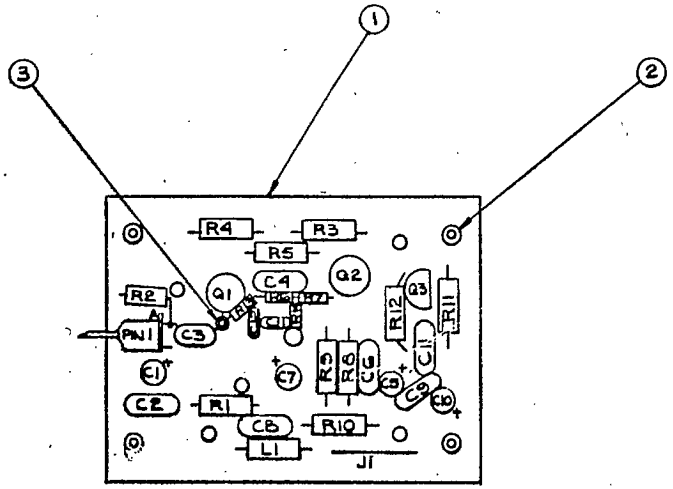
DATE: 82-09-17 | PROJ. NO: 810113 | DRAWN BY: RG.

F/O. RX MODULE - SCHEMATIC

MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: R.Ups 09/02/83 | DWG NO: 2426

FIGURE 10



REVISIONS		
REV	DATE	DESCRIPTIONS

ITEM	QTY	PART NO.	DESCRIPTION	
J1			JUMPER, COPPER, SOLID, INSULATED, #22 AWG	
PIN 1	1	FI-IRD-3-2	PIN. DIODE	FI
L1	1	1025-86	COIL. 560 uH	DELEVAN
Q3	1	2N5770	TRANSISTOR	
Q2	1	MRF901	TRANSISTOR	
Q1	1	MRF931	TRANSISTOR	
C12	1	2222-638-03567	CAPACITOR, 0.56pF, CERAMIC	PHILIPS
C11	1	638-09568	CAPACITOR, 5.6pF, CERAMIC	PHILIPS
C6,8,9 C2,3,4,	6	5439-050E-104M	CAPACITOR, 0.1 uF, CERAMIC, 50V.	AUX
C10 C1,5,7,	4	TAP 10M16	CAPACITOR, 10 uF, TANTALUM, 16 WVDC	ITT
R14	1		RESISTOR, 10KΩ, 1/8W, 5%	
R12	1		RESISTOR, 75 Ω, 1/2W, 5%	
R11	1		47Ω, 1/4W	
R9	1		510 Ω, 1/4W	
R6,7,8	3		5.6KΩ, 1/8W	
R5	1		510Ω, 1/4W	
R4	1		8.2 KΩ	
R3,8,10	3		100Ω	
R2	1		220 KΩ	
R1	1		RESISTOR, 100 KΩ, 1/4W, 5%	
3	1		INSULATED TERMINAL	
2	4	1589-2	SWAGE TYPE THREADED STAND-OFFS	KEYSTONE
1	1	2427	PRINTED CIRCUIT BOARD	F.I.

NEXT ASSY. | DWG.# 2424

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

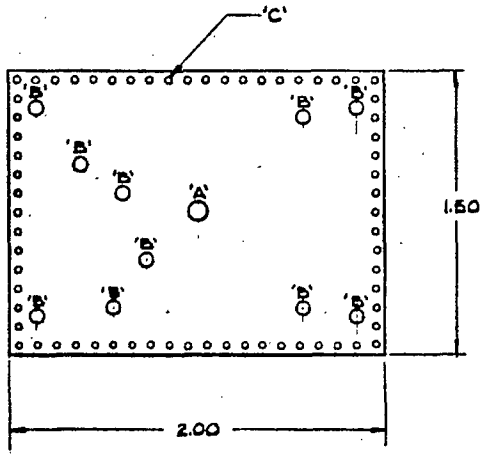
DATE: 82-09-20 | PROJ. NO: 810113 | DRAWN BY: RG.

F/O RX MODULE - COMP LAY

MATERIAL: | SCALE: 2/1 | SHEET OF

FINISH: | APPROVAL: R. Yee 09/02/92 | DWG NO: 2428

FIGURE 11



HOLE DATA		
SYM	DESCRIPTION	QTY
'A'	.201 DIA.	1
'B'	.128 DIA.	10
'C'	.037 DIA.	66

NOTE:
1) ALL HOLES TO BE DIMENSIONED AFTER PLATING.
2) ALL HOLES TO BE DRILLED ON PAD CENTERS.

REV	DATE	REVISIONS DESCRIPTIONS

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY		DWG #	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-09-13 | PROJ. NO: 810113 | DRAWN BY: P.G.

F/O. RX MODULE - MASTER

MATERIAL: G10, .062 THK. GLASS EPOXY 1OZ. COPPER EACH SIDE. | SCALE: 2/1 | SHEET OF

FINISH: TIN LEAD PLATE .0002/.0003 THK | APPROVAL: R.Lyn 09/02/82 | DWG NO: 2429

3.5 Transmitter/Receiver Packaging

The optical transmitter and receiver are mounted on the Elco electrical connector (see Figure 12 and Figure 13) and mounted into the U-185 B/G connector (see Figure 14). Figure 15 is the LED heatsink and Figure 16 is the receiver circuit shield cover used to reduce RFI pick-up.

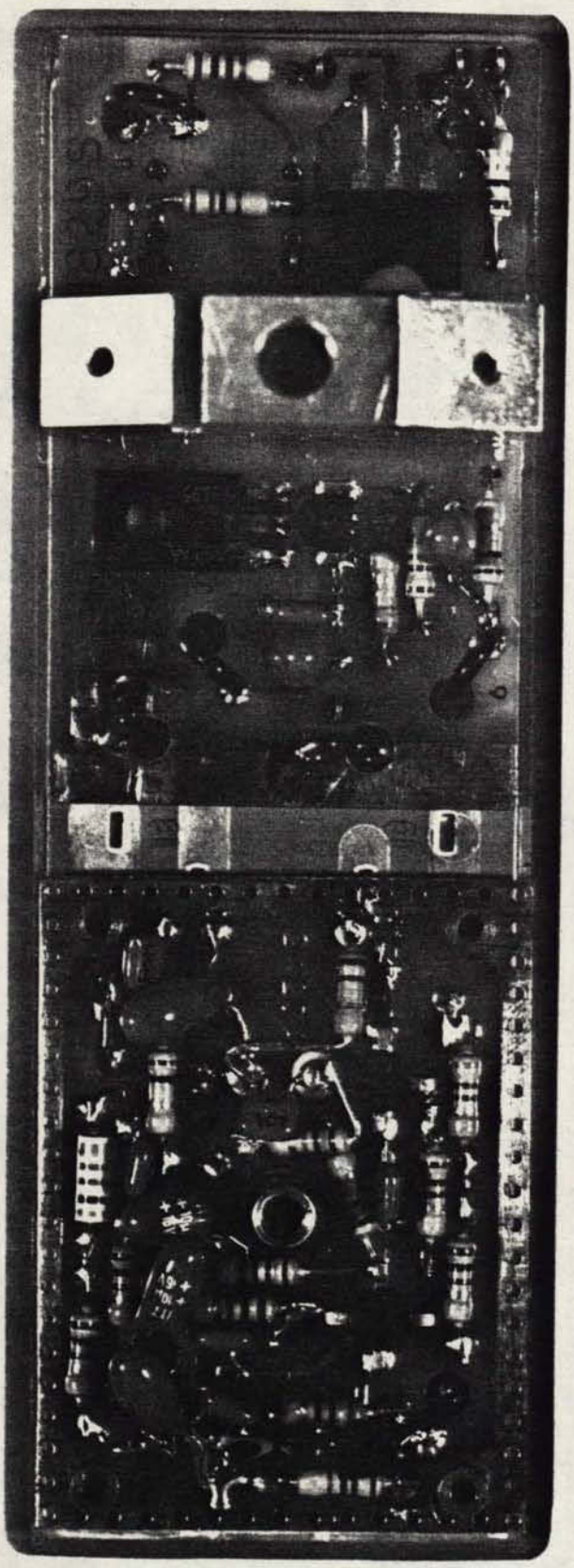


FIGURE 12

FIGURE 13

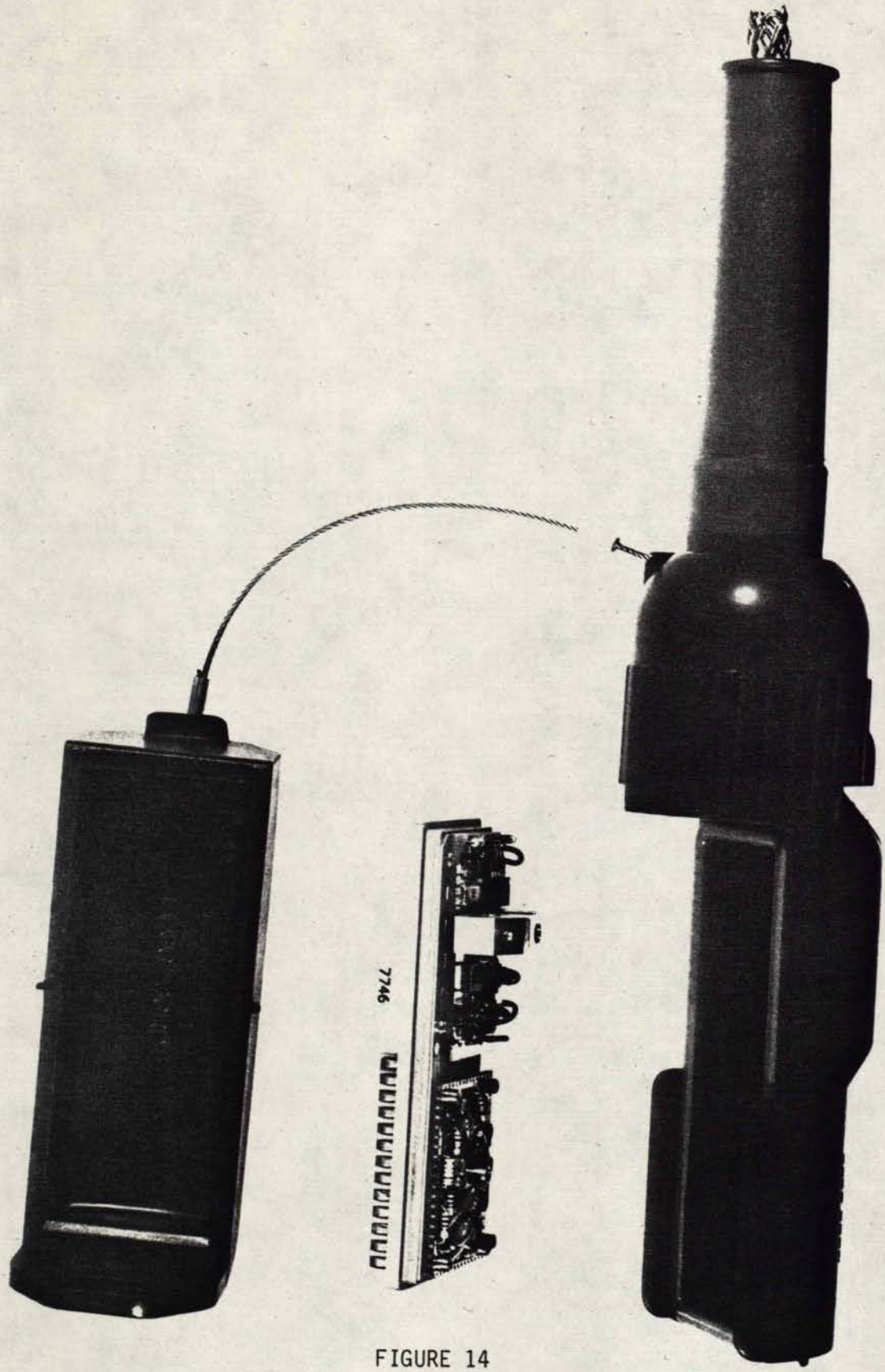
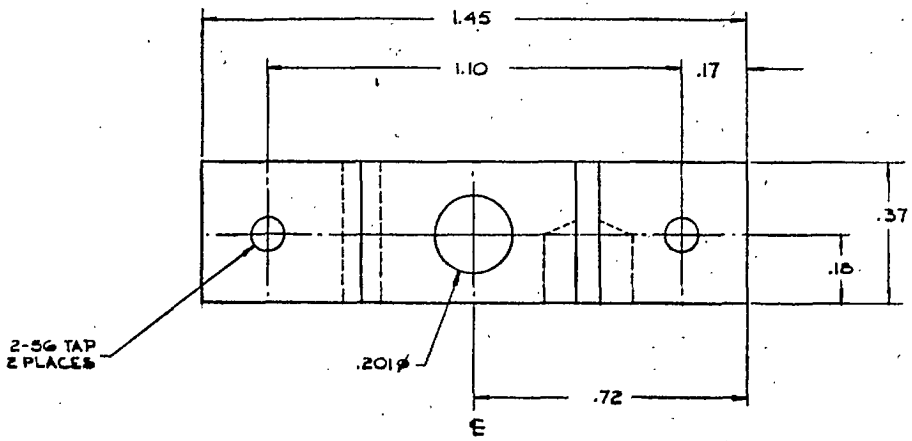


FIGURE 14

REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-01-29	DESIGN CHANGE
B	82-09-13	SLOT ADDED
C	82-10-06	.059 ø HOLE REMOVED



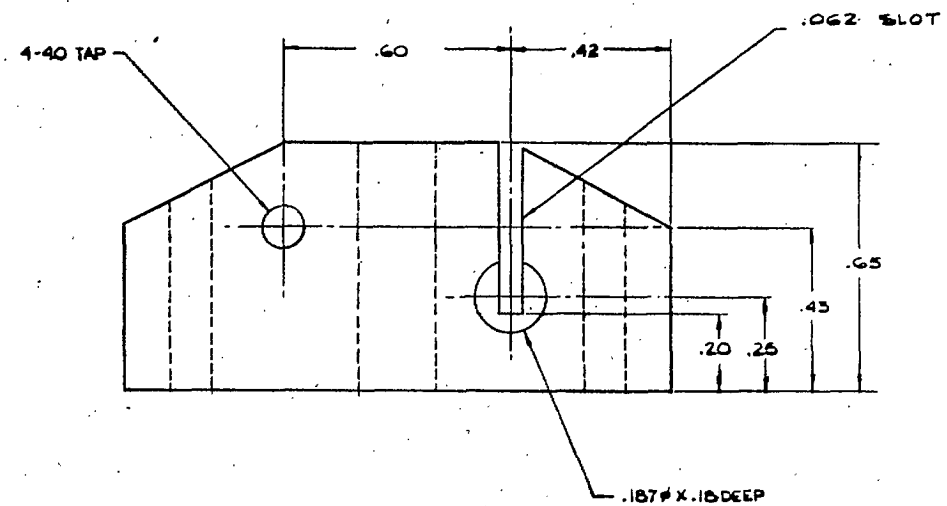
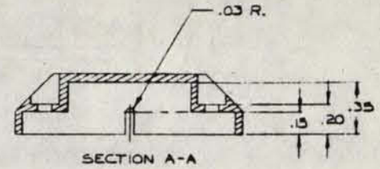


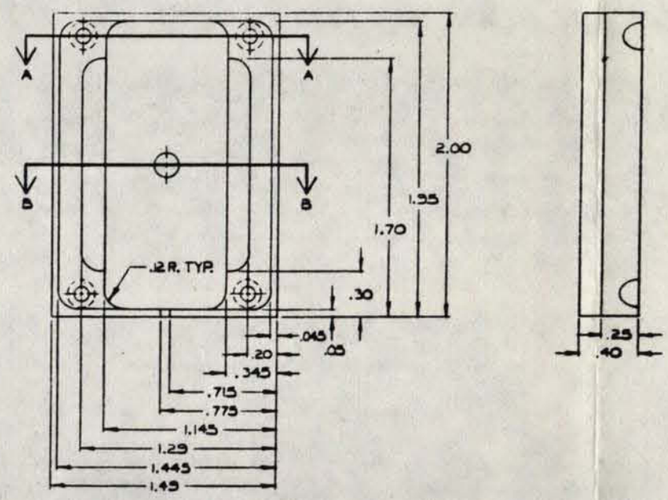
FIGURE 15

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010, .XXX ±.005, ANGLES ±1/2°	FOUNDATION INSTRUMENTS OTTAWA		
SURFACES:	DATE: 82-01-28	PROJ. NO: 810113	DRAWN BY: P.G.
REMOVE BURRS & SHARP EDGES	TX HEAT SINK - MECHANICAL		
MATERIAL: ALUMINUM		SCALE: 4/1	SHEET OF
FINISH: BLK. ANODIZE		APPROVAL: R.G. 17/02/82	DWG NO: 1861

REV	DATE	REVISIONS DESCRIPTIONS





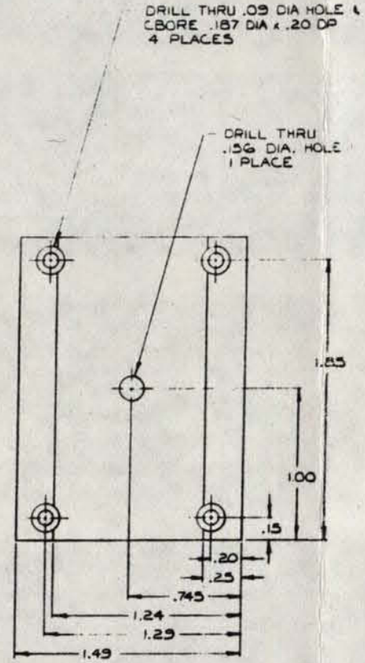
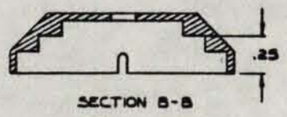


FIGURE 16



ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS | SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-05-23	PROJ. NO: 810113	DRAWN BY: J. WHITEMAN
	SHIELD COVER		
MATERIAL: ALUMINUM		SCALE: 2/1	SHEET OF
FINISH: CLEAR ANODIZE		APPROVAL: 17/05/83	DWG. NO: 2389

3.6 Duplex Voice Transmission Codec

This section describes the theory of operation of the duplex voice transmission codec. Additional information on the codec circuit is contained in Appendix 4. This section consists of:

i) Block diagram
ii) Schematics D2385, 1 through 6
iii) Overlay D2387, 1 and 2
iv) Photographs PCB 2386A component and solder side
v) Photographs PCB 2386A partial assembly
vi) Photograph PCB's 2 wire and 4 wire interface
vii) Mechanical 2437 PCB drilling diagram
viii) Mechanical 2437 PCB drilling diagram
ix) Mechanical 2388 PCB drilling diagram
x) Overlay 2432
xi) Overlay 2436.

THEORY OF OPERATION

Module: Duplex Voice Transmission Codec (F1-2386A)
Schematic D2385 Sheets 1-6.
Component Overlay D2387

Associated Modules:

a) 4-wire Audio Interface (F1-2431A)
Component Overlay No. 2432
Master No. 2433

b) 2-wire Audio Interface (F1-2435)
Component Overlay No. 2436
Master No. 2437

Operational Description:

See accompanying block diagram and schematic D2385 Sheets 1-6.

2 and 4 Wire Hybrid:

Provides a customer interface. Codec channels 1-5 and 7-11 have 4-wire hybrids, channels 6 and 12 have 2-wire hybrids.

Low Pass Filter:

Band limits incoming and outgoing analogue signals to approximately 4 Khz.

Tx & Rx Codecs:

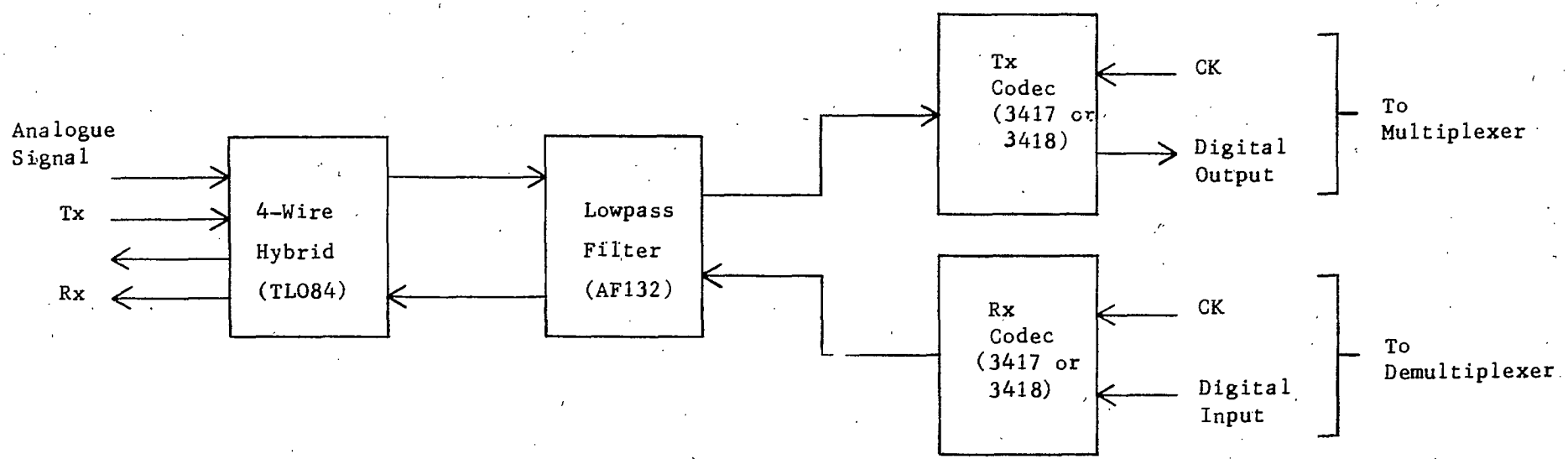
Converts the analogue signal to a digital serial stream and vice versa for analogue signal recovery. Employs a continuously variable slope modulator-demodulator algorithm in its encode and

decode operations. The codecs are driven by a 37Khz clock, either generated at the multiplexer or recovered at the demultiplexer.

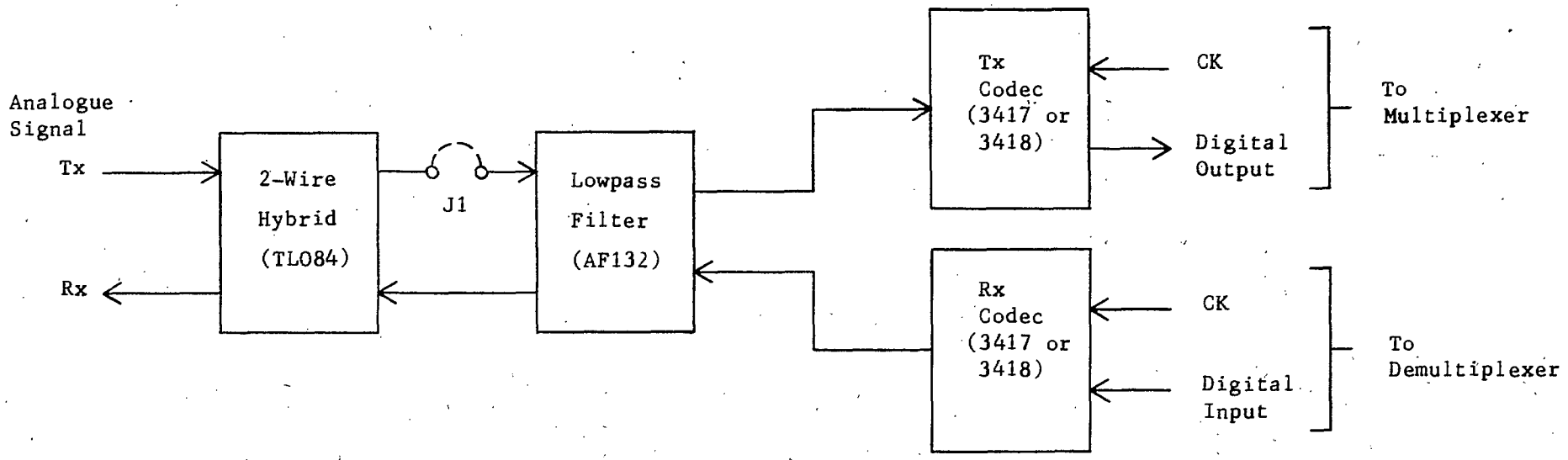
Please Note:

Two of the FI-2386A boards contain Motorola 3418 devices as opposed to the Motorola 3417. When these two are installed, they must be placed in the same slot in the housings at each end of the link. The 3418 chips will not operate correctly when paired with the 3417 codec devices.

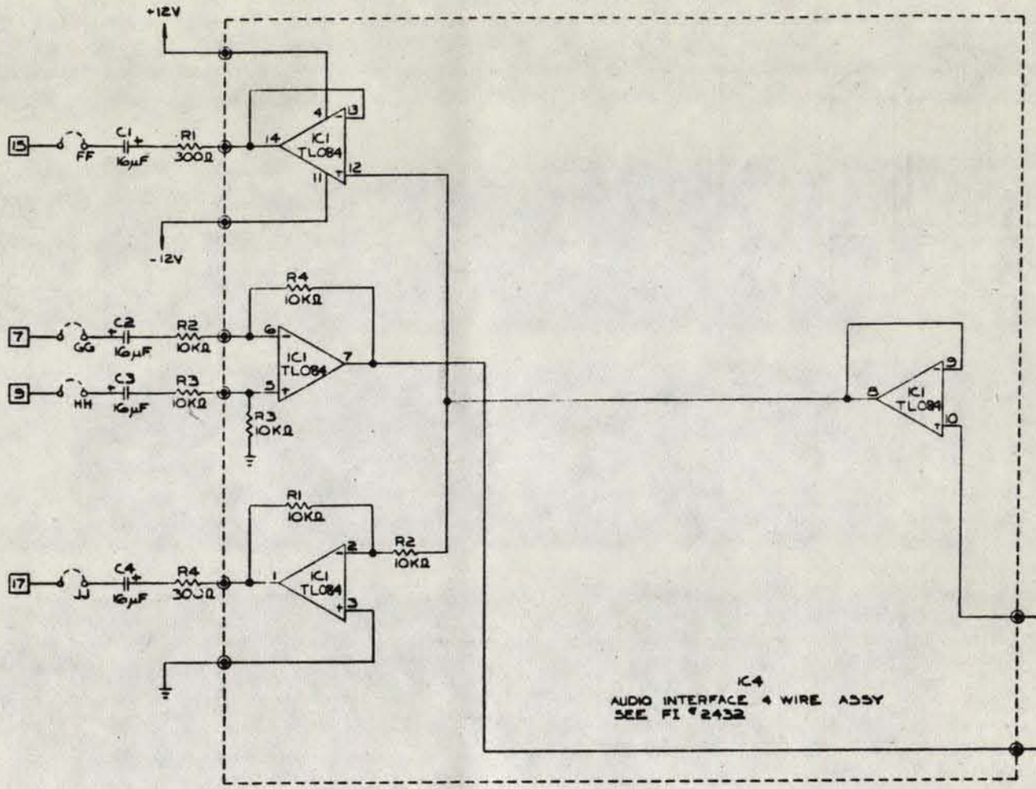
4-Wire Full Duplex Codec

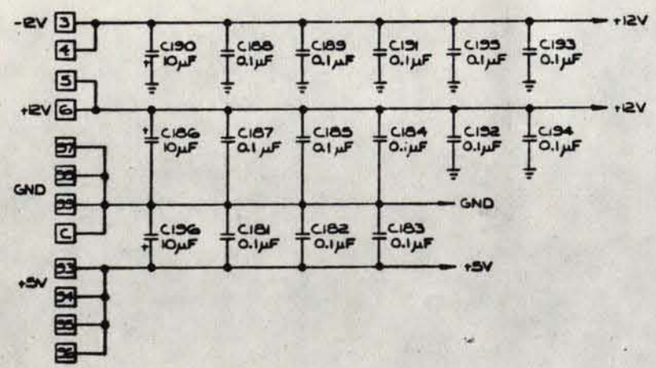


2-Wire Full Duplex Codec

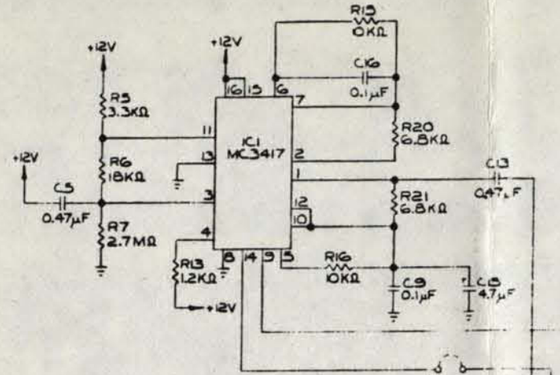


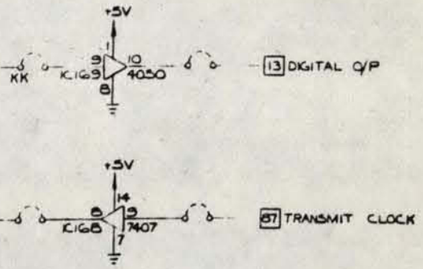
REV	DATE	REVISIONS DESCRIPTIONS

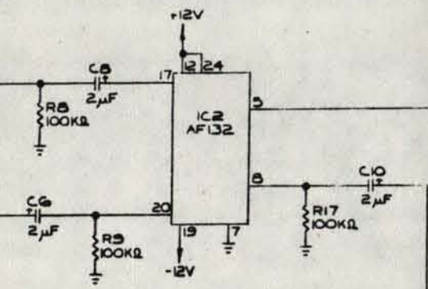


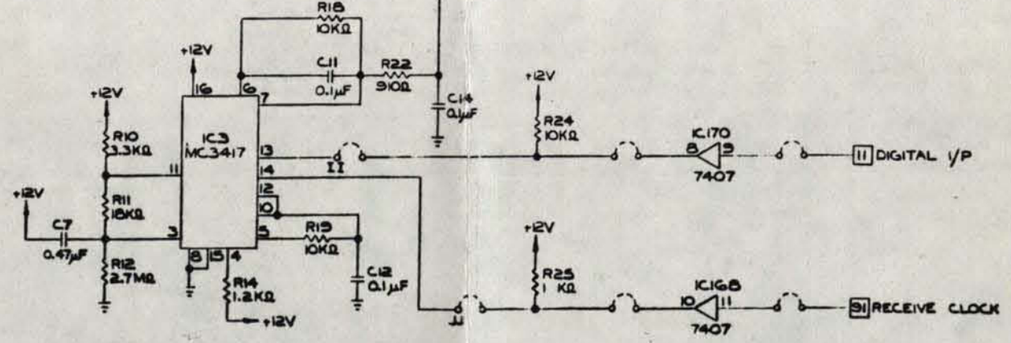


CHANNEL 1









ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY #D2387, #2432			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: XX ±.010
XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

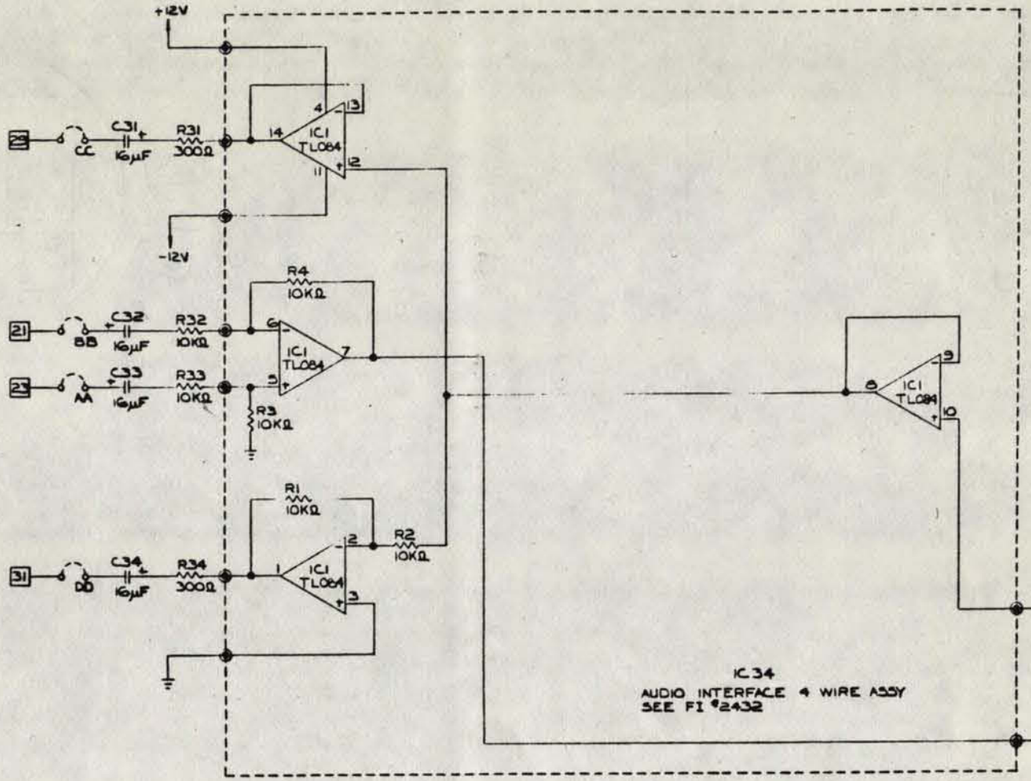
DATE: 82-07-16 | PROJ NO: 81013 | DRAWN BY: J. WHITEMAN

DUPLEX VOICE TRANSMISSION CODEC

MATERIAL: | SCALE: | SHEET 1 OF 6

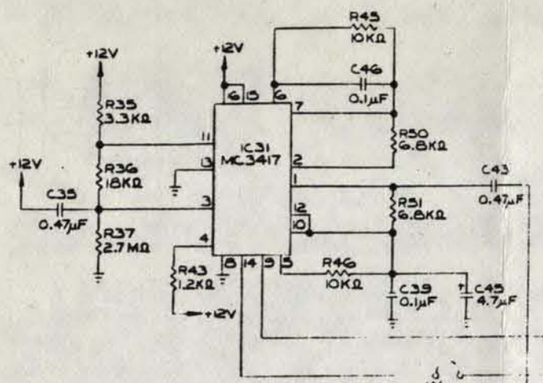
FINISH: | APPROVAL: R. Yow 17/07/82 | DWG NO: #D2385

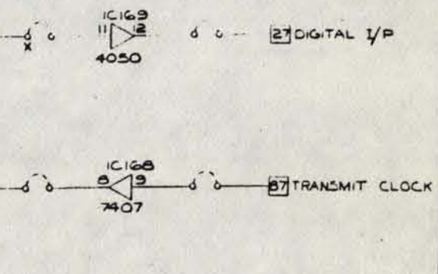
REV	DATE	REVISIONS DESCRIPTIONS

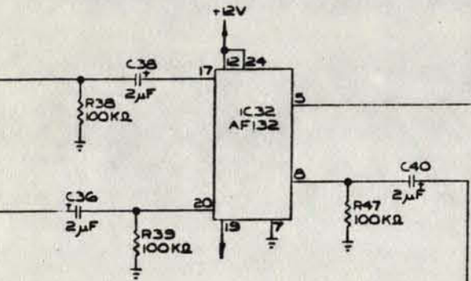


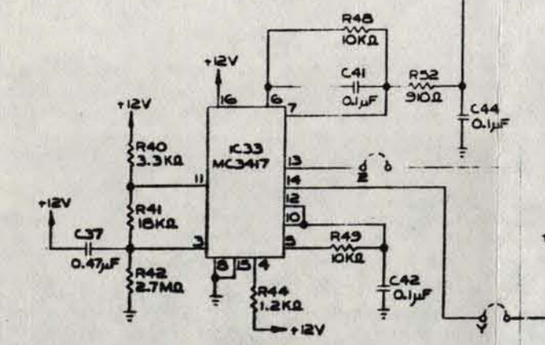
IC 34
AUDIO INTERFACE 4 WIRE ASSY
SEE FI #2432

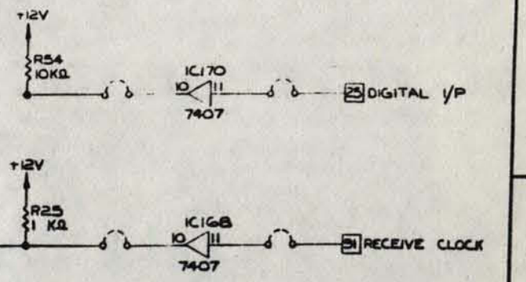
CHANNEL 2











ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS
OTTAWA

DATE: 82-07-16 | PROJ NO: 81013 | DRAWN BY: J. WHITEMAN

DUPLEX VOICE TRANSMISSION CODEC

MATERIAL: | SCALE: | SHEET 2 OF 6

FINISH: | APPROVAL: R. Yuen 17/08/82 | DWG NO: D2385

REVISIONS		
REV	DATE	DESCRIPTIONS

CHANNEL 3

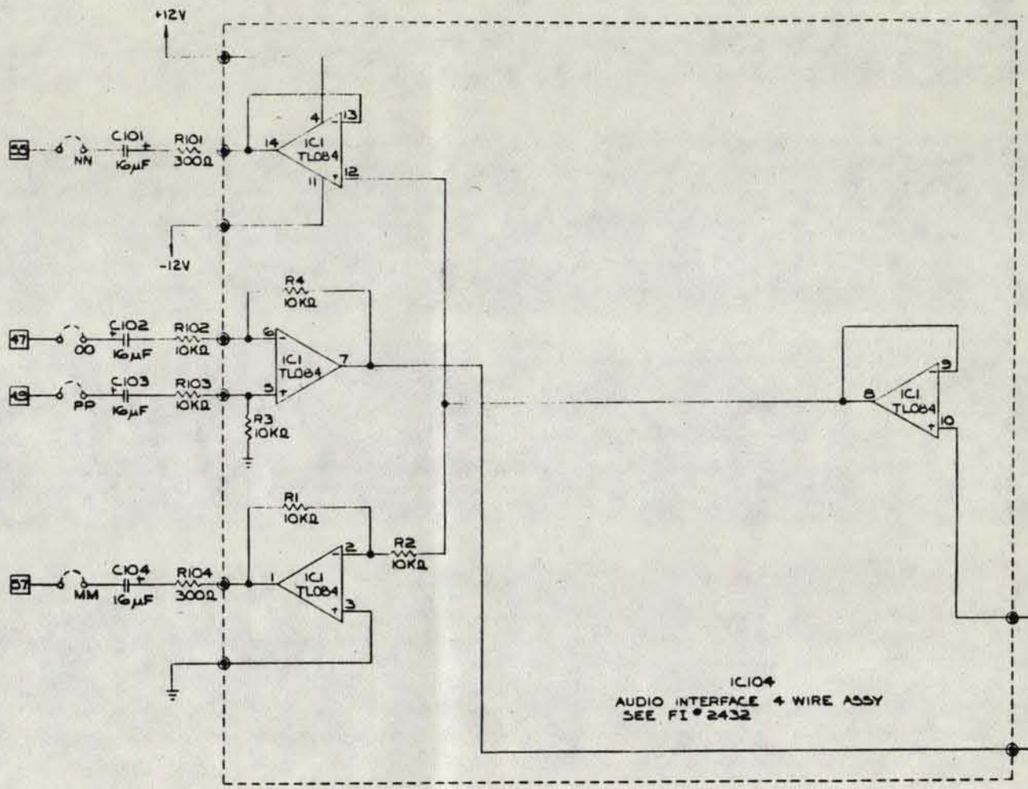
IC64
AUDIO INTERFACE 4 WIRE ASSY
SEE FI #2432

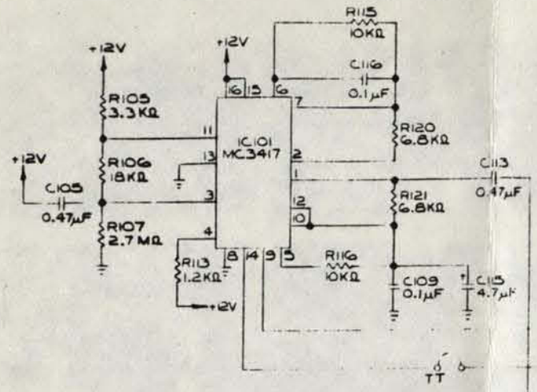
INFORMATION CONTAINED IN THIS DRAWING IS PROPRIETARY TO FOUNDATION INSTRUMENTS AND SHALL NOT BE DISCLOSED TO ANYONE OTHER THAN PERSONS AUTHORIZED BY THE COMPANY TO WHOM FOUNDATION INSTRUMENTS HAS FURNISHED THIS DRAWING

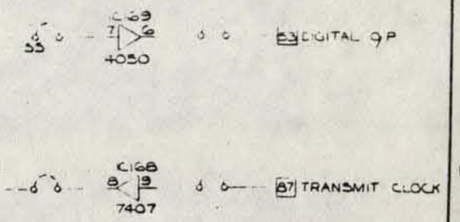
ITEM	QTY	PART NO.	DESCRIPTION

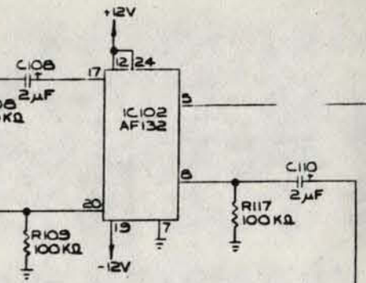
UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-07-16	PROJ NO: 810113	DRAWN BY: J.WHITEMAN
	DUPLEX VOICE TRANSMISSION CODEC		
MATERIAL:		SCALE:	SHEET 3 OF 6
FINISH:		APPROVAL:	DWG NO: D2385

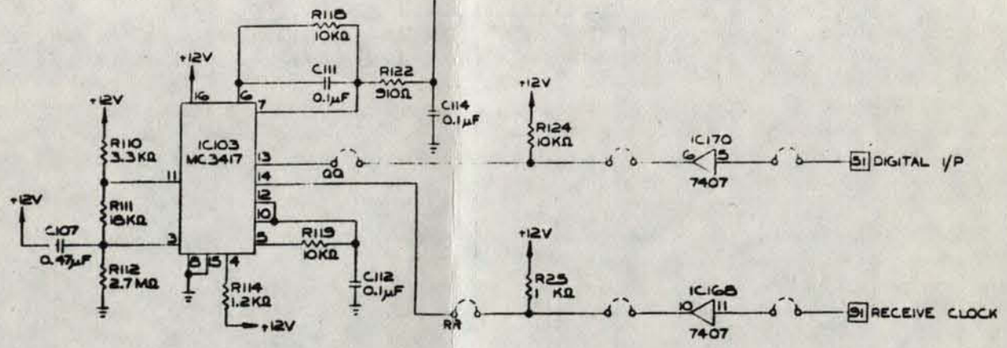
REV	DATE	REVISIONS / DESCRIPTIONS











CHANNEL 4

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

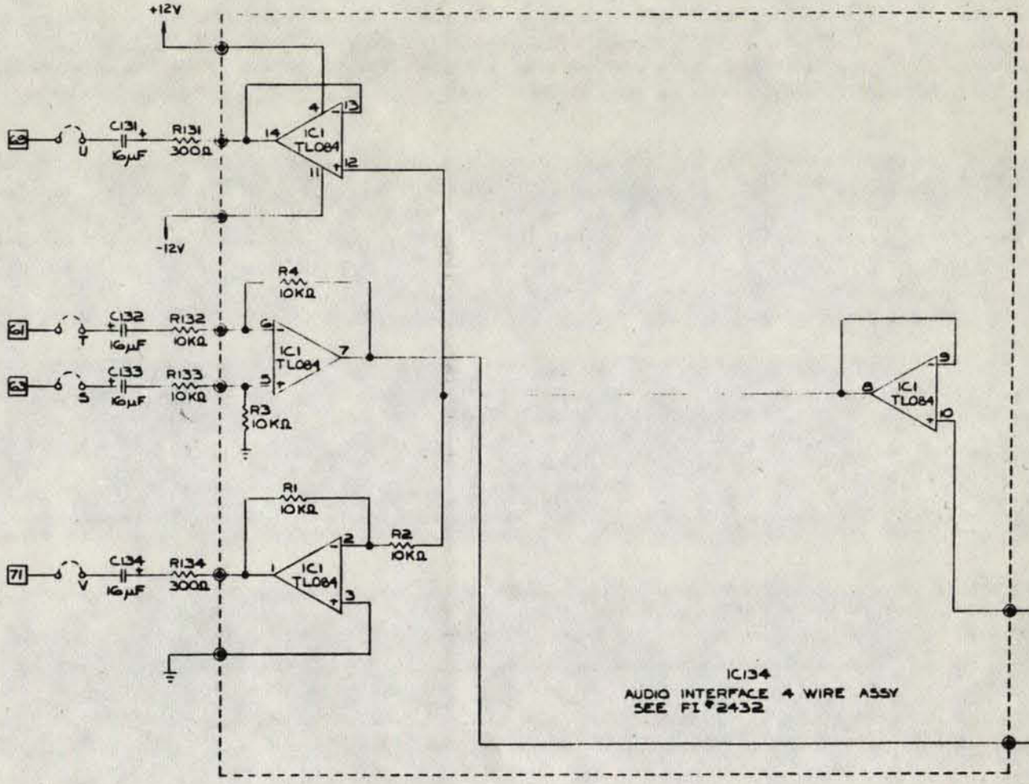
DATE: 82-07-16 | PROJ NO: 810113 | DRAWN BY: J. WHITEMAN

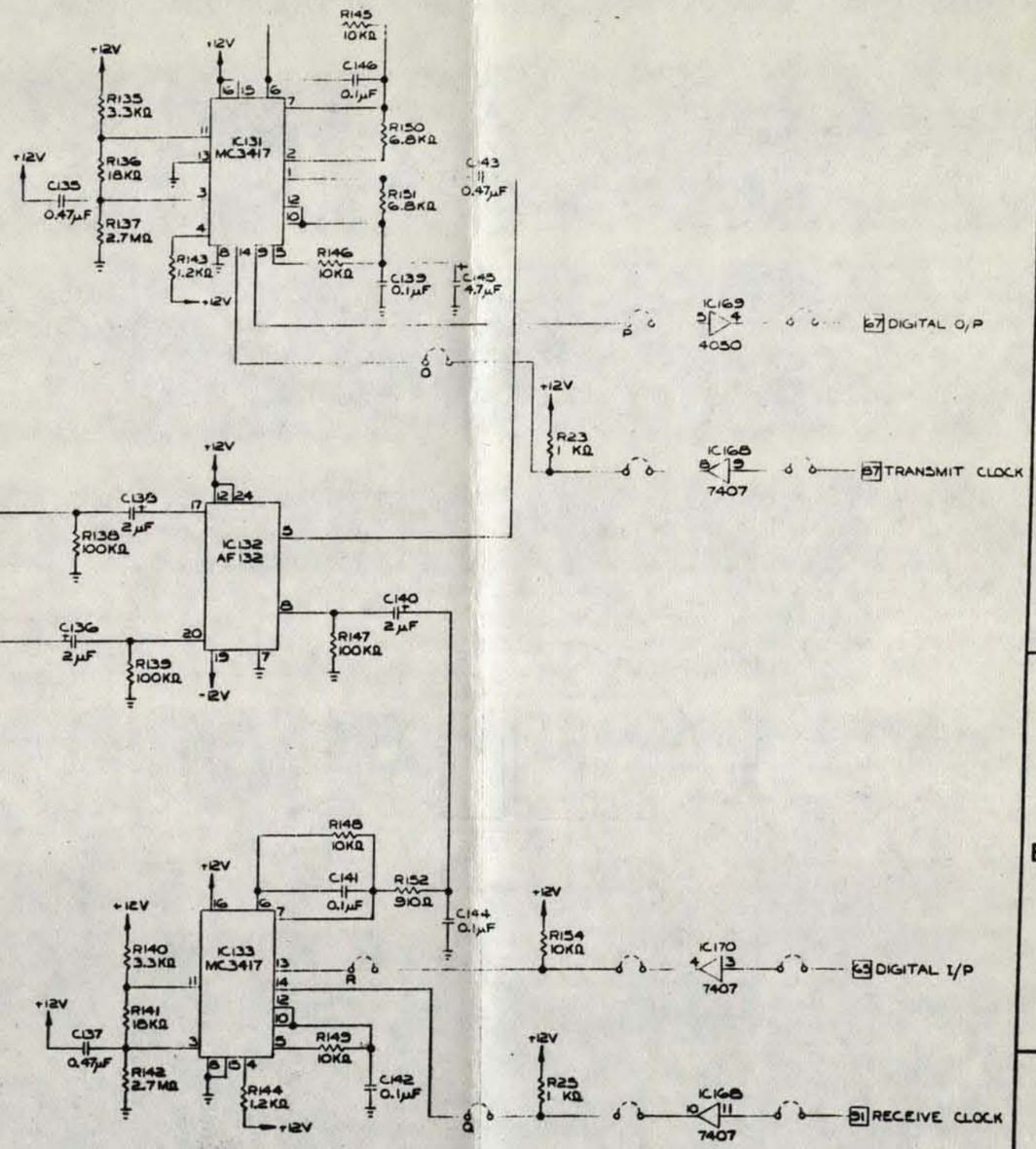
DUPLEX VOICE TRANSMISSION CODEC

MATERIAL: | SCALE: | SHEET 4 OF 6

FINISH: | APPROVAL: R. Yuen 17/07/83 | DWG NO: D2385

REV	DATE	REVISIONS DESCRIPTIONS





CHANNEL 5

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-07-16 | PROJ. NO: 81013 | DRAWN BY: J. WHITEMAN

DUPLEX VOICE TRANSMISSION CODEC

MATERIAL: | SCALE: | SHEET 5 OF 6

FINISH: | APPROVAL: C. Gar 17/8/82 | DWG NO: D2385

REVISIONS		
REV	DATE	DESCRIPTIONS

IC.164
AUDIO INTERFACE 4 WIRE ASSY
SEE FI #2432

GAIN ADJUST

CHANNEL 6

IC.166
AUDIO INTERFACE 2 WIRE ASSY
SEE FI #2436

PHASE LAG ADJUST

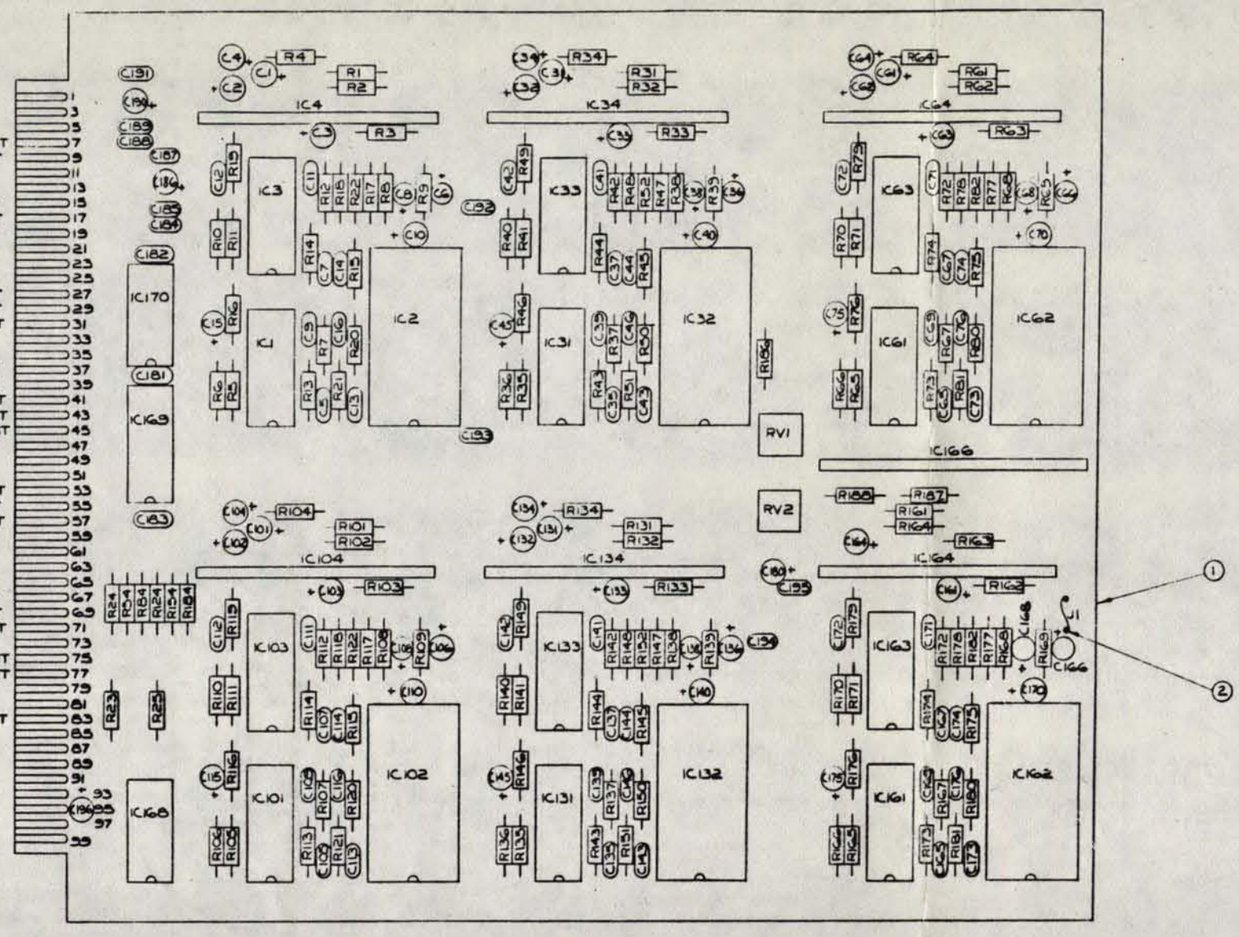
IC.166
AUDIO INTERFACE 2 WIRE ASSY
SEE FI #2436

NOTE
1) C.162 & C.163 ARE NOT USED

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY #D2387, #2432 #2436			

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES 1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-06-21	PROJ NO: 810113	DRAWN BY: J. WHITEMAN
	DUPLEX VOICE TRANSMISSION CODEC		
MATERIAL:		SCALE:	SHEET 6 OF 6
FINISH:		APPROVAL: R.J. 17/82/05	DWG NO: #D2385

REVISIONS		
REV	DATE	DESCRIPTIONS



INFORMATION CONTAINED IN THIS DRAWING IS PROPRIETARY TO FOUNDATION INSTRUMENTS AND SHALL NOT BE DISCLOSED TO ANYONE OTHER THAN PERSONS AUTHORIZED BY THE COMPANY TO WHOM FOUNDATION INSTRUMENTS HAS FURNISHED THIS DRAWING

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ± .010, .XXX ± .005, ANGLES ±1/2°	FOUNDATION INSTRUMENTS OTTAWA		
SURFACES:	DATE: 82-08-24	PROJ. NO: 810113	DRAWN BY: J. WHITEMAN
REMOVE BURRS & SHARP EDGES	DUPLEX VOICE TRANSMISSION CODEC - COMP. LAY		
MATERIAL:		SCALE: 2/1	SHEET 1 OF 2
FINISH:		APPROVAL: R. Yuen 17/02/83	DWG NO: D2387

ITEM	QTY	PART NO.	DESCRIPTION
C180	1		CAPACITOR, 1 µF, TANTALUM
C196	3		CAPACITOR, 10µF, TANTALUM
C186, 190			
C175	6		4.7 µF, TANTALUM
C178, 195			
C15, 45, 75			
C188, 189	43		0.1µF, CERAMIC
C185, 187			
C194, 195			
C192, 193			
C184, 191			
C182, 183			
C176, 181			
C172, 174			
C163, 171			
C144, 146			
C141, 142			
C116, 133			
C112, 114			
C105, 111			
C72, 79, 76			
C46, 69, 71			
C41, 42, 44			
C19, 1639			
C3, 11, 12			
C170	18		2µF, TANTALUM
C166, 168			
C138, 140			
C10, 136			
C106, 108			
C66, 68, 70			
C36, 38, 40			
C6, 8, 10			
C173	18		0.47µF, CERAMIC
C165, 167			
C137, 143			
C113, 135			
C103, 107			
C63, 67, 73			
C35, 37, 43			
C5, 7, 13			
C161, 164	22		CAPACITOR, 16µF, TANTALUM
C133, 134			
C131, 132			
C103, 104			
C101, 102			
C63, 64			
C34, 61, 62			
C31, 32, 33			
C1, 2, 3, 4			
RV2	1		VARIABLE RESISTOR, 1KΩ
RV1	1		VARIABLE RESISTOR, 10KΩ
R188	3		RESISTOR, 1/4W, 1KΩ, ±5%
R186, 187			
R182	6		510Ω
R122, 152			
R22, 52, 82			
R180, 181	12		6.8KΩ
R150, 151			
R120, 121			
R51, 80, 81			
R20, 21, 50			
R173, 174	12		RESISTOR, 1/4W, 1.2KΩ, ±5%
R143, 144			
R113, 114			
R44, 73, 74			
R13, 14, 43			

ITEM	QTY	PART NO.	DESCRIPTION
R177	18		RESISTOR, 1/4W, 100KΩ, ±5%
R168, 169			
R139, 147			
R117, 138			
R108, 109			
R8, 6, 77			
R38, 39, 47			
R8, 9, 17			
R167, 172	12		2.7MΩ
R137, 142			
R107, 112			
R42, 72			
R7, 2, 37			
R166, 171	12		18KΩ
R136, 141			
R106, 111			
R41, 66, 71			
R6, 11, 36			
R165, 170	2		3.3KΩ
R135, 140			
R105, 110			
R40, 65, 70			
R5, 10, 35			
R184	42		10KΩ
R178, 179			
R175, 176			
R162, 163			
R149, 154			
R146, 148			
R133, 145			
R129, 132			
R118, 119			
R115, 116			
R102, 103			
R79, 84			
R75, 76, 78			
R54, 62, 63			
R46, 48, 49			
R32, 33, 45			
R24			
R16, 18, 19			
R2, 3, 15			
R164	12		RESISTOR, 1/4W, 300Ω, ±5%
R134, 161			
R104, 131			
R2, 69, 101			
R1, 4, 31, 34			
R23, 25	2		RESISTOR 1/4W, 1KΩ, ±5%
IC169	1	4050	INTEGRATED CIRCUIT
IC168, 170	2	7407	INTEGRATED CIRCUIT
IC166	1	*2436	AUDIO INTERFACE 2 WIRE ASSY FI
IC134, 164	6	*2432	AUDIO INTERFACE 4 WIRE ASSY FI
IC64, 104			
IC4, 34			
IC162	6	AF132	INTEGRATED CIRCUIT
IC102, 132			
IC2, 32, 62			
IC163	12	MC3417	INTEGRATED CIRCUIT
IC133, 161			
IC103, 131			
IC63, 101			
IC33, 61			
IC1, 3, 31			
2	2	1553763-0104-00	PIN, WIRE WRAP .025SQx.787 LONG CAMBION
1	1	*2386A	PRINTED CIRCUIT BOARD FI
ITEM	QTY	PART NO.	DESCRIPTION

REV	DATE	REVISIONS DESCRIPTIONS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

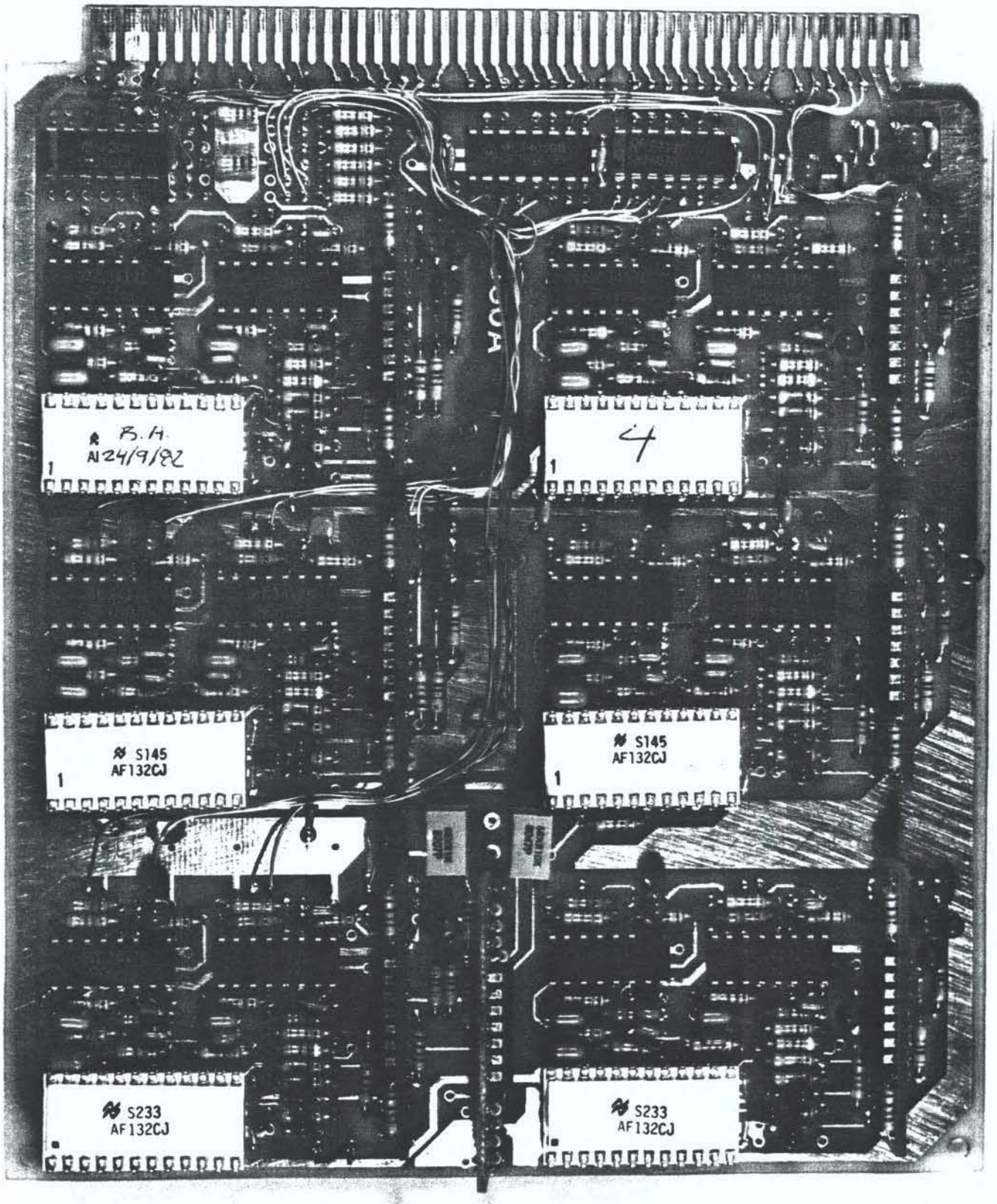
FOUNDATION INSTRUMENTS OTTAWA

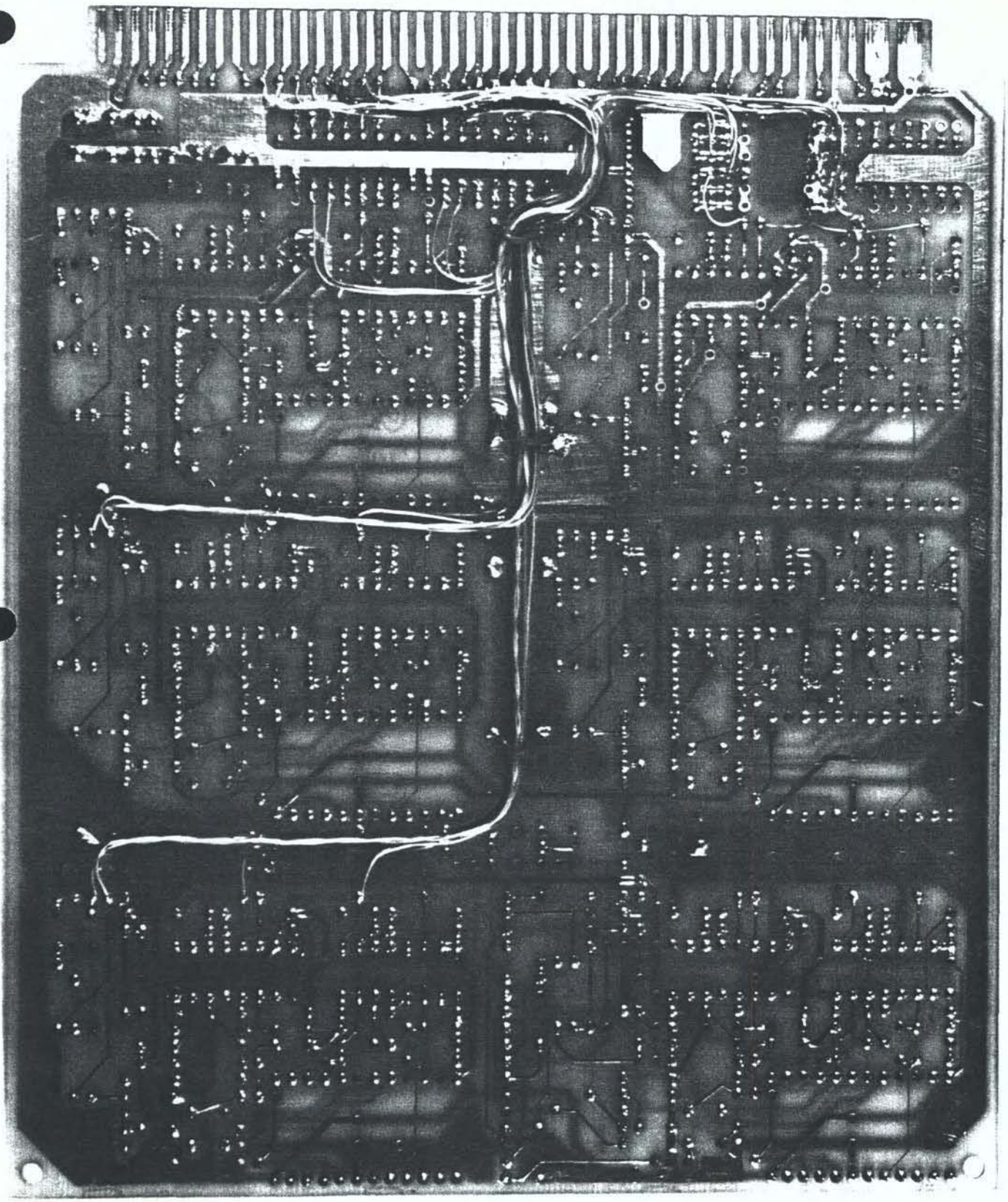
DATE: 82-08-24 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

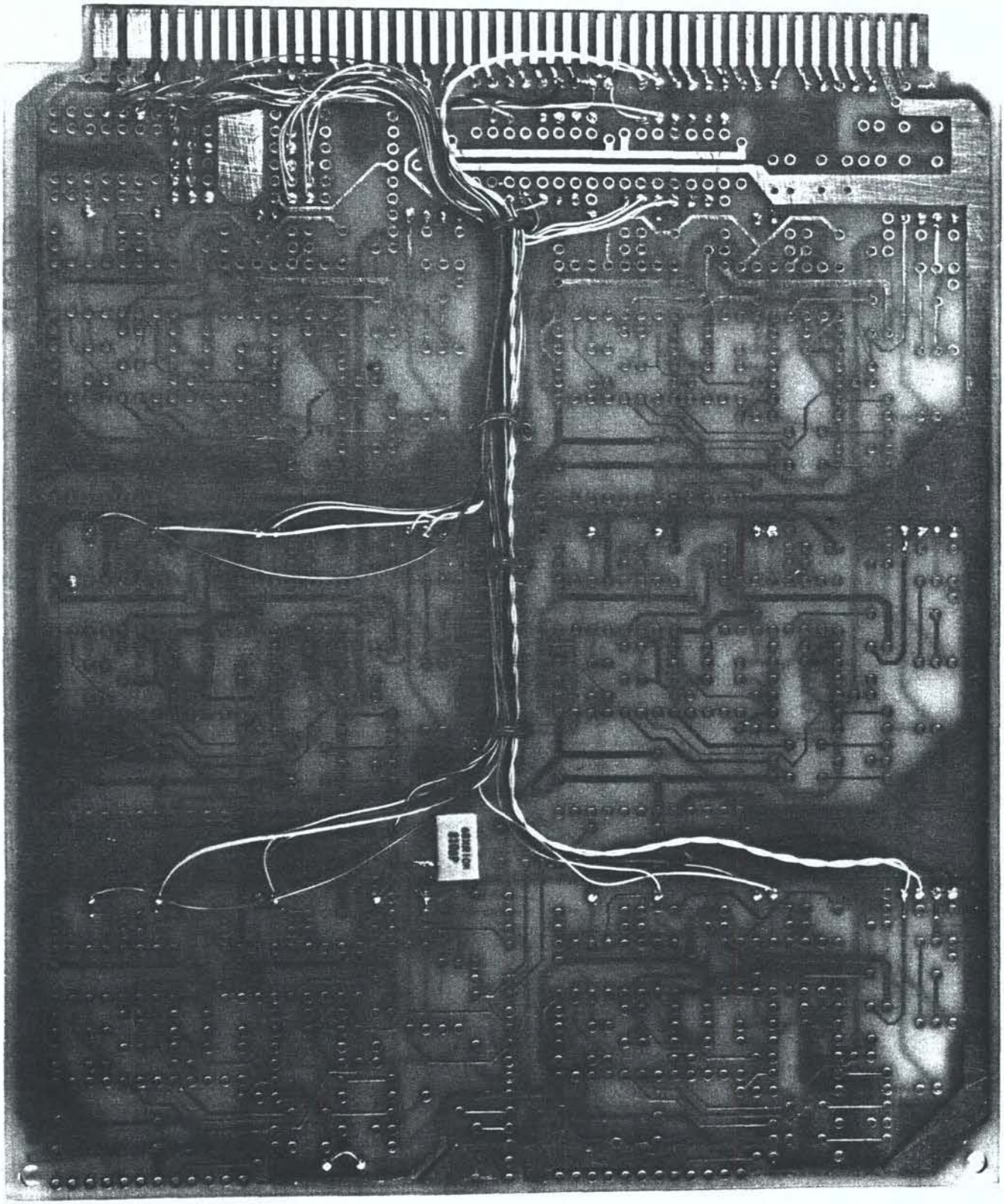
DUPLEX VOICE TRANSMISSION CODEC-COMP. LAY

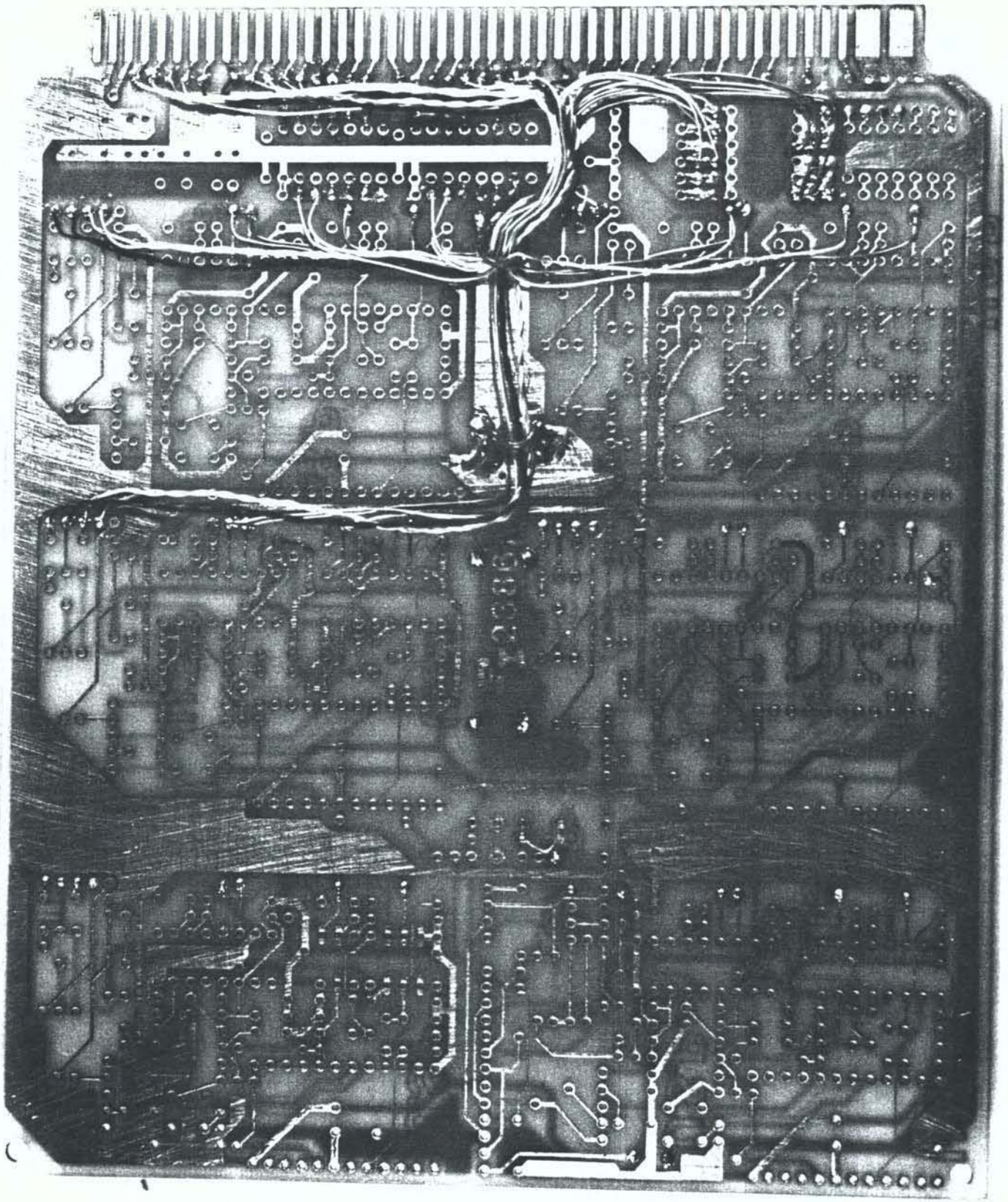
MATERIAL: | SCALE: | SHEET 2 OF 2

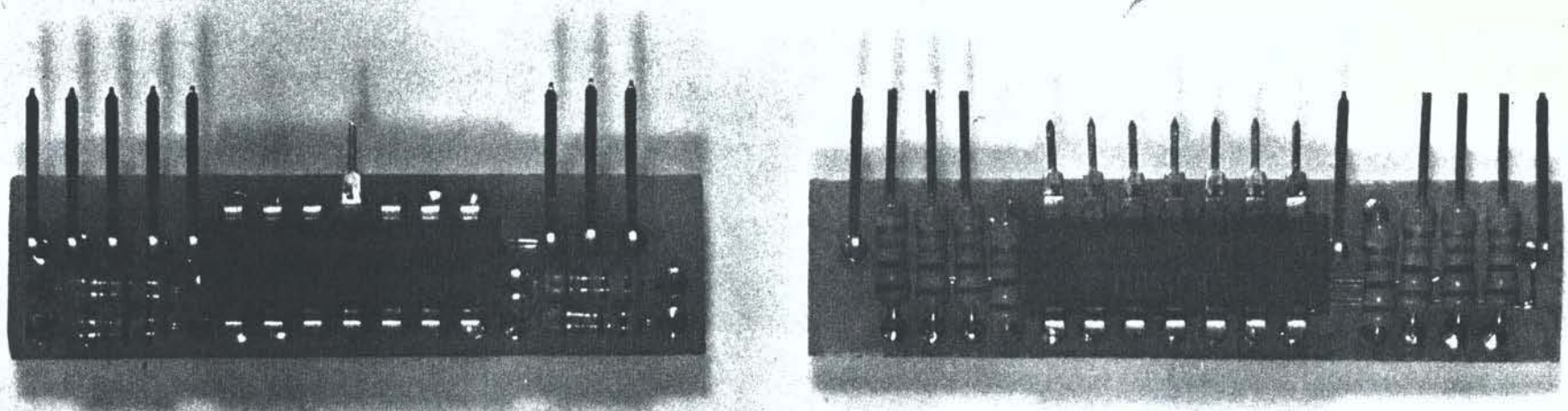
FINISH: | APPROVAL: 17/08/83 | DWG NO: *D2387


B.H.
AI 24/9/82
4
S145
AF132CJ
S145
AF132CJ
S233
AF132CJ
S233
AF132CJ

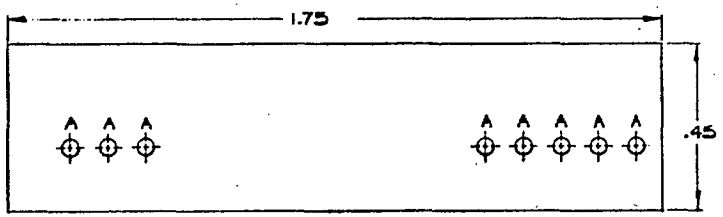








REVISIONS		
. REV	DATE	DESCRIPTIONS



COMP. SIDE

HOLE DATA		
SYM	DESCRIPTION	QTY
A	.045 DIA. (FINISHED)	8
OTHER	.037 DIA. (FINISHED)	

NOTES
1) ALL HOLES TO BE DRILLED ON PAD CENTERS

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS
OTTAWA

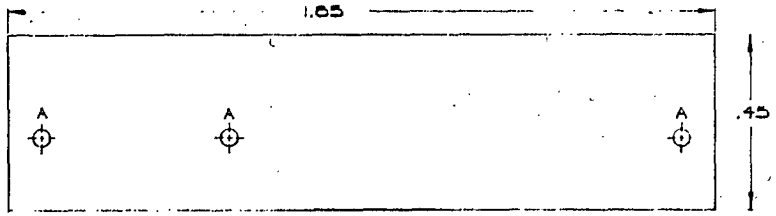
DATE: 82-07-20 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

AUDIO INTERFACE, 4 WIRE - MASTER

MATERIAL: G10, .062 THK GLASS EPOXY 1 OZ. COPPER EACH SIDE | SCALE: 4/1 | SHEET OF

FINISH: TIN-LEAD PLATE, .0002/.0003 THK | APPROVAL: R.Yor 11/02/95 | DWG NO: #2433

REVISIONS		
REV	DATE	DESCRIPTIONS



-44-

HOLE DATA		
SYM	DESCRIPTION	QTY
A	.045 DIA. (FINISHED)	3
OTHER	.037 DIA. (FINISHED)	

NOTES
1) ALL HOLES TO BE DRILLED ON PAD CENTERS

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

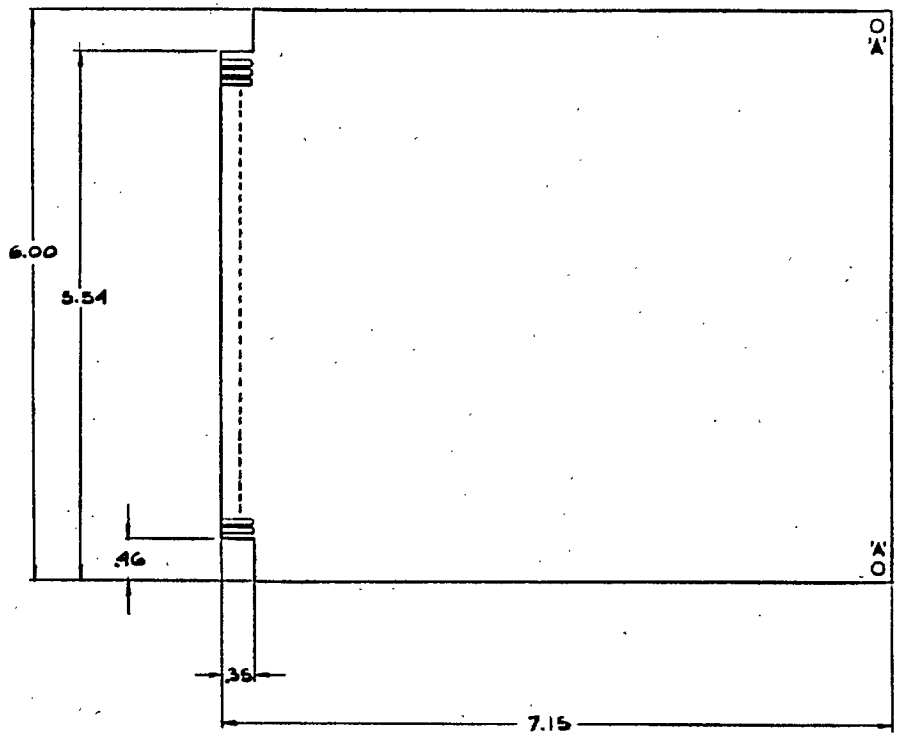
DATE: 82-07-20 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

AUDIO INTERFACE, 2 WIRE - MASTER

MATERIAL: G10, .062 THK, GLASS EPOXY 1 OZ COPPER EACH SIDE | SCALE: 4/1 | SHEET OF

FINISH: TIN-LEAD PLATE, .0002/.0003 THK | APPROVAL: R. Yan 17/08/82 | DWG NO: *2437

REVISIONS		
REV	DATE	DESCRIPTIONS



HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA (FINISH)	2
OTHER	.037 DIA (FINISH)	

-45-

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY		2387	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

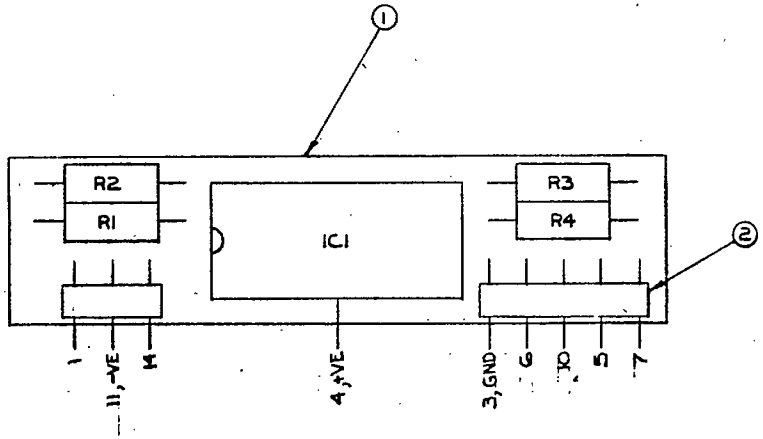
DATE: 82-08-18 | PROJ. NO: 810113 | DRAWN BY: P.D.

DUPLEX TX VOICE CIRCUIT MASTER

MATERIAL: G10, .062 THK. GLASS EPOXY 1 OZ. COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

FINISH: TIN PLATE .0002/.0003 THK CTS. GOLD .0001/.0002 THK | APPROVAL: R. Yu 17/08/93 | DWG NO: 2388

REVISIONS		
REV	DATE	DESCRIPTIONS



ITEM	QTY	PART NO.	DESCRIPTION	
R3,4 R1,2	4		RESISTOR, 1/4W, 10KΩ, ±5%	
IC1	1	TL084	INTEGRATED CIRCUIT	
2		929835-01-R	HEADER STRIP	AP
1	1	PCB# 2431A	PRINTED CIRCUIT BOARD	FI

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

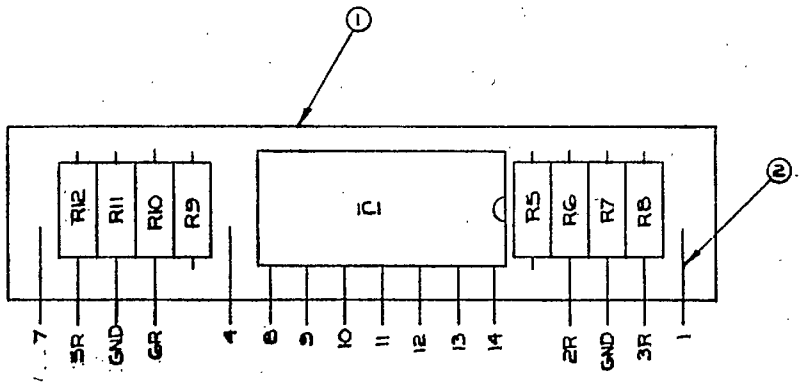
DATE: 82-07-20 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

AUDIO INTERFACE, 4 WIRE - COMP. LAYOUT

MATERIAL: | SCALE: 4/1 | SHEET OF

FINISH: | APPROVAL: R.G. 1982/10/21 | DWG NO: # 2432

REVISIONS		
REV	DATE	DESCRIPTIONS



ITEM	QTY	PART NO.	DESCRIPTION	
R11, R12 R8,9,10 R5,6,7	8		RESISTOR, 1/4W, 10KΩ, ±5%	
IC1	1	TL084	INTEGRATED CIRCUIT	
2		929835-01-R	HEADER STRIP	AP
1	1	PCB*2435	PRINTED CIRCUIT BOARD	FI

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-07-20	PROJ. NO: 810113	DRAWN BY: J.WHITEMAN
	AUDIO INTERFACE, 2 WIRE - COMP. LAYOUT		
MATERIAL:		SCALE: 4/1	SHEET OF
FINISH:		APPROVAL: R Yee 17/02/83	DWG NO: *2436

3.7 Data Multiplexer

This section describes the data multiplexer theory of operation. This section contains the following:

i) Block diagram
ii) Schematic D2205
iii) Overlay D2207
iv) Photographs, PCB 2206A component and solder side
v) Mechanical 2208 drilling diagram.

THEORY OF OPERATION

Module: Land Tactical Data Multiplexer (FI-2206A)
Schematic No. D2205
Component Overlay No. D2207

Operational Description:

See accompanying block diagram and schematic no. D2205.

MIL-STD-188C Interface:

Converts incoming data from MIL-STD-188C to TTL levels.

S1 to S6:

Manual switches that provide a choice between codec or data information to be supplied to the multiplexer over channels 1-12.

Multiplexer:

IC14 and IC18 multiplex 11 and 16 channels of digital information respectively, and are coordinated by the Multiplexer Controller.

Combiner:

Logically ANDs the outputs of IC14 and IC18 into one multiplexed stream of 27 channels, 24 channels being data. The others are the parity, F-bit and Codec clock channels. Jumper J1 provides the option of isolating the multiplexer from the remainder of the system for trouble shooting purposes.

Multiplexer Controller:

Coordinates the multiplexing operation by enabling IC14 and IC18 alternately and generating the multiplexer sequence.

The controller consists of 2 cascaded synchronous counters. The first, IC15 sequences through either multiplexer channels 1-11 or channels 12-27 depending whether IC14 or IC18 is enabled by the second synchronous counter, IC17. After one complete multiplexer cycle both counters are preset. IC15 is preset to count from decimal 5 to 15 and IC17 is preset to enable IC14 throughout this 11 channel sequence. Upon count 16, IC17 enables IC18 instead, and a 1 to 16 count is initiated by IC15 to cycle through the remaining 16 channels. On the next clock cycle, the counters are preset again and the multiplexing sequence is repeated.

F-Bit Generator:

Provides an alternating frame-synch bit at channel 27 of the multiplexer by means of a toggling D-type flip-flop, clocked by the 27th count transition of the cascaded counters IC15 and IC17.

Codec CK Generator:

Divides the alternating F-bit frequency by 2 and is sent to the transmitting codecs as well as through multiplexer channel 26, so as to drive both transmitting and receiving codecs by the same clock.

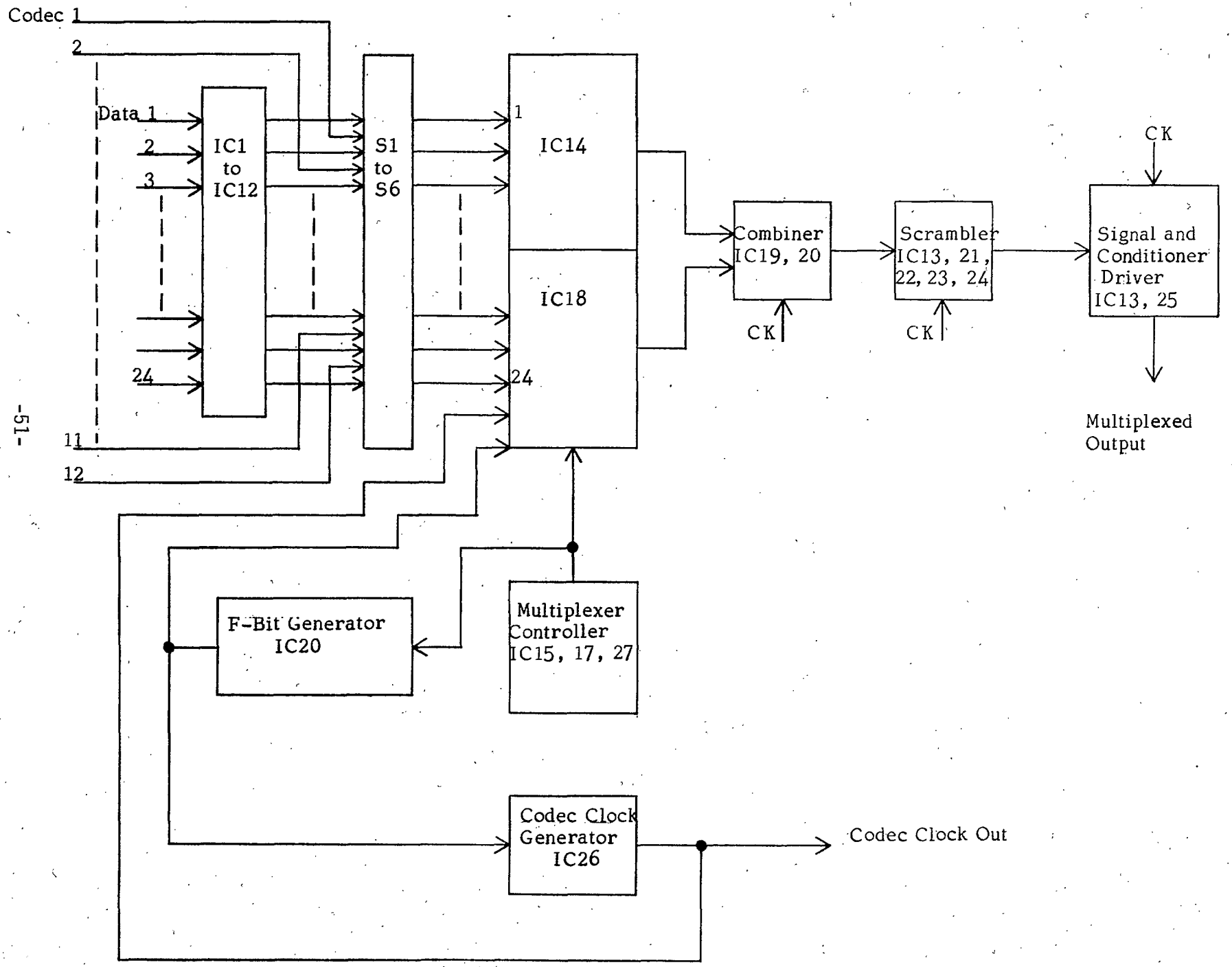
Scrambler:

Encodes the multiplexed digital stream. IC23 prevents more than ten digital HIGHs or LOWs appearing in a row. Jumper J2 may be optionally set to connect IC24 pin 12 to GND so as to disable the scrambler.

Signal Conditioner and Driver:

Corrects output clock/data relationship and provides off board drive capibility at TTL levels.

Land Tactical Multiplexer (D2205)



REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-05-03	DESIGN CHANGE W.O.# 2146
B	82-05-06	IC.20 ADDED W.O. # 2153
D	82-10-25	DESIGN CHANGE W.O.# 2340

LAST NO. USED
R3
C56
IC27
SG
J2
TP48

NOTES
1) IC1 THRU IC12, PIN 3.14, +5V
PIN 16, +12V
PIN 9, -12V
PIN 8 - GND (G3)
2) IC1 THRU IC12, PIN 16 IS A.C. COUPLED TO GND THRU A 0.1UF CAPACITOR (C21 TO C32)
3) IC1 THRU IC12, PIN 9 IS A.C. COUPLED TO GND (G3) THRU A 0.1UF CAPACITOR (C33 TO C44)
4) IC1,2,3,7,8,9 PINS 3 & 14 ARE A.C. COUPLED TO GND THRU A 0.1μF CAPACITOR (C52,C53,C54,C55,C56,C13)
5) ALL GNDS ARE G3
6) S1 - S6 ARE GRAYHILL 76ST002 DPDT DIP SWITCHES
7) ALL UNUSED EDGE CONNECTOR CONTACTS ARE TO BE CONNECTED TO BOARD DIGITAL GND G3

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

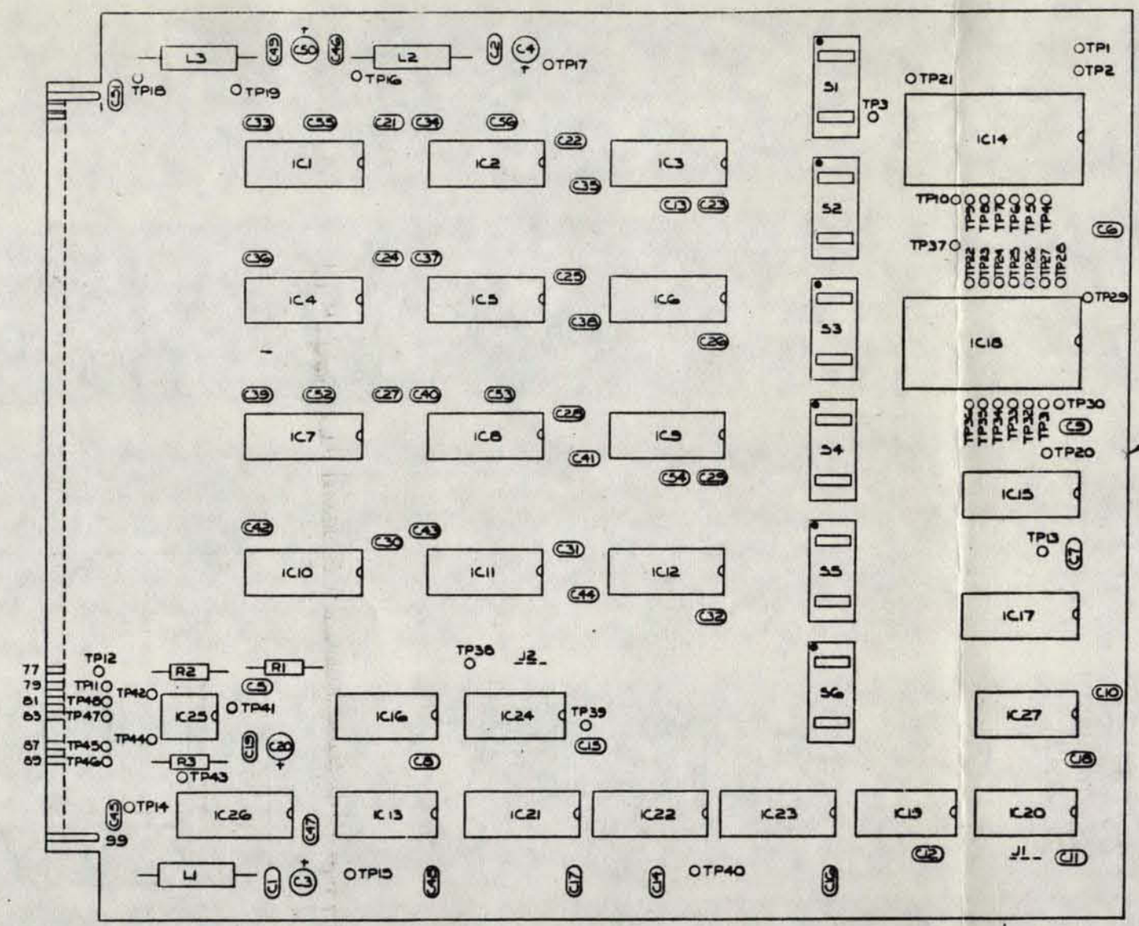
DATE: 82-03-24 | PROJ. NO: 81013 | DRAWN BY: LWHITEMAN

LAND TACTICAL DATA MULTIPLEXER - SCHEM.

MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: R Uber 04/02/83 | DWG NO: D2205

REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-10-25	DESIGN CHANGE W.O.# 2340



ITEM	QTY	PART NO.	DESCRIPTION
J1, 2			JUMPER, INSULATED, SOLID #22 AWG
TP1-48	48	20-2137D	TEST POINT VERO
S4,5,6 S1,2,3	6	76STD02	SWITCH, DIP, TOGGLE, DPDT GRAYHILL
L1,2,3	3	VK200-20/4B	COIL FERROXCUBE
C20,50 C3,4	4	TAP10M16	CAPACITOR, 10μF, 16V, TANTALUM ITT
C54,55,56 C51,52,53 C47,48,49 C44,45,46 C41,42,43 C38,39,40 C35,36,37 C32,33,34 C29,30,31 C26,27,28 C23,24,25 C19,21,22 C16,17,18 C13,14,15 C10,11,12 C7,8,9 C1,2,3,4	52	3439-050E-104M	CAPACITOR, 0.1μF, 50V, CERAMIC AVX
R1,2,3	3		RESISTOR, 220Ω, 1/4W, ±5%
IC27	1	74LS04	INTEGRATED CIRCUIT
IC25	1	75451	
IC24	1	74LS86	
IC21,22	2	74LS175	
IC20,13	2	74LS74	
IC19	1	74LS20	
IC16	1	7404	
IC23,26	4	74LS163	
IC15,17			
IC14,18	2	74150	
IC12 IC10,11 IC7,8,9 IC4,5,6 IC1,2,3	12	3627	INTEGRATED CIRCUIT
1	1	#2206	PRINTED CIRCUIT BOARD FI

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: XX ±.010
XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

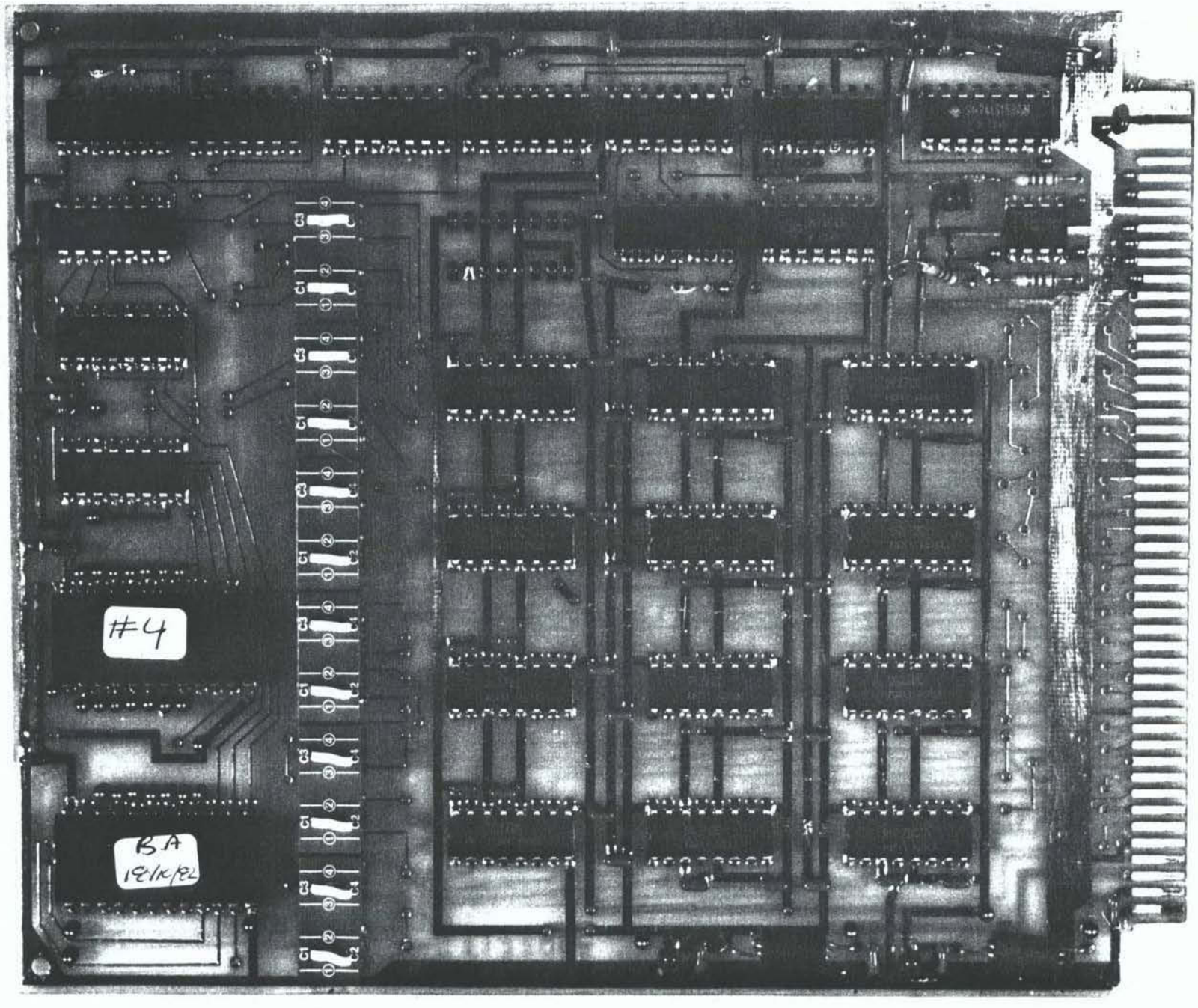
FOUNDATION INSTRUMENTS OTTAWA

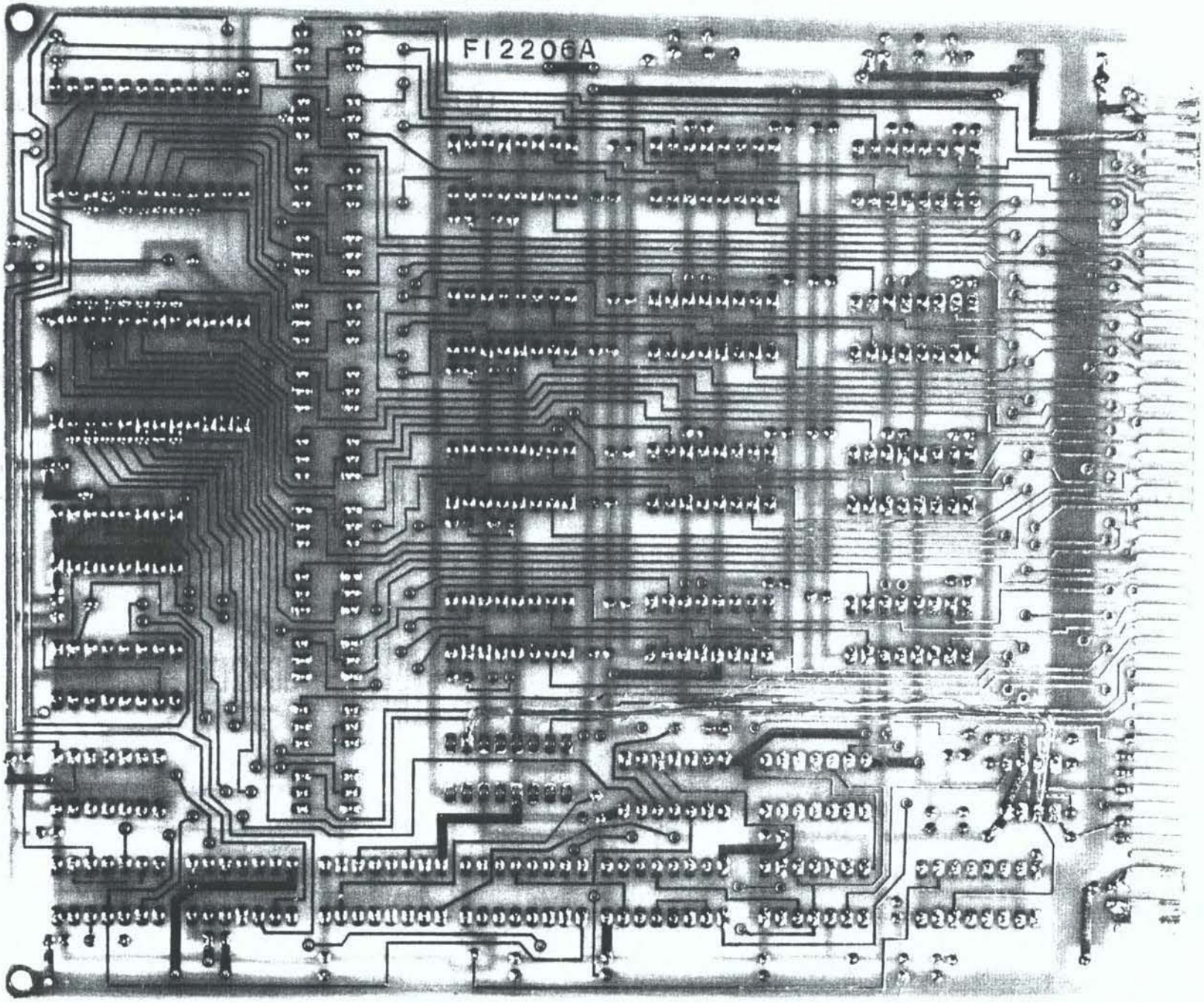
DATE: 82-09-03 | PROJ. NO: 81013 | DRAWN BY: L.WHITEMAN

LAND TACTICAL DATA MULTIPLEXER - COMP. LAYOUT

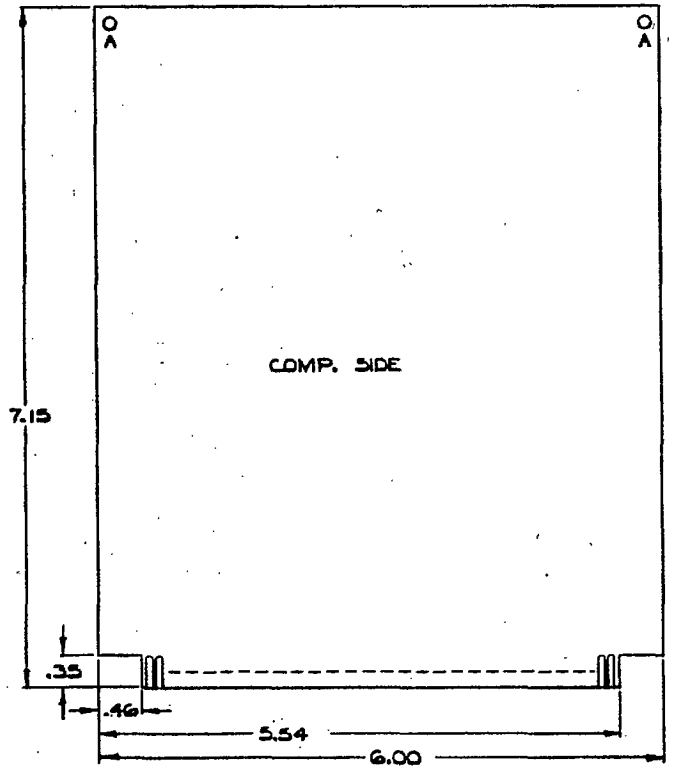
MATERIAL: | SCALE: 2/1 | SHEET OF

FINISH: | APPROVAL: K.Y. 01/02/84 | DWG NO: #D2207


#4
BA
16K/82


FI2206A

REVISIONS		
REV	DATE	DESCRIPTIONS



HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA. (FINISHED)	2
OTHER	.037 DIA. (FINISHED)	

NOTE
1) ALL HOLES TO BE DRILLED ON PAD CENTERS

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-09-02 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

LAND TACTICAL DATA MULTIPLEXER - MASTER

MATERIAL: G10, .062 THK, GLASS EPOXY 1 OZ. COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

FINISH: TIN-LEAD PLATE, .0002/.0003 THK CONT. GOLD .0001/.0002 THK | APPROVAL: K. Yor 17/02/84 | DWG NO: #2208

3.8 Data and Video Transmitter

This section contains the theory of operation for the data and video transmitter. Included in this section are the following:

i) Block diagram
ii) Schematic D2201
iii) Overlay 2203
iv) Photograph, PCB 2202B component and solder side
v) Mechanical 2204 drilling diagram.

THEORY OF OPERATION

Module: Data and Video Transmitter Board (FI-2202B)
Schematic D2201
Component Overlay D2203

Operational Description:

The circuitry on this card takes the video input signal and the multiplexed data signal which it encodes by phase-shift keying (PSK) and combines them for transmission by the fibre optic transmitter (FOTX). It also generates the clock which drives the data multiplexer. See accompanying block diagram and schematic D2201.

Oscillator:

Provides a 12.0000 Mhz square wave which is used to generate the PSK carrier and the multiplexer clock. The frequency of oscillation of the quartz crystal, Y1 (parallel, resonnance, fundamental mode, AT cut) can be adjusted slightly by trimming C67 and C73.

Multiplexer Clock Generator:

Generates a TTL level square wave at one third the frequency of the oscillator output signal (4Mhz) using two flip-flops.(IC4)

Duty Cycle Adjustment:

The divide by 3 process accomplished by the multiplexer clock generator does not give rise to an even duty cycle in the output waveform. It is therefore rounded off by C69 and a d.c. shift is applied, using R51, at the input to the output driver IC3 such that a 50-50 duty cycle is present at the output to the multiplexer.

Output Driver:

Provides off-board drive capability at TTL levels.

PSK Carrier Lowpass Filter:

A lowpass filter with moderately sharp cut-off at a frequency of approximately 14Mhz to provide a 12 Mhz sinewave PSK data carrier from the oscillator output signal.

PSK Carrier Level Adjustment:

The level of PSK carrier at the LO (local oscillator) input to the double balanced mixer (M1) is set by adjusting RV1.

Input Data Buffer:

Provides buffering and on-board drive capability to data signal in at 4 megabits per second (Mbits/sec) from the data multiplexer board.

PSK Data Signal Generator:

The mode of data encoding used in this system is Phase-Shift Keying (PSK). In this scheme, a carrier at 12.0000 Mhz is modulated by a 4 Mbit/sec data stream using a double balanced mixer (M1). The carrier is applied to the local oscillator (LO) port of the double balanced mixer (DBM) while the data is applied to the intermediate frequency (IF) port. When a data transition occurs, the carrier at the radio frequency (RF) port of the DBM (M1) shifts in phase by 180°. Thus the data is now represented by the phase reversals of the carrier. For proper information transfer, the carrier must be suppressed and this is achieved by adjusting RV2. At optimum, the carrier levels on either side of a transition are equal at the output

of the DBM.(See figure 1)

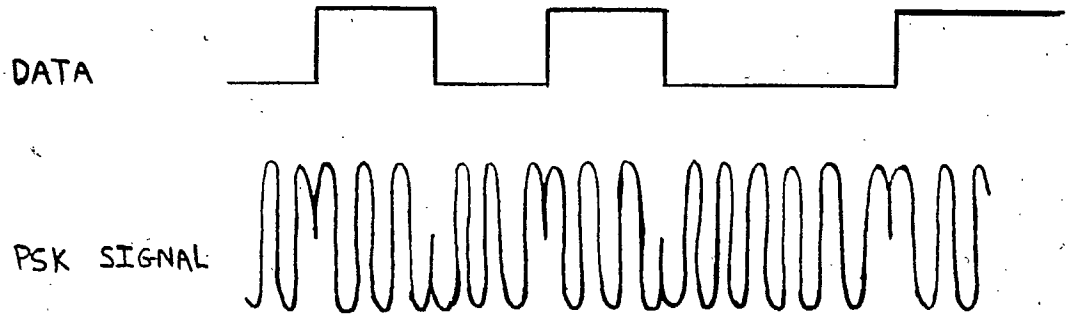


FIGURE 1

For a 12.000 Mhz carrier and a 4 Mbit/sec data stream we get a signal at the RF port which has a spectrum with a suppressed carrier at 12 Mhz, a first upper sideband extending to 16 Mhz and a first lower sideband extending to 8 Mhz. Other sidebands are present but only the first upper and lower ones are required in order to be able to recover the data. So the signal may be band limited from 8 Mhz to 16 Mhz without any degradation of the recovered data.(See figure 2)

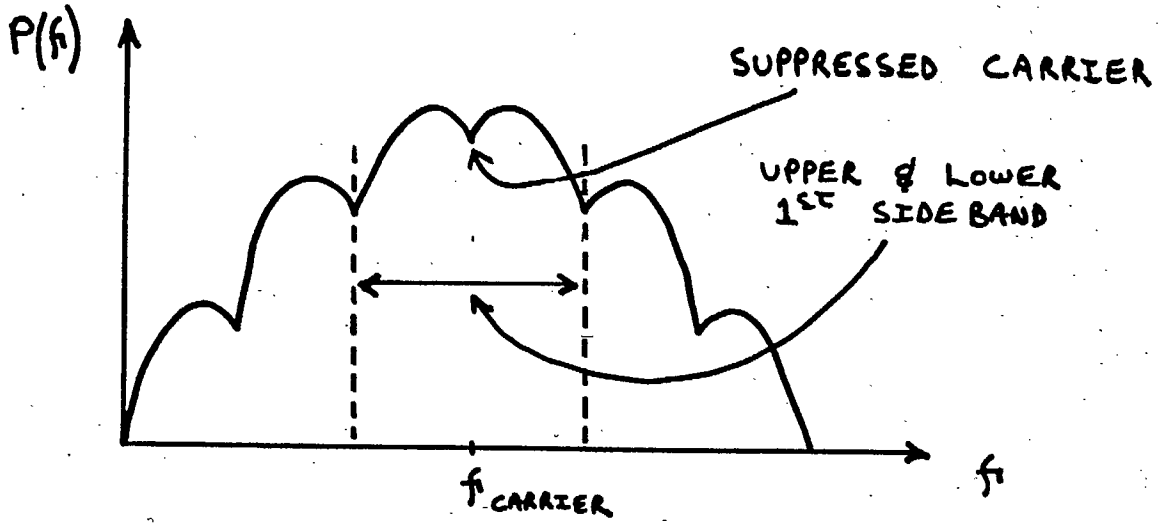


FIGURE 2

PSK Data Signal Highpass Filter:

This filter has a very sharp roll-off below 8 Mhz to remove as much data information as possible from the 0-5Mhz band which is to be dedicated to video. Since the fibre optic transmitter/receiver (FOTX/FORX) pair has a bandwidth of at least 16 Mhz, the data is easily extracted from this signal by the data recovery circuitry.

PSK Data Level Adjustment:

The PSK data signal level desired at the output to the fibre optic transmitter (FOTX) is set by adjusting RV4.

Video Signal Input:

It is differential, A.C. coupled and has an input impedance of 75 OHMS. There is an input attenuation of about 10 since the gain of the video amplifier (IC1) is approximately 10, giving close to unity gain for the combination of both. RV6 is used to null out any signals common to both inputs due to pick-up (such as 60HZ).

Video Amplifier:

IC1 is used in differential mode with the gain set by R13 approximately equal to 10. The frequency response of the video through the system can be compensated for premature roll-off by adjusting C78 to boost the input signal as desired to achieve a flat frequency response up to 5 Mhz.

Video Lowpass Band Limiting Filter:

This filter has a very sharp roll-off below 5.5 Mhz to remove as much video signal as possible from the band above 8 Mhz in which the data information is located so as to not interfere

with the data recovery.

Video Signal Level Adjustment:

The video signal level desired is set by adjusting RV3.

Video and PSK Data Signal Combiner:

The video signal voltage is converted to a signal current at the emitter of Q5 and the PSK data signal voltage is converted to a signal current at the emitter of Q6. These currents are summed at the emitter of Q7 and converted back to a voltage at the collector of Q7 via R42 which sets the gain of this stage. High frequency band limiting is provided by C77 to reject some picked up components of the 12 Mhz TTL level squarewave oscillator output.

Output Driver:

Provides a low impedance drive for the signal into the 75 ohm coax cable going to the FOTX.

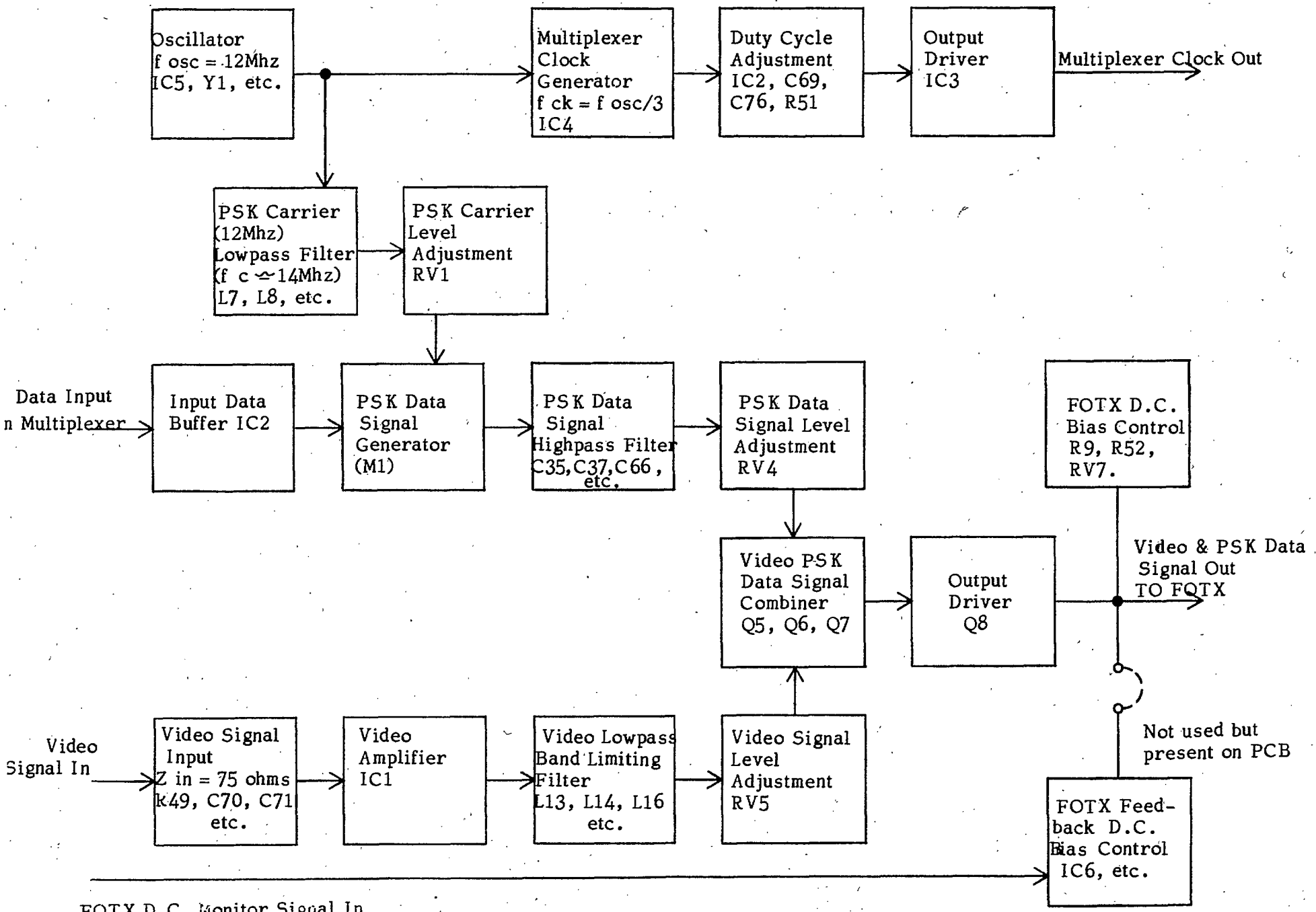
FOTX D.C. Bias Control:

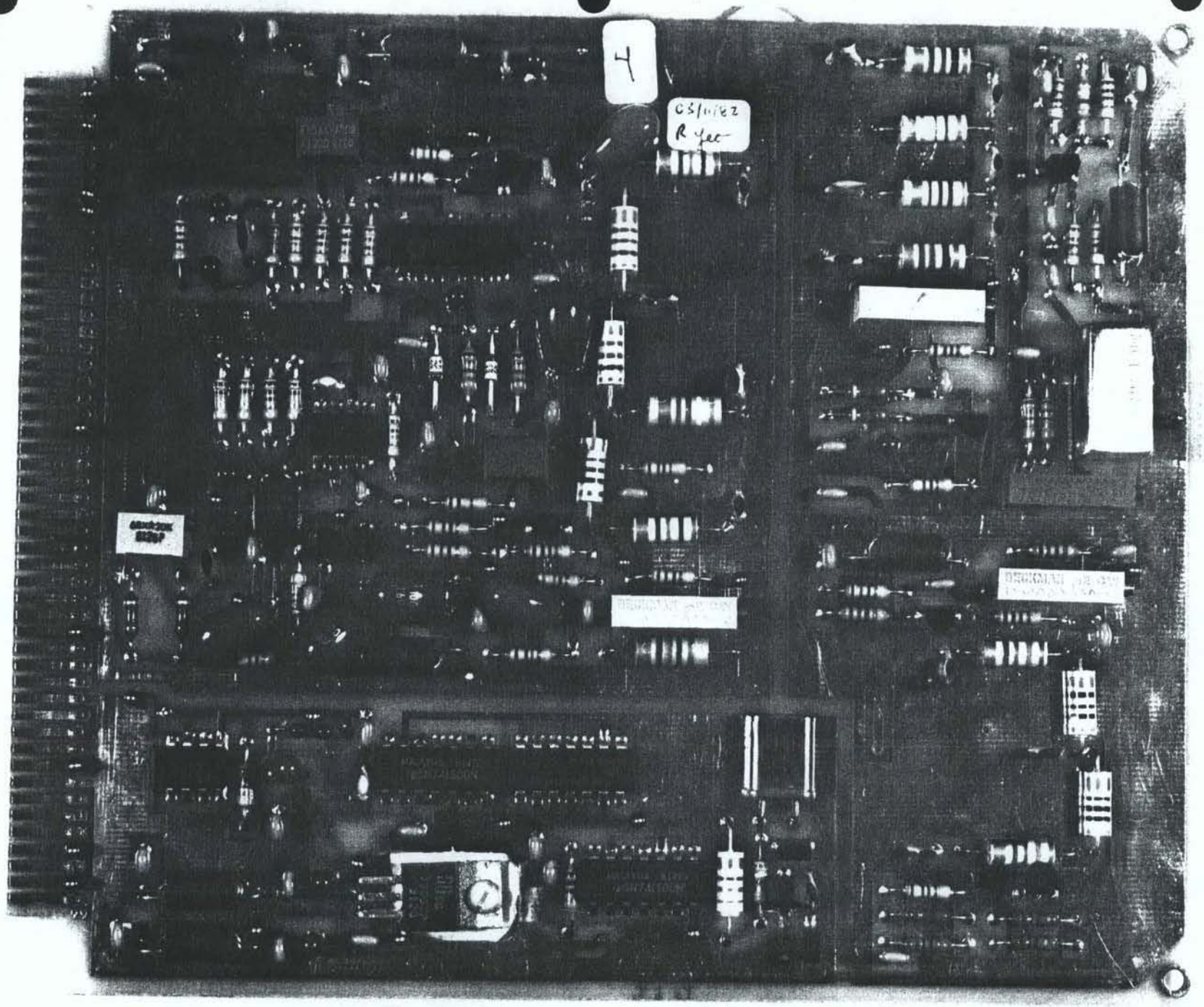
RV7 is used to set the d.c level which is required to bias the FET in the FOTX to achieve the desired LED d.c. operating current.

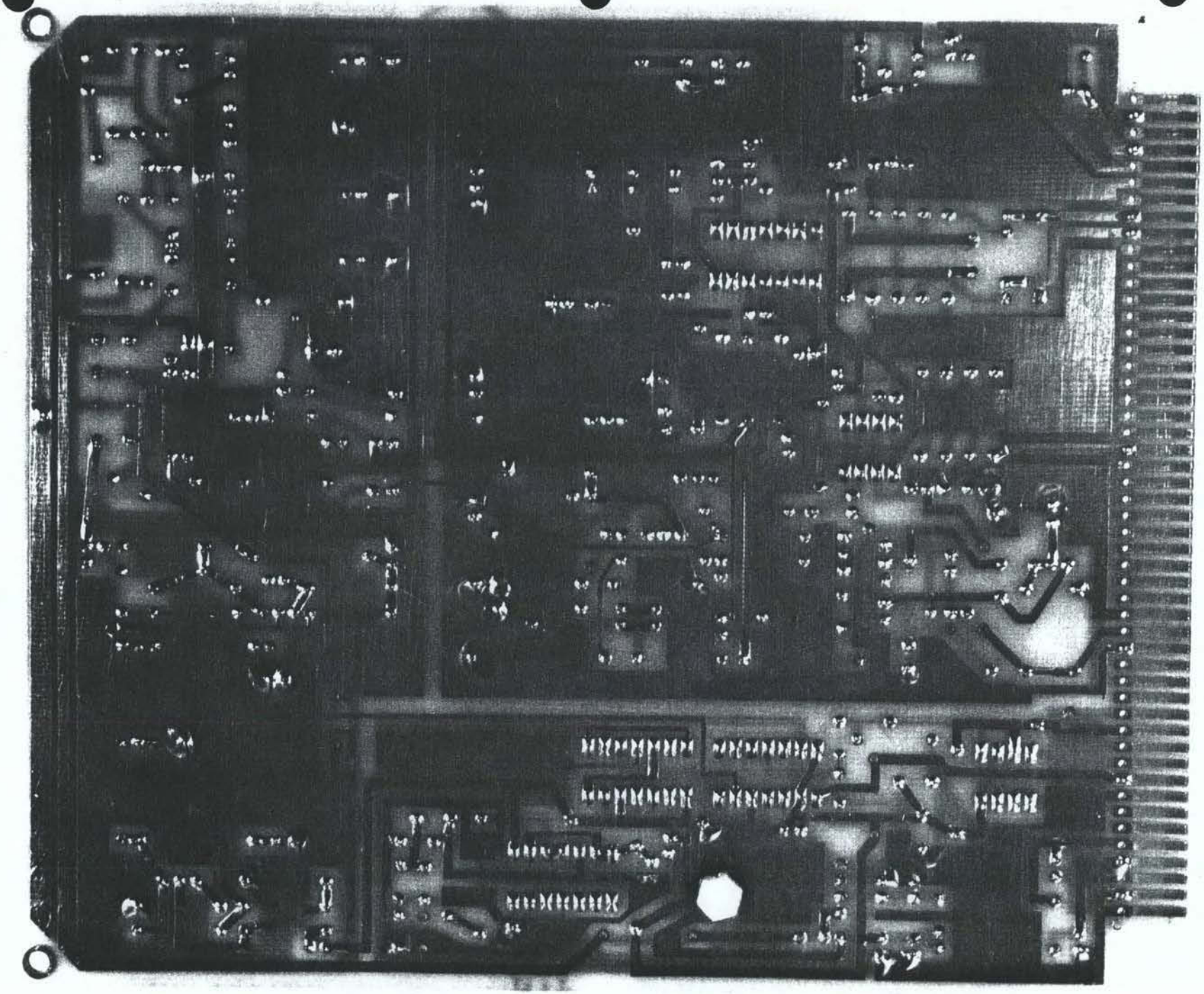
FOTX Feedback D.C. Bias Control:

Present on the board but no longer used, it monitored the current going throught the LED and adjusted the d.c. bias on the output to ensure that the current remained constant. It has been superseded by the bias control circuitry described above.

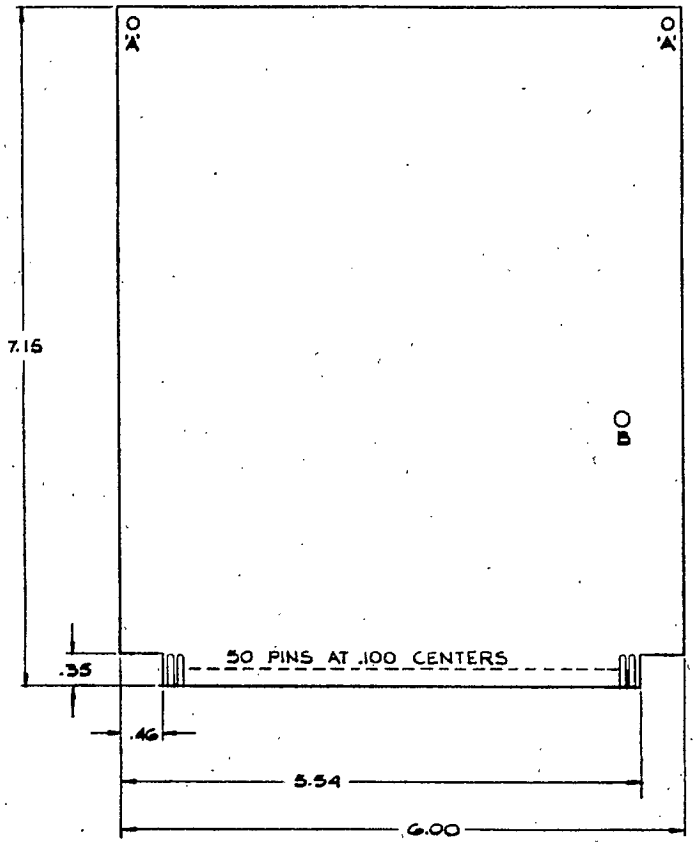
Land Tactical Data & Video Transmitter (D2201)




4
CS/11/82
R Yee



REVISIONS		
REV	DATE	DESCRIPTIONS



-88-

HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA (FINISH)	2
B	.128 DIA. (FINISH)	1
OTHER	.037 DIA (FINISH)	

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY.		# 2203	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-04-30 | PROJ. NO: 810113 | DRAWN BY: P.G.

PSK DATA & VIDEO TX - MASTER

MATERIAL: G10, .062 THK, GLASS EPOXY 1 OZ. COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

FINISH: TIN PLATE .0002/.0003 THK CONT. GOLD .0001/.0002 THK | APPROVAL: R. Yee 17/04/83 | DWG NO: 2204

3.9 PSK Data Recovery

This section contains the PSK data recovery theory of operation. Included in this section are the following:

i) Block diagram
ii) Schematic D2217
iii) Overlay 2219 sheets 1 and 2
iv) Photograph 2218B component and solder side
v) Mechanical 2220 drilling diagram.

THEORY OF OPERATION

Module: PSK Data Recovery (FI-2218B)

Schematic D2217

Component Overlay D2219

Operational Description:

As was described in the theory of operation of the data and video transmitter, the PSK data signal was obtained by modulating a local oscillator carrier with a data stream using a double balanced mixer. It can be proven from theory that if this same PSK data signal is mixed with the local oscillator carrier that was used to create it then the data can be recovered.

The circuitry on this card achieves this by recovering the local oscillator from the PSK signal, mixing it with the PSK signal and conditioning the data to achieve the desired output format.(See accompanying block diagram and schematic D2217)

Carrier Recovery:

PSK Signal Squarer:

When a PSK signal is mixed with itself, it can be shown from theory that the resultant signal has only one frequency component at twice the frequency of the PSK carrier. As a result of band limiting and pick up of higher frequency TTL signals, we get other mixing products which must be filtered out. We also get amplitude variations with bit patterns which give rise to some edge jitter in the recovered carrier. This is minimized

by having a very selective filter set to twice the carrier frequency.

In this application, the PSK input signal is buffered and adjusted for proper input levels to the double balanced mixer (M1) by Q1 and Q2. One signal is applied to the local oscillator (LO) port of M1 while the other is injected into the intermediate frequency (IF) port of M1. The output at the radio frequency (RF) port of M1 is a low level signal whose main frequency component is at exactly twice the PSK carrier frequency. In this case, the PSK carrier used is 12.0000 Mhz and the recovered signal has a main frequency component at 24.0000 Mhz.

Tuned Filters:

Two tuneable tuned filters using Q6 and Q8 are used to provide high gain and a high degree of selectivity to the output signal of the squarer around 24.0000 Mhz. Two stages are used for better performance. CV2 and CV3 are adjusted to achieve a maximum output signal at 24.0000 Mhz.

This is the most sensitive adjustment on this circuit board and care must be exercised in setting CV2 and CV3 if proper data recovery is to occur.

Buffer and Gain Stage:

As in the case of the tuned filters, FETs are used since they provide a very high input impedance which is necessary to achieve high Q filters. So Q10 simply acts as a unity gain

high input impedance buffer while Q12 provides the gain necessary to make the signal at its collector compatible with TTL logic elements.

Signal Conditioner:

It consists of an a.c. coupled d.c. biased Schmitt trigger NAND gate which provides a TTL level version of the 24.0000 Mhz signal while removing some edge uncertainty due to noise.

Carrier Recovery:

Since we have a signal at twice the carrier frequency, in digital form, it is easy to produce the carrier by dividing the signal by 2 digitally, using a flip-flop (IC2). We now have a signal which has exactly the same fundamental frequency as the PSK data carrier. It is not necessary to filter the signal to produce a sinewave since the higher frequency mixing products will be rejected at a later stage by the data signal lowpass filter.

Carrier Level Adjust Driver:

The carrier level is set by adjusting RV2 and Q15 provides the drive to the double balanced mixer (M2).

Data Recovery:

Data Signal Regenerator:

As was mentioned in the introduction, the data signal can be recovered by mixing the PSK signal with the recovered

carrier using a double balanced mixer (M2). The PSK signal is supplied to the RF port of M2 via Q3 and the recovered carrier is applied at the LO port. The data signal, with higher frequency mixing products superposed on it, is then present at the IF port of M2.

The relative phase between the PSK signal carrier and the recovered carrier will determine if the recovered data is inverted or in phase with the transmitted data. This factor is of little concern since the demultiplexer will recognize and rectify any data inversion. However, it should be noted that once the system is operating and data is recovered, the data should no longer flip from a non-inverted to an inverted state. If this condition arises, then CV2 and CV3 in the carrier recovery circuit are not properly adjusted or some transient condition caused a temporary phase shift in the recovered carrier.

Data Signal Lowpass Filter:

This lowpass filter with a very sharp roll-off above 5 Mhz is used to remove high frequency components from the data signal. It enhances the data recovered by threshold detection.

Constant Fraction Threshold Generator:

The filtered data signal is monitored and a threshold level is produced at the output of IC4. The threshold voltage is a constant fraction of the peak-to-peak voltage of the data signal regardless of data signal amplitude variations arising from different data bit patterns. The threshold level is set by RV1 and is used to adjust the duty cycle of the unconditioned recovered data at the output of the comparator, IC3.

Data Recovery:

This is performed by IC3 which compares the incoming filtered data signal to the set threshold voltage and produces the recovered, unconditioned, TTL level data. Some jitter is present on the edges of this data but this will be removed in the data conditioner once the data clock is recovered from the unconditioned data.

Clock Recovery:

Clock Extractor Ringing Circuit:

Consists of a "tank" circuit set to resonnate at a frequency equal to half the data baud rate (e.g. 2 Mhz). The scrambler circuit on the multiplexer board ensures that there will be no more than 10 consecutive ones or zeroes between transitions in the multiplexed data stream. Every time a transition appears at TP39 (see schematic), it is differentiated by the C18, R15 combination to produce a negative going pulse which sets the resonnant circuit formed by L6, C24, and CV6 into a decaying oscillation. CV6 is adjusted to obtain the right oscillating frequency such that we have a signal which is of the same frequency as the clock that was used to generate the data.

Phase Shifter:

It is used to produce a phase shift in the recovered clock such that it falls in the center of the unconditioned data bit at the conditioning flip-flop (IC10). This removes the possibility of data errors due to edge jitter of the data bit rising edge relative to that of the data clock.

Limiter:

Limits the oscillating clock signal such that its amplitude and frequency information will remain constant regardless of the data bit stream present.

Extracted Clock Conditioner:

Adjusts the unconditioned extracted clock duty cycle and produces a TTL level extracted clock signal.

Phase Comparator:

Compares the phase of the extracted clock with that of the output of the voltage controlled oscillator (VCO) and produces a control voltage which changes the frequency of oscillation of the VCO until both signals are of the same frequency and phase. At this point, there is no longer any change in the control voltage and the output of the VCO is stable.

Voltage Controlled Oscillator:

With the phase comparator, it produces a phase-locked loop (PLL) which is used to lock on to the major frequency component of the extracted clock and produce a stable recovered clock output. It is used to clock the unconditioned recovered data through the data conditioner flip-flop (IC10). The PLL removes clock edge jitter and suppresses the negative effects of minor transients on the clock recovery process.

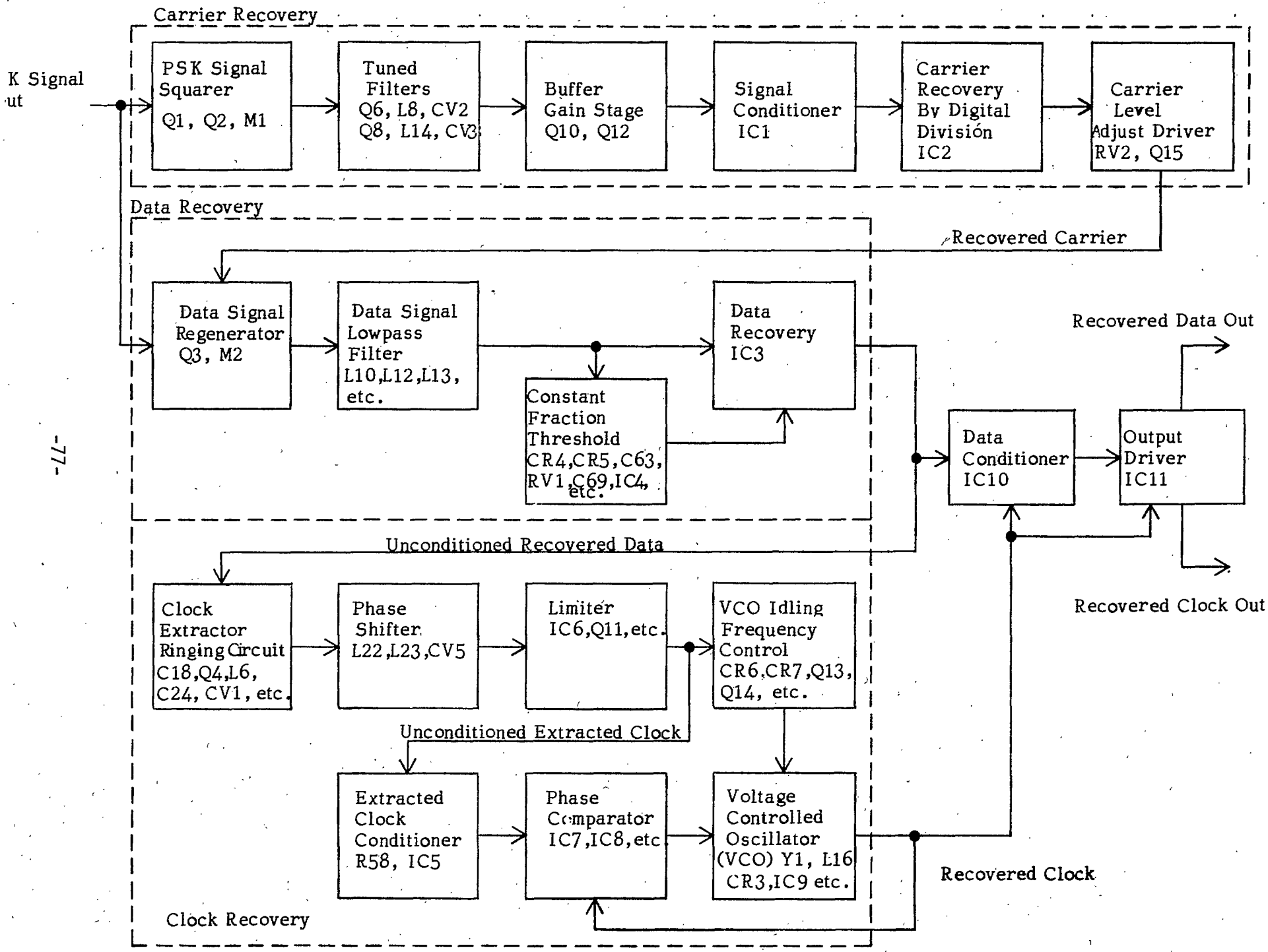
Data Conditioner:

A D-type flip-flop which produces the recovered data from the unconditioned recovered data. It also corrects the data/clock relationship required for the demultiplexer.

Output Driver:

Provides off-board drive capability at TTL levels for the recovered data and recovered clock signals.

Land Tactical PSK Data Recovery (D2217)



REV	DATE	REVISIONS / DESCRIPTIONS

PSK SIGNAL INPUT FROM DATA & VIDEO SEPARATOR

PSK SIGNAL GND

NOTES
1) EDGE CONNECTOR CONTACTS 59,60,79,80 ARE CONNECTED TO DIGITAL GND (G3)
2) EDGE CONNECTOR CONTACTS 13 & 14 ARE CONNECTED TO ANALOG GND G1

LAST NO. USED
IC11
M2
R75
RV2
C84
CV5
Q15
CR7
Y1
L24
TP46

+12V REG.
+12V GND
-12V REG.
+5V REG.
+5V GND

RECOVERED CLOCK OUT TO DEMULTIPLEXER AND TO DESCRAMBLER & FBIT RECOVERY CIRCUIT
CLOCK OUT GND
RECOVERED DATA OUT TO DESCRAMBLER & FBIT RECOVERY CIRCUIT
DATA OUT GND

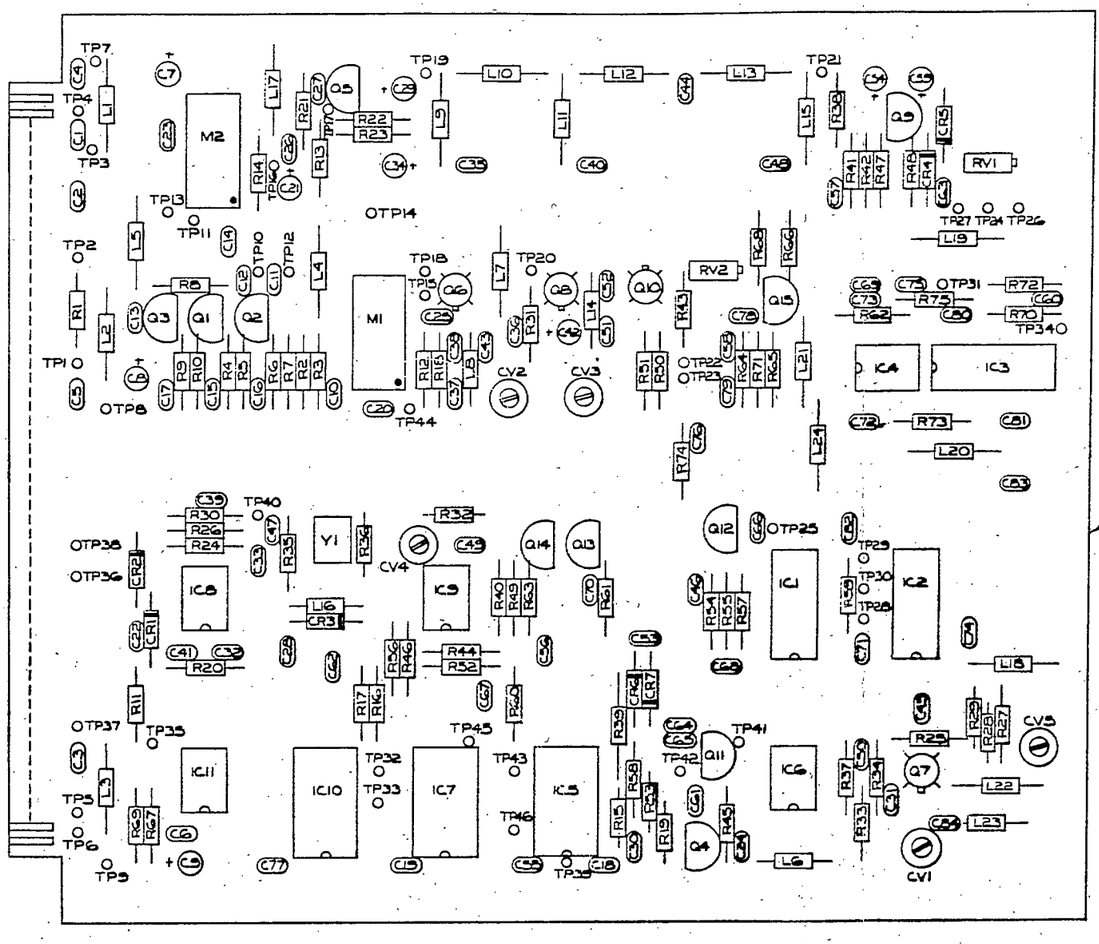
ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES
MATERIAL:
FINISH:

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-06-02 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN
LAND TACTICAL PSK DATA RECOVERY - SCHEM
SCALE: | SHEET OF
APPROVAL: R.Y. 09/23/82 | DWG NO: D2217

REV	DATE	REVISIONS / DESCRIPTIONS



NOTES
1) BLUE DOT ON BOTTOM OF M1 & M2 INDICATES PIN 1
(DOT SHOWN ON TOP ON DWG)

ITEM	QTY	PART NO.	DESCRIPTION

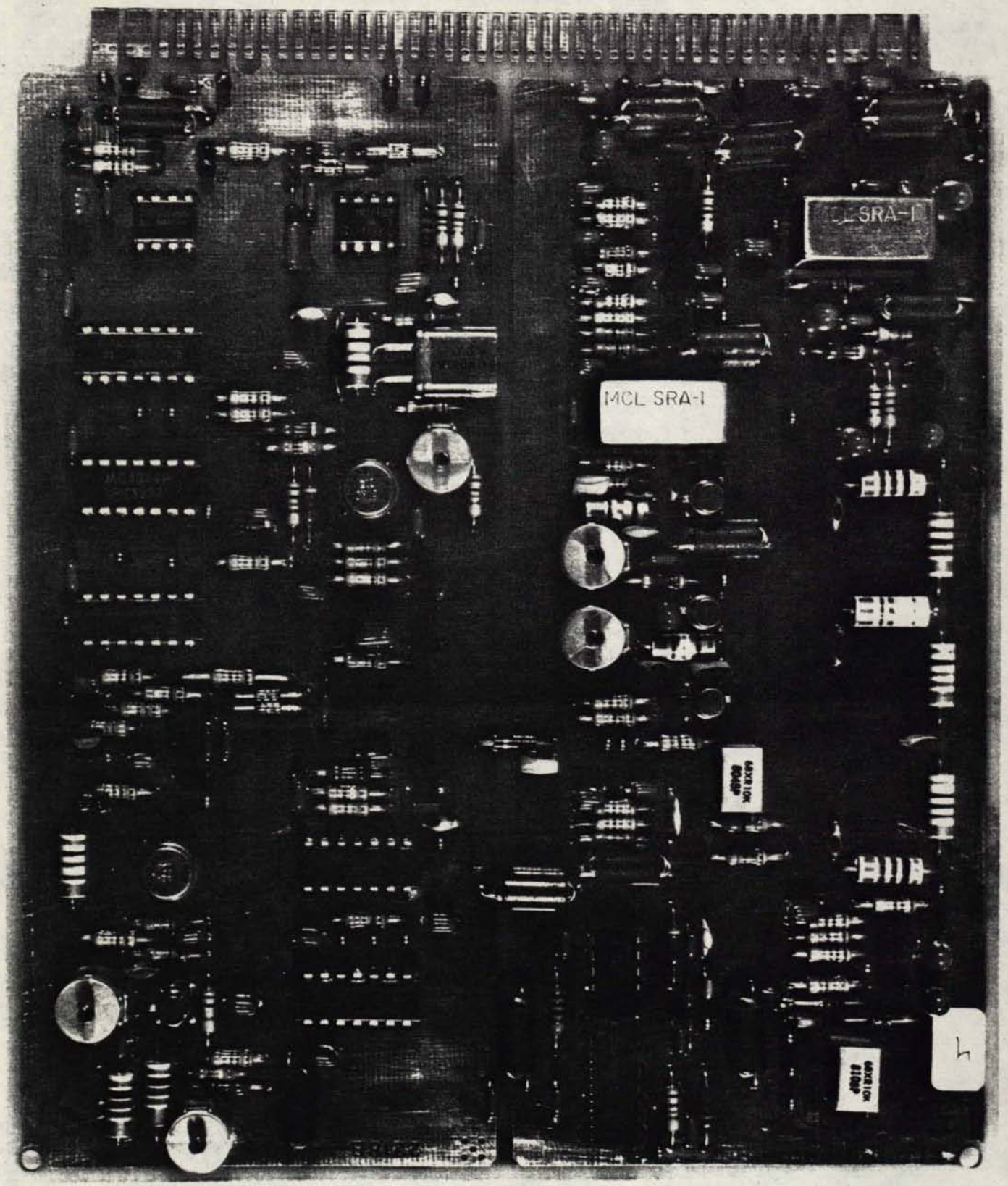
UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2°	FOUNDATION INSTRUMENTS OTTAWA	
SURFACES:	DATE: 82-09-27	PROJ. NO: 8A0113 — DRAWN BY: J. WHITEMAN
REMOVE BURRS & SHARP EDGES	LAND TACTICAL PSK DATA RECOVERY - COMP. LAYOUT	
MATERIAL:	SCALE: 2/1	SHEET 1 OF 2
FINISH:	APPROVAL: 04/02/83	DWG NO: 2219

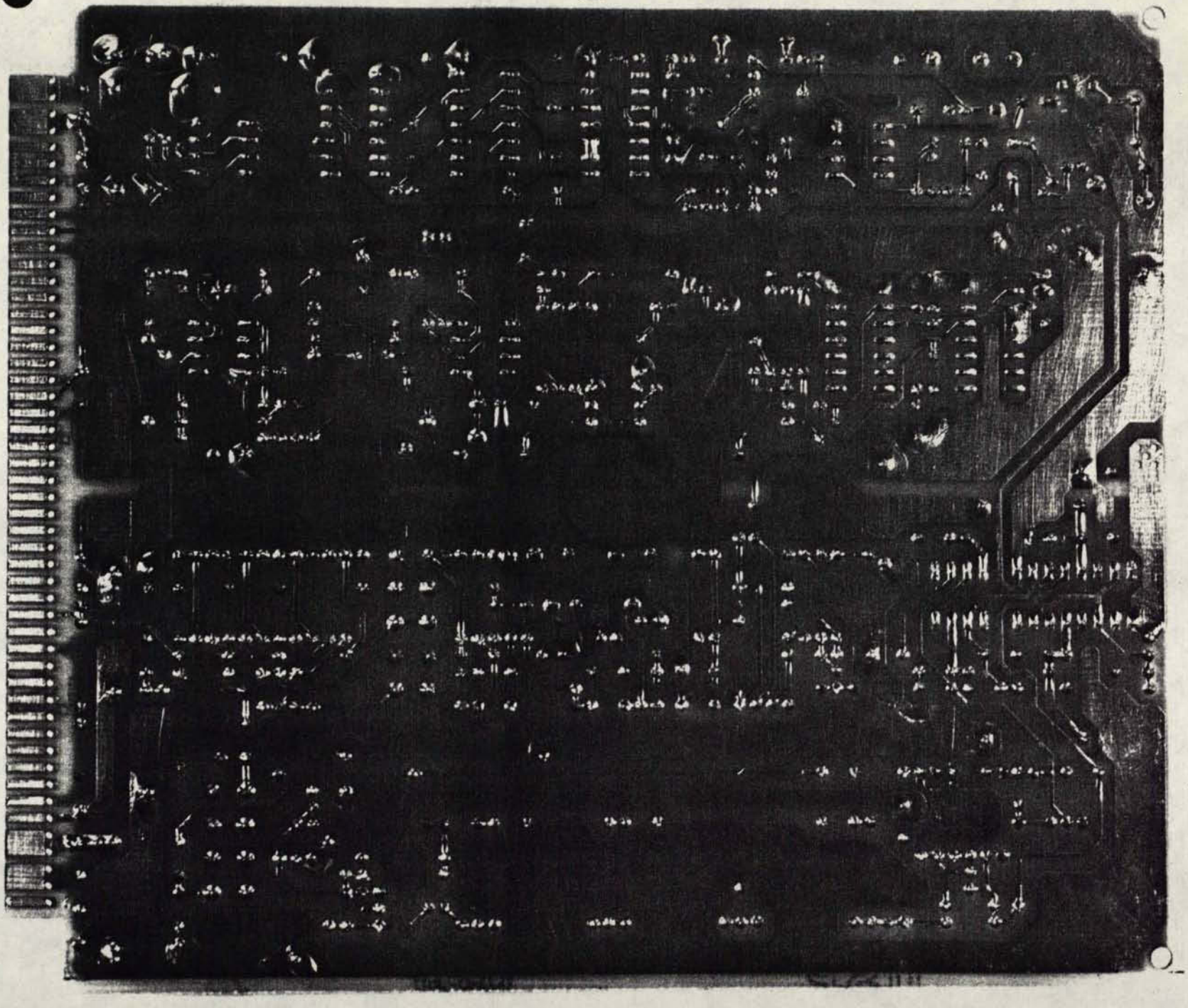
REV	DATE	REVISIONS DESCRIPTIONS

TP1-4	46	2137-D	TEST POINT	VERO
L22,23	2	1537-64	COIL, 56µH	DELEVAN
L16	1	1537-42	18µH	
L12	1	1537-52	33µH	
L11	1	1537-26	3.9µH	
L10,13	2	1537-48	27µH	
L9,15	2	1537-44	22µH	
L8,14	2	1537-12	1µH	
L6	1	1537-38	COIL, 12µH	DELEVAN
L20,21,24 L18,19 L5,7,17 L1,2,3,4	11	VK200-20/4B	WIDE BAND CHOKE	FERROXCUBE
Y1	1	FOX040A HC-18/U	CRYSTAL, 4.000 MHZ	FOX
CR3	1	IN5146	DIODE	
CR5,6,7 CR1,2,4	6	IN4148	DIODE	
Q11	1	2N3904	TRANSISTOR	
Q8,10	4	2N4416		
Q6,7				
Q4,13,14	3	2N3506		
Q9,12,15 Q1,2,3,5	7	2N5770	TRANSISTOR	
CV4,5 CV1,2,3	5	0106AG0E	VARIABLE CAPACITOR, 5.5-65pF	PHILIPS
C76,78	2	629-03472	CAPACITOR, 4.7nF, CERAMIC	PHILIPS
C67	1		.047µF, CERAMIC	
C66,69	2	630-03122	1.2nF, CERAMIC	PHILIPS
C63,75	2	3439-050E-103M	.01µF, CERAMIC	AVX
C52	1	638-10829	82pF, CERAMIC	PHILIPS
C47	1	630-03221	220pF, CERAMIC	PHILIPS
C44	1	638-10121	120pF, CERAMIC	PHILIPS
C37,43	2	638-34151	150pF, CERAMIC	PHILIPS
C51 C35,48	3	638-10339	33pF, CERAMIC	PHILIPS
C70 C32,33	3	3430-0506-105M	1µF, CERAMIC	AVX
C31	1	629-03103	10nF, CERAMIC	PHILIPS
C28	1	630-03182	1.8nF, CERAMIC	PHILIPS
C27,38	2	638-10279	27pF, CERAMIC	PHILIPS
C25,40	2	638-10101	100pF, CERAMIC	PHILIPS
C24	1	DM5-101J	100pF, SILVER MICA	MICONICS
C22	1	3430-050E-474M	0.47µF, CERAMIC	AVX
C18	1	DM5-500J	50pF, SILVER MICA	MICONICS
C54,55 C34,42 C21,25 C7,8,9	9	TAP10M16	10µF, 16WVDC, TANTALUM	ITT
C82,83,84 C79,80,81 C74,77 C72,73 C68,71 C64,65 C61,62 C58,60 C56,57 C53,55 C49,50 C45,46 C39,41 C30,36 C23,28 C17,19,20 C14,15,16 C11,12,13 C5,6,10 C1,2,3,4	46	3439-050E-104M	CAPACITOR, 0.1µF, 50V, CERAMIC	AVX
ITEM	QTY	PART NO.	DESCRIPTION	

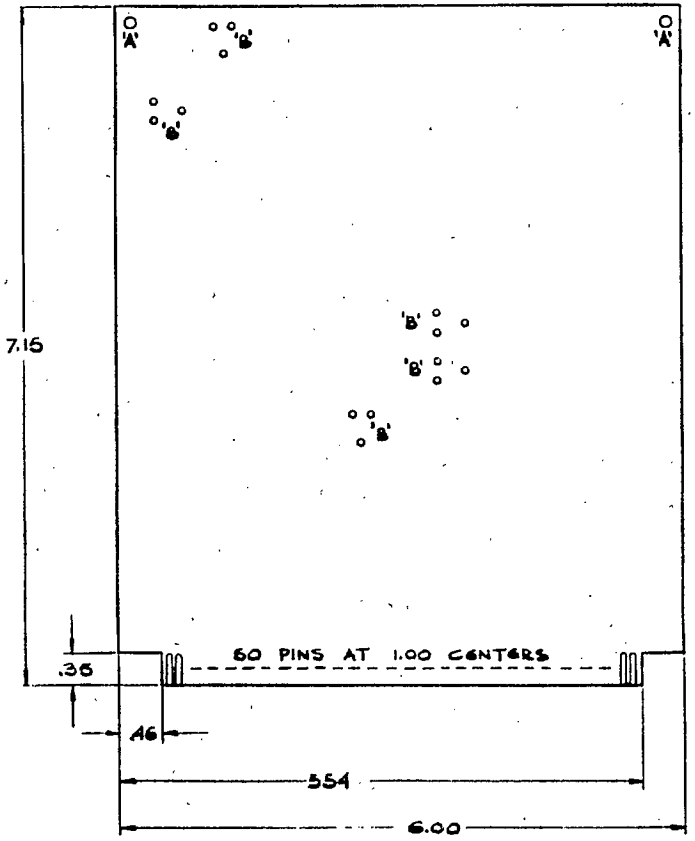
RV1,2	2	3299X-1-103	VARIABLE RESISTOR, 10KΩ	BOURNS
R47	1		RESISTOR, 100Ω, 1/4W, ±5%	
R73,74,75	3		RESISTOR, 10Ω, 1/4W, ±5%	
R72	1		12KΩ	
R68	1		39Ω	
R64,71	2		3.3KΩ	
R55	1		330Ω	
R54	1		150Ω	
R51	1		680Ω	
R43	1		120Ω	
R42,59	2		1.8KΩ	
R52,56,60 R36,37 R33,34	7		10KΩ	
R29,40	2		2.2KΩ	
R28,46	2		3.9KΩ	
R27	1		8.2KΩ	
R26	1		1.2KΩ	
R25,63	2		100KΩ	
R24	1		68KΩ	
R23,66	2		270Ω	
R22	1		33Ω	
R21,53	2		560Ω	
R20	1		5.6KΩ	
R67,69 R65	3		220Ω	
R50,61 R18,31	4		1MΩ	
R16,17	2		180Ω	
R15	1		1KΩ	
R41,45 R14,38	4		1.5KΩ	
R56,62 R13,44	4		4.7KΩ	
R35,70 R11,30,32	5		22KΩ	
R48,57 R7,10	4		330Ω	
R5	1		82Ω	
R4	1		27Ω	
R39,49 R8,9,12 R2,3,6	8		51Ω	
R1,19	2		RESISTOR, 470Ω, 1/4W, ±5%	
M1,2	2	MCLSRA-1	DOUBLE BALANCED MIXER	MINI-CIRCUITS
IC11	1	75451	INTEGRATED CIRCUIT	
IC10	1	74LS74		
IC7	1	MC4044		
IC6,9	2	CA3028		
IC5	1	74LS14		
IC4,8	2	741CP		
IC3	1	HA4925		
IC2	1	74LS73		
IC1	1	745132	INTEGRATED CIRCUIT	
1	1	#2218	PRINTED CIRCUIT BOARD	FI
ITEM	QTY	PART NO.	DESCRIPTION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 82-09-27	PROJ. NO: 8103	DRAWN BY: J. WHITEMAN
	LAND TACTICAL PSK DATA RECOVERY - COMP. LAYOUT		
MATERIAL:	SCALE:		SHEET 2 OF 2
FINISH:	APPROVAL: 09/02/83		DWG NO: #2219


SRA-1
MCL SRA-1



REV	DATE	REVISIONS / DESCRIPTIONS



HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA	2
B	.060 DIA	15
OTHERS	.037 DIA	

NOTES.
1) ALL HOLES TO BE DRILLED ON PAD CENTERS
2) HOLE DIAMETERS TO BE AFTER PLATING

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY		2219	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS
OTTAWA

DATE: 82-10-14 | PROJ. NO: 810113 | DRAWN BY: P.D.

PSK DATA RECOVERY

MATERIAL: G10, .062 THK, GLASS EPOXY 1 OZ COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

FINISH: TIN PLATE .0002/.0003 THK CTS. GOLD .0001/.0002 THK | APPROVAL: R. Lyn 17/02/83 | DWG NO: 2220

3.10 Data and Video Separator

This section contains the data and video separator theory of operation. Included in this section are the following:

i) Block diagram
ii) Schematic D2209
iii) Overlay D2211
iv) Photograph PCB 2210B component and solder side
v) Mechanical PCB drilling diagram.

THEORY OF OPERATION

Module: Data and Video Separator (FI-2210B)
Schematic D2209
Component Overlay D2211

Operational Description:

The circuitry on this card takes the signal from the fibre optic receiver (FORX) and separates the data signal from the video signal. The data signal is monitored and an amplitude gain control (AGC) circuit maintains constant output signal levels thus reducing any effects due to degradation of the optical link. (See accompanying block diagram and schematic D2209)

Variable Gain Amplifier:

Amplifies the low level output signal of the FORX. Its gain is variable and is set by the value of a voltage controlled variable resistance (RV4). Both elements are part of an amplitude gain control (AGC) loop that is used to maintain a constant data signal output level regardless of variations in the amplitude of the signal received by the FORX. Such variations could arise fom the use of fibre optic links of different lengths or optical power losses due to splices, sharp bends or long term degradations in the optical fibre. The amplifier has two outputs. One leads to a circuit dedicated to recovery of the video signal while the other goes to a circuit dedicated to the recovery of the data signal.

Video Separator Lowpass Filter:

A lowpass filter with very high roll-off and signal rejection above 5.5 Mhz. It is used to suppress any data signal that would

degrade the video signal quality.

Video Output Level Adjustment:

The video signal level desired at the video output is set by adjusting RV2.

Video Output Driver:

Provides an output impedance of 75 ohms and the drive capability required for the video output signal.

Data Signal Separator Highpass Filter:

A highpass filter with very high roll-off and signal rejection below 8 Mhz. It is used to remove the video signal from the data signal which regulates the AGC action and is used by the data recovery circuitry on card FI-2218B.

Gain Stages:

Q1 and Q3 provide the required gain as well as buffering and driving their respective filters.

Data Signal High Frequency Rejection Filter:

A lowpass filter with sharp roll-off above about 20 Mhz. It is used to suppress any high frequency interference that might have been picked up by the low level signal at the FOTX and FORX.

Data Signal Output Driver and Level Adjustment:

Provides a low impedance drive for the output data signal whose level can be set by adjusting RV3.

Peak Detector:

Monitors the data signal and provides a d.c. voltage to the feedback

gain controller which is proportional to the peak value of the data signal.

Gain Control Voltage Reference:

IC4 is a stable voltage source and RV1 provides an adjustable reference voltage to the feedback gain controller which represents the desired output data signal level.

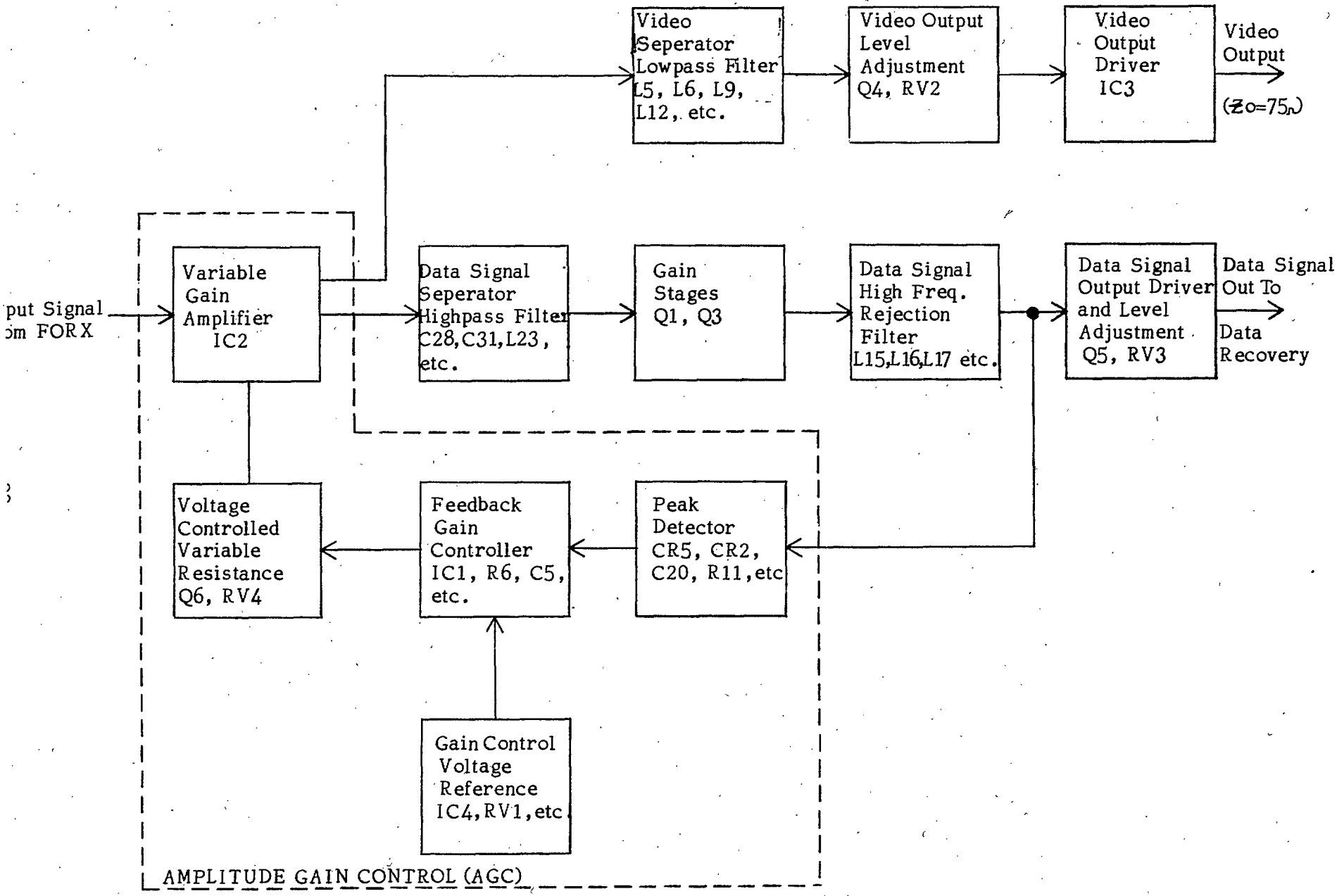
Feedback Gain Controller:

Consists of an integrator amplifier which compares the set reference voltage and the output of the peak detector and generates an error voltage which is used to change the gain of the input amplifier. This in turn changes the output of the peak detector and the process stabilizes when the desired output data level is reached and the output of the peak detector is equal to the set voltage reference. Capacitor C5 is selected large enough to ensure the stability of the AGC loop. The AGC can maintain a constant output data signal level for an input level variation of about 12 decibels. The circuit is set up somewhere within this range to allow for both increases or decreases in the input level while maintaining the desired output levels.

Voltage Controlled Variable Resistance:

It is a Vactrol which consists of a light emitting diode (LED) and a photoresistor whose resistance changes as the current through the LED changes. So a change in the output voltage of the feedback gain controller will result in a change in the resistance which sets the gain of the input amplifier. This characteristic allows the AGC action to occur.

Land Tactical Data & Video Seperator (D2209)



REVISIONS		
REV	DATE	DESCRIPTIONS
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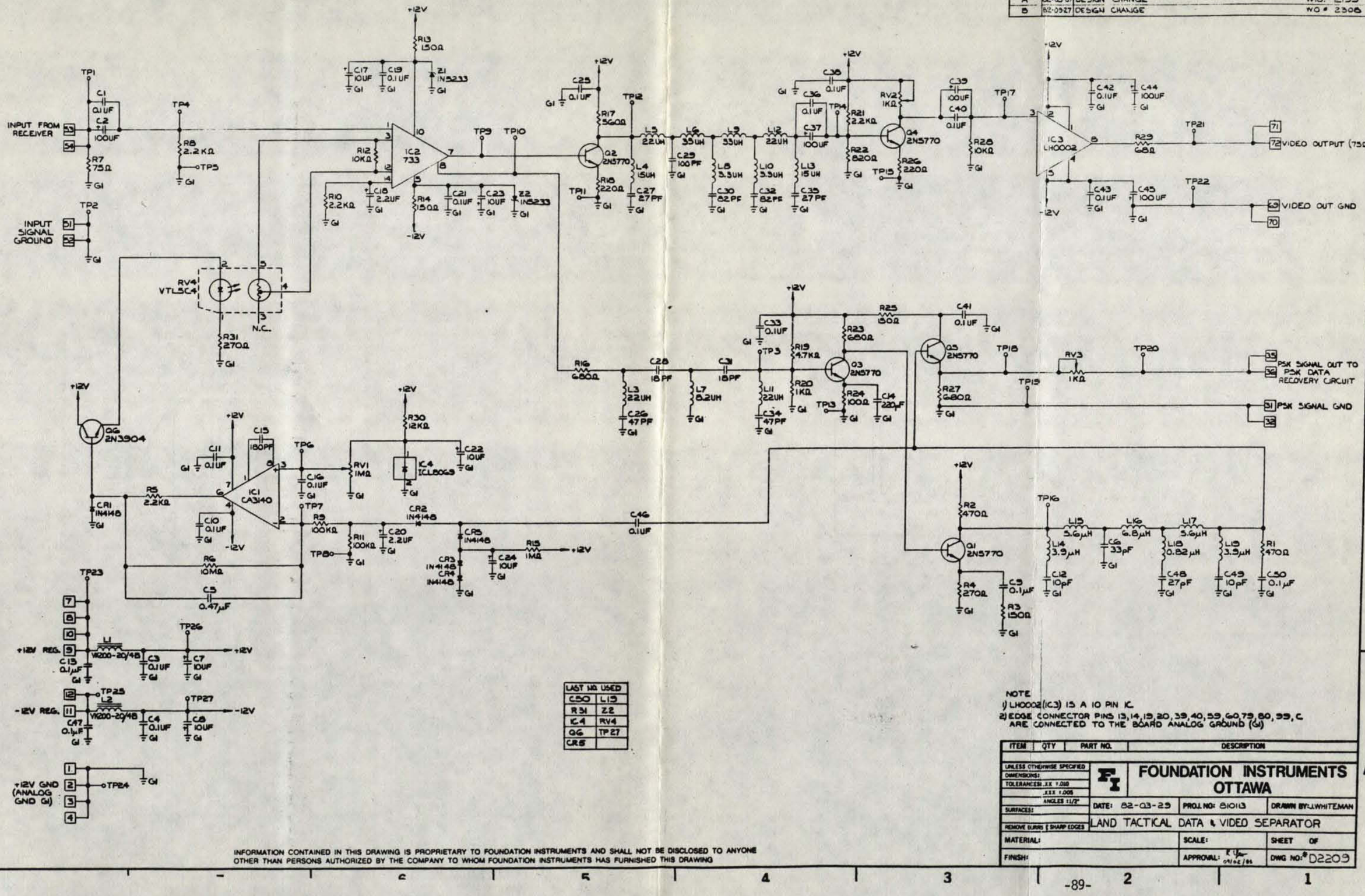
B	82-09-27	DESIGN CHANGE W.O.# 2308



LAST NO USED	
C50	L13
R31	Z2
IC4	RV4
Q6	TP27
CR5	

NOTE
1) LH0002 (IC3) IS A 10 PIN IC.
2) EDGE CONNECTOR PINS 13,14,19,20,39,40,59,60,79,80,99,C ARE CONNECTED TO THE BOARD ANALOG GROUND (G)

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

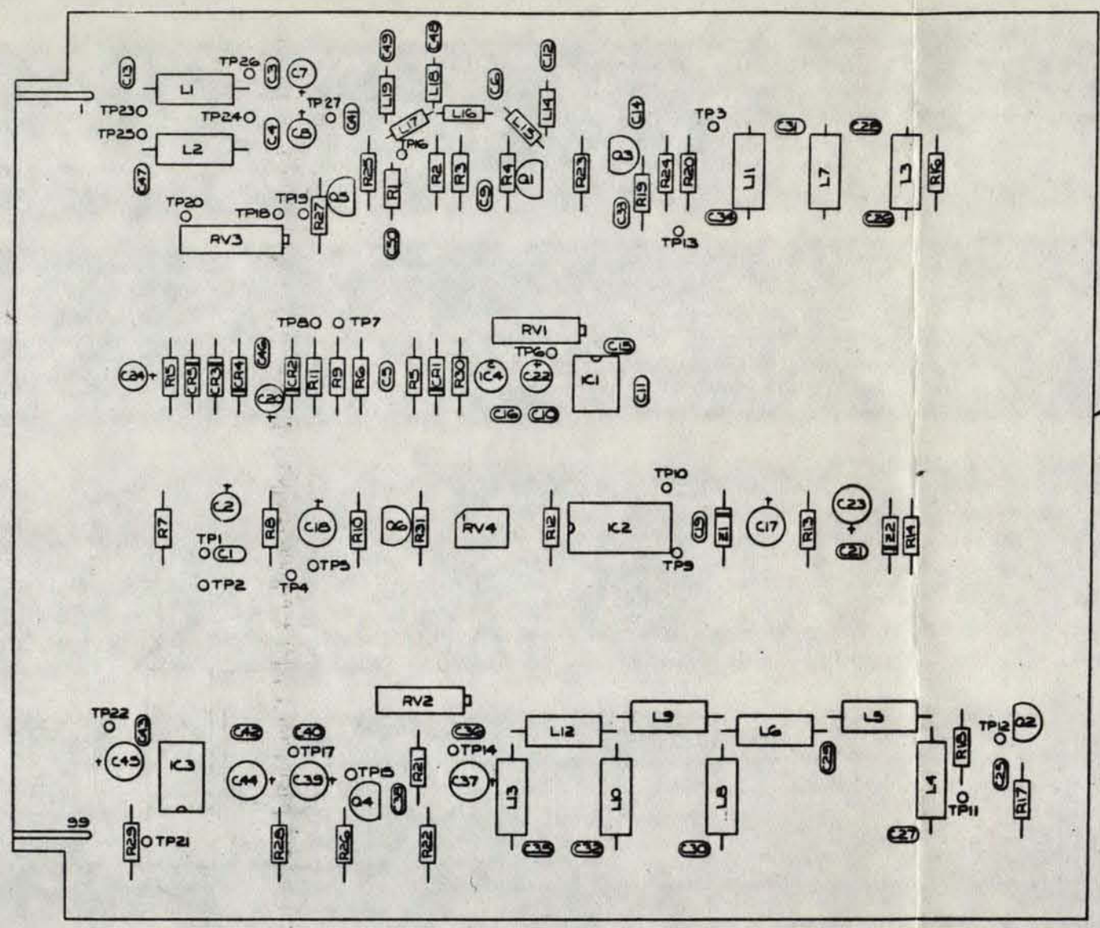
FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-03-29 | PROJ. NO: 81013 | DRAWN BY: L.WHITEMAN

LAND TACTICAL DATA & VIDEO SEPARATOR

MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: R.Y. 09/02/86 | DWG NO: D2209

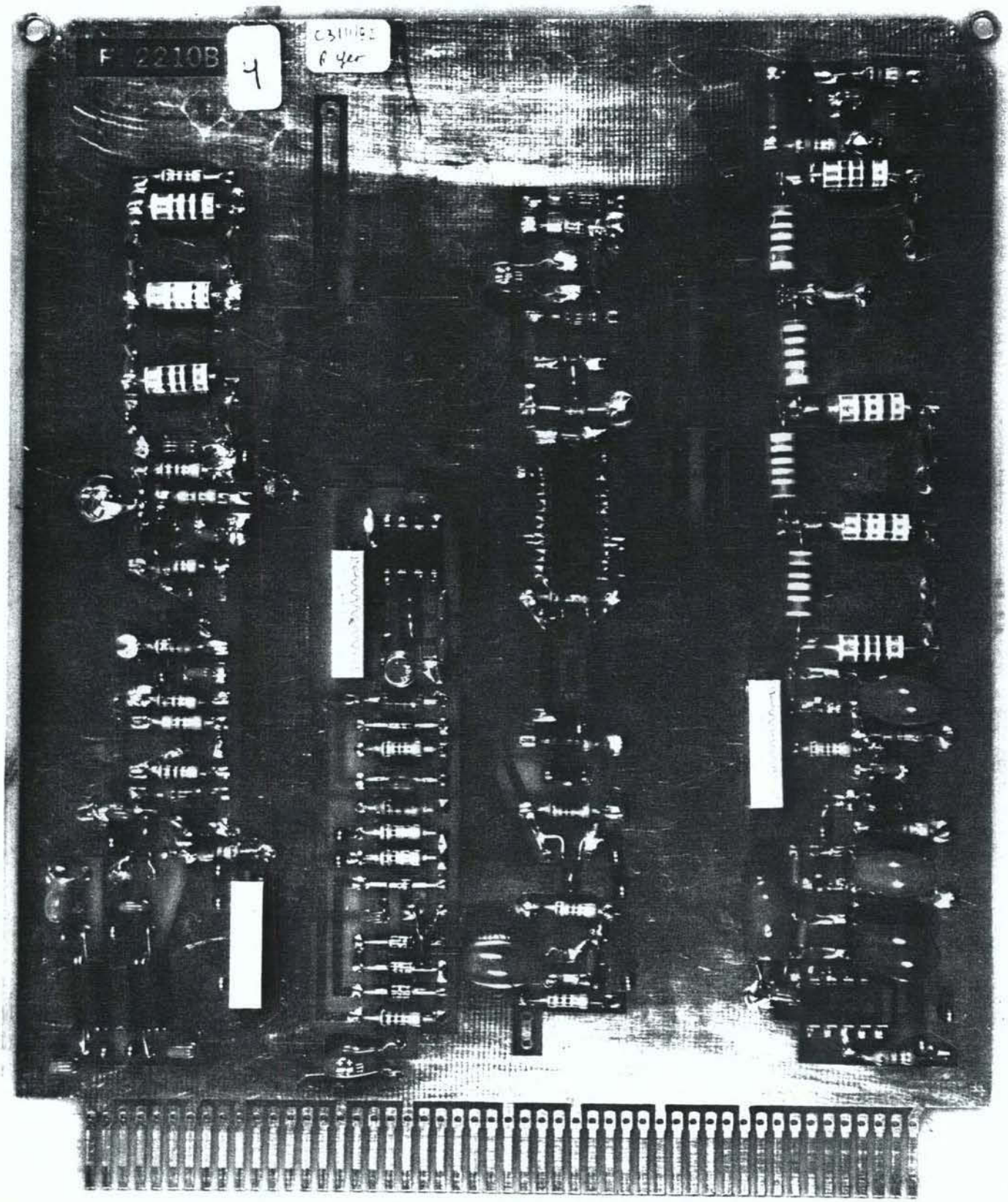


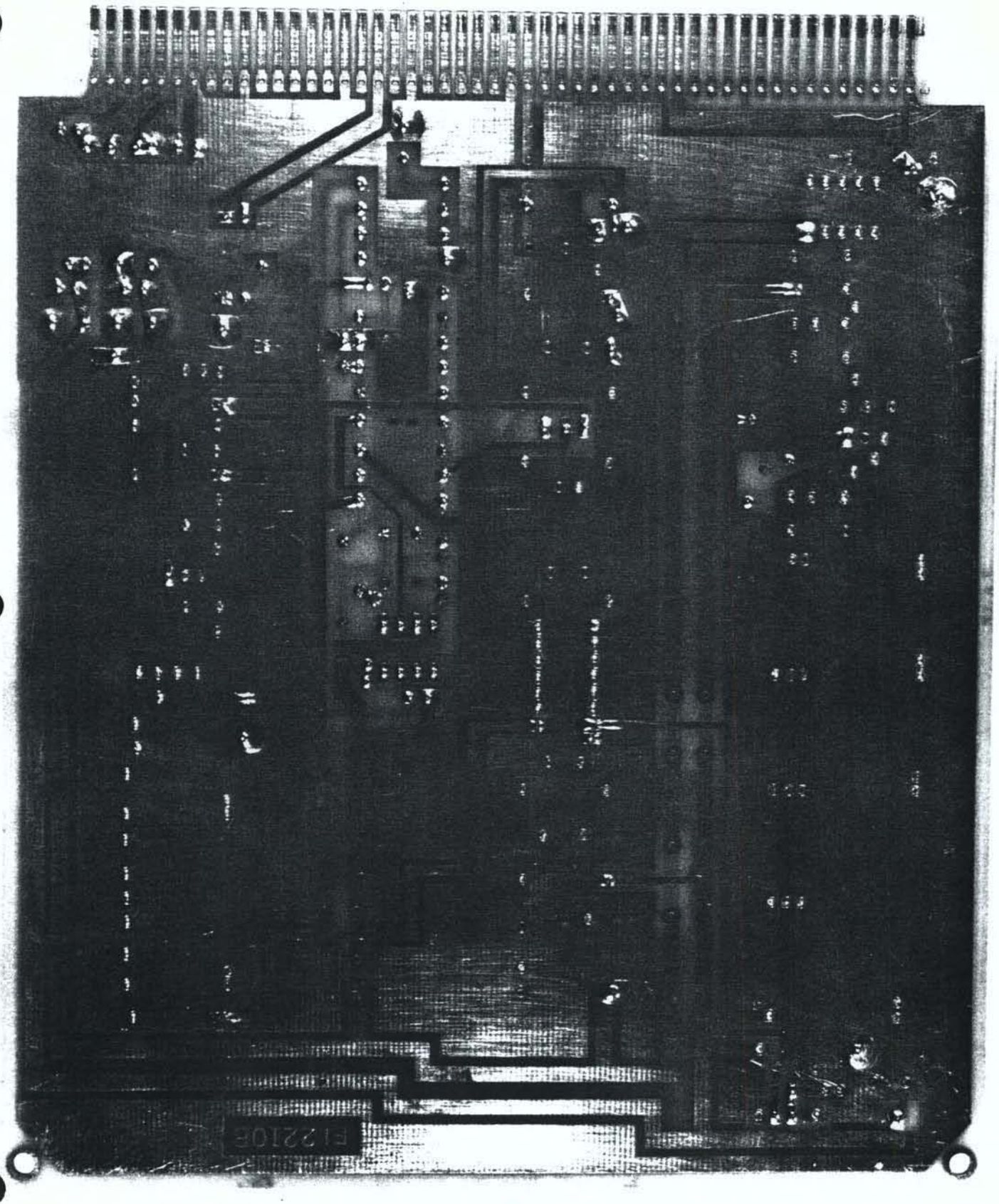
REVISIONS		
REV	DATE	DESCRIPTIONS

TP1-28	28	20-2137D	TEST POINT	VERO
Z1, 2	2	IN5233	ZENER DIODE	
CR4,5 CR1,2,3	5	IN4148	DIODE	
Q6	1	2N3904	TRANSISTOR	
Q4,5 Q1,2,3	5	2N5770	TRANSISTOR	
C6	1	638-10339	CAPACITOR, 33 pF, 100VDC, CERAMIC	PHILIPS
C30,32	2	638-10829	CAPACITOR, 82 pF, 100VDC, CERAMIC	PHILIPS
C29	1	638-10101	100pF, 100VDC, CERAMIC	PHILIPS
C28,31	2	638-10189	18pF, 100VDC, CERAMIC	PHILIPS
C5	1	3439-050E-474M	0.47µF, 50VDC, CERAMIC	AVX
C26,34	2	638-10479	47pF, 100VDC, CERAMIC	PHILIPS
C18,20	2	TAP2.2M16	2.2µF, 16WVDC, TANTALUM	ITT
C15	1	630-03181	180pF, 100VDC, CERAMIC	PHILIPS
C12,49	2	638-10109	10pF, 100VDC, CERAMIC	PHILIPS
C22,23,24 C7,8,17	6	TAP10M16	10µF, 16WVDC, TANTALUM	ITT
C27,35,48	3	638-10279	27pF, 100VDC, CERAMIC	PHILIPS
C14	1	638-58221	220pF, 100VDC, CERAMIC	PHILIPS
C44,45	2	TAP100M16	100µF, 16 WVDC, TANTALUM	ITT
C2,37,39	3	TAP100M10	100µF, 10 WVDC, TANTALUM	ITT
C13,50 C43,46,47 C40,41,42 C33,36,38 C19,21,25 C10,11,16 C1,3,4,9	21	3439-050E-104M	CAPACITOR, 0.1µF, 50V, CERAMIC	AVX
RV4	1	VTL 5C4	LED PHOTOCONDUCTOR	VACTEC
RV2,3	2	3006P-1-102	VARIABLE RESISTOR, 1KΩ	BOURNS
RV1	1	3006P-1-105	VARIABLE RESISTOR, 1MΩ	BOURNS
R31,4	2		RESISTOR, 270Ω, 1/4W, ±5%	
R30	1		12KΩ	
R29	1		68Ω	
R26,18	2		220Ω	
R22	1		820Ω	
R20	1		1KΩ	
R19	1		4.7KΩ	
R17	1		560Ω	
R6,23,27	3		680Ω	
R15	1		1MΩ	
R12,28	2		10KΩ	
R9,11	2		100KΩ 1/4W	
R7	1		75Ω 1/2W	
R6	1		10MΩ, 1/4W	
R10,21 R5,8	4		2.2KΩ	
R14,25 R3,13	4		150Ω	
R24	1		100Ω	
R1,2	2		RESISTOR, 470Ω, 1/4W, ±5%	
IC4	1	ICL8069	INTEGRATED CIRCUIT	INTERSIL
IC3	1	LH0002		
IC2	1	733		
IC1	1	CA3140	INTEGRATED CIRCUIT	
1	1	#2210 A	PRINTED CIRCUIT BOARD	FI
ITEM	QTY	PART NO.	DESCRIPTION	

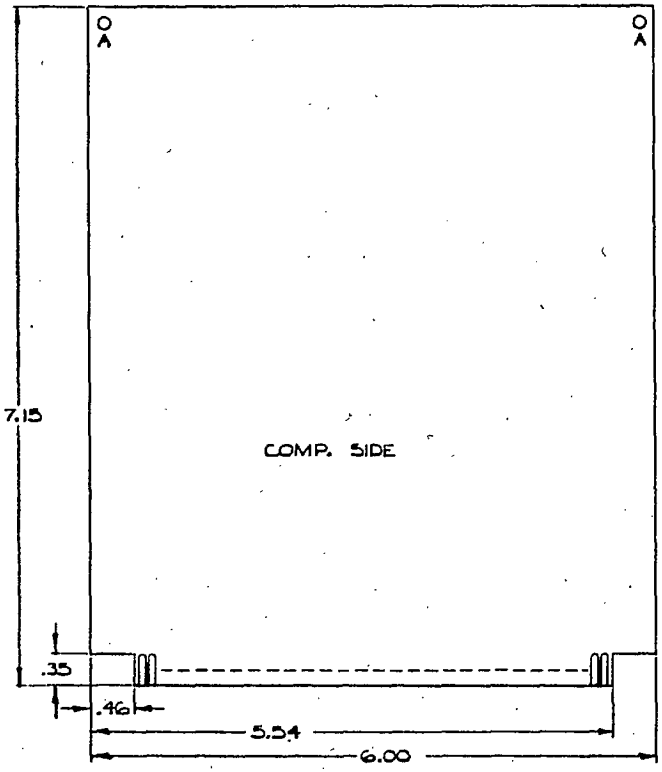
L18	1	1025-18	MOLDED RF COILS, 0.82µH	DELEVAN
L16	1	1025-40	6.8µH	
L15,17	2	1025-38	5.6µH	
L14,19	2	1025-34	3.9µH	
L8,10	2	1537-24	3.3 UH	
L7	1	1637-34	8.2 UH	
L6,9	2	1537-52	33 UH	
L4,13	2	1537-40	18 UH	
L12	4	1537-44	MOLDED RF COILS, .22UH	DELEVAN
L3,5,11				
L1,2	2	VK200-20/4B	WIDEBAND CHOKES	FERROXCUBE
ITEM	QTY	PART NO.	DESCRIPTION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FI	FOUNDATION INSTRUMENTS OTTAWA	
	DATE: 82-09-14	PROJ. NO: 810113	DRAWN BY: J. WHITEMAN
	LAND TACTICAL DATA & VIDEO SEPARATOR - COMP. LAYOUT		
MATERIAL:		SCALE: 2/1	SHEET OF
FINISH:		APPROVAL: 27/09/82	DWG NO: #D2211


F 2210B
4



REV	DATE	REVISIONS / DESCRIPTIONS



HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA. (FINISHED)	2
OTHER	.037 DIA. (FINISHED)	

NOTE
1) ALL HOLES TO BE DRILLED ON PAD CENTERS

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FI **FOUNDATION INSTRUMENTS OTTAWA**

DATE: 82-09-16 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

PSK DATA & VIDEO SEPARATOR-MASTER

MATERIAL: G10, .062 THK, GLASS EPOXY 1 OZ. COPPER EACH SIDE
FINISH: TIN-LEAD PLATE .0002/.0003 THK CONT. GOLD .0001/.0002 THK

SCALE: 1/1 | SHEET OF | APPROVAL: R. Yee 17/02/83 | DWG NO: 2212

3.11 Descrambler and F. Bit Recovery

This section details the descrambler and F. bit recovery theory of operation. In addition, this section contains the following:

i) Block diagram
ii) Schematic D2213
iii) Overlay D2215
iv) Photograph PCB 2214A component and solder side
v) Mechanical 2216 drilling diagram.

THEORY OF OPERATION

Module: Descrambler and F-Bit Recovery Board (FI-2214A)
Schematic No. D2213
Component Overlay D2215

Operational Description:

See accompanying block diagram and schematic no. D2213.

Descrambler:

Decodes incoming data stream to original multiplexed format. An option to disable the descrambler from the system can be accomplished by removing jumper J1 and configuring J2 and J3 such that pin 5 and 2 of IC3 are connencted to GND.

Signal Conditioner:

Corrects the output clock/data relationship.

Parity Corrector:

Detects an inversion in the descrambled data stream and corrects it. Incorporates two cascaded D-type flip-flops, the first of which is clocked by a signal in phase with the F-Bit of the data stream, the second being toggled by the first. The parity bit channel at the demultiplexer is detected by the first flip-flop and if low implies that the descrambled data is inverted. Under this condition the first flip-flop can clock and toggle the second and reinvert the data at the EX.OR gate IC9. The parity bit will then be high indicating correct data polarity. This signal will now disable the first flip-flop preventing any further toggling, preserving the status quo.

The possibility of inverted descrambled data arises from the PSK transmission method used. An inversion has no effect on the ability of the F-bit recovery scheme.

F-bit Generator:

Produces a signal that coincides with the frame synch bit in the data stream. Consists of tow cascaded synchronous counters, IC21 and IC22, whose 26th count is detected by a NAND gate and is used to reset the counters synchronously on the next clock cycle, (count 27), which coincides with the detection by a D-type flip-flop IC17. Essentially this flip-flop generates an output signal in phase with the data stream frame synch bit, once synchronization has been achieved.

F-bit Synchronizer:

Aligns the frame synch bit generated with the F-bit in the descrambled data stream. A shift register, IC18 initially clocks in two bits in the descrambled stream, 27 bits apart. The 27 bit spacing means these two bits occupy the same channel slot in the multiplexed stream, and if alignment is made this slot will be occupied by the alternating F-bit.

If IC18 does not clock in the correct slot the D-type flip-flop, IC17 will output a one clock cycle long reset signal to the F-bit generator counters such that counting begins one slot over in the multiplexed stream. This implies IC18 will latch in data in the adjacent slot as well. In this way, a search is made of the descrambled data for the F-bit position.

In greater detail after a reset from pin 5 of IC17, 2 data bits are selected by IC18 before a decision is made whether a shift in the

data stream is required or more data bits in this time slot need to be observed. This is accomplished by the F-bit Counter holding the D input to the resetting flip-flop high for the two initial IC18 shift cycles. The first two shift register outputs are then examined for an alternating pattern, (eg. 10 or 01). If none exists a reset occurs and the process repeats itself with an adjacent time slot. If an alternating pattern exists, the shift register cycles four more times before the F-bit Synchronizer determines that the frame synch bit has been detected. If at any time within these four cycles the alternating pattern is not preserved, the reset procedure is initiated. Once an alternating pattern is present across the first six outputs of the shift register, the F-bit Counter forces a condition at the input to the reset flip-flop that prevents single errors in the descrambled F-bit from causing a reset. In fact, complete synch loss, meaning no alternation at all of the 3 EX.OR gates (IC16) that detect this condition would necessitate a reset.

F-bit Conditioner:

Corrects the data/Frame-synch bit timing required for the demultiplexer.

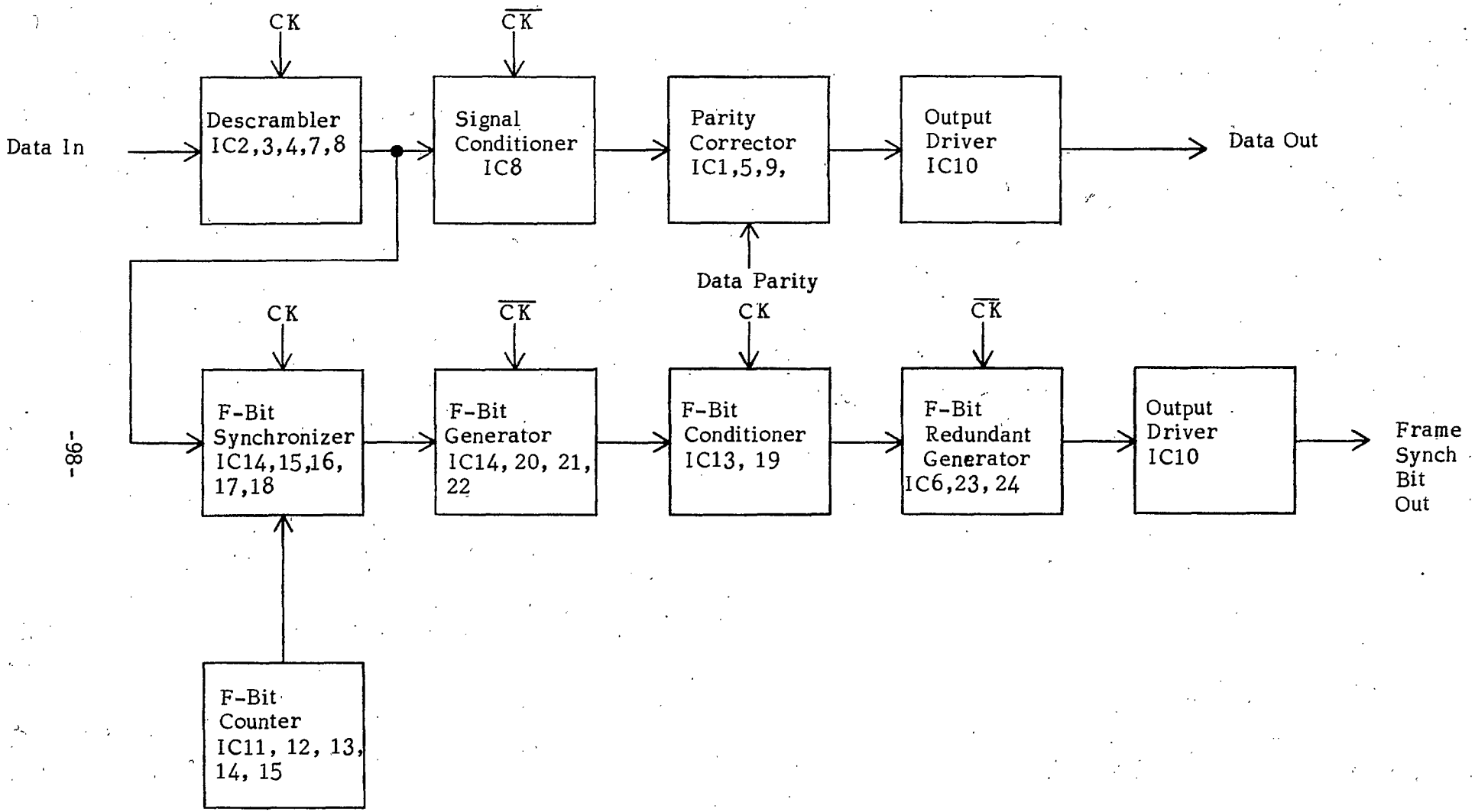
F-bit Redundent Generator:

Cascaded synchronous counters that generate a pulse coincident with the frame synch. If one frame synch pulse is lost, this generator will substitute its own frame synch to prevent loss in data transmission.

Output Driver:

Allows the Descrambled Data Out and Frame Synch Bit Out signals to drive off board components.

Land Tactical Descrambler and F-Bit Recovery (D2213)



NOTE
1) EDGE CONNECTOR CONTACTS 1,2,19,20,35,40,63,64,67,68,71,72,75,76, 83,84,87,88 ARE CONNECTED TO BOARD DIGITAL GND (G3)

REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-04-23	DESIGN CHANGE W.O.#2134
C	82-05-05	DESIGN CHANGE W.O.#2152
D	82-08-12	DESIGN CHANGE W.O.#2357
E	82-09-28	DOCUMENTATION CHANGE W.O.#2310
F	82-10-25	DOCUMENTATION CHANGE W.O.#2340

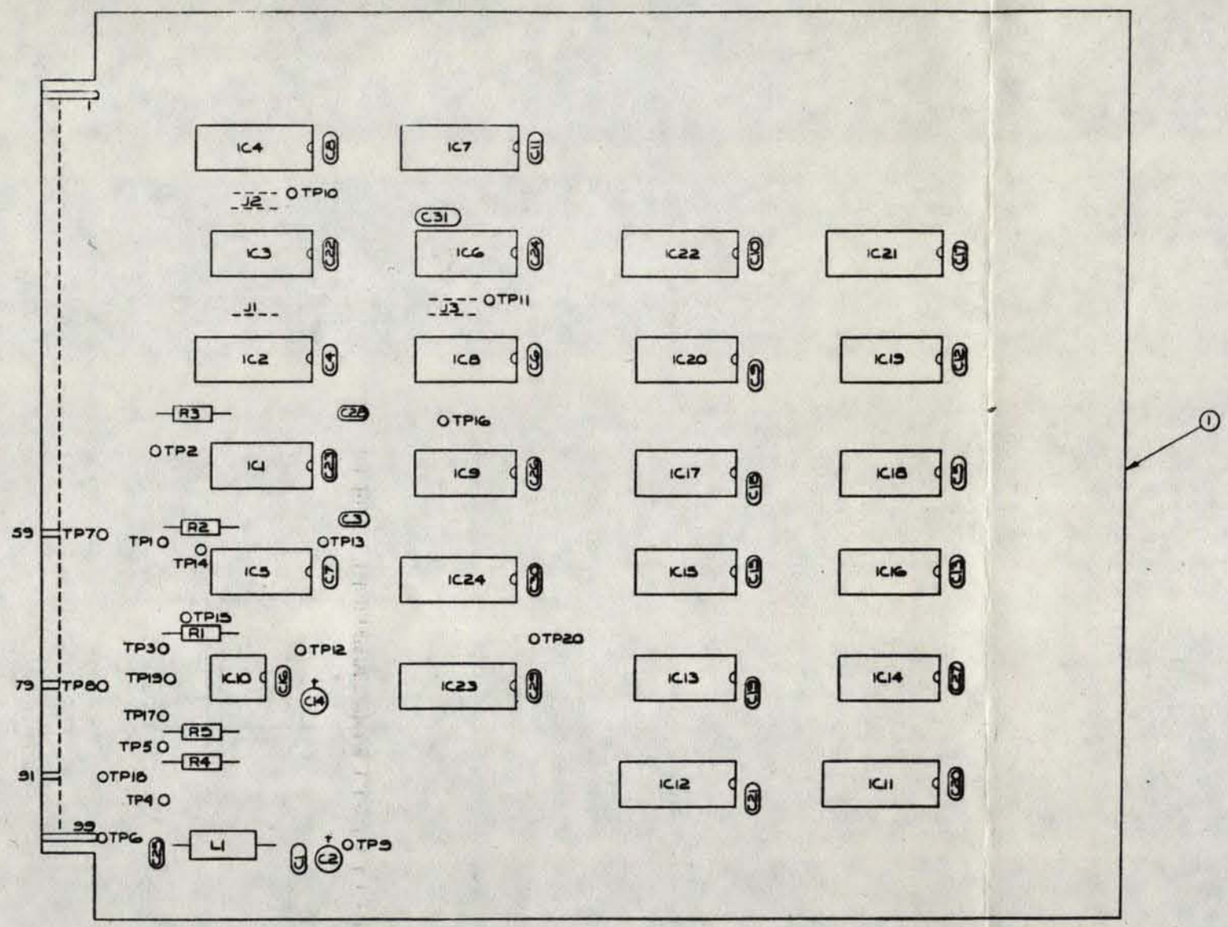
DATA IN FROM DATA RECOVERY CIRCUIT 61 62
CLOCK IN FROM DATA RECOVERY CIRCUIT 81 82
DATA IN GND 59 60
CLOCK IN GND 79 80
DATA PARITY IN FROM DEMUX 69 70
+5V REG.
+5V GND DIGITAL GND (G3) 37 38 39 C

FRAME SYNC BIT TO DATA DEMULTIPLEXER 85 86
DATA OUT TO DEMULTIPLEXER 89 90
DATA OUT GND 91 92

LAST NO. USED
R5
C31
IC24
L1
J3
TP20

ITEM	QTY	PART NO.	DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES			FOUNDATION INSTRUMENTS OTTAWA
			DATE: 82-03-29 PROJ NO: 810113 DRAWN BY: J. WHITEMAN
			LAND TACTICAL DESCRAMBLER & F BIT RECOVERY
MATERIAL:			SCALE: SHEET OF
FINISH:			APPROVAL: 01/02/83 DWG NO: D2213

REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-09-28	DOCUMENTATION CHANGE WO# 2310
B	82-10-25	DOCUMENTATION CHANGE WO# 2340



ITEM	QTY	PART NO.	DESCRIPTION
J1,2,3	3		JUMPER, INSULATED, SOLID, #22 AWG
TP1-20	20	20-2137D	TEST POINT VERO
L1	1	VK200-20/4B	COIL FERROXCUBE
C31	1	63003271	CAPACITOR, 270 PF PHILIPS
C2,14	2	TAP10M16	CAPACITOR, 10μF, 16V, TANTALUM ITT
C28,29,30			
C25,26,27			
C22,23,24			
C19,20,21			
C16,17,18	28	3439-050E-104M	CAPACITOR, 0.1μF, 50V, CERAMIC AVX
C12,13,15			
C9,10,11			
C6,7,8			
C1,3,4,5			
R4,5	5		RESISTOR, 220Ω, 1/4W, ±5%
R1,2,3			
IC18	1	74LS164	INTEGRATED CIRCUIT
IC20	1	7410	INTEGRATED CIRCUIT
IC15	1	74LS32	
IC14	1	7408	
IC13	1	74LS04	
IC12	1	74LS42	
IC11	1	74LS161	
IC10	1	75451	
IC23,24	5	74LS163	
IC7,21,22			
IC6	1	74LS00	
IC17,19	4	74LS74	
IC5,8			
IC3,16	3	74LS86	
IC2,4	2	74LS175	
IC1	1	7404	INTEGRATED CIRCUIT
1	1	*2214	PRINTED CIRCUIT BOARD FI

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

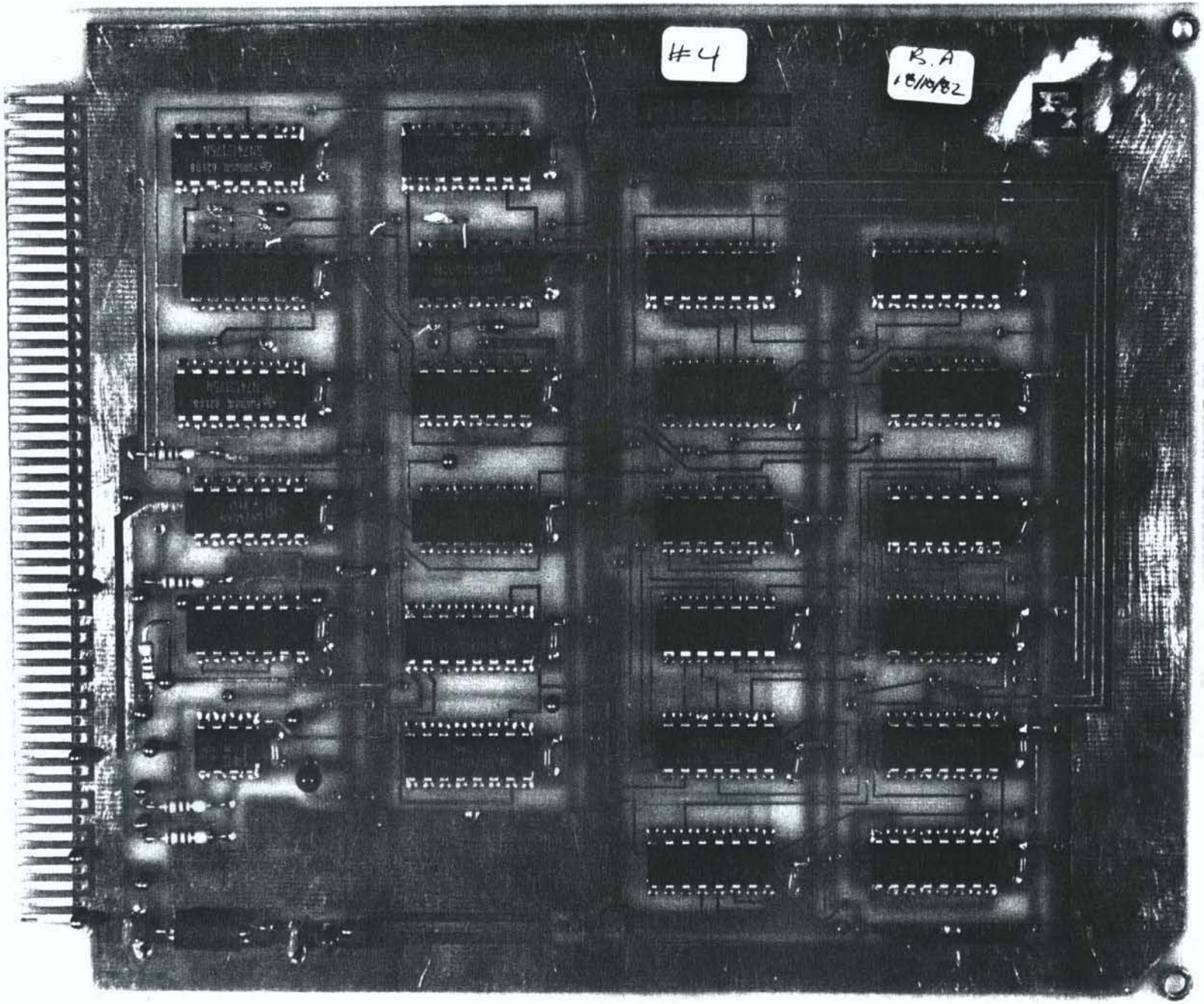
FOUNDATION INSTRUMENTS OTTAWA

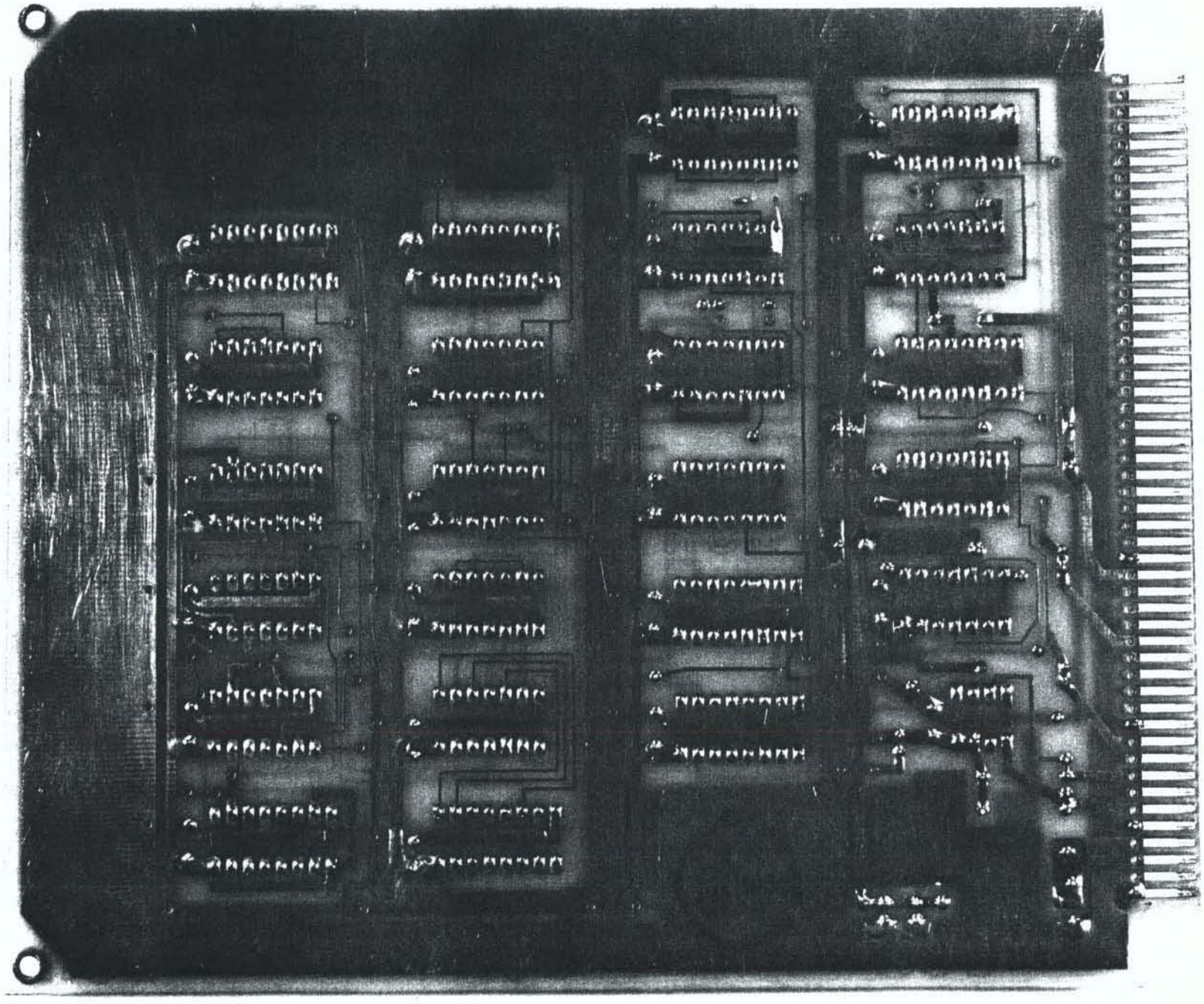
DATE: 82-09-03 | PROJ NO: 81013 | DRAWN BY: J.WHITEMAN

LAND TACTICAL DESCRAMBLER & F BIT RECOVERY

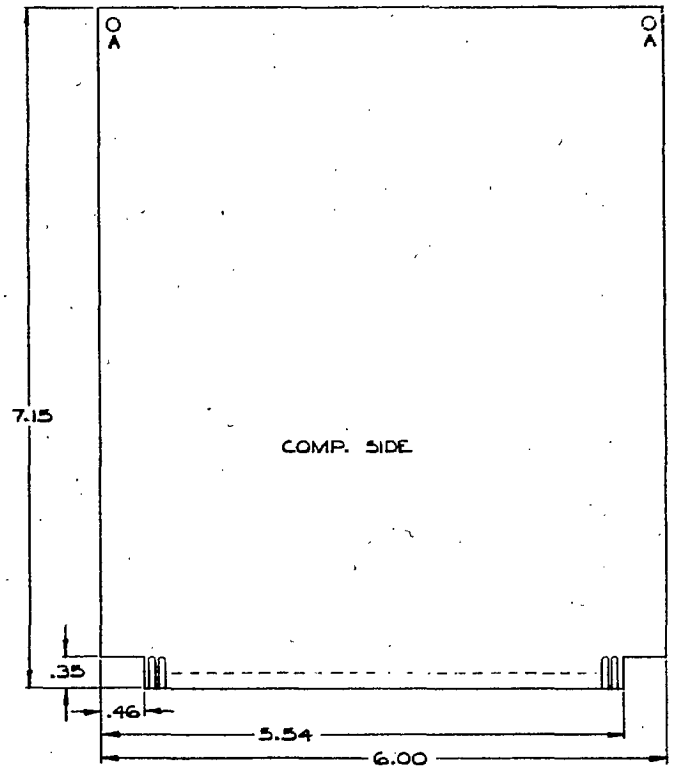
MATERIAL: | SCALE: 2/1 | SHEET OF

FINISH: | APPROVAL: R.U. 09/22/83 | DWG NO: *D2215


#4
B. A
10/19/82



REV	DATE	REVISIONS DESCRIPTIONS



HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA. (FINISHED)	2
OTHER	.037 DIA. (FINISHED)	

NOTE
1) HOLES TO BE DRILLED ON PAD CENTERS

-103-

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-09-02 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

LAND TACTICAL DESCRAMBLER & F BIT RECOVERY - MASTER

MATERIAL: G10, .062 THK GLASS EPOXY 1 OZ. COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

FINISH: TIN-LEAD PLATE .0002/.0003 THK CONT. GOLD, .0001/.0002 THK | APPROVAL: R Yu 17/09/82 | DWG NO: *2216

3.12 Data Demultiplexer

This section explains the data demultiplexer theory of operation. Included in this section are the following:

i) Block diagram
ii) Schematic D2221
iii) Overlay D2223
iv) Photograph, PCB 2222B component and solder side
v) Mechanical 2224 drilling diagram.

THEORY OF OPERATION

Module: Data Demultiplexer (FI-2222B)
Schematic No. D2221
Component Overlay D2223

Operational Description:

See accompanying block diagram and schematic no. D2221

Signal Conditioner:

An input D-type flip-flop that connects the incoming clock/data relationship for proper shift register operation.

Shift Registers

Cascaded shift registers whose parallel outputs expose the entire multiplexed stream to the inputs of the output latches.

Output Latches:

Loaded every 27 shift register clock cycles by an external load command that is synchronized to the F-bit.

Output Driver:

Interfaces the Codec CK and Data Parity Out channels with the Descrambler and F-Bit Recovery board.

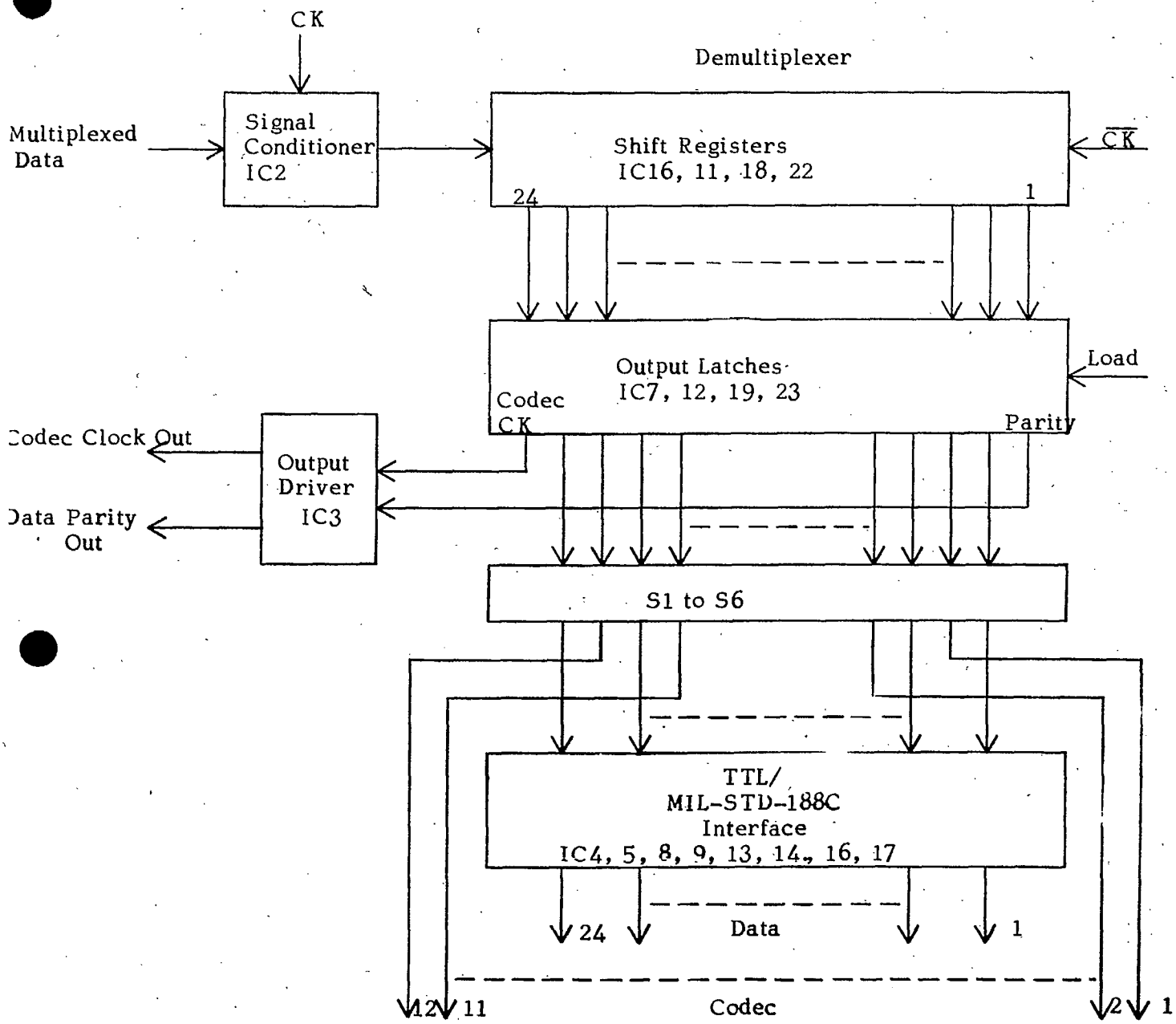
S1 to S6:

Manual switches that provide a choice between codec or data information over channels 1-12. They must be toggled identically to those on the multiplexer.

TTL/MIL-STD-188C Interface:

Converts outgoing data from TTL to MIL-STD-188C levels.

Land Tactical Demultiplexer (D2221)



REVISIONS		
REV	DATE	DESCRIPTIONS
E	82-10-26	DESIGN & DOCUMENTATION CHANGED W.O.# 2340

DATA IN FROM DATA DESCRAMBLER

DATA IN GND

CLOCK IN FROM DATA RECOVERY CCT.

CLOCK IN GND

FRAME SYNC. BIT FROM DATA DESCRAMBLER

F BIT

CODEC CK

PARITY BIT

CODEC CLOCK OUT

DATA PARITY OUT TO DATA DESCRAMBLER

+5V REG

+5V GND G3 (DIGITAL GND)

±12V REG.

-12V REG.

DECOUPLING CAPACITORS

74LS04 × 4

5GIG × 8

CH.24 DATA
CH.12 DATA
CH.8 CODEC DATA
CH.23 DATA
CH.11 DATA
CH.11 CODEC DATA
CH.22 DATA
CH.10 DATA
CH.10 CODEC DATA
CH.21 DATA
CH.9 DATA
CH.9 CODEC DATA
CH.20 DATA
CH.8 DATA
CH.8 CODEC DATA
CH.19 DATA
CH.7 DATA
CH.7 CODEC DATA
CH.18 DATA
CH.6 DATA
CH.6 CODEC DATA
CH.17 DATA
CH.5 DATA
CH.5 CODEC DATA
CH.16 DATA
CH.4 DATA
CH.4 CODEC DATA
CH.15 DATA
CH.3 DATA
CH.3 CODEC DATA
CH.14 DATA
CH.2 DATA
CH.2 CODEC DATA
CH.13 DATA
CH.1 DATA
CH.1 CODEC DATA

LAST NO USED
R4
C37
IC 23
L3
TP 74
SG

NOTES

1) IC 8, 13, 17, 24 PIN 14 - +5V
PIN 7 - GND (G3)

2) IC 8, 13, 17, 24 PIN 14 ARE A.C. COUPLED TO GND (G3) THRU A 0.1UF CAPACITOR (C20 TO C22)

3) IC 9, 10, 14, 15, 16, 20, 21, 5 PIN 14 - +12V
PIN 8 - -12V
PINS 3, 6, 7, 11 - GND (G3)

4) IC 9, 10, 14, 15, 16, 20, 21, 6 PIN 14 ARE A.C. COUPLED TO GND (G3) THRU A 0.1UF CAPACITOR (C23 TO C30)

5) IC 9, 10, 14, 15, 16, 20, 21, 5 PIN 8 ARE A.C. COUPLED TO GND (G3) THRU A 0.1 UF CAPACITOR (C31 TO C37, C7)

6) ALL GNDS ARE G3

7) S1-S6 ARE GRAYHILL 76ST08B DPDT DIP SWITCHES.

8) ALL UNUSED EDGE CONNECTOR CONTACTS ARE TO BE CONNECTED TO BOARD DIGITAL GROUND G3

9) MOST EDGE CONNECTOR DIGITAL GROUND PINS ARE SHARED BY TWO OUTPUTS AND HAVE BEEN LABELLED TO REFLECT THIS.

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

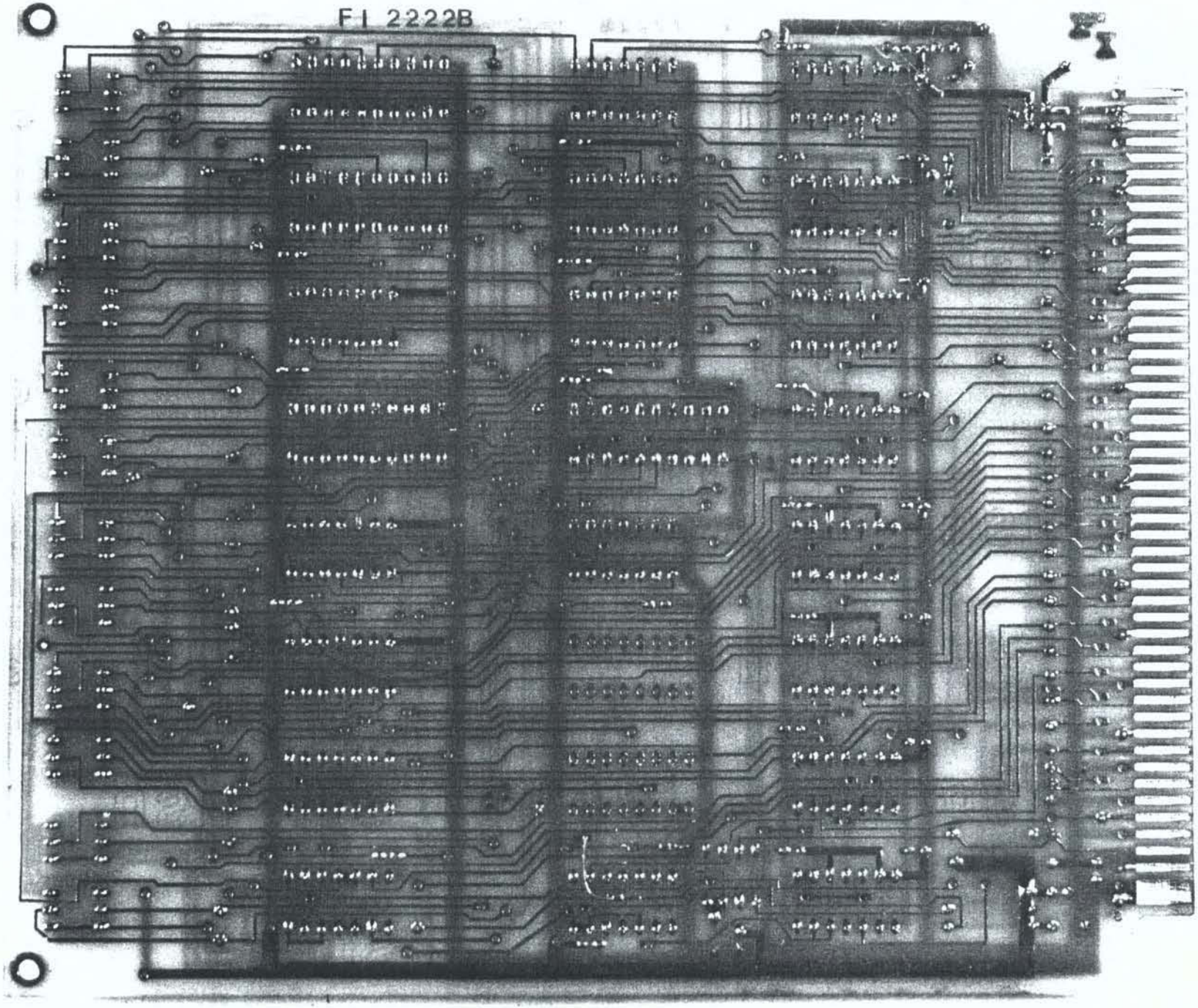
FOUNDATION INSTRUMENTS OTTAWA

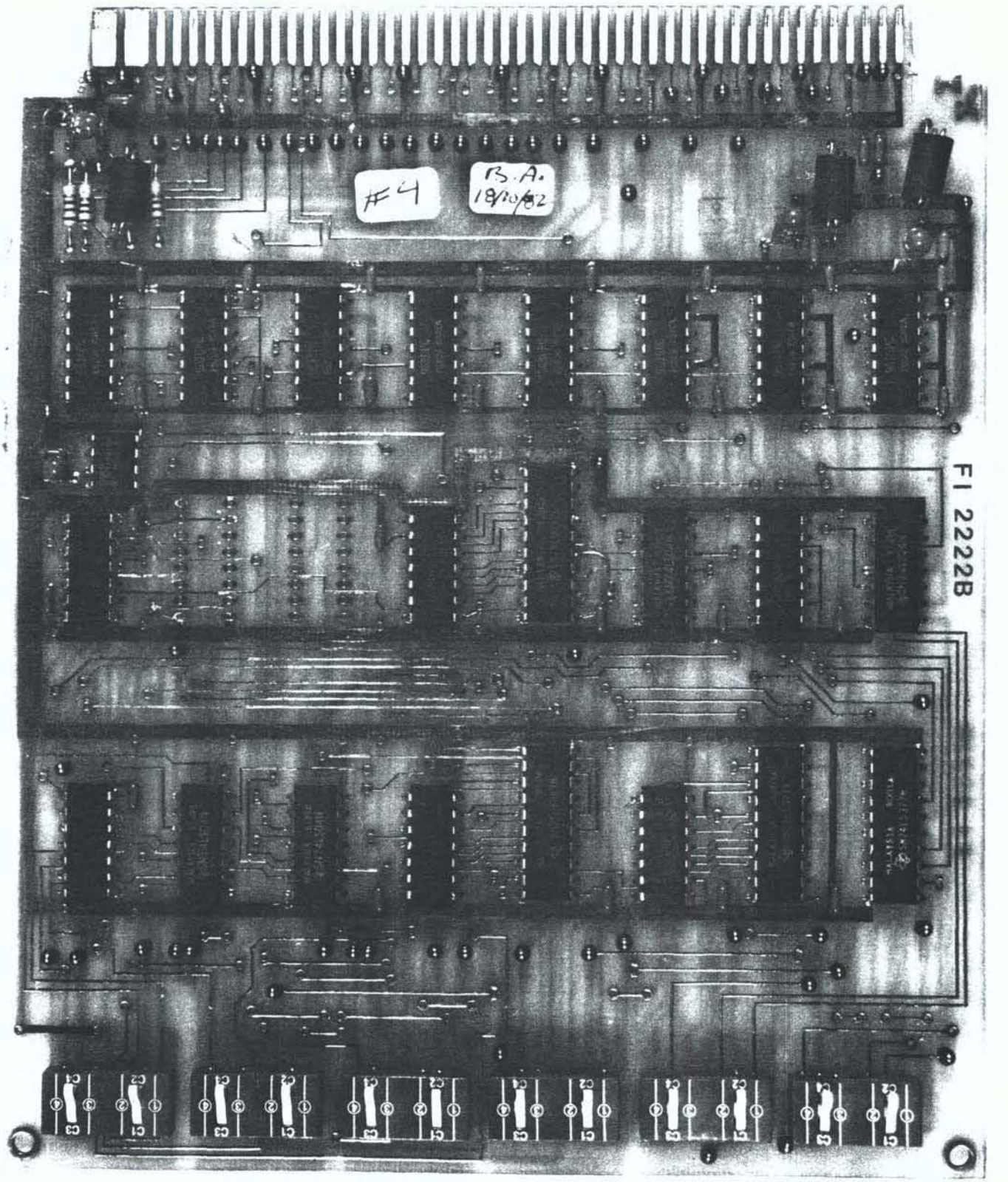
DATE: 82-04-05 | PROJ. NO: 810113 | DRAWN BY: J. WHITEMAN

LAND TACTICAL DATA DEMULTIPLEXER - SCHEM.

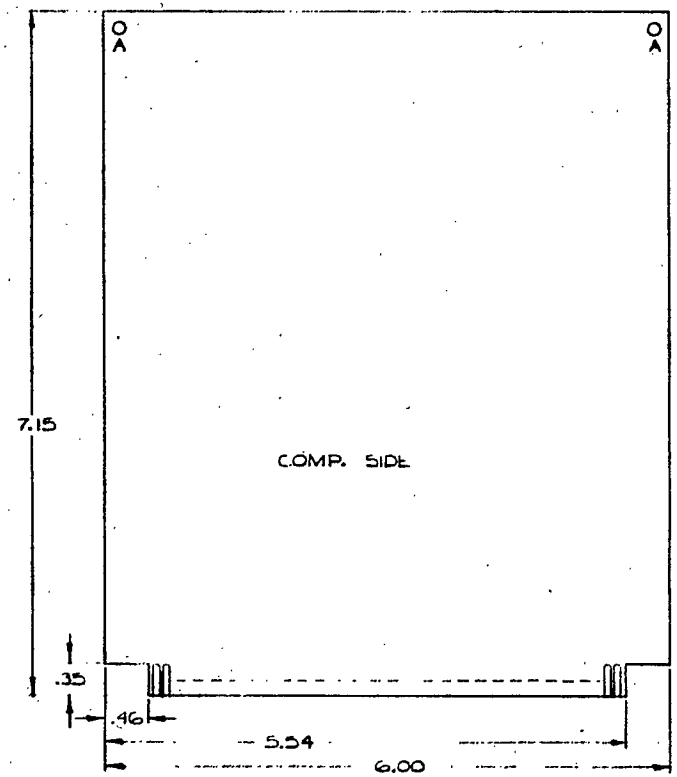
MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: R. Lamb 04/22/83 | DWG NO: D2221


FI 2222B


#4
B.A.
18/10/82
FI 2222B

REVISIONS		
REV	DATE	DESCRIPTIONS



HOLE DATA		
SYM	DESCRIPTION	QTY
A	.125 DIA. (FINISHED)	2
OTHER	.037 DIA. (FINISHED)	

NOTE
1) ALL HOLES TO BE DRILLED ON PAD CENTERS

-112-

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-09-02 | PROJ. NO: 810113 | DRAWN BY: J.WHITEMAN

LAND TACTICAL DATA DEMULTIPLEXER - MASTER

MATERIAL: G10, .062 THK, GLASS EPOXY 1 OZ. COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

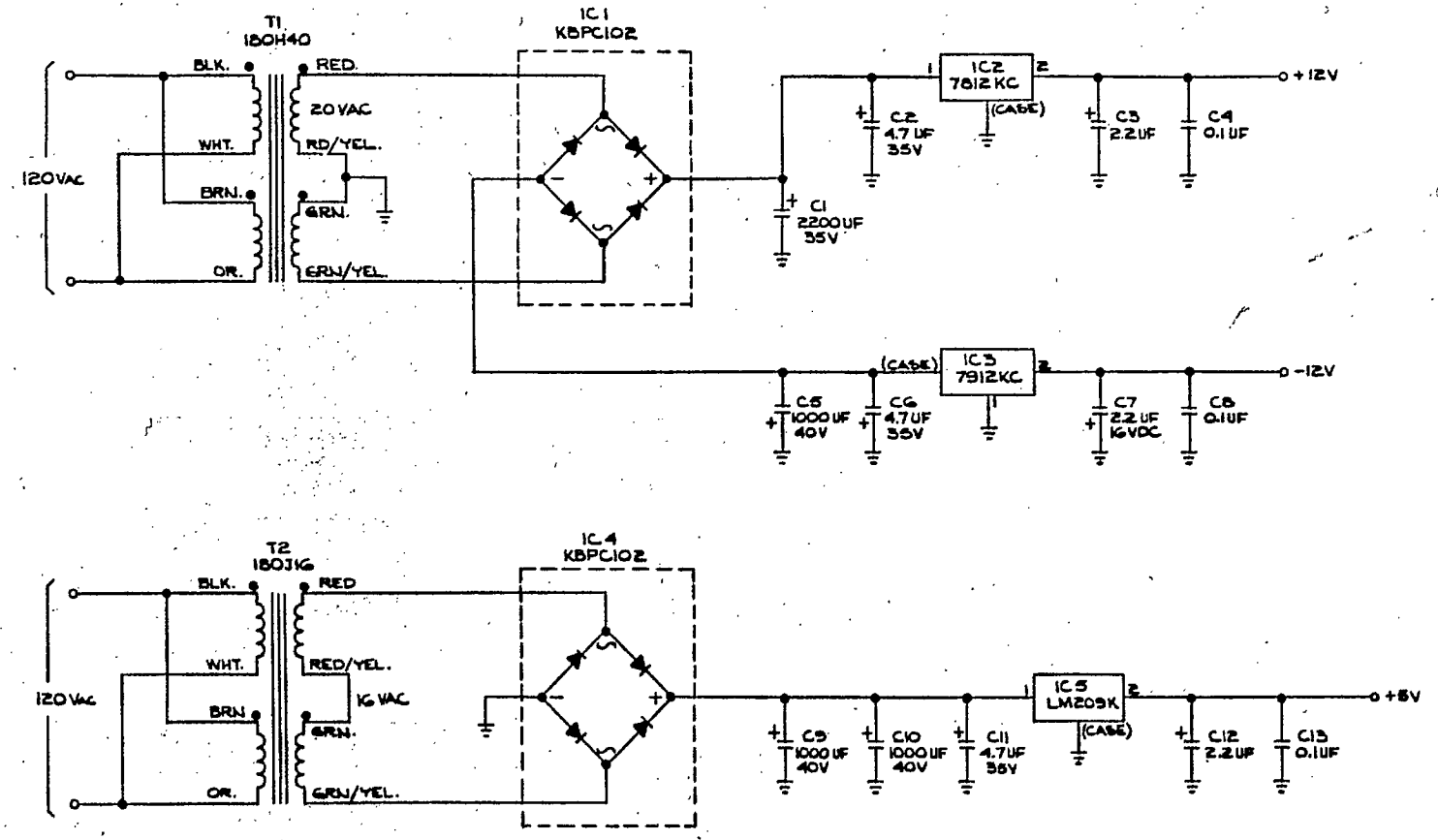
FINISH: TIN-LEAD PLATE .0002/.0003 THK CONT. GOLD .0001/.0002 THK | APPROVAL: R.Y. 17 Oct 82 | DWG NO: #2224

3.13 Power Supply

The Land Tactical power supply is designed to fit into a prespecified, constricting mechanical space. As a result, the transformers employed are toroidals, mounted on the case for heatsinking. The following includes:

i) Schematic 2588
ii) Parts list 2589
iii) Toroidal Transformer data sheet
iv) Mechanical D2022 extender case flange.

REVISIONS		
REV	DATE	DESCRIPTIONS



NOTE: (1) FILTERING CAPACITORS ARE TO BE MOUNTED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE IC'S.

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010 .XXX ±.005 ANGLES ±1/2° SURFACES: REMOVE BURRS & SHARP EDGES	FOUNDATION INSTRUMENTS OTTAWA		
	DATE: 83-03-02	PROJ. NO: 810113	DRAWN BY: RG.
	PWR SUPPLY. CDN. LAND TACTICAL		
MATERIAL:		SCALE:	SHEET OF
FINISH:		APPROVAL: R.Y. 16/03/83	DWG NO: 2588

REV	DATE	REVISIONS / DESCRIPTIONS

ITEM	QTY	PART NO.	DESCRIPTION	
T2	1	180J16	TRANSFORMER	HAMMOND
T1	1	180H40	TRANSFORMER	HAMMOND
IC5	1	LM209K	VOLTAGE REGULATOR, +5V	NATIONAL
IC3	1	7912KC	VOLTAGE REGULATOR, -12V	FAIRCHILD
IC2	1	7812KC	VOLTAGE REGULATOR, +12V	FAIRCHILD
IC1,4	2	KBPC102	BRIDGE RECTIFIER, 3A.	MOTOROLA
C5,9,10	3		CAPACITOR, 1000 UF, 40V. ELECTROLYTIC	
C4,8,13	3		0.1 UF, 50V, CERAMIC	
C3,7,12	3		2.2 UF, 16 VDC, TANTALUM	
C2,6,11	3		4.7 UF, 35V. TANTALUM	
C1	1		CAPACITOR. 2200 UF, 35V. ELECTROLYTIC	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 83-05-03 | PROJ. NO: 810113 | DRAWN BY: RG.

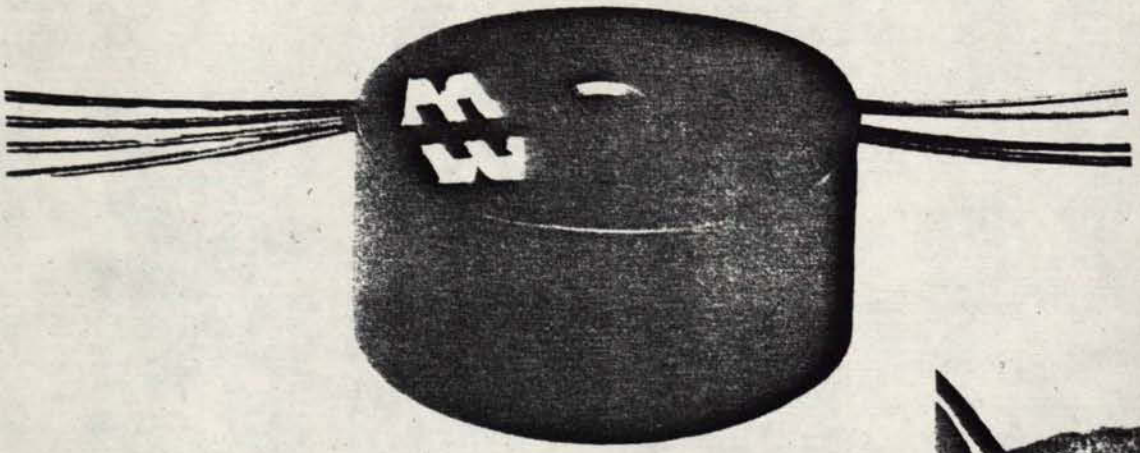
PWR. SUPPLY. CDN. LAND TACTICAL

MATERIAL: | SCALE: | SHEET OF

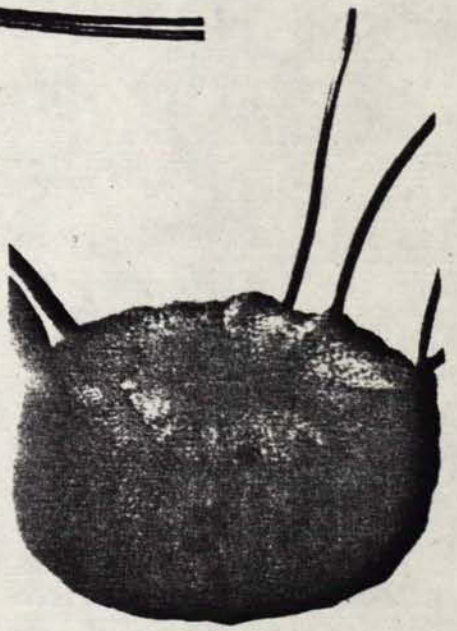
FINISH: | APPROVAL: R Yee 16/05/83 | DWG NO: 2589

TOROIDAL POWER TRANSFORMERS

180 & 181 SERIES



Typical 181 K20



Typical 180 K12

Open or Potted — Flexible Leads

- All models have 120/240 V, 50/60 Hz primaries.
- Split winding secondaries for single or dual output power supplies.
- Open or potted models have 8 " long flexible leads.
- Regulation from 4.3 to 25%.
- Hipot test between primary & secondary is 2500 volts RMS.
- Max. ambient temp. is 55°C for full power rating.
- Available in open (180 Series) or potted (181 Series) models.
- Centre hole clearance for #8 hardware.
- Open units supplied with 2 insulating washers and 1 metal centering washer.

PRIMARIES 120/240 VOLTS, 50/60 Hz

Secondary Volts Series	Secondary Volts Parallel	Secondary Amps Series	Secondary Amps Parallel	Total VA	Cat. No. Open	Dimensions Outside Dia.	Dimensions Height	Cat. No. Potted	Dimensions Outside Dia.	Dimensions Height
12.6	6.3	1.19	2.38	15	180 K12	2.38	1.38	181 K12	2.5	1.5
16	8	.94	1.88	15	180 J16	2.38	1.38	181 J16	2.5	1.5
20	10	.75	1.50	15	180 H20	2.38	1.38	181 H20	2.5	1.5
30	15	.50	1.0	15	180 G30	2.38	1.38	181 G30	2.5	1.5
12.6	6.3	2.38	4.76	30	180 L12	2.75	1.63	181 L12	3.00	1.75
16	8	1.88	3.76	30	180 L16	2.75	1.63	181 L16	3.00	1.75
20	10	1.5	3.0	30	180 K20	2.75	1.63	181 K20	3.00	1.75
24	12	1.25	2.5	30	180 K24	2.75	1.63	181 K24	3.00	1.75
30	15	1.0	2.0	30	180 J30	2.75	1.63	181 J30	3.00	1.75
40	20	.75	1.5	30	180 H40	2.75	1.63	181 H40	3.00	1.75
16	8	3.13	6.26	50	180 M16	3.13	1.63	181 M16	3.38	1.75
20	10	2.5	5.0	50	180 M20	3.13	1.63	181 M20	3.38	1.75
24	12	2.1	4.2	50	180 L24	3.13	1.63	181 L24	3.38	1.75
30	15	1.67	3.34	50	180 K30	3.13	1.63	181 K30	3.38	1.75
40	20	1.25	2.5	50	180 K40	3.13	1.63	181 K40	3.38	1.75
50	25	1.0	2.0	50	180 J50	3.13	1.63	181 J50	3.38	1.75
20	10	4.5	9.0	90	180 N20	3.50	1.88	181 N20	3.63	2.0
24	12	3.75	7.5	90	180 N24	3.50	1.88	181 N24	3.63	2.0
30	15	3.0	6.0	90	180 M30	3.50	1.88	181 M30	3.63	2.0
40	20	2.25	4.5	90	180 L40	3.50	1.88	181 L40	3.63	2.0
50	25	1.80	3.6	90	180 K50	3.50	1.88	181 K50	3.63	2.0
70	35	1.29	2.58	90	180 J70	3.50	1.88	181 J70	3.63	2.0
240	120	.38	.76	90	180 F240	3.50	1.88	181 F240	3.63	2.0

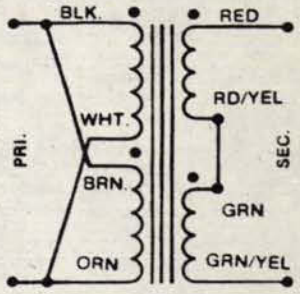
HAMMOND MANUFACTURING.

TOROIDAL POWER TRANSFORMERS CONT'D.
180 & 181 SERIES

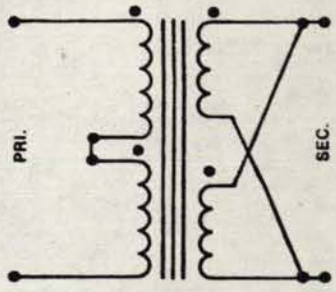
Secondary Volts Series	Secondary Volts Parallel	Secondary Amps Series	Secondary Amps Parallel	Total VA	Cat. No. Open	Dimensions Outside Dia.	Dimensions Height
24	12	5	10	120	**180 P24**	4.00	2.25
30	15	4	8	120	**180 N30**	4.00	2.25
40	20	3	6	120	**180 M40**	4.00	2.25
50	25	2.4	4.8	120	**180 L50**	4.00	2.25
70	35	1.7	3.4	120	**180 K70**	4.00	2.25
240	120	.5	1.0	120	**180 G240**	4.00	2.25
40	20	4	8	160	**180 N40**	4.20	2.25
50	25	3.2	6.4	160	**180 M50**	4.20	2.25
70	35	2.29	4.58	160	**180 L70**	4.20	2.25
240	120	.67	1.34	160	**180 H240**	4.20	2.25
40	20	5.63	11.26	225	**180 Q40**	4.63	2.50
50	25	4.5	9.0	225	**180 P50**	4.63	2.50
70	35	3.2	6.4	225	**180 M70**	4.63	2.50
240	120	.94	1.88	225	**180 J240**	4.63	2.50
50	25	6	12	300	**180 Q50**	5.00	2.63
70	35	4.29	8.58	300	**180 N70**	5.00	2.63
90	45	3.33	6.66	300	**180 M90**	5.00	2.63
56	28	8.93	17.86	500	**180 R56**	5.75	3.00
70	35	7.14	14.28	500	**180 Q70**	5.75	3.00
90	45	5.56	11.12	500	**180 P90**	5.75	3.00
110	55	4.55	9.10	500	**180 N110**	5.75	3.00

NOTE — All dimensions in inches, tolerance .125 inches max.

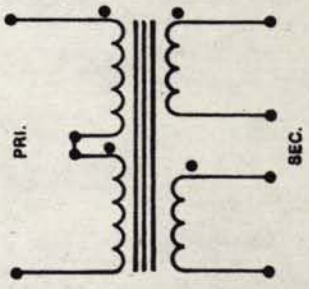
Typical Connections



120V PARALLEL PRIMARIES
SERIES CONNECTED SECONDARIES



240V SERIES PRIMARIES
PARALLEL CONNECTED SECONDARIES

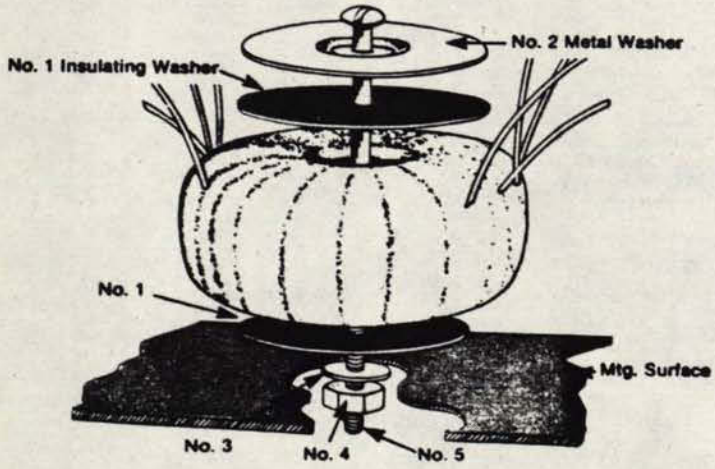


240V SERIES PRIMARIES
INDEPENDENT SECONDARIES

Application benefits for Toroidal Power Transformers

1. They are generally smaller and lighter.
2. Their low magnetising VA can give savings in open circuit power,e.g. instant-on circuitry.
3. The toroidal core provides lower core loss and a reduction in electrically induced noise (hum).
4. The inherent characteristic of the toroidal design reduces audible noise.
5. Another physical characteristic is its low profile being more adaptable to requirements of power supplies in modern electronic equipment.

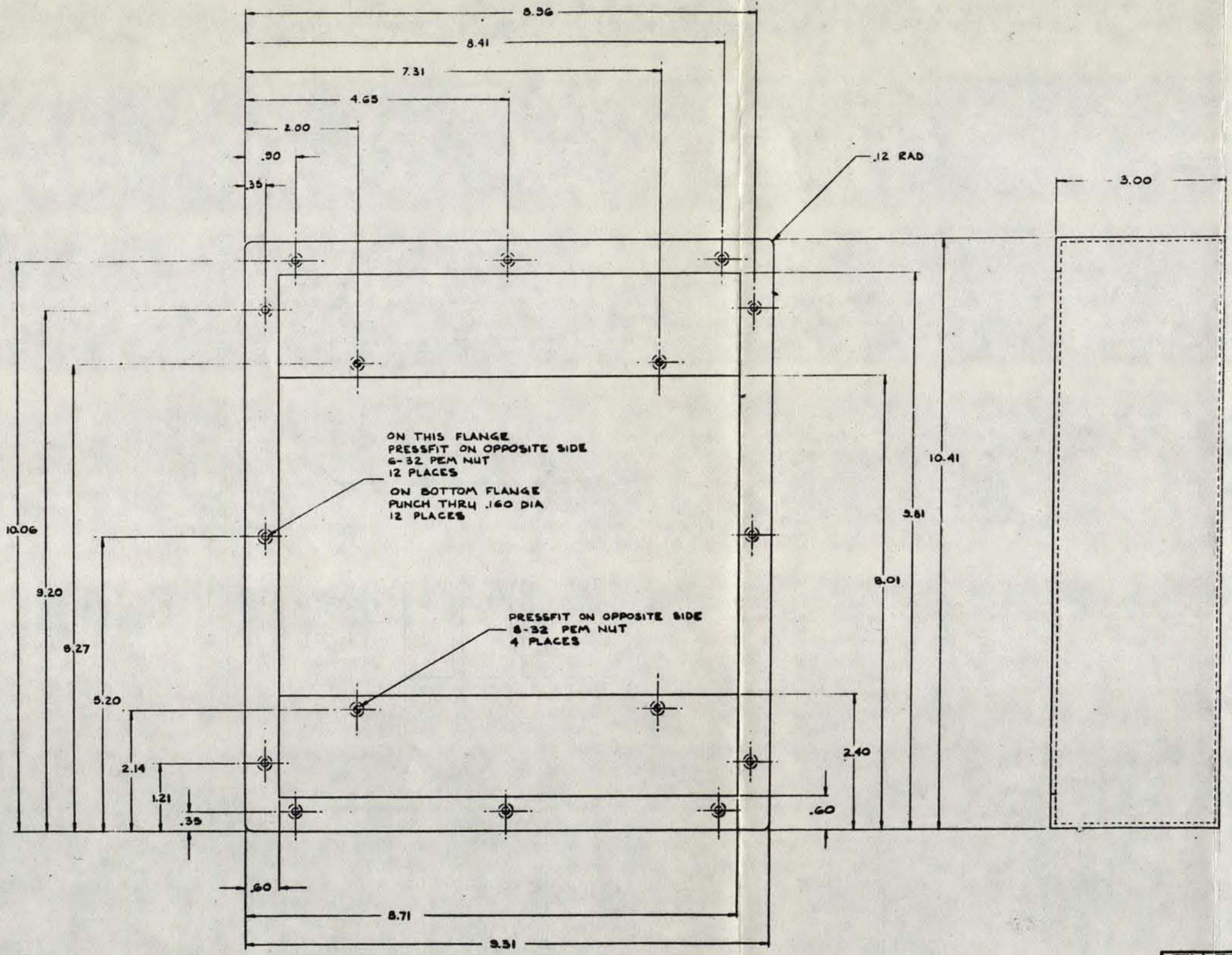
Typical Mounting Method 180 Series



Item 1 & 2 Supplied.
Items 3, 4, 5 not supplied.

NOTE: Do not short plate #2 to mounting surface.

REV	DATE	REVISIONS / DESCRIPTIONS



ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-05-06 | PROJ NO: 810113 | DRAWN BY: P.D.

EXTENDER FLANGE

MATERIAL: ALUMINUM .080 THK | SCALE: 1/1 | SHEET OF

FINISH: SMOOTH, BAKED-ON ENA. GREY | APPROVAL: R.L. 11/01/82 | DWG NO: D2022

3.14 Backplane Connections

This section details the interconnections from the Malco connector to the rear backplane. The following are included:

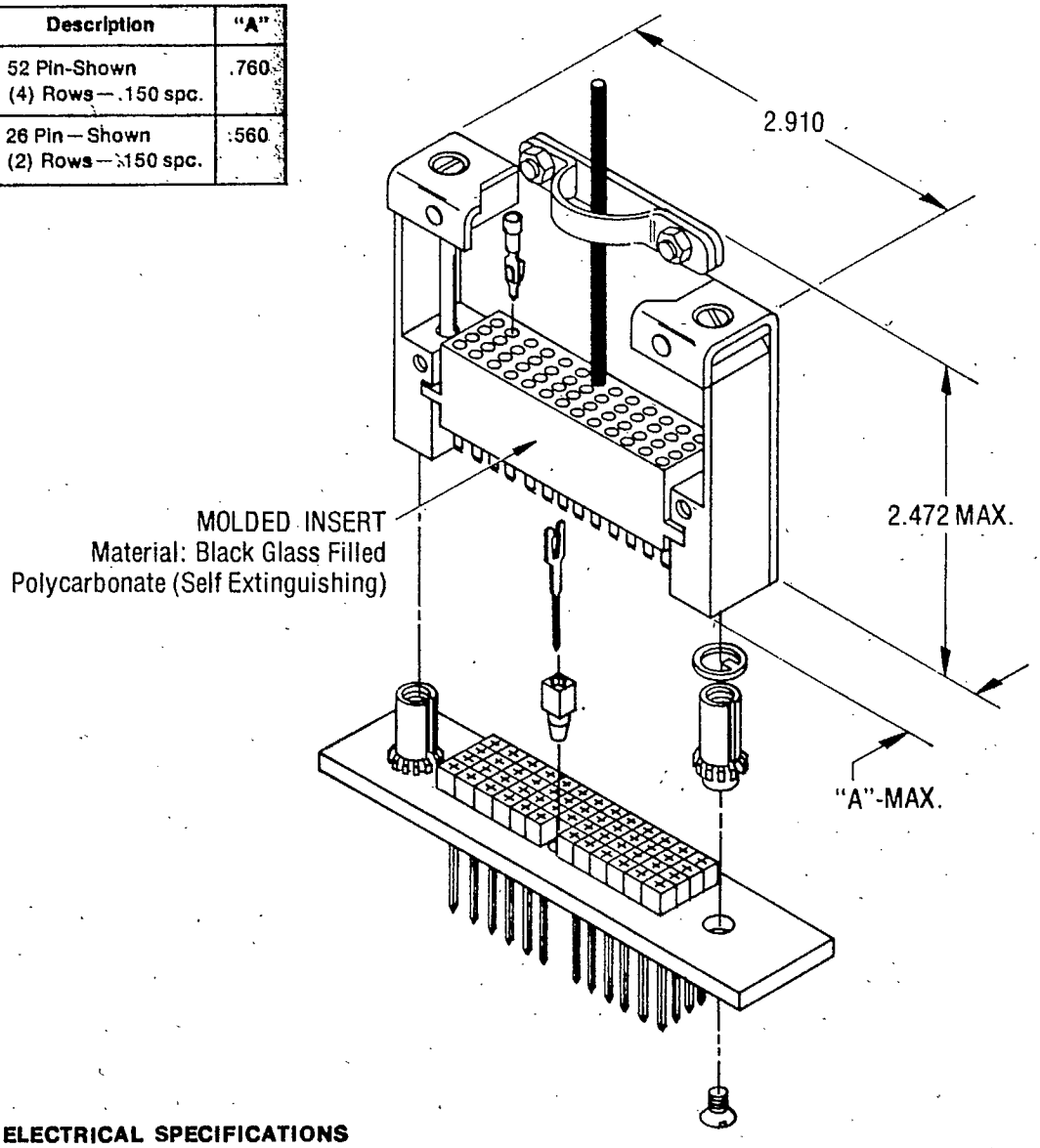
i) Malco connector assembly
ii) Photograph Malco connector
iii) Overlay - pin connections
iv) Overlay - PCB locations
v) Overlay - 2447 designated pin outs
vi) Wiring List - 2423 sheets 1 through 5
vii) Photograph - backplane wiring
viii) Photograph - assembled card cage and signal input panel
ix) Mechanical - 2020 - edge connector bracket
x) Mechanical - 2334 - ground buss
xi) Mechanical - 2024 Extender PCB master.

CAN CONNECTORS
MINI-CAN ASSEMBLIES

MINI-CAN ASSEMBLY WITH MOLDED INSERTS

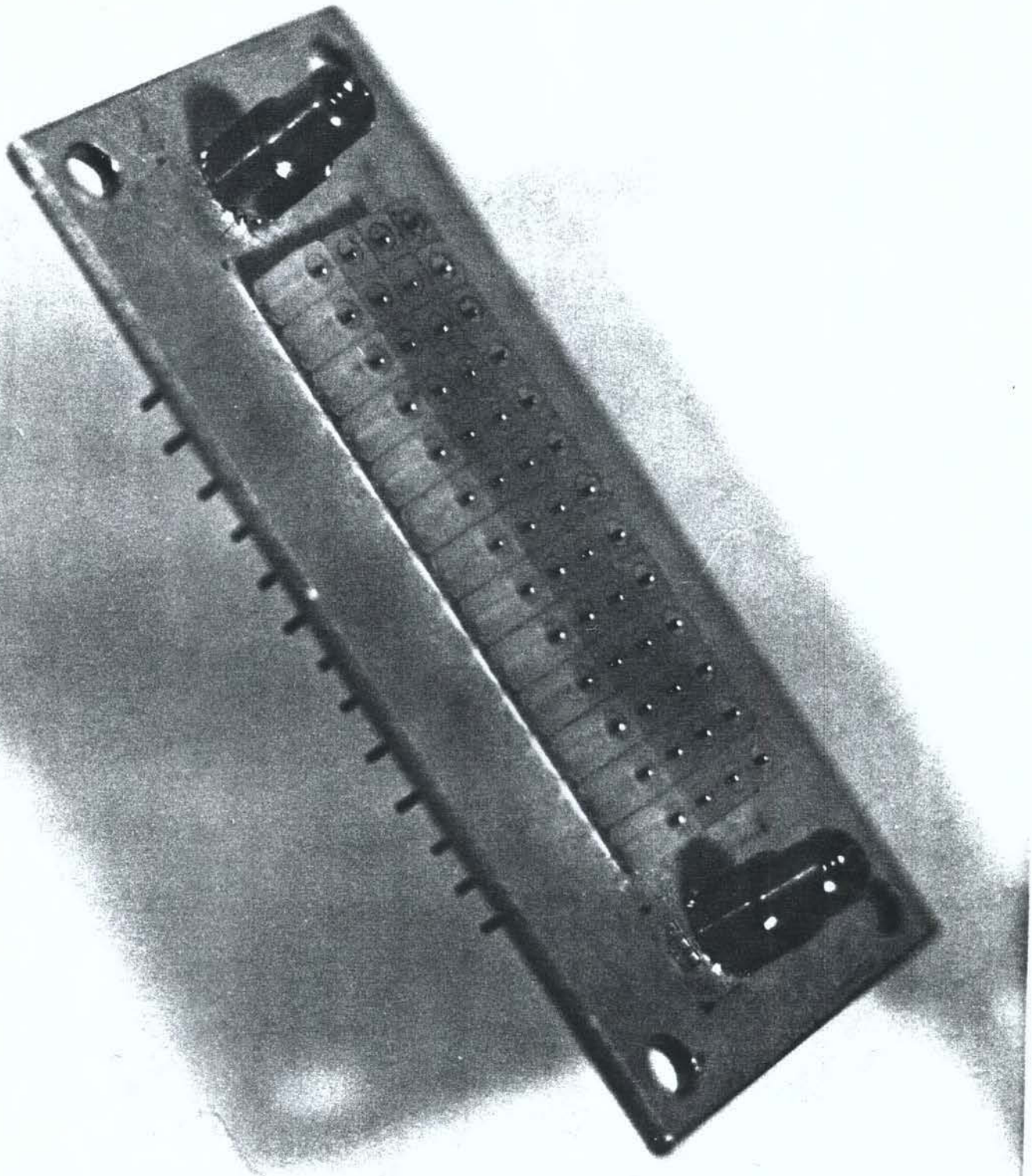
STANDARD OFF-THE-SHELF CONFIGURATIONS

Part No.	Description	"A"
451-1001-303	52 Pin-Shown (4) Rows—.150 spc.	.760
451-1000-303	26 Pin—Shown (2) Rows—.150 spc.	.560

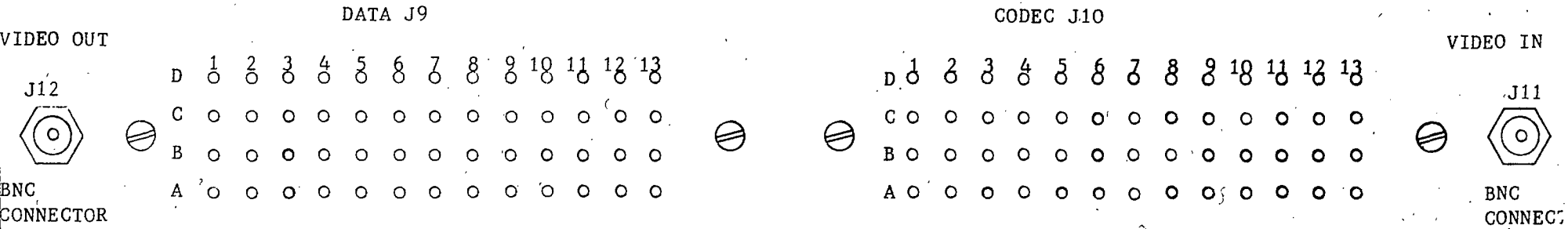


MINI-RACK ELECTRICAL SPECIFICATIONS
(per connection)

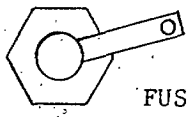
Current Rating..... 3 amps V.C. or A.C.
Working Voltage..... 300 V.A.C.
Breakdown Voltage..... approx. 1.5 KV
Contact Resistance..... below .004 ohms
Insulation Resistance..... 5000 megohms
Dry Circuitry..... 0.1 microvolt .10 milliamps
Operating Temperature..... max. continuous, 95°C



VIEW OF LAND TACTICAL EXTERNAL CONNECTORS
FROM INSIDE OF INPUT SIGNAL PANEL



MALCO CONNECTORS 451-1001-303

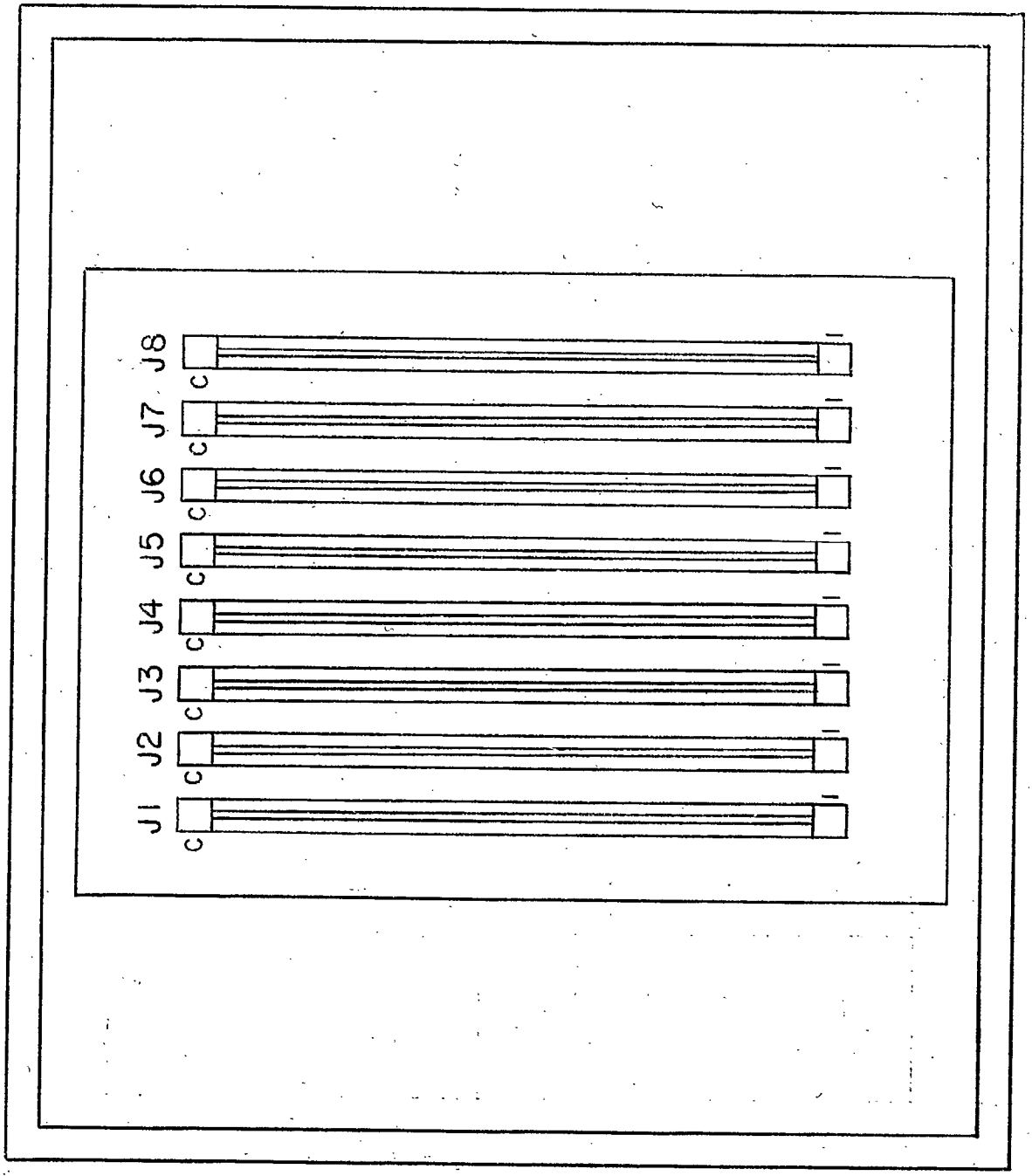


FUSE HOLDER

POWER CABLE

NOTE: ON TWO INPUT SIGNAL PANELS THE FUSE HOLDER AND POWER CABLE ARE ON THE RIGHT HAND SIDE.

LAND TACTICAL PCB LOCATION



REV	DATE	REVISIONS / DESCRIPTIONS

GB1

TO +12V P.S. (RED) | TO -12V P.S. (ORANGE) | TO +12V P.S. (RED) | TO +12V P.S. GND (BLACK, COPPER BRAID) | TO -12V P.S. (ORANGE)

CODEC (D2385) J1 | MUX. (D2205) J2 | PSK & VIDEO TX (D2201) J3

CH.7 ANALOG IN
CH.7 ANALOG IN
CH.7 DIGITAL IN
CH.7 DIGITAL OUT
CH.7 ANALOG OUT
CH.7 ANALOG OUT

CH.8 ANALOG IN
CH.8 ANALOG IN
CH.8 DIGITAL IN
CH.8 DIGITAL OUT
CH.8 ANALOG OUT
CH.8 ANALOG OUT

CH.9 ANALOG IN
CH.9 DIGITAL IN
CH.9 DIGITAL OUT
CH.9 ANALOG OUT
CH.9 ANALOG OUT

CH.10 ANALOG IN
CH.10 ANALOG IN
CH.10 DIGITAL IN
CH.10 DIGITAL OUT
CH.10 ANALOG OUT
CH.10 ANALOG OUT

CH.11 ANALOG IN
CH.11 ANALOG IN
CH.11 DIGITAL IN
CH.11 DIGITAL OUT
CH.11 ANALOG OUT
CH.11 ANALOG OUT

CH.12 ANALOG IN/OUT
CH.12 ANALOG IN/OUT

CH.12 DIGITAL IN
CH.12 DIGITAL OUT

TX CLOCK
RX CLOCK

DATA CH.1 CODEC DATA
CH.14 DATA CH.13 DATA
CODEC DATA CH.2 DATA — VIDEO IN (TO J11)

DATA CH.3 CODEC DATA
CH.16 DATA CH.15 DATA
CODEC DATA CH.4 DATA

DATA CH.5 CODEC DATA
CH.18 DATA CH.17 DATA
CODEC DATA CH.6 DATA

DATA CH.7 CODEC DATA
CH.20 DATA CH.19 DATA
CODEC DATA CH.8 DATA

DATA CH.9 CODEC DATA
CH.22 DATA CH.21 DATA
CODEC DATA CH.10 DATA

DATA CH.11 CODEC DATA
CH.24 DATA CH.23 DATA
CODEC DATA CH.12 DATA

MUX CLOCK IN — MUX CLOCK OUT
MUX DATA OUT — DATA IN
CODEC CK OUT

TX D.C. MONITOR (TO J13-2A)

SIGNAL OUT TO POTX (TO J13-2B)

GB3

TO +5V P.S. GND (BLACK, COPPER BRAID) | TO +5V P.S. (VIOLET) | TO -12V P.S. (ORANGE)

TO +12V P.S. GND (BLACK, COPPER BRAID) | TO +12V P.S. (RED) | TO -12V P.S. (ORANGE) | TO +12V P.S. (RED) | TO -12V P.S. (ORANGE)

GB2

PSK & VIDEO SEPARATOR (D2209) J4 | PSK DATA RECOVERY (D2217) J5 | DESCRAMBLER (D2213) J6 | DEMUX. (D2221) J7 | CODEC (D2385) J8

PSK DATA SIGNAL OUT — PSK DATA SIGNAL IN

SIGNAL IN FROM FOREX (TO J13-3A)

VIDEO OUT (TO J12)

DATA OUT — DATA IN
DATA PARITY IN
RX CLOCK OUT — CLOCK IN
FRAME SYNCH. OUT
DEMUX. DATA OUT
FERROXCUBE VK200-20/4B

DATA CH.1 CODEC DATA
CH.13 DATA
DATA CH.2 CODEC DATA
CH.14 DATA
DATA CH.3 CODEC DATA
CH.15 DATA
DATA CH.4 CODEC DATA
CH.16 DATA
DATA CH.5 CODEC DATA
CH.17 DATA
DATA CH.6 CODEC DATA
CH.18 DATA
DATA CH.7 CODEC DATA
CH.19 DATA
DATA CH.8 CODEC DATA
CH.20 DATA
DATA CH.9 CODEC DATA
CH.21 DATA
DATA CH.10 CODEC DATA
CH.22 DATA
DATA CH.11 CODEC DATA
CH.23 DATA
DATA CH.12 CODEC DATA
CH.24 DATA

CLOCK IN — CLOCK IN
FRAME SYNCH. IN
DEMUX. DATA IN
CODEC CK OUT
DATA PARITY OUT

CH.1 ANALOG IN
CH.1 ANALOG IN
CH.1 DIGITAL IN
CH.1 DIGITAL OUT
CH.1 ANALOG OUT
CH.1 ANALOG OUT

CH.2 ANALOG IN
CH.2 ANALOG IN
CH.2 DIGITAL IN
CH.2 DIGITAL IN
CH.2 ANALOG OUT
CH.2 ANALOG OUT

CH.3 ANALOG IN
CH.3 ANALOG IN
CH.3 DIGITAL IN

CH.3 DIGITAL OUT
CH.3 ANALOG OUT
CH.3 ANALOG OUT

CH.4 ANALOG IN
CH.4 ANALOG IN
CH.4 DIGITAL IN
CH.4 DIGITAL OUT
CH.4 ANALOG OUT
CH.4 ANALOG OUT

CH.5 ANALOG IN
CH.5 ANALOG IN
CH.5 DIGITAL IN
CH.5 DIGITAL OUT
CH.5 ANALOG OUT
CH.5 ANALOG OUT

CH.6 ANALOG IN/OUT
CH.6 ANALOG IN/OUT

CH.6 DIGITAL IN
CH.6 DIGITAL OUT

TX CLOCK
RX CLOCK

GB4

TO +5V P.S. (VIOLET)

TO +5V P.S. GND (BLACK, COPPER BRAID)

NOTE: SHOWN ABOVE ARE PRELIMINARY CONNECTIONS. SEE WIRING LISTS # 2423 (SHEET 1 TO 5) FOR ADDITIONAL CONNECTIONS.

ITEM	QTY	PART NO.	DESCRIPTION
NEXT ASSY # 2450			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .X ± .010
.XXX ± .005
ANGLES ± 1/2°
SURFACES:
REMOVE BURRS | SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-09-16 | PROJ. NO: 81013 | DRAWN BY: J. WHITEMAN

LAND TACTICAL RACK BACKPLANE - WIRING DIAGRAM

MATERIAL: | SCALE: | SHEET OF

FINISH: | APPROVAL: R.I. 17/02/83 | DWG NO: # 2447

WIRE LIST	FI	FOUNDATION INSTRUMENTS OTTAWA	DWG NO. 2423	REV.
APPROVAL	CONTRACT NO. 810113	CONTRACT LAND TACTICAL	SHEET 1 OF 5	DATE

WIRE NO.	FUNCTION	AWG	TYPE	FROM Connector - Pin	TO Connector - Pin	COLOR
	CH.1 Codec	22	Stranded	J7 - 9	J8 - 12	
	CH.2 "	"	"	J7 - 15	J8 - 26	
	CH.3 "	"	"	J7 - 21	J8 - 38	
	CH.4 "	"	"	J7 - 27	J8 - 52	
	CH.5 "	"	"	J7 - 33	J8 - 66	
	CH.6 "	"	"	J7 - 39	J8 - 82	YELLOW/
	CH.7 "	"	"	J7 - 45	J1 - 11	WHITE
	CH.8 "	"	"	J7 - 51	J1 - 25	
	CH.9 "	"	"	J7 - 57	J1 - 37	
	CH.10 "	"	"	J7 - 63	J1 - 51	
	CH.11 "	"	"	J7 - 69	J1 - 65	
	CH.12 "	"	"	J7 - 75	J1 - 81	
	CH.1 Codec	22	Stranded	J2 - 11	J8 - 14	
	CH.2 "	"	"	J2 - 18	J8 - 28	
	CH.3 "	"	"	J2 - 21	J8 - 42	
	CH.4 "	"	"	J2 - 28	J8 - 54	
	CH.5 "	"	"	J2 - 31	J8 - 68	
	CH.6 "	"	"	J2 - 38	J8 - 84	BLUE
	CH.7 "	"	"	J2 - 41	J1 - 13	
	CH.8 "	"	"	J2 - 48	J1 - 27	
	CH.9 "	"	"	J2 - 51	J1 - 41	
	CH.10 "	"	"	J2 - 58	J1 - 53	
	CH.11 "	"	"	J2 - 61	J1 - 67	
	CH.12 "	"	"	J2 - 68	J1 - 83	

WIRE LIST	FI	FOUNDATION INSTRUMENTS OTTAWA	DWG NO. 2423	REV.
APPROVAL	CONTRACT NO. 810113	CONTRACT LAND TACTICAL	SHEET 2 OF 5	DATE

WIRE NO.	FUNCTION	AWG	TYPE	FROM Connector - Pin	TO Connector - Pin	COLOR
	CH.1 Data	22	Stranded	J2 - 12	J9 - D1	
	CH.2 "	"	"	J2 - 17	J9 - D2	
	CH.3 "	"	"	J2 - 22	J9 - D3	GREEN/ WHITE
	CH.4 "	"	"	J2 - 27	J9 - D4	
	CH.5 "	"	"	J2 - 32	J9 - D5	
	CH.6 "	"	"	J2 - 37	J9 - D6	
	CH.7 "	"	"	J2 - 42	J9 - D7	
	CH.8 "	"	"	J2 - 47	J9 - D8	BLUE/ WHITE
	CH.9 "	"	"	J2 - 52	J9 - D9	
	CH.10 "	"	"	J2 - 57	J9 - D10	
	CH.11 "	"	"	J2 - 62	J9 - D11	
	CH.12 "	"	"	J2 - 67	J9 - D12	
	CH.13 "	"	"	J2 - 13	J9 - C1	YELLOW/ WHITE
	CH.14 "	"	"	J2 - 16	J9 - C2	
	CH.15 "	"	"	J2 - 23	J9 - C3	
	CH.16 "	"	"	J2 - 26	J9 - C4	
	CH.17 "	"	"	J2 - 33	J9 - C5	
	CH.18 "	"	"	J2 - 36	J9 - C6	
	CH.19 "	"	"	J2 - 43	J9 - C7	BLUE
	CH.20 "	"	"	J2 - 46	J9 - C8	
	CH.21 "	"	"	J2 - 53	J9 - C9	
	CH.22 "	"	"	J2 - 56	J9 - C10	
	CH.23 "	"	"	J2 - 63	J9 - C11	
	CH.24 "	"	"	J2 - 66	J9 - C12	

WIRE LIST	FI	FOUNDATION INSTRUMENTS OTTAWA	DWG NO. 2423	REV.
APPROVAL	CONTRACT NO. 810133	CONTRACT LAND TACTICAL	SHEET 3 OF 5	DATE

WIRE NO.	FUNCTION	AWG	TYPE	FROM Connector - Pin	TO Connector - Pin	COLOR	
	CH.1 Codec	22	Stranded	J8 - 7	J10 - D1		
		"	"	J8 - 9	J10 - D2		
	CH.2 "	"	"	J8 - 21	J10 - D3		
		"	"	J8 - 23	J10 - D4		
	CH.3 "	"	"	J8 - 33	J10 - D5		
		"	"	J8 - 35	J10 - D6		
	CH.4 "	"	"	J8 - 47	J10 - D7	YELLOW/	
		"	"	J8 - 49	J10 - D8	WHITE	
	CH.5 "	"	"	J8 - 61	J10 - D9		
		"	"	J8 - 63	J10 - D10		
	CH.6 "	"	"	J8 - 75	J10 - D11		
		"	"	J8 - 77	J10 - D12		
	CH.7 "	"	"	J1 - 8	J10 - C1		
		"	"	J1 - 10	J10 - C2		
	CH.8 "	"	"	J1 - 22	J10 - C3		
		"	"	J1 - 24	J10 - C4		
	CH.9 "	"	"	J1 - 34	J10 - C5		
		"	"	J1 - 36	J10 - C6		
	CH.10 "	"	"	J1 - 48	J10 - C7	BLUE	
		"	"	J1 - 50	J10 - C8		
	CH.11 "	"	"	J1 - 62	J10 - C9		
		"	"	J1 - 64	J10 - C10		
	CH.12 "	"	"	J1 - 76	J10 - C11		
		"	"	J1 - 78	J10 - C12		
	SIGNAL GROUND	"	"	POWER SUPPLY GROUND	J10 - D13		
	" "	"	"	" " "	J10 - C13	BLACK	

WIRE LIST	FI	FOUNDATION INSTRUMENTS OTTAWA	DWG NO. 2423	REV.
APPROVAL	CONTRACT NO. 810113	CONTRACT LAND TACTICAL	SHEET 4 OF 5	DATE

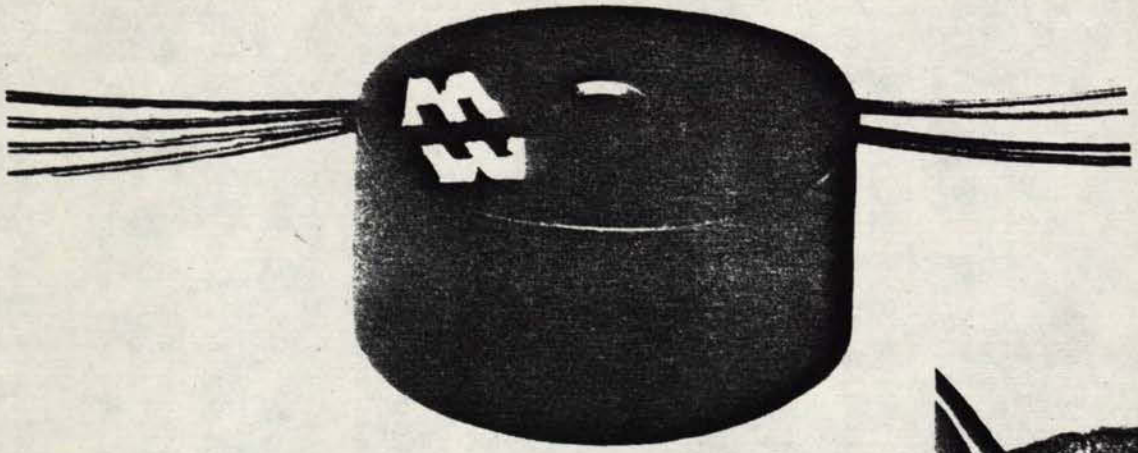
WIRE NO.	FUNCTION	AWG	TYPE	FROM Connector - Pin	TO Connector - Pin	COLOR
	CH.1 Data	22	Stranded	J7 - 10	J9 - B1	GREEN/ WHITE
	CH.2 "	"	"	J7 - 16	J9 - B2	
	CH.3 "	"	"	J7 - 22	J9 - B3	
	CH.4 "	"	"	J7 - 28	J9 - B4	
	CH.5 "	"	"	J7 - 34	J9 - B5	
	CH.6 "	"	"	J7 - 40	J9 - B6	BLUE/ WHITE
	CH.7 "	"	"	J7 - 46	J9 - B7	
	CH.8 "	"	"	J7 - 52	J9 - B8	
	CH.9 "	"	"	J7 - 58	J9 - B9	
	CH.10 "	"	"	J7 - 64	J9 - B10	
	CH.11 "	"	"	J7 - 70	J9 - B11	YELLOW/ WHITE
	CH.12 "	"	"	J7 - 76	J9 - B12	
	CH.13 "	"	"	J7 - 11	J9 - A1	
	CH.14 "	"	"	J7 - 17	J9 - A2	
	CH.15 "	"	"	J7 - 23	J9 - A3	
	CH.16 "	"	"	J7 - 29	J9 - A4	BLUE
	CH.17 "	"	"	J7 - 35	J9 - A5	
	CH.18 "	"	"	J7 - 41	J9 - A6	
	CH.19 "	"	"	J7 - 47	J9 - A7	
	CH.20 "	"	"	J7 - 53	J9 - A8	
	CH.21 "	"	"	J7 - 59	J9 - A9	
	CH.22 "	"	"	J7 - 65	J9 - A10	
	CH.23 "	"	"	J7 - 71	J9 - A11	
	CH.24 "	"	"	J7 - 77	J9 - A12	
	SIGNAL GROUND	"	"	POWER SUPPLY GROUND	J9 - B13	BLACK
	" "				J9 - A13	

WIRE LIST	FI	FOUNDATION INSTRUMENTS OTTAWA	DWG NO. 2423	REV.
APPROVAL	CONTRACT NO. 810113	CONTRACT LAND TACTICAL	SHEET 5 OF 5	DATE

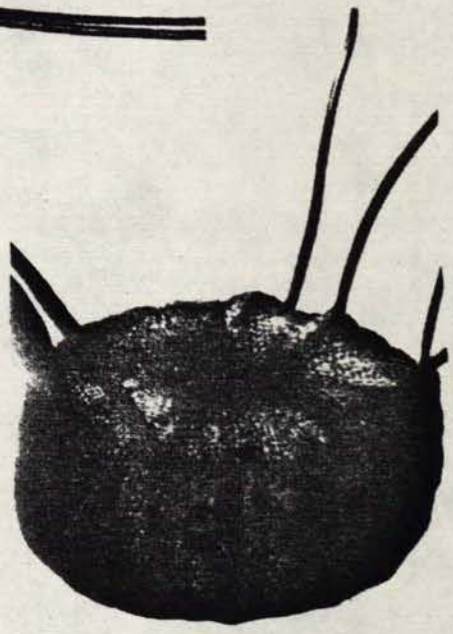
WIRE NO.	FUNCTION	AWG	TYPE	FROM Connector - Pin	TO Connector - Pin	COLOR
	CH.1 Codec	22	Stranded	J8 - 15	J10 - B1	
	"	"	"	J8 - 17	J10 - B2	
	CH.2 "	"	"	J8 - 29	J10 - B3	
	"	"	"	J8 - 31	J10 - B4	GREEN/
	CH.3 "	"	"	J8 - 43	J10 - B5	WHITE
	"	"	"	J8 - 45	J10 - B6	
	CH.4 "	"	"	J8 - 55	J10 - B7	
	"	"	"	J8 - 57	J10 - B8	
	CH.5 "	"	"	J8 - 69	J10 - B9	
	"	"	"	J8 - 71	J10 - B10	
	CH.7 "	"	"	J1 - 16	J10 - A1	
	"	"	"	J1 - 18	J10 - A2	
	CH.8 "	"	"	J1 - 30	J10 - A3	
	"	"	"	J1 - 32	J10 - A4	BLUE/
	CH.9 "	"	"	J1 - 44	J10 - A5	WHITE
	"	"	"	J1 - 46	J10 - A6	
	CH.10 "	"	"	J1 - 56	J10 - A7	
	"	"	"	J1 - 58	J10 - A8	
	CH.11 "	"	"	J1 - 70	J10 - A9	
	"	"	"	J1 - 72	J10 - A10	
	SIGNAL GROUND	"	"	POWER SUPPLY GROUND	J10 - B11	
	" "	"	"	" " "	J10 - B12	
	" "	"	"	" " "	J10 - B13	
	" "	"	"	" " "	J10 - A11	BLACK
	" "	"	"	" " "	J10 - A12	
	" "	"	"	" " "	J10 - A13	

TOROIDAL POWER TRANSFORMERS

180 & 181 SERIES



Typical 181 K20



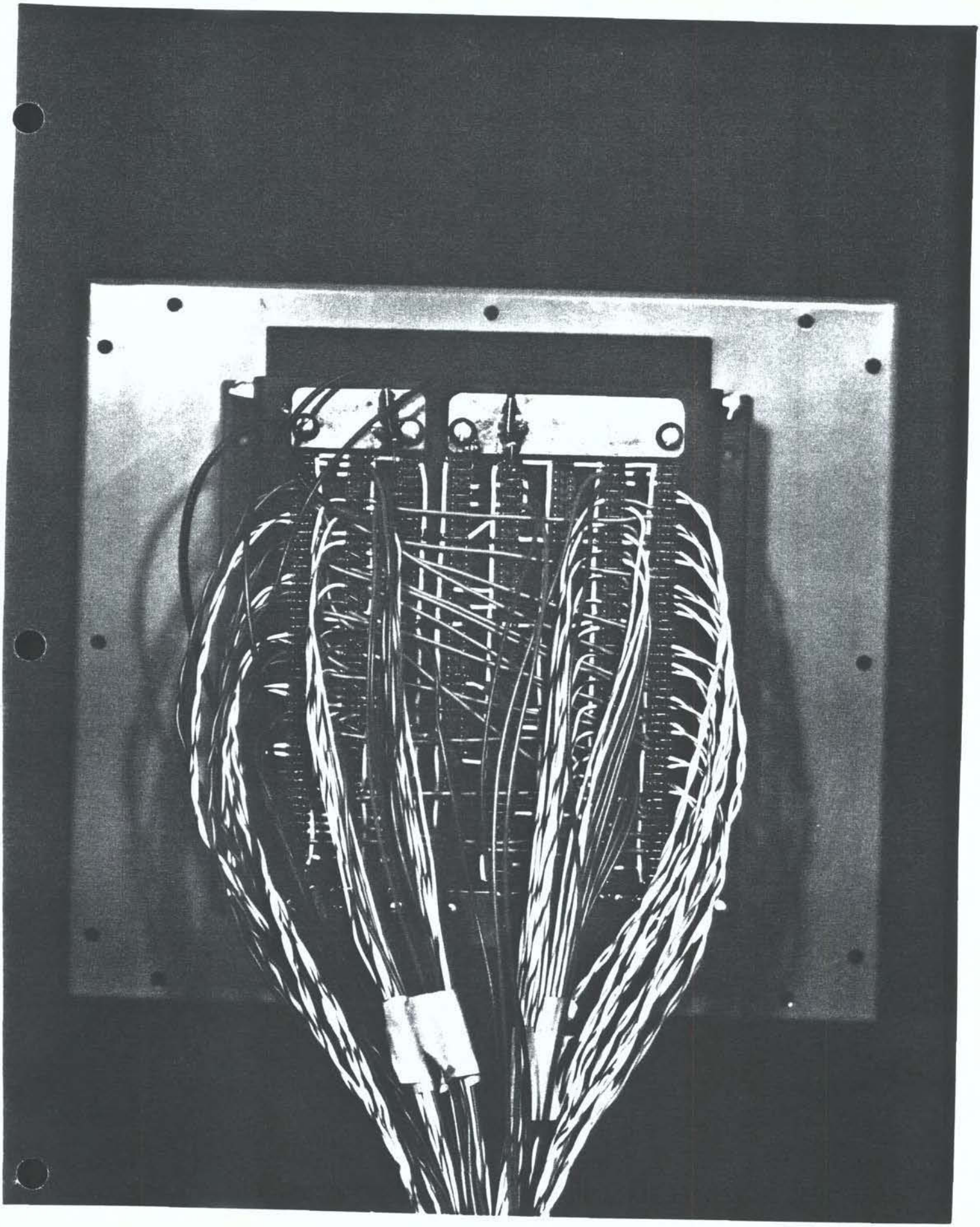
Typical 180 K12

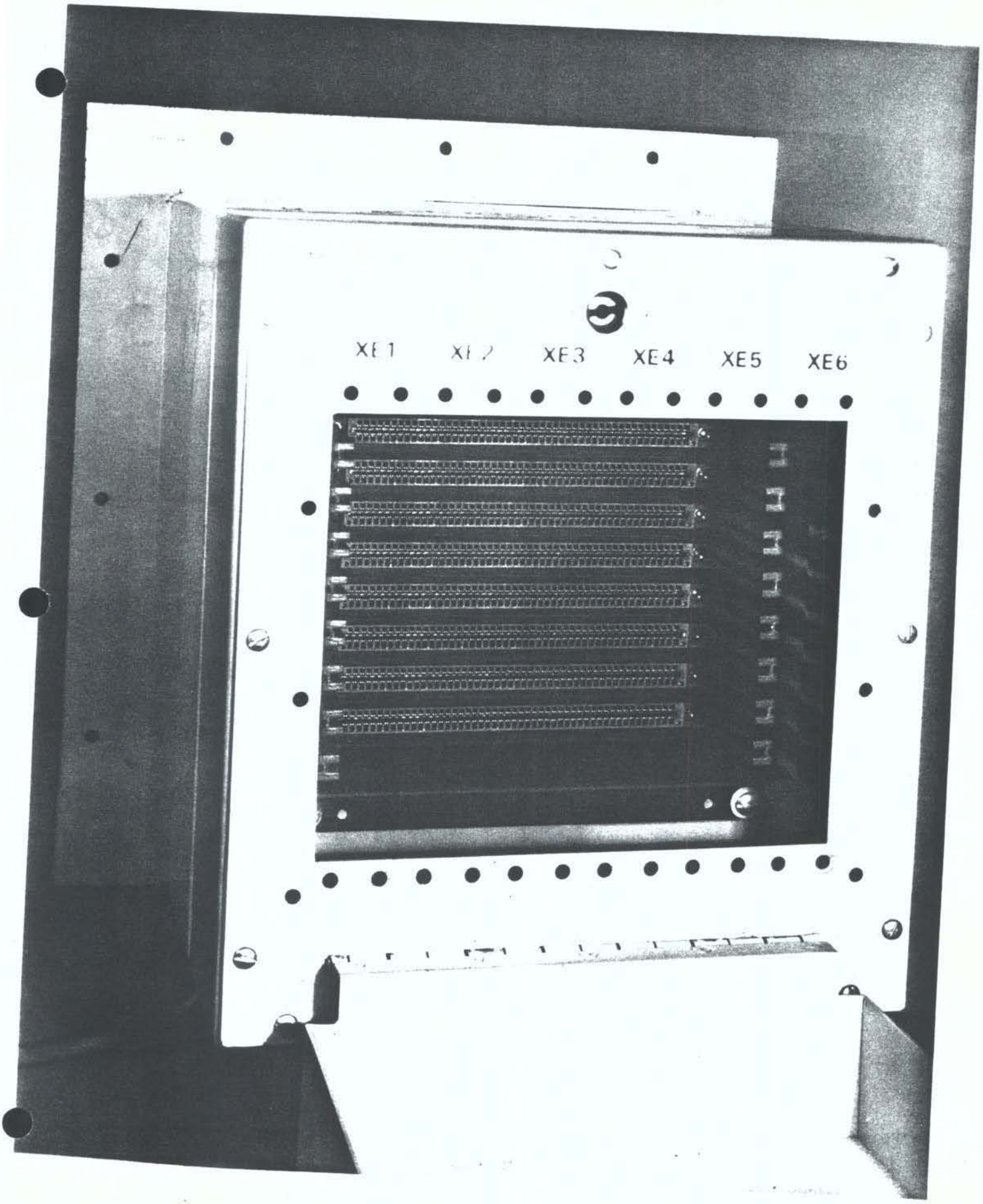
Open or Potted — Flexible Leads

- All models have 120/240 V, 50/60 Hz primaries.
- Split winding secondaries for single or dual output power supplies.
- Open or potted models have 8" long flexible leads.
- Regulation from 4.3 to 25%.
- Hipot test between primary & secondary is 2500 volts RMS.
- Max. ambient temp. is 55°C for full power rating.
- Available in open (180 Series) or potted (181 Series) models.
- Centre hole clearance for #8 hardware.
- Open units supplied with 2 insulating washers and 1 metal centering washer.

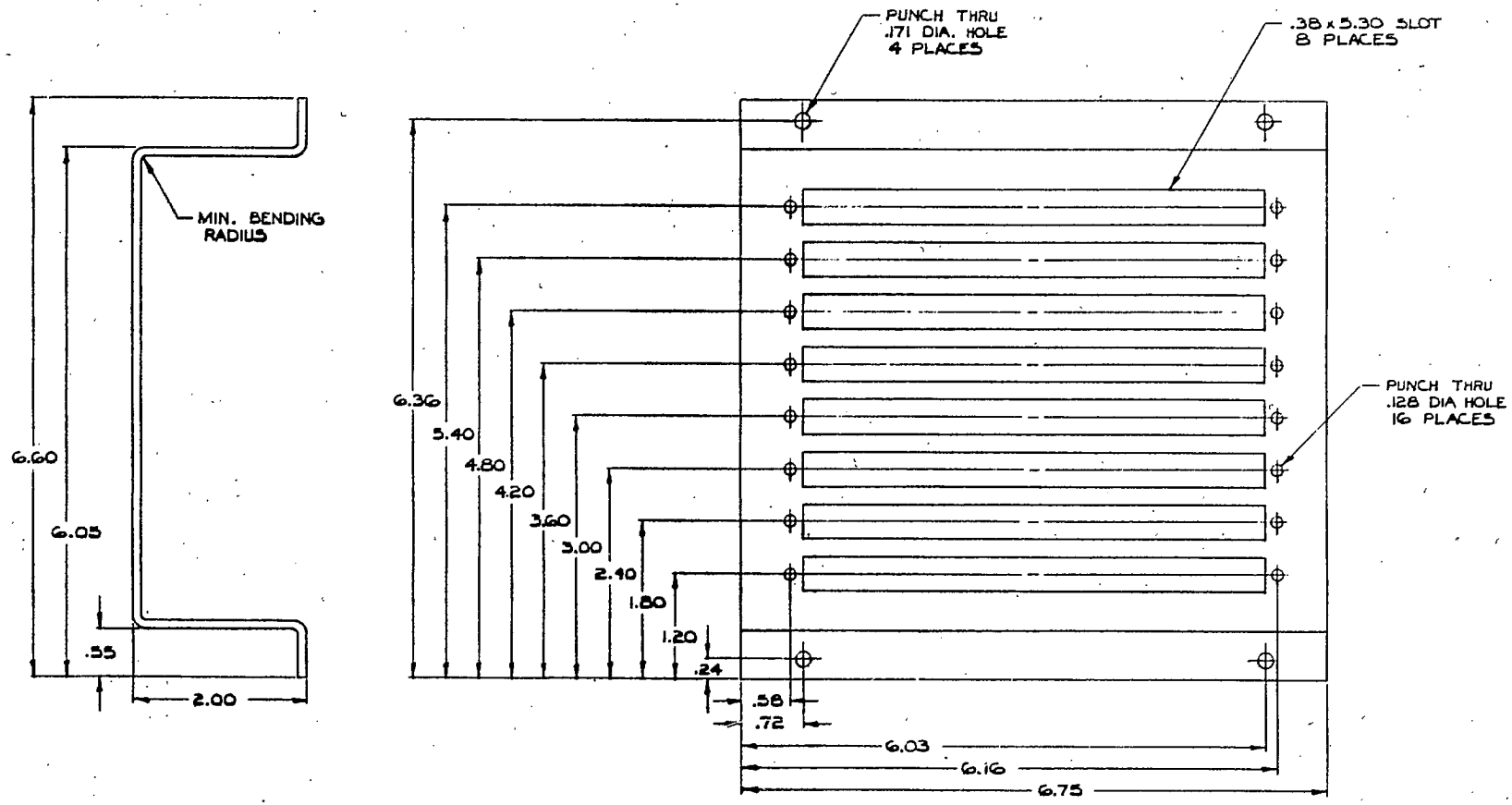
PRIMARIES 120/240 VOLTS, 50/60 Hz

Secondary Volts		Secondary Amps		Total	Cat. No.	Dimensions		Cat. No.	Dimensions	
Series	Parallel	Series	Parallel	VA	Open	Outside Dia.	Height	Potted	Outside Dia.	Height
12.6	6.3	1.19	2.38	15	180 K12	2.38	1.38	181 K12	2.5	1.5
16	8	.94	1.88	15	180 J16	2.38	1.38	181 J16	2.5	1.5
20	10	.75	1.50	15	180 H20	2.38	1.38	181 H20	2.5	1.5
30	15	.50	1.0	15	180 G30	2.38	1.38	181 G30	2.5	1.5
12.6	6.3	2.38	4.76	30	180 L12	2.75	1.63	181 L12	3.00	1.75
16	8	1.88	3.76	30	180 L16	2.75	1.63	181 L16	3.00	1.75
20	10	1.5	3.0	30	180 K20	2.75	1.63	181 K20	3.00	1.75
24	12	1.25	2.5	30	180 K24	2.75	1.63	181 K24	3.00	1.75
30	15	1.0	2.0	30	180 J30	2.75	1.63	181 J30	3.00	1.75
40	20	.75	1.5	30	180 H40	2.75	1.63	181 H40	3.00	1.75
16	8	3.13	6.26	50	180 M16	3.13	1.63	181 M16	3.38	1.75
20	10	2.5	5.0	50	180 M20	3.13	1.63	181 M20	3.38	1.75
24	12	2.1	4.2	50	180 L24	3.13	1.63	181 L24	3.38	1.75
30	15	1.67	3.34	50	180 K30	3.13	1.63	181 K30	3.38	1.75
40	20	1.25	2.5	50	180 K40	3.13	1.63	181 K40	3.38	1.75
50	25	1.0	2.0	50	180 J50	3.13	1.63	181 J50	3.38	1.75
20	10	4.5	9.0	90	180 N20	3.50	1.88	181 N20	3.63	2.0
24	12	3.75	7.5	90	180 N24	3.50	1.88	181 N24	3.63	2.0
30	15	3.0	6.0	90	180 M30	3.50	1.88	181 M30	3.63	2.0
40	20	2.25	4.5	90	180 L40	3.50	1.88	181 L40	3.63	2.0
50	25	1.80	3.6	90	180 K50	3.50	1.88	181 K50	3.63	2.0
70	35	1.29	2.58	90	180 J70	3.50	1.88	181 J70	3.63	2.0
240	120	.38	.76	90	180 F240	3.50	1.88	181 F240	3.63	2.0




XE1
XE2
XE3
XE4
XE5
XE6

REV	DATE	REVISIONS / DESCRIPTIONS



ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

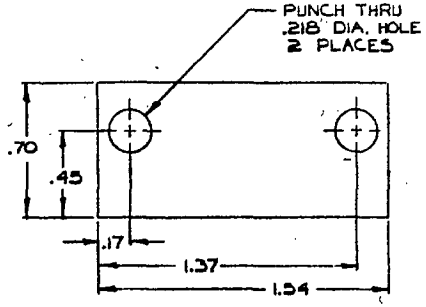
DATE: 82-02-05 | PROJ. NO: B10113 | DRAWN BY: J. WHITEMAN

CONNECTOR MOUNTING BRACKET - MECHANICAL

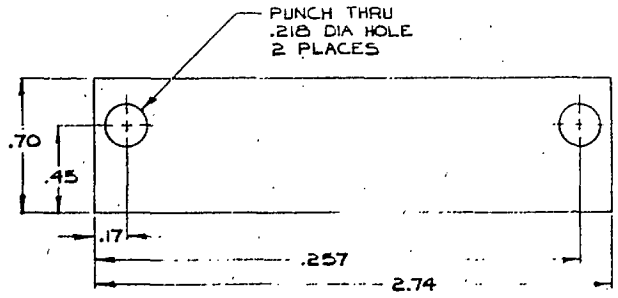
MATERIAL: ALUMINUM, .09 THK | SCALE: 1/1 | SHEET OF

FINISH: BLACK ANODIZE | APPROVAL: R Yu 1/10/83 | DWG NO: * 2020

REVISIONS		
REV	DATE	DESCRIPTIONS



GROUND BUSS I
*2334-A



GROUND BUSS II
*2334-B

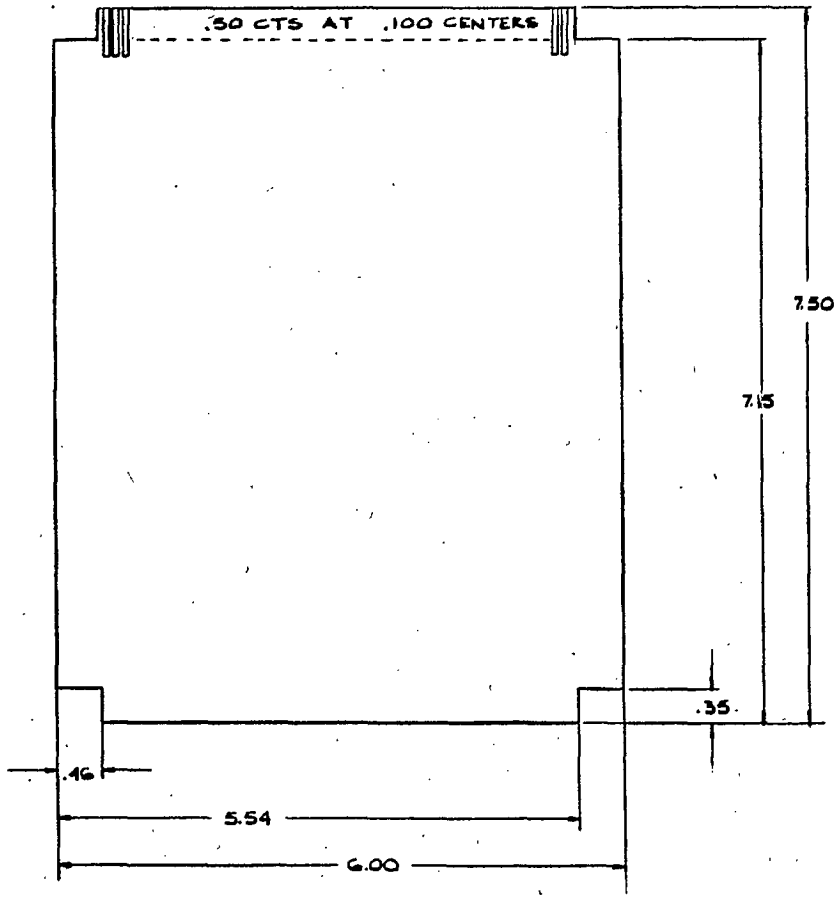
-133-

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS: TOLERANCES: .XX ±.010, .XXX ±.005, ANGLES ±1/2°	FOUNDATION INSTRUMENTS OTTAWA		
SURFACES:	DATE: 82-06-15	PROJ. NO: 810113	DRAWN BY: J. WHITEMAN
REMOVE BURRS & SHARP EDGES	GROUND BUSS I & II - MECHANICAL		
MATERIAL: COPPER, .033 THK	SCALE: 2/1		SHEET OF
FINISH: SMOOTH	APPROVAL: 17/02/93		DWG NO: *2334

REVISIONS		
REV	DATE	DESCRIPTIONS
A	82-05-03	3 INCHES ADDED TO EXTENDER PCB W.O. # 2143

GOLD CTS BOTH SIDES THIS END ONLY



NOTE.
USE SAME ARTWORK TO PRODUCE A TWO SIDED PCB

-134-

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS:
TOLERANCES: .XX ±.010
.XXX ±.005
ANGLES ±1/2°
SURFACES:
REMOVE BURRS & SHARP EDGES

FOUNDATION INSTRUMENTS OTTAWA

DATE: 82-04-23 | PROJ. NO: 810113 | DRAWN BY: P. D.

EXTENDER PCB MASTER

MATERIAL: 410, G62 THK. GLASS EPOXY 1OZ COPPER EACH SIDE | SCALE: 1/1 | SHEET OF

FINISH: TIN PLATE .0002/.0003 THK CTS:- GOLD .0001/.0002 THK | APPROVAL: R. Yip 17/02/83 | DWG NO: 2024

4.0 OPERATING PROCEDURE

This section details the set-up required for the correct operation of the Land Tactical System.

4.1 LAND TACTICAL SYSTEM OPERATING PROCEDURE OVERVIEW

INTRODUCTION:

The following describes the hardware, test equipment, input signals and procedures required to make full use of the Land Tactical communication system's video, audio and data transmission capabilities.

HARDWARE REQUIRED:

2 - Land Tactical modified signal input panels.
1 - 1000m or 500m connectorized fibre optic link.
2 - Multiplexer boards (FI-2206A)
2 - Data and Video Transmitter boards (FI-2202B)
2 - Data and Video Seperator boards (FI-2210B)
2 - PSK Data Recovery boards (FI-2218B)
2 - Descrambler and F-Bit Recovery boards (FI-2214A)
2 - Data Demultiplexer boards (FI-2222B)
4 - Duplex Voice Transmission Codec boards (FI-2386A)

TEST EQUIPMENT REQUIRED:

Video Signal Source - Video camera or test pattern generator.

Video Monitoring Equipment - Video Monitor or video test equipment.

Audio Signal Source - Microphone and microphone amplifier or audio signal generator.

Audio Monitoring Equipment - Audio amplifier and audio headset or audio test equipment.

Data Signal Source - MIL-STD-188C data pattern generator or TTL data pattern generator with TTL to MIL-STD-188C data level converter.(e.g. data interface cable constructed for factory testing.)

Data Monitoring Equipment - MIL-STD-188C data error detector or TTL data error detector with TTL to MIL-STD-188C data level converter (e.g. data interface cable constructed for factory testing.)

SUGGESTED EQUIPMENT:

VIDEO - Any video camera with BNC output, video monitor or video test equipment as sophisticated as desired.

AUDIO - See check out procedure for Duplex Voice Transmission Codec (FI-2386A)

DATA - Pattern Generator/Error Detector (HP-3780A)

GENERAL SYSTEM SET-UP:

- Remove line power from both signal input panel boxes.
- Insert Land Tactical circuit boards that have been set-up and tested according to provided procedures into the appropriate slots of the connector mounting bracket (DWG. C2020). (For details see backplane wiring diagram (DWG. D2447) or the board placement diagram inside the extender flange (DWG. D2022).
- Attach selected fibre optic link to both signal input panels.
- Apply line power to both signal input panel boxes.

A bi-directional link should now exist between the SIGNAL INPUT boxes. The following procedures describe how to establish video, audio and data communications over the link.

VIDEO LINK SET-UP:

- A 1.0 vp-p (140 i.r.e. units) differential or single-ended video signal is applied to connector J11 of the transmit end signal input panel via a BNC terminated cable.
- The transmission level adjustments as well as the 60Hz hum suppression adjustments are done internally and are discussed in the Data and Video Transmitter board (FI-2202B) check out procedure.
- A single-ended video output signal of approximately 1.0 Vp-p should then appear at connector J12 (BNC) of the receive end signal input panel when terminated by a 75 ohm load (video

monitor or video test equipment) via a 75 ohm BNC coax cable.

- The output level adjustment is done internally and is discussed in the Data and Video Separator board (FI-2210B) check out procedure.

Note: Slight output level adjustments may be required after initial set-up if the fibre optic link is replaced by another.

AUDIO LINK SET-UP:

- A -4 dBm differential audio input signal (e.g. 1.4 Vp-p sinewave from a 600 ohm audio signal source is applied at the 2 pins on the Malco connector, J10, of the transmit end signal input panel corresponding to the desired channel (see wire list #A2423, sheet #3 for the external (TX) codec connector pinout designation). Interfacing to the signal input panel connector J10 may be done using a multi-wire twisted pair cable coming from a patch panel and terminated with the mating Malco connector or using a Codec Interface cable provided for the factory acceptance test.
- The appropriate selector switches (S1-S6) on the Data Multiplexer board (FI-2206A) and the Data Demultiplexer board (FI-2222B) must be toggled such that the channel selected is dedicated to Codec data. (See Data Multiplexer schematic (DWG. D2205), Data Demultiplexer schematic (DWG. D2222) and markings on the circuit boards for details on the switch positions.)
- A differential audio output signal of approximately -7 dBm (into a 600 ohm load) should be present at the 2 pins on the Malco connector J10, of the receive end signal input panel corresponding to the desired channel (See wire list #A2423, Sheet #5 for the external (RX) Codec connector pinout designation). Interfacing to the input signal panel connector J10 may be done as described above.

Note: For the 2-wire channels (6 and 12), the pins designated on wire list #A2423, Sheet #3 are used for simultaneous transmission and reception of the audio signal via 2-wire devices like telephones and teletypes.

DATA LINK SET-UP:

- A MIL-STD-188C data signal (±6Vdc) is applied to the pin on the Malco connector, J9, of the transmit end signal input panel corresponding to the desired channel (See wire list #A2423, Sheet #2 for the external (TX) data connector pinout designation). Interfacing to the signal input panel connector J9 may be done using a multi-wire cable coming from a patch panel and terminated with the mating Malco connector or using a Data Interface Cable provided for the factory acceptance test.
- The appropriate selector switches (S1-S6) on the Data Multiplexer board (FI-2206A) and the Data Demultiplexer board (FI-2222B) must be toggled such that the channel selected is dedicated to data. (See Data Multiplexer schematic (DWG. D2205), Data Demultiplexer schematic (DWG. D2222) and markings on the circuit boards for details on the switch positions.)
- A MIL-STD-188C data signal should be present at the pin on the Malco connector, J9, of the receive end signal input panel corresponding to the desired channel (See wire list #A2423, sheet for the external (RX) data connector pinout designation). Interfacing to the signal input panel connector J9 may be done as described above.

NOTE: For MIL-STD-188C signals, a data "HIGH" state corresponds to a signal "LOW" (e.g. approximately -6Vdc.) and a data "LOW" state corresponds to a signal "HIGH" (e.g. approximately +6Vdc.)

4.2 CHECK OUT PROCEDURE

Module: Duplex Voice Transmission Codec (FI-2386A)
Schematic D2385 Sheets 1-6
Component Overlay D2387

Associated Modules:

a) 4-wire Audio Interface (FI-2431A)
Component Overlay No. 2432
Master No. 2433

b) 2-wire Audio Interface (FI-2435)
Component Overlay No. 2436
Master No. 2437

Hardware Required:

One Land Tactical Backplane Housing (Signal Input Panel)
PSK Data and Video Tx (FI-2202B)
Data Multiplexer (FI-2206A)
Descrambler and F-Bit Recovery Board (FI-2214A)
Data Demultiplexer (FI-2222B)
Two Alligator Clip Leads
One Codec Interface Cable

Test Equipment Required:

One Microphone Mixer (FI-1500)
One Dynamic Microphone
One Audio Headset
Associated Audio Connector Cables
General Purpose Oscilloscope - 2 channels
Audio Generator

Audio Frequency Distortion Analyser (eg. HP-331A)
Noise Measuring Test Set (eg. Wilcom TI32)
Extender Card (FI-2023A)

Connections:

1. In the backplane housing, insert the Data Multiplexer (FI-2206A) into J2, the PSK Data and Video Tx (FI-2202B) into J3, the Descrambler and F-Bit Recovery board (FI-2214A) into J6, the Data Demultiplexer (FI-2222B) into J7 and the Duplex Voice Transmission Codec (FI-2386A) into J8.

2. Jumper the following test points accordingly;
   a) TP47 of FI-2206A to TP2 of FI-2214A
   b) TP12 of FI-2206A to TP3 of FI-2214A

3. Toggle the switches on the Data Multiplexer (FI-2206A) and the Data Demultiplexer (FI-2222B) to the CODEC position.

4. Connect the Codec Interface Cable to J10.

Procedure:

1. Apply power and check for:
   a) +5 volts at the following locations;

IC Number	Pin Number
168	14
169	1
170	14

   b) GND (OV) at the following locations;

IC Number	Pin Number
168	7

IC Number	Pin Number
169	8
170	7
1	8
31	8
61	8
101	8
131	8
161	8

c) +12 volts at the following locations:

IC Number	Pin Number
1	16
2	24 and 12
3	16
31	16
32	24 and 12
33	16
61	16
62	24 and 12
63	16
101	16
102	24 and 12
103	16
131	16
132	24 and 12
133	16
161	16
162	24 and 12
163	16

1 of Vertically / 4
Mounted Modules (FI-2431A and FI-2435)

d) -12 volts at the following locations:

IC Number	Pin Number
2	19
32	19
62	19
102	19
132	19
162	19
1 of Vertically Mounted Module s (FI-2431A and FI-2435)	11

2. Check for the Codec Tx Clock and Codec output data at:

IC Number	Clock Pin Number	Data Pin Number
1	14	9
31	14	9
61	14	9
101	14	9
131	14	9
161	14	9

3. Check for the Codec Rx Clock and ensure that its falling edge coincides with approximately the middle of an incoming data bit.

IC Number	Clock Pin Number	Data Pin Number
3	14	13
33	14	13
63	14	13
103	14	13
133	14	13
163	14	13

The following describes the audio tests required of the 4-wire channels 1 through 5:

4. Idle Channel Noise:
   Connect the Noise Measuring Set to the output of an audio channel with its input terminated into 600 ohms. Make sure, as with all these tests that the test set input is terminated into 600 ohms. Idle channel noise should not exceed -60 dBm.

5. Cross Channel Isolation:
   Apply to an audio input channel a 1 Khz. sinewave at 0 dBm. A 0 dBm signal is somewhat larger than the expected voice input magnitude of -4 dBm, (1.4 volts p-p).

   With the Noise Measuring Set, measure the output of an adjacent channel with its input terminated into 600 ohms. Crosstalk should not be distinguishable from idle channel noise and thus cross channel isolation should be better than -60 dB.

6. Insertion Loss and Frequency Response:
   Apply a 0 dBm, 1 Khz signal into a channel and ensure the output attenuation does not exceed 3 dB when terminated into 600 ohms.

   Then sweep the audio generator to check the channel frequency response. Make sure the audio generator produces a constant output signal level over this frequency range.

   The lower 3 dB cutoff frequency should not exceed 80 Hz. and the upper should not be less than 2.9 Khz when measured with respect to the attenuation seen at 1 Khz. As well, no frequency between 500 and 2500 Hz. should vary more than approximately 2 dB in magnitude from that at 1 Khz.

7. Harmonic Distortion:

Due to the nonlinearities created by the quantizing of the analogue signal, some harmonics will be generated by the codec operation. These will become more significant as the input level is decreased and the audio frequency increased.

The harmonic distortion can be measured by inserting a test tone on a channel and then "nulling" it out at the receive end with a distortion analyser and then measuring the sum total of all harmonics that remain. Typical worst case measurements are listed below. It is important to realize that these figures do not represent channel noise in the normal sense. In fact, voice is still very intelligible with the seemingly large value of harmonics measured on the line.

Input Signal Level (dBm)	Output Signal/Harmonic Distortion (dB)		
	500 Hz	1000 Hz	2500 Hz
0	28	24	21
-4	27	22	17
-10	15	22	17
-20	22	16	12

8. Audio Check:

Connect the microphone to the mixer and then the mixer to the channel input, with the headset connected to the channel output. Voice should be easily intelligible and the speaker identifiable. Some harmonic distortion will be evident in background crackle and "roughness" on the voice inflections.

The 2-wire codec channel, channel 6, was installed as an experimental set-up and has yet to be proved practical. Lack of equipment has

prevented a full system test on these 2-wire channels with a 2-wire device such as the household telephone. However, a preliminary set-up and test procedure has been devised.

Steps 4 and 5 of the 4-wire test follow exactly.

Set-Up:

The 2-wire hybrid requires some adjustment to improve cross channel isolation. This isolation is important in preventing both feedback of voice transmission to the sender as well as the positive feedback oscillations that may occur.

To facillitate this adjustment, jumper J1 must be removed. A 1 Khz, 0 dBm. signal should be inserted on the J1 pin connected to C166 and the other J1 pin monitored with an oscilloscope.

Ideally there should be no signal seen on the oscilloscope. If there is, RV1 and RV2 need to be adjusted alternately until the 1 Khz signal is nulled out. Reconnect J1 once this adjustment has been made.

4.3 CHECK OUT PROCEDURE

Module: Data Multiplexer (FI-2206A)
Schematic No. D2205
Component Overlay No. D2207

Test Equipment Required:

Land Tactical Backplane Housing (Signal Input Panel)
Extender Card (FI-2023A)
PSK Data and Video Tx (FI-2202B)
General Purpose Oscilloscope
Dolch Lam 4850 Logic Analyzer
Data Interface Cable (FI)

Procedure:

1. Insert the PSK Data and Video Tx into J3 of the backplane, so as to supply the Mux clock.

2. Insert the Data Multiplexer card into J2 of the backplane.

3. Apply power and ensure the correct power levels appear at TP15, 17 and 19.

4. Check the Mux clock at pin 11 of IC16 for correct TTL levels, with the oscilloscope.

5. Ensure Mux clock or $\overline{\text{clock}}$ appears at:

IC Number	Pin Number
15	2
17	2
20	11
13	3
13	11
21	9
22	9
23	2

6. For the following ICs, check that the rising edge of the clock coincides approximately with the middle of an incoming data bit, using either measuring device.

IC Number	Clock Pin Number	Data Pin Number
20	11	9
13	3	6
13	11	9

The remaining tests require the use of the Logic Analyzer set on Timing Mode and sampling TTL levels at 50 ns intervals.

7. Check IC17 pin 14 for a signal alternately HIGH for 16 Mux clock cycles and LOW for 11 cycles.

8. Check IC18 pin 16 for the F-Bit signal being alternately HIGH and LOW for 27 Mux clock cycles.

9. Check the Codec Clock Out at IC26 pin 14 simultaneously with the F-Bit at IC18 pin 16. The Codec Clock should be ½ the frequency of the F-Bit.

10. Connect the Data Interface cable to J9. Leave all Interface channels floating so that all multiplexer inputs are low. This is

to allow easy observation of the F-Bit. Simultaneously compare the Mux clock at IC20 pin 11 with the Mux output at IC20 pin 9, the F-Bit at IC18 pin 16 as well as the Codec Clock Out at IC25 pin 5. These relationships should agree with that described in FIG. 1.

11. While observing the multiplexed stream on IC20 pin 9, tie each input data channel HIGH in turn to ascertain whether each channel occupies a unique position within the 27 bit multiplexer frame.

12. Observe the Scrambled Data Output on IC25 pin 3 simultaneously with the Mux clock on IC13 pin 11. Check to make sure no more than 10 HIGH or LOW data bits appear in a row in the scrambled data stream.

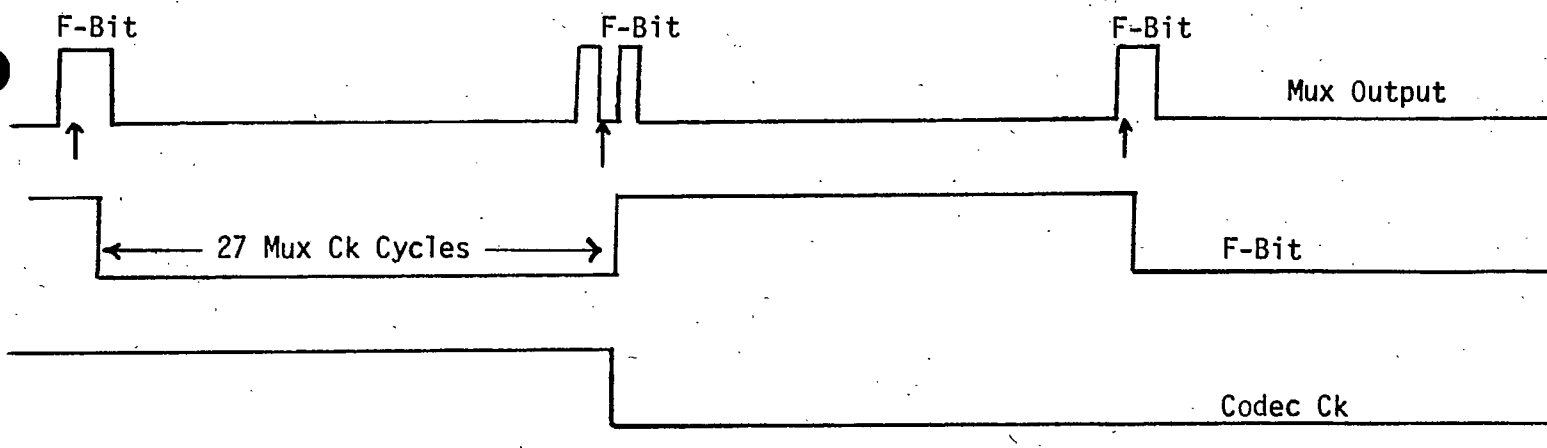


FIG. 1

Please Note: Be sure the multiplexer switches are toggled in the DATA position.

4.4 SET-UP AND CHECK OUT PROCEDURE

Module: Data and Video Transmitter Board (FI-2202B)
Schematic D2201
Component Overlay D2203

Introduction:

The following describes the adjustments that are required for proper operation of the circuitry as well as typical waveforms and signal levels that should give rise to rapid testing and trouble shooting of this board.

Hardware Required:

1 - Land Tactical Modified Signal Input Panel
1 - Data and Video Transmitter Board (FI-2202B)
1 - 1000m. or 500m. connectorized Fibre Optic Link
1 - Extender Card (FI-2023A)
2 - 5 Ft. long 75 ohm coax cables with a BNC connector at one end and alligator clip leads at the other.
1 - 75 ohm coax BNC cable.

Suggested Test Equipment:

Pattern Generator/Error Detector (HP-3780A)
Video Pattern Generator (Leader LCG-397)
Frequency Counter
General Purpose Oscilloscope (60 Mhz)
Digital Multimeter
Audio Signal Generator

PROCEDURE:

A) General

1. Remove power from Signal Input Panel.
2. Disconnect fibre optic link from Signal Input Panel.
3. Insert Data and Video Transmitter board (FI-2202B) into connector J3 of the Signal Input Panel card rack. (See Rack Backplane Wiring Diagram (DWG#D2447) for details).
4. Apply power and check that the proper power levels appear at TP14 (+12V), TP11 (-12V), TP12 (+5V) and TP8 (-5V).

B) Digital Section

1. Check +5V and ground pins on all I.C.'s.
2. Check operation of 12 Mhz oscillator at TP26.

   Expected Characteristics:
   - 3.2 Vp-p square wave
   - f osc = 12,000,000 $\pm$ 30 Hz.

Note: The frequency of oscillation may be trimmed by adding small capacitor values in parallel with C67 and C73.

3. At TP44, expected characteristics:
   - 2.7 Vp-p skewed triangular wave
   - f = f osc./3 = 4,000,000 $\pm$ 10 Hz

Note: The multiplexer clock duty cycle may be adjusted by changing R51.

5. Use BNC coax cable with alligator clip leads to take the multiplexer clock from TP39 to the 75 ohm clock input of the Bit Pattern Generator (HP-3780A). Run Bit Pattern Generator on external clock NRZ data, binary code. Use another BNC coax cable with alligator clip leads to apply the data pattern from the Bit Pattern Generator to the data input of the board at TP10.

6. Set bit pattern generator to 1010 pattern and check data at TP10.

   Expected Characteristics:
   - 2,000,000 $\pm$ 5 Hz TTL Level Squarewave (e.g. 4,000,000 $\pm$ 10 bits/sec 1010 data).

7. Check data signal level at input to the double balanced mixer, TP21.

   Expected Characteristics:
   - 0.40 Vp-p squarewave (1010 pattern)

C) PSK Data Generation Section

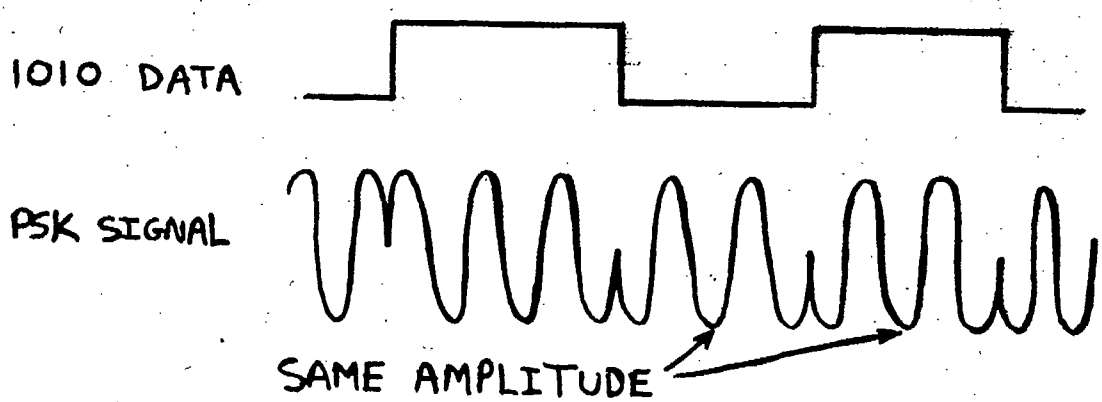
1. Remove 1010 pattern data siganl from data input at TP10.
2. Check PSK carrier level at TP20.

   Expected Characteristics:
   - Approximately 0.90 Vp-p, 12.00 Mhz sinewave.
3. Adjust RV1 to give 0.60 Vp-p sinewave at TP22.

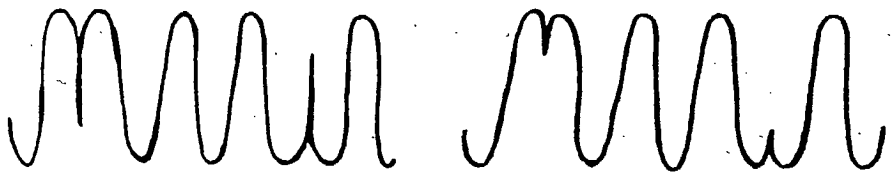
Note: It may be distorted due to a misadjustment of RV2.

4. Set bit pattern generator to 1010 pattern and apply signal to data input at TP10.
5. Look at the waveform at TP25 and adjust RV2 until a proper PSK signal is obtained for a 4 Mbits/sec 1010 pattern data input.

Note: Look for equal amplitudes on both sides of phase reversals.



The phase transitions may not be exactly symmetrical in height as shown above but rather as follows:



OR

6. Readjust the voltage at TP22 using RV1 until it is 0.60 Vp-p in amplitude.
7. Recheck amplitude of PSK signal at TP25. It should still be 0.40 Vp-p and have a good PSK waveform.

   Continue testing using only 12.0000 Mhz sinewave data carrier (0000 pattern on bit pattern generator) unless otherwise specified.

8. Check that the amplitude of the PSK data carrier hasn't changed at TP25.
9. Set fibre optic transmitter (FOTX) bias by adjusting RV7 until the voltage read with the digital multimeter at TP38 is 3.80 V d.c
10. Remove power from Signal Input Panel and connect Fibre Optic Link to Signal Input Panel. Power up Signal Input Panel.
11. Set the transmitted data carrier level by adjusting RV4 until a 0.080 Vp-p sinewave is present at TP38.

Note: Higher frequency components may be present at this point due to pick up from the TTL oscillator used to generate the data carrier. These are filtered out in the data and video separator circuitry and are no cause for concern.

D) Video Section

1. Apply a 1.0 Vp-p (140 I.R.E. units) differential or single-ended video signal to connector J11 of the Signal Input Panel via a BNC terminated cable.
2. Set the transmitted video level by looking at TP38 and adjusting RV3 until the combined video and data carrier signal level is 0.50 Vp-p.
3. If 60 Hz is present, its effect may be reduced by adjusting RV6 at the video input to null it out.

4.5 SET-UP AND CHECK OUT PROCEDURE

Module: PSK Data Recovery (FI-2218B)
Schematic D2217
Component Overlay D2219

Introduction:

The following describes the adjustments that are required for proper operation of the circuitry as well as typical signal levels that should give rise to rapid testing and troubleshooting of this board.

Hardware Required:

2 - Land Tactical Modified Signal Input Panels
1 - Data and Video Transmitter Board (FI-2202B)
1 - Data and Video Separator Board (FI-2210B)
1 - PSK Data Recovery Board (FI-2218B)
1 - 1000 m. or 500 m. connectorized Fibre Optic Link
4 - 5 ft. long 75 ohm coax cables with a BNC connector at one end and alligator clip leads at the other.

Suggested Test Equipment:

Pattern Generator/Error Detector (HP-3780A)
General Purpose Oscilloscope (60 Mhz)
Frequency Counter
Digital Multimeter

PROCEDURE:

A) General

1. Remove power from both signal input panels.
2. Designate one signal input panel as the transmit end and the other as the receive end.
3. Connect a fibre optic link to both transmit and receive signal input panels.

4. Insert a fully tested Data and Video Transmitter board (FI-2202B) into connector J3 of the transmit end signal input panel card rack. (See rack backplane wiring diagram (DWG#2447) for details.)
5. Insert a fully tested Data and Video Separator board (FI-2210B) into connector J4 of the receive signal input panel card rack.
6. Insert the PSK Data Recovery board (FI-2218B) into connector J5 of the receive signal input panel card rack.
7. Apply power to both signal input panels and check that proper power levels appear at TP7 (+12V), TP8 (-12V) and TP9 (+5V) of the PSK Data Recovery board.)

B) Off-Line Board Set-Up

1. With only the Data and Video Transmitter board (FI-2202B) in the transmit signal input panel, the PSK data carrier should be present at the input of the PSK Data Recovery board (i.e. TP1). With a properly adjusted Data and Video Separator board, the signal at TP1 should be 0.85 Vp-p, 12.0000 Mhz sinewave.
2. Given such an input signal, the following waveforms should be observed:
   - TP12: 0.70 Vp-p slightly distorted sinewave
   - TP10: 0.30 Vp-p clipped sinewave
   - TP11: 0.55 Vp-p slightly distorted sinewave
3. The carrier recovery circuit is initially set-up by adjusting CV2 and CV3 for a maximum in the squewed 24.0000 Mhz sinewave at TP28. The expected signal level should be about 2.8 Vp-p or greater.

   A 24.0000 Mhz distorted sinewave with clipped peaks of about 4.4 Vp-p should be present at TP25. At TP28, there should be a 24.0000 Mhz TTL level squarewave with slightly rounded edges.

   The 12.0000 Mhz recovered carrier should be present at the output (TP30) of the frequency divider flip-flop (IC2).

With CV2 and CV3 properly adjusted, the frequency of the recovered carrier at TP30 of the PSK Data Recovery board in the receive signal input panel should be identical to that measured at TP31 of the Data and Video Transmitter board in the transmit signal input panel when no data is being sent. Also there should be virtually no jitter (less than 2nsec.) in the recovered carrier at TP30.

The final fine tuning adjustment of the carrier recovery circuit must now be done with pseudo-random (PRBS) data going through the system.

4. To inject data into the system, extract the 4.0000 Mhz data clock from TP39 of the Data and Video Transmitter board (FI-2202B) via a 75 ohm BNC coax cable with alligator clip leads at one end and apply it to the clock input of the bit pattern generator. Take the data signal from the data output of the bit pattern generator and apply it to the data input of the Data and Video Transmitter board at TP10 via another 75 ohm BNC coax cable with alligator clip leads at one end.

Set the bit pattern generator frequency control to "external". Set the output format to "NRZ" (non return to zero data) and the data pattern to "normal".

Various data patterns are now available. No data consists of pattern 0000, words correspond to patterns 1000, 1010 or 1100 and pseudo-random data (PRBS) is available with n=9, 15 or 20 giving pseudo-random patterns of bit length equal to the nth exponent of 2, (2^n), before the pattern repeats itself.

Set the pattern generator to a 1010 word and check that the appropriate 4 Mbits/sec 1010 bit pattern is present at TP10, the data input to the Data and Video Transmitter board. Measure the frequency of the square wave at TP10. It should be 2.0000 Mhz.

5. Check the input signal to the PSK Data Recovery board at TP1 to verify that a good PSK signal is present with the data transitions obvious but rounded off due to the bandlimiting involved in the transmission and recovery processes.
6. The PSK carrier recovery circuit can now be fine tuned. It is very important to realize that this adjustment is the most critical one on this board and care must be taken to ensure that it is done properly. If not, intermittent errors in the Data Recovery process may occur.

   Set the bit pattern generator to PRBS n=15 data.

   Look at the recovered PSK carrier at TP30 with the oscilloscope and fine tune CV2 and CV3 in order to minimize the jitter on the leading edge of 12.0000 Mhz signal. The edge jitter of the PSK carrier at any point on the oscilloscope screen compared to the starting point of the sweep should not exceed 4 nsec.(Typically 3 nsec.)

   Check the jitter for different bit patterns to confirm that it meets the specifications.

   Measure the frequency of the PSK carrier at TP30 and check that it doesn't change when the bit pattern is changed or when no data is applied (0000 pattern).

7. Set RV2 to give a 0.7Vp-p PSK carrier signal level at TP14.

8. Set the bit pattern generator to 1010 word and for a proper setting of RV2, a sinewave of approximately 2.4 Vp-p should be present at TP26.
9. Set the bit pattern generator to PRBS n=15 and adjust RV1 until an approximate duty cycle of 50% is observed in the unconditioned recovered data at TP33.

10. Tune the unconditioned clock extraction circuit by adjusting CV1 for minimum jitter on the leading edge of the unconditioned clock at TP46 with the oscilloscope externally triggered by the clock output of the bit pattern generator. In this way, the unconditioned clock which is recovered from the data can be directily compared to the clock that generated the data.
11. The frequency of the unconditioned clock at TP46 should be 4.0000 Mhz while the duty cycle should be 50%.
12. Adjust the clock recovery pahse-locked loop by using the oscilloscope in the "alternate" mode with the trigger set to "internal" and "channel 1". Look at the recovered clock at TP43 on channel 1 and the unconditioned extracted clock at TP46 on channel 2.

    Adjust CV4 until there is no relative motion between the traces of channel 1 and channel 2. When this occurs, the phase-locked loop is locked to the fundamental frequency component of the unconditioned extracted clock. The lock range is quite wide so CV4 can be adjusted clockwise until lock is lost and then adjusted in the counterclockwise direction until lock is lost again. In this way, the extent of the lock range is determined and CV4 should be adjusted to be in the center of it. Having done this, the voltage controlled oscillator free running frequency will lie in the middle of the lock range.

    Change bit patterns on the bit pattern generator and check that the phase-locked loop lock is maintained. Apply 0000 and then PRBS n=15 data and check lock.

13. Adjust the phase shift of the recovered clock at TP45 so that its rising edge is in the middle of the unconditioned data bits at TP33 for a 1010 data word by changing the setting of CV5.
14. Set the bit pattern generator to PRBS n=15 and repeat the set-up of step 10 to ensure that the clock phase adjustment hasn't affected the clock recovery process.
15. Check for TTL level clock output at TP35. Check for TTL level data data output at TP36.

16. Use two 75 ohm BNC coax cables with alligator clip leads to take the recovered clock from TP35 to the clock input in the receiver section of the bit pattern generator/error detector as well as the recovered data from TP36 to the data input.

Note: The 75 ohm impedances will load down the outputs from TTL levels to about 1.5 Vp-p which is good enough for the bit pattern generator/error detector.

Set the error detector input format to "Binary", the measurement to "Binary", the data threshold to "200 mv" or 600 mv", the clock threshold to "Auto" and the clock to "EXT" or "$\overline{\text{EXT}}$" depending on the clock output format setting of the pattern generator.

Perform bit error rate (BER) tests for various bit patterns including words and PRBS n=15.

Note: At a 4 Mbits/sec. data rate, BER = 1×10^{-8} error/sec. corresponds to a 25 second accumulation of data and BER = 1×10^{-9} error/sec. corresponds to a 4 min. 10 sec. accumulation of data.

C) On-Line Board Check Out

When the system is complete and running, the multiplexer output data is scrambled and is just as good as PRBS data for the purpose of this test.

Perform the checks described in steps 6 to 15 inclusive of the previous section, disregarding any bit pattern generator considerations since the data is scrambled.

4.6 SET-UP AND CHECK OUT PROCEDURE

Module: Data and Video Separator board (FI-2210B)
Schematic D2209
Component Overlay D2211

Introduction:

The following describes the adjustments that are required for proper operation of the circuitry as well as typical levels that should give rise to rapid testing and troubleshooting of this board.

Hardware Required:

2 - Land Tactical Modified Signal Input Panels
1 - Data and Video Transmitter Board (FI-2202B)
1 - Data and Video Separator Board (FI-2210B)
1 - PSK Data Recovery Board (FI-2218B)
1 - Data Multiplexer Board (FI-2206A)
1 - Extender card (FI-2023A)
1 - 1000m. or 500m. Connectorized Fibre Optic Link
2 - 4 Ft. long 75 ohm Coax Cables with BNC Connectors at both ends.
1 - 75 ohm BNC Termination.

Suggested Test Equipment:

Video Pattern Generator (Leader LCG-397)
Video Monitor
General Purpose Oscilloscope (60 Mhz)
Digital Multimeter

Note: For a detailed video signal analysis, the following are required:
- NTSC Test Signal Generator (Tektronix 149A)

- NTSC Vectorscope (Tektronix 520A)
- Waveform Monitor (Tektronix 1480R)

PROCEDURE:

1. Remove power from both signal input panels.
2. Designate one signal input panel as the transmit end and the other as the receive end.
3. Connect fibre optic link to both transmit and receive end signal input panels.
4. Insert a fully tested Data and Video Transmitter board (FI-2202B) into connector J3 of the transmit end signal input panel card rack (See rack backplane wiring diagram (DWG.#D2447) for details.)
5. Insert data and video separator board (FI-2210B) into connector J4 of the receive signal input panel card rack.
6. Apply power to both signal input panels and check that proper power levels appear at TP26 (+12V) and TP27(-12V) of Data and Video Separator board.
7. Apply 1.0 Vp-p video test signal to video input (J11) of transmit signal input panel (See System Operating Procedure, Video Link Set-Up, for more details).
8. Connect video output (J12) of receive signal input panel to a 75 Ohm input impedance video monitor via 75 Ohm BNC coax cable or to a 75 ohm BNC termination.
9. Look at TP1 of Data and Video Separator board with oscilloscope. A combined video and data carrier signal of between 100 mVp-p and 180mVp-p should be present with the video signal approximately five times greater than the data carrier sinewave peak-to-peak amplitude. If such a signal is present, a communication link has been established between the two signal input panels. If not, check the following:
   - Power in receive end signal input panel.
   - Power in transmit end signal input panel.
   - Fibre optic link connections to signal input panels.

- Signal at TP38 of Data and Video Transmitter board which should be a 500mVp-p combined video and data carrier signal.
- D.C. bias for Fibre Optic Transmitter (FOTX) at TP38 which should be 3.80V d.c.

If the problem is found to be in the output of the Data and Video Transmitter board, see the set-up and check out procedure for details as to proper operating conditions.

If the signal and bias conditions at the output of the Data and Video Transmitter board seem to be fine and yet no signal is present at the input to the Data and Video Separator board, replace or switch the ends of the fibre optic link around to determine if it has been damaged.

10. Look at the base of Q5 and set the AGC control pot (RV1) until a 1.4 Vp-p sinewave data carrier is present. If for the full range of RV1, the signal level is greater than 1.4 Vp-p then the AGC is in minimum gain mode which means that the level of the transmitted data carrier is too high and should be reduced until the proper level is obtained.

11. Set the RV2 until a 1.0Vp-p video signal appears at TP21, the video output, when terminated in a 75 ohm load.

12. Remove the power from the recieve signal input panel and insert the PSK data recovery board (FI-2218B) into connector J5 of the receive signal input panel card rack. Power up the signal input panel. Set RV3 until a 0.85 Vp-p sinewave data carrier output to the data recovery board is present at TP20.

13. Remove the power from the transmit signal input panel and insert the Data Multiplexer board (FI-2206A) into connector J2 of the

receive signal input panel card rack. Power-up the signal input panel. Scrambled data will now be going through the system and a bandlimited PSK signal should be present at TP20 and the base of Q5 on the Data and Video Separator board in the Receive Signal Input Panel. Check to see that the adjustments made in steps 10, 11 and 12 are still consistent.

Note: When a communication link in the opposite direction is established by inserting another fully tested Data and Video Transmitter board into connector J3 of the Receive Input Signal Panel Card rack, a slight interaction occurs. The received data carrier is amplitude modulated at a "beat" frequency equal to the difference in the two carrier frequencies.

4.7 CHECK OUT PROCEDURE

Module: Descrambler and F-Bit Recovery Board (FI-2214A)
Schematic No. D2213
Component Overlay D2215

Hardware Required (If a complete link available):

Two Land Tactical Backplane Housings (Signal Input Panels)
PSK Data and Video Tx (FI-2202B)
Data Multiplexer (FI-2206A)
Data and Video Separator (FI-2210B)
PSK Data Recovery Board (FI-2218B)
Two FOTx/Rx Modules with Fibre Optical Link

If a complete link is not available:

One Land Tactical Backplane Housing (Signal Input Panel)
PSK Data and Video Tx (FI-2202B)
Data Multiplexer (FI-2206A)
Two Alligator Clip Leads

Additional Equipment Required:

Extender Card (FI-2023A)
General Purpose Oscilloscope (~20 MHz)
Dolch Lam 4850 Logic Analyzer
Data Input Interface Cable (FI)

Connection Procedure:

If a complete link is available:

1. Designate one housing as Tx and the other as Rx.

2. In the Tx housing install the Data Multiplexer into J2, the PSK Data and Video Tx into J3 and the Data Input Interface cable to J9.

3. In the receive end of the link, install the Data and Video Separator into J4, the PSK Data Recovery board into J5 and the Descrambler and F-Bit Recovery Board into J6 of the Rx housing.

If a complete link is not available:

1. Install the PSK Data and Video Tx into J3 of the housing, the Data Multiplexer into J2, the Descrambler and F-Bit Recovery Board into J6 and the Data Input Interface cable to J9.

2. To supply clock and data to the Descrambler and F-Bit Recovery Board, jumper the following test points:

a. TP47 of FI-2206A to TP2 of FI-2214A

b. TP12 of FI-2206A to TP3 of FI-2214A

Procedure:

1. Apply power and ensure the correct power levels appear at TP9 and 6.

2. Ensure clock or $\overline{\text{clock}}$ appears at the following locations, (at the correct TTL levels) using an oscilloscope.

IC Number	Pin Number
1	5
2	9
4	9
7	2
8	3
8	11
13	9
23	2
24	2
17	3
17	11
21	2
22	2
19	3

3. Using either measuring device, ensure that the rising edge of the clock coincides approximately with the middle of an incoming data bit for the following ICs:

IC Number	Clock Pin Number	Data Pin Number
8	3	2
8	11	12
19	3	2
18	8	1

4. Check that IC17 pin 5 is HIGH.

5. Tie TP1 HIGH and allow all data channel inputs to float on the interface so that all multiplexer inputs are low. The signal on IC10 pin 5 should be identical to that seen in the multiplexer test. (Use the logic analyzer on Timing Mode at 50 ns. sampling). Simultaneously observe IC10 pin 3 for a signal that is normally HIGH switching LOW for one clock cycle period, such that the falling edge coincides with the middle of the F-Bit in the multiplexed stream.

6. In turn, tie each multiplexer input channel high and check that their position in the descrambled stream (IC10 pins) is unique.

Please Note: **Be sure the multiplexer and demultiplexer switches are toggled in the DATA position.**

4.8 CHECK OUT PROCEDURE

Module: Data Demultiplexer (FI-2222B)
Schematic No. D2221
Component Overlay D2223

Hardware Required if a Complete Link is Available:

Two Land Tactical Backplane Housings (Signal Input Panels)
PSK Data and Video Tx (FI-2202B)
Data Multiplexer (FI-2206A)
PSK Data and Video Separator (FI-2210B)
PSK Data Recovery Board (FI-2218B)
Descrambler and F-Bit Recovery Board (FI-2214A)
Two FOTx/Rx Modules and a Fibre Optical Link

If a Complete Link is Not Available:

One Land Tactical Backplane Housing (Signal Input Panel)
PSK Data and Video Tx (FI-2202B)
Data Multiplexer (FI-2206A)
Descrambler and F-Bit Recovery Board (FI-2214A)
Two Alligator Clip Leads

Additional Equipment Required:

Extender Card (2023A)
General Purpose Oscilloscope
Dolch Lam 4850 Logic Analyzer
Data Input Interface Cable (FI)
Data Output Interface Cable (FI) - for complete link set up only

Connection Procedure:

If a complete link is available:

1. Designate one housing as Tx and the other as Rx.

2. Insert into the Tx housing the PSK Data and Video Tx into J3 and the Data Multiplexer into J2.

3. At the receive end of the link, insert the PSK Data and Video Separator into J4, the PSK Data Recovery board into J5, the Descrambler and F-Bit Recovery board into J6, and the Data Demultiplexer into J7 of the Rx housing.

4. Connect the Data Input Interface cable to J9 of the Tx housing, and the Data Output Interface cable to J9 of the Rx housing.

If a complete link is not available:

1. Insert into the backplane housing the PSK Data and Video Tx into J3, the Data Multiplexer into J2, the Descrambler and F-Bit Recovery board into J6, and the Data Demultiplexer into J7.

2. Connect the Data Input Interface cable to J9.

3. Jumper the following test points accordingly:

a. TP47 of FI-2206A to TP2 of FI-2214A

b. TP12 of FI-2206A to TP3 of FI-2214A

Procedure:

1. Apply power and check for correct levels at TP7, 10, 11 and 12.

2. Ensure the correct TTL levels for Demux clock appear at IC1 pin 13 using the oscilloscope.

3. Check for Demux clock or $\overline{\text{clock}}$ at the following locations using the oscilloscope:

IC Number	Pin Number
2	3
6	8
11	8
18	8
22	8

4. Ensure the rising edge of the clock coincides approximately with the middle of the incoming data bit for the following locations using either measuring device:

IC Number	Clock Pin Number	Data Pin Number
2	3	2
6	8	1
11	8	1
18	8	1
22	8	1

The remaining tests require the use of the Logic Analyzer on Timing Mode at 50 ns sampling.

5. Be sure the switches on the multiplexer and demultiplexer boards are toggled in the DATA position.

6. Check that the rising edge of the LOAD pulse at IC7 pin 11 coincides with the centre of the F-Bit in the multiplexed stream at IC6 pin 3.

7. Display simultaneously the Demux clock at IC1 pin 8, the F-Bit Out at IC7 pin 2, and the codec Ck Out at IC3 pin 3.

The F-Bit should be alternating between HIGH and LOW every 27 Demux clock cycles. The Codec Ck should be switching at 1/2 the frequency of the F-Bit.

8. Check that the Parity Out at IC3 pin 5 is HIGH.

9. In turn, tie each Data Input Interface channel HIGH and ensure the correct channel responds at the demultiplexer (or at the Data Output Interface if the complete link arrangement is used).

APPENDIX 1
FIBRE-OPTIC CABLE INFORMATION

Performance Characterisitics of Acrylate Composite Coated Fibers in a Tight Buffer Cable Design

R. K. Lichtenberger
Belden Corporation, 2000 S. Batavia Ave., Geneva, IL 60134
(312) 232-8900

The purpose of this paper is to demonstrate the potential of low-loss tight buffer cable designs using Corning's composite acrylate buffered fibers. Discussion will be limited to the single-fiber construction depicted in Figure 1. The fiber is Corning's 100/140 um partially-graded index SDF. The SDF fiber is protected by a composite acrylate buffer coating. The fibers used for the major part of this study were buffered to a 400 um diameter. That dimension has since been increased to 500 um. Eight ends of 1420 denier Kevlar™ 49 are helically placed about the fiber at a 10 cm pitch and encapsulated inside a polyurethane jacket. The total diameter of the cable is 3.0 mm.

The quality of an optical cable is measured by the cable's ability to protect the fiber from the environment. This is accomplished in loose tube designs by isolating the fiber inside a plastic annulus with an inner diameter much greater than the fiber diameter. Alternatively, a tight buffer cable depends upon the cushioning effect of the buffer coating over the fiber to absorb environmental forces which would otherwise be sustained by the fiber. Such forces would distort the fiber and result in excess attenuation due to microbending.

Attenuation: The initial success or failure of the cable design will be determined by the amount of attenuation increase induced during cabling. Figure 2 tracks the attenuations at 854 mm of 10 representative tight buffer cabling runs. The average increase for this cable construction using the SDF fiber buffered to 400 ums is 2.66 dB/Km with 0.206 dB/Km standard deviation. These cables have a typical attenuation of 8.1 dB/Km, which may make them unsuited to many long distance applications. However, if the buffer diameter is increased to 500 um, the induced cabling loss is only 1.0 dB/Km, resulting in an average cable attenuation of 6.4 dB/Km. See Fig. 5.

NA: The increase in attenuation occurs as higher order leaky modes are lost. Because of this loss we also observe a moderate drop in numerical aperture (NA). Figure 3 compares the NA change with length for the 400 um diameter fiber before and after cabling.

Temperature vs. Attenuation: Because of the variation in thermal expansions of the individual cable components, loose tube cables are often constrained to a rather limited operating temperature range. Tight buffer designs can greatly extend the

operating temperature range provided the fiber is sufficiently buffered. Figure 4 illustrates the differences in temperature vs. attenuation performance between our tight tube design using SDF buffered to 400 um and the same fiber buffered to 500 um. The 400 um fiber shows a net improvement in room temperature attenuation after the first cycle due to stress relaxation. After the first cycle, the cable falls into a repeatable response curve where the total increase between +20° and -40°C is +5 dB/Km and between +20° and +85°C is +2.5 dB/Km. This is a very respectable temperature response in comparison with that of most loose tube designs. However, note the dramatic improvement that an additional 50 um in buffer thickness makes. With the 500 um diameter fiber, the attenuation remains virtually unchanged from +85°C to -20°C, where we see +0.2 dB/Km increase. The increase at -60°C is only +3.0 dB/Km. No hysteresis is evident. Given that all other aspects of cable processing were held constant, it is apparent that the additional buffering is successful in absorbing stresses that would otherwise cause microbending. The result is a small, flexible, lightweight cable with superior temperature performance.

Mechanical and Environmental Performance: In order to establish the suitability of tight buffer cables for long term use in a wide variety of applications, the cable must be extensively tested for mechanical endurance and environmental stability. A performance summary for our tight buffer cables using the 400 um outer diameter fiber appears in Table I. Comparative data using the 500 um diameter fiber is currently being compiled.

TABLE I Mechanical & Environmental Performance--Tight Buffer Cable #226101

These values hold true for both 400μm and 500μm cable samples, however the 500μm samples show greater repeatability under iterated testing

Load to Fiber Breakage:	2150 Newtons	(475 lb-force)
Recommended Installation Load:	544 Newtons	(120 lb-force)
Long Term Bend Radius:	5 cm (2 in.)	
Short Term Bend Radius:	7 mm (0.27 in.)	
Cyclic Flexing:	50,000 cycles over 1.4 cm bend radius under 10 Newtons tension. No jacket degradation and no fiber breakage.	
Impact Resistance:	1000 impacts at 37 N-cm (3.2 lb-in) No mechanical degradation and no attenuation increase.	
Solar Radiation Resistance:	Very good	
Fungal and Bacterial Resistance:	Very good per ASTM G-22-76	
Ozone & High Humidity Performance:	Very good per MIL-I-3930D	
Flame Retardency:	Passes IEEE-383 70,000 BTU-flame test.	

Conclusions

It has been demonstrated that a low-loss optical cable of tight buffer design can be produced with optical, mechanical and environmental performance rivaling that of loose tube designs. The effectiveness of the tight buffer cable depends critically upon the buffer's microbending resistance. In the case of the Corning SDF fiber, the 500 um buffer diameter has been found to be far superior to the 400 um diameter in reducing cable attenuation and in optimizing temperature performance.

In addition to the tests described in the text above, the program was extended to include 12 different cable types supplied by 5 manufacturers. The purpose of the extended program was to determine categorically the relative ~~differ~~ performance of loose tube vs. tight buffer cable designs. The results of some of the testing are shown in Figs. 6-8. I believe Figs. 6+7 are self-explanatory.

There are a number of comments to be made concerning Fig. 8. First, only Belden cables were included in the Fig. 8 comparison in order to simplify the graphic display, however the performance trends demonstrated are found to be typical of all the suppliers tested. Additionally, although only Crush Load test values are displayed, we've seen that the relative response to Tensile Loading of the loose tube and tight buffer designs is very similar to Fig. 8 (The numerical values are different, of course.) For both Crush and Tensile loading, we find that the close mechanical coupling of the tight buffer design causes a more immediate increase in attenuation under load, and a steeper response slope throughout. Because of the minimal mechanical coupling between →

the fiber and the rest of the cable in the loose tube designs, a substantial load can be sustained before a) the tube collapses about the fiber during the crush loading test, and b) the cable structure is elongated to the point where the fiber itself is placed under load in the case of tensile loading.

Our general conclusion is that tight buffer designs are superior in flex fatigue and impact endurance. They are extremely strong tensiley and under crush loading, but exhibited marked increases under these loads. Loose tube designs are superior performers under tensile and crush loads at the expense of flex and impact resistance. (As always, the user is the finial judge.)

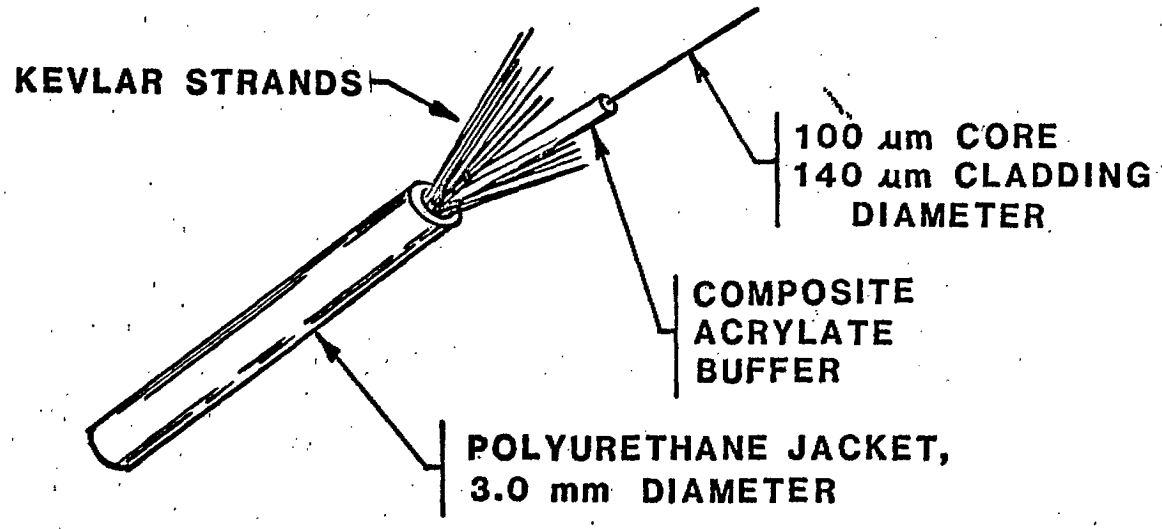

KEVLAR STRANDS
100 μm CORE
140 μm CLADDING
DIAMETER
COMPOSITE
ACRYLATE
BUFFER
POLYURETHANE JACKET,
3.0 mm DIAMETER

Fig. 1

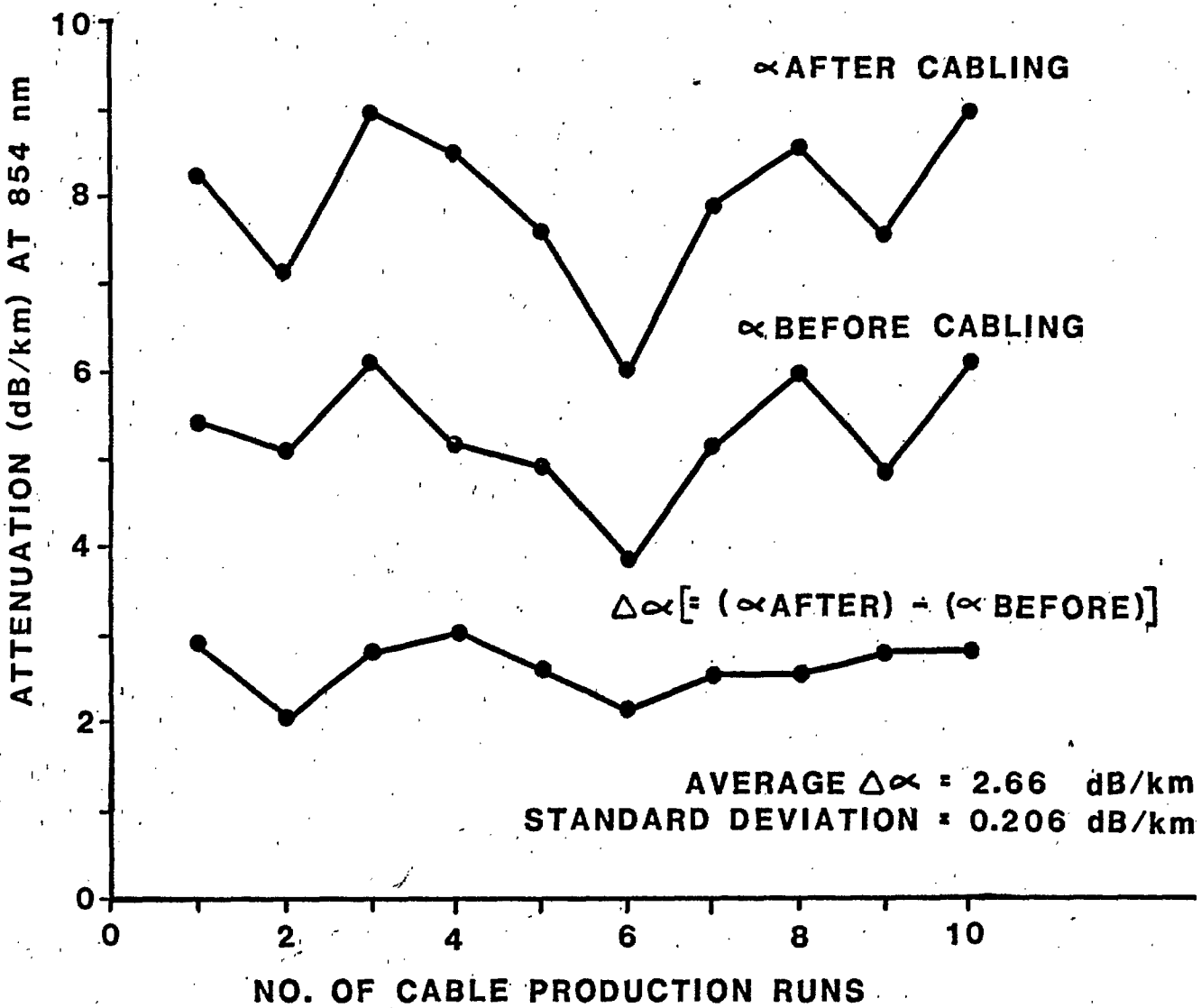

ATTENUATION (dB/km) AT 854 nm
10
8
6
4
2
0
0
2
4
6
8
10
NO. OF CABLE PRODUCTION RUNS
∝AFTER CABLING
∝BEFORE CABLING
Δ∝[= (∝AFTER) − (∝BEFORE)]
AVERAGE Δ∝ = 2.66 dB/km
STANDARD DEVIATION = 0.206 dB/km

Fig. 2

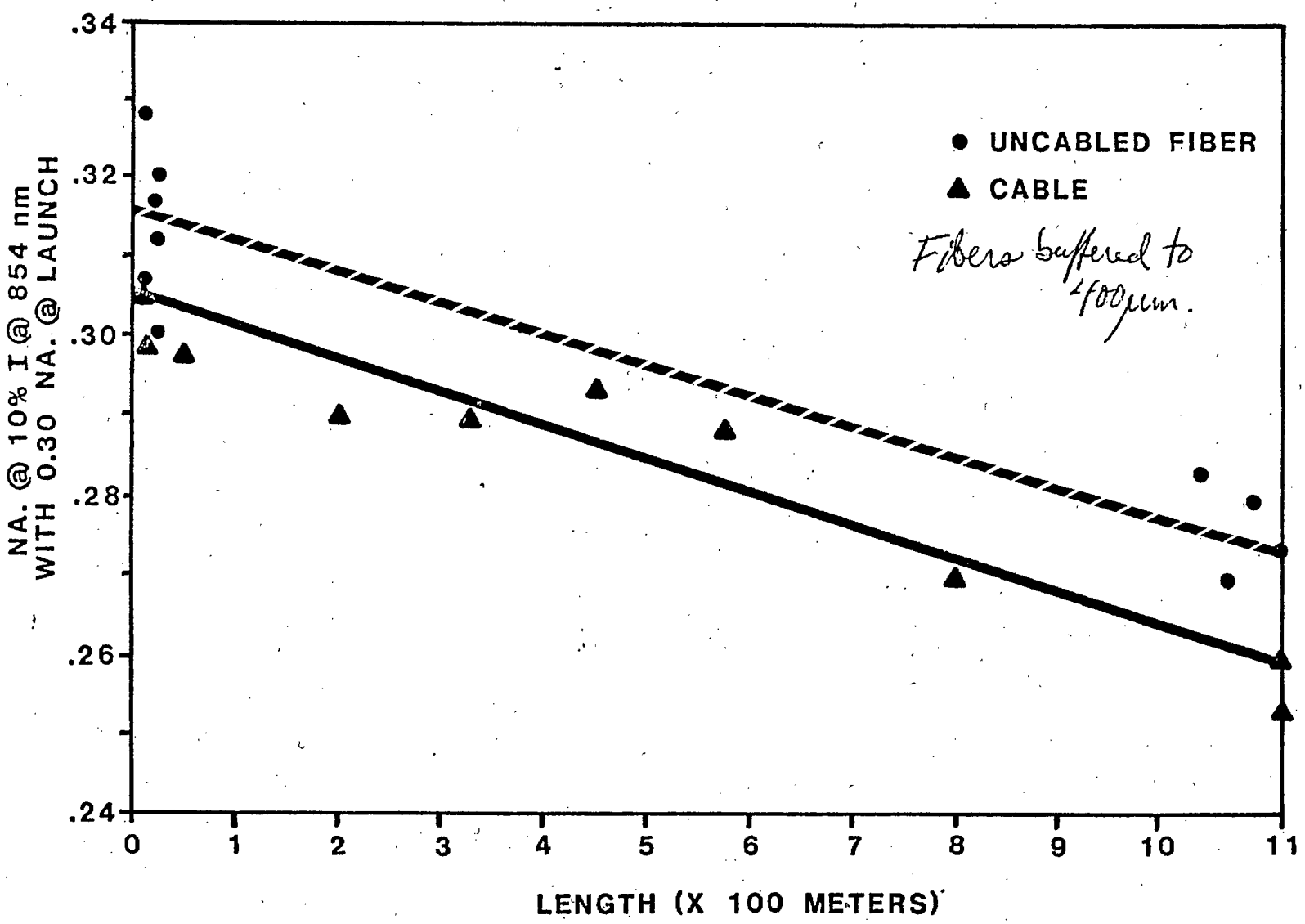

.34
.32
.30
.28
.26
.24
NA. @ 10% I @ 854 nm
WITH 0.30 NA. @ LAUNCH
UNCABLED FIBER
CABLE
Fibers buffered to
400μm.
0
1
2
3
4
5
6
7
8
9
10
11
LENGTH (X 100 METERS)

Fig. 3

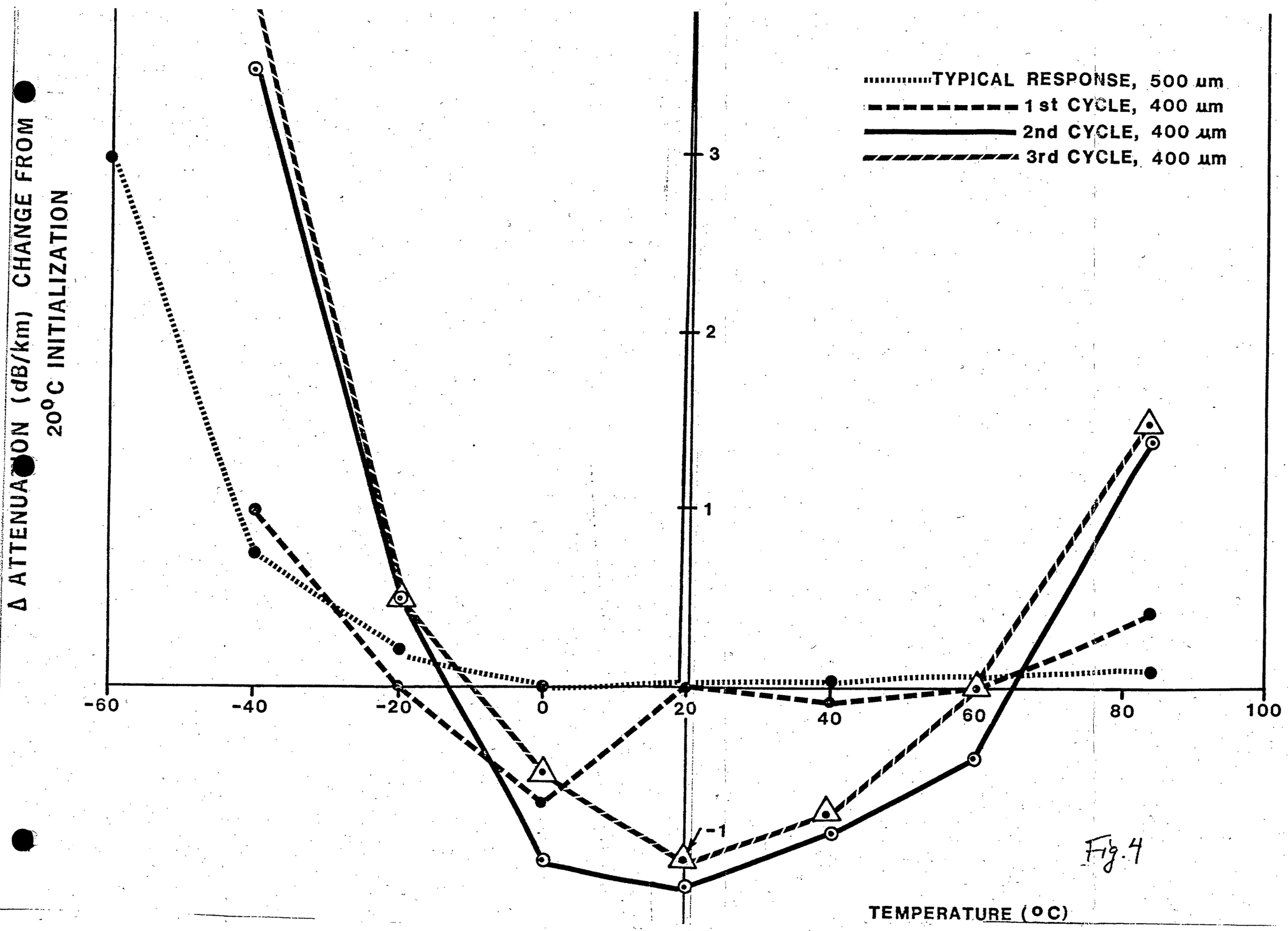

TYPICAL RESPONSE, 500 μm
1 st CYCLE, 400 μm
2nd CYCLE, 400 μm
3rd CYCLE, 400 μm
Δ ATTENUATION (dB/km) CHANGE FROM 20°C INITIALIZATION
3
2
1
-1
-60
-40
-20
0
20
40
60
80
100
TEMPERATURE (°C)

Fig. 4

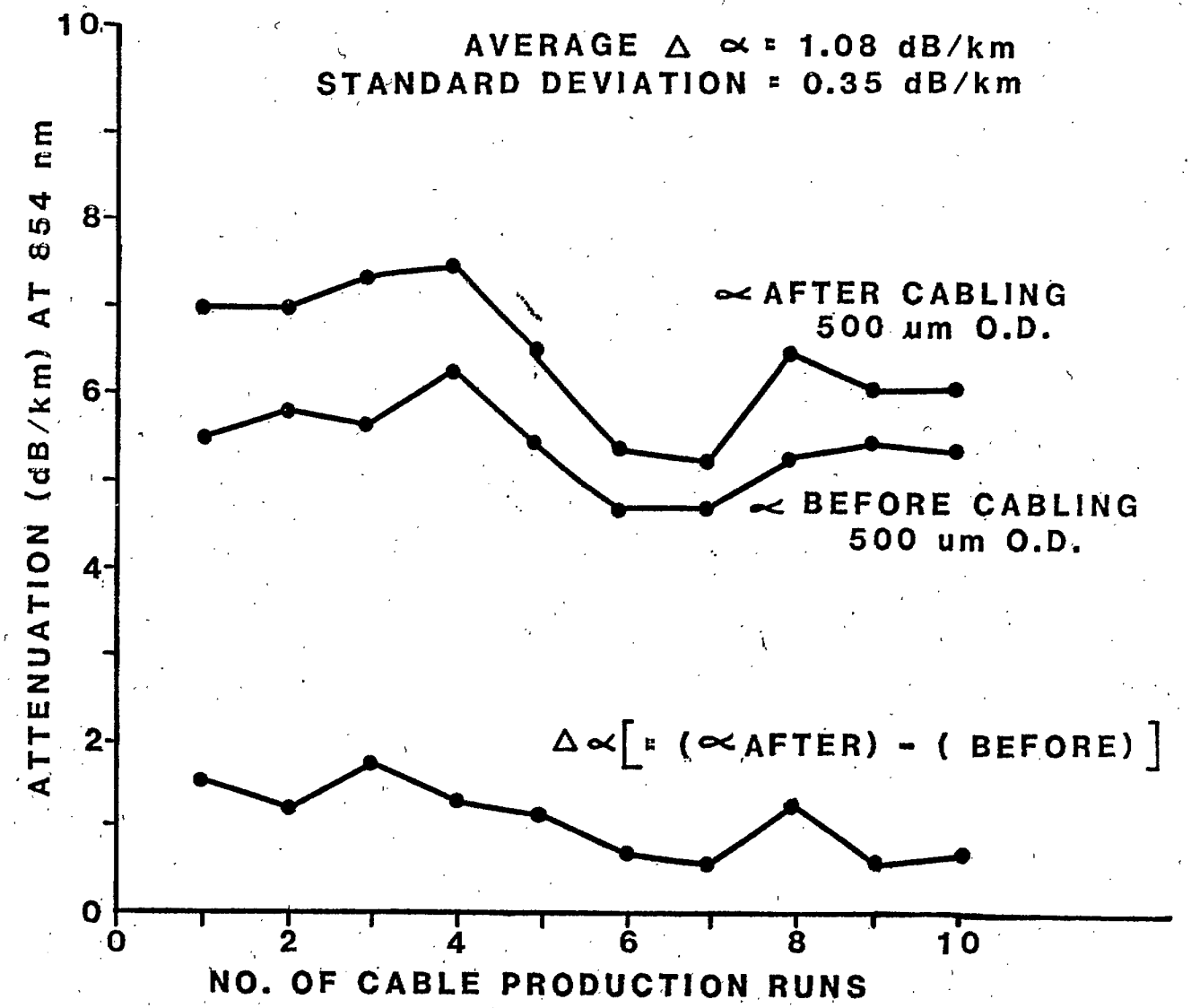
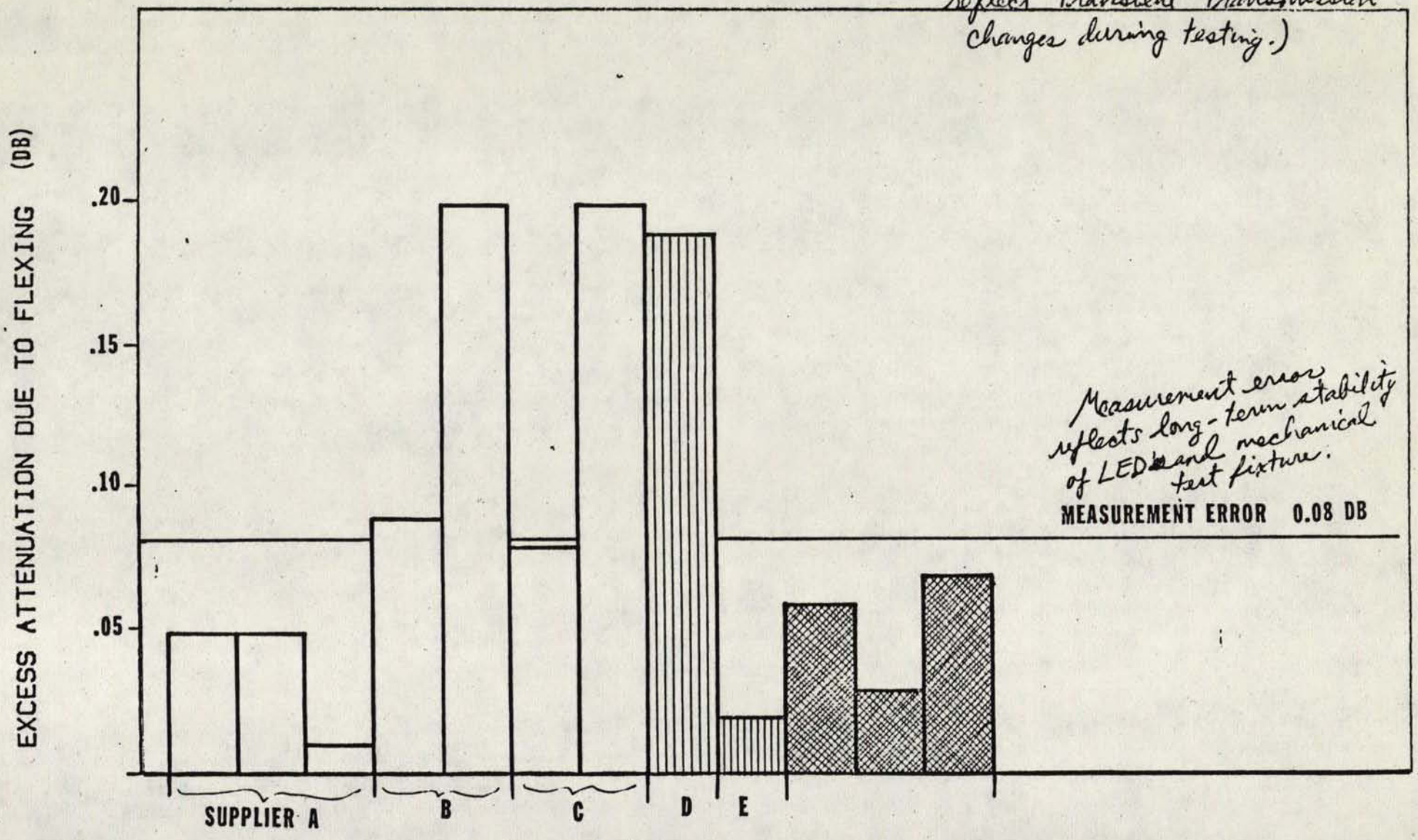

AVERAGE Δ ∝ = 1.08 dB/km
STANDARD DEVIATION = 0.35 dB/km
∝ AFTER CABLING
500 µm O.D.
∝ BEFORE CABLING
500 um O.D.
Δ∝[= (∝AFTER) - (BEFORE)]
ATTENUATION (dB/km) AT 854 nm
NO. OF CABLE PRODUCTION RUNS
0
2
4
6
8
10

Fig. 5

FLEX TEST

CABLE FLEXED 180 DEGREES BETWEEN A PAIR OF 40 MM RADIUS MANDRELS UNDER 1 KG LOAD. ATTENUATION CHANGE MEASURED AFTER 2000 CYCLES (i.e., this does not reflect transient transmission changes during testing.)



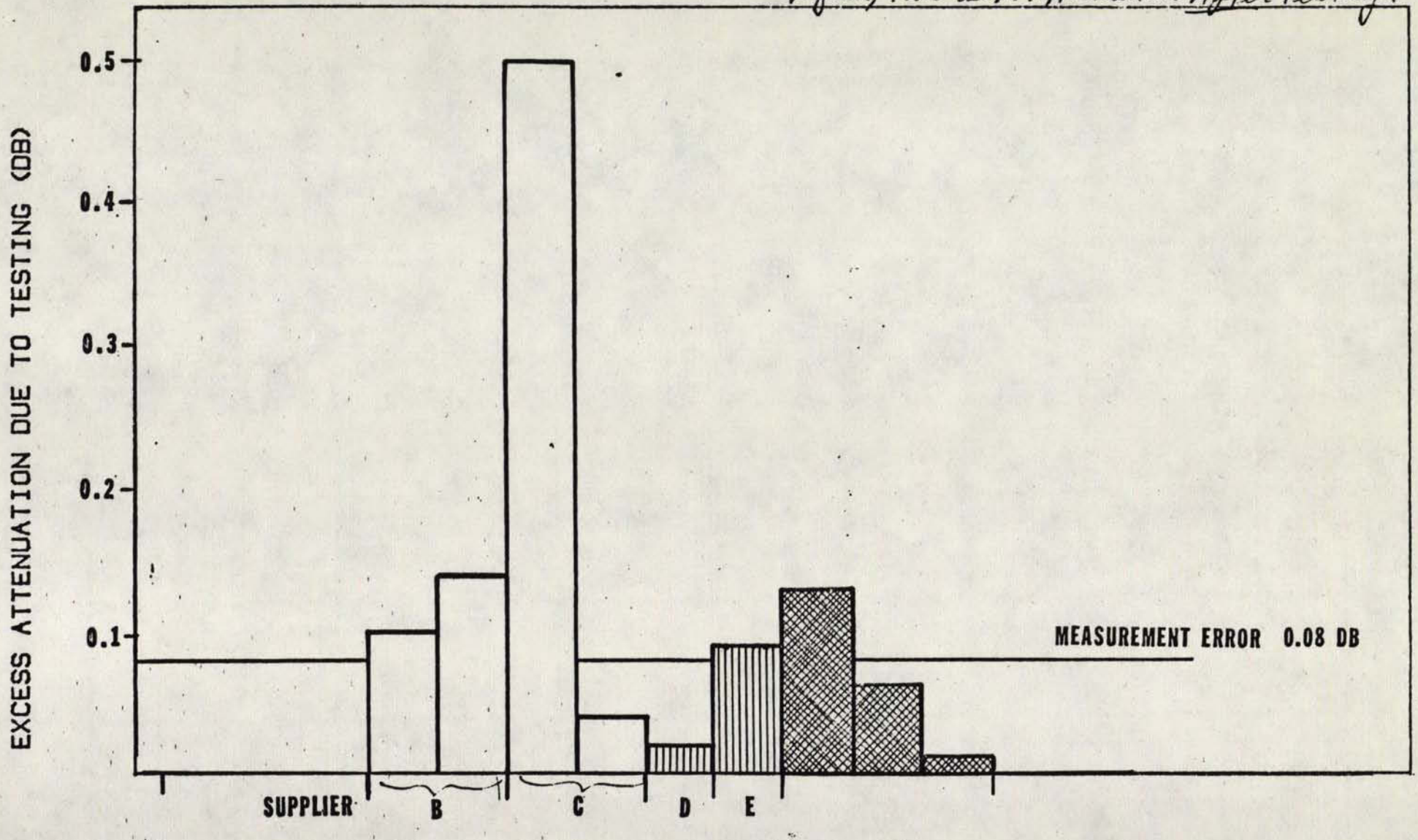
Measurement error reflects long-term stability of LED and mechanical test fixture.

DIFFERENT SUPPLIER'S SINGLE FIBER CABLES

Fig. 6

EIA FOTP # 25 IMPACT TEST
G ≡ TOTAL FORCE APPLIED = FORCE OF IMPACT X NUMBER OF IMPACTS
G = 3,200 LB-INCHES

Again, this is Δ Attenuation After testing.



DIFFERENT SUPPLIER'S SINGLE FIBER CABLES

Fig. 7

CRUSH LOADS

LOAD WAS APPLIED TO CABLE BETWEEN A PAIR OF 2 INCH PARALLEL PLATES.

ATTENUATION CHANGE WAS MEASURED UNDER LOAD.

The relationship between attenuation change with load, and the length of cable tested is not commonly linear. Therefore I could not normalize to lbs/inch.

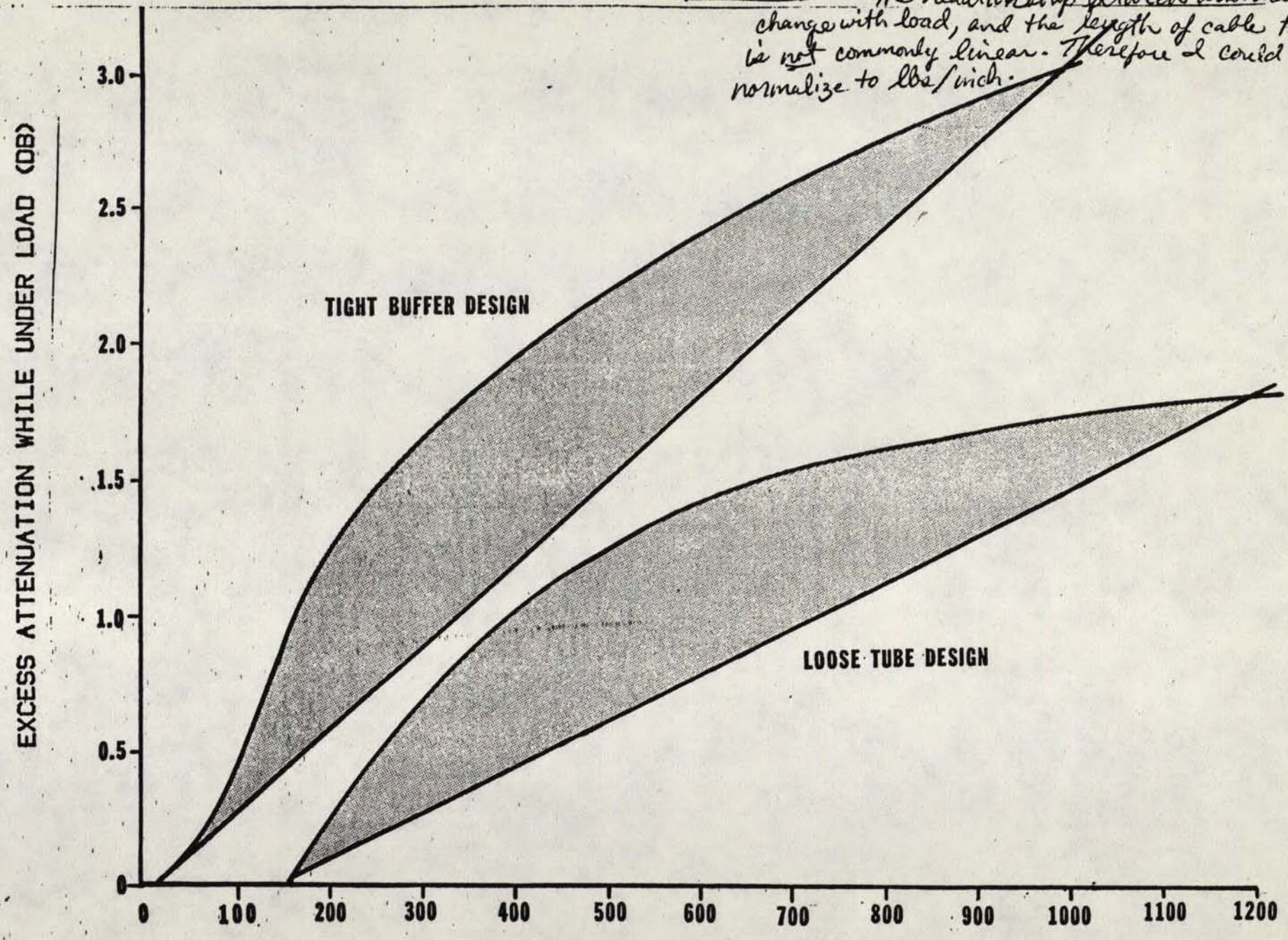


Fig. 8

PRODUCT DESCRIPTION:

Belden Fiber Optic Cables: BitLite™
Product Trade Numbers: 226101 and 226102
Partially-Graded Index Optical Fiber Cables

1. General

Belden's BitLite cables are lightweight and ruggedized for a wide variety of applications. These cables are 100% dielectric and highly flexible.

The partially-graded index fiber is concentrically surrounded by Kevlar™ for added strength and protection. An outer jacket of tough, durable polyurethane lends a high degree of flame retardency to the finished cable. The trade number 226101 is a single fiber cable while 226102 is a two fiber cable with each fiber separately isolated.

2. Properties of the Cabled Fiber

A. Optical Properties

1. Attenuation: The optical attenuation represents the amount of optical power lost as a result of absorption and scattering of radiation at a specified radiation wavelength over a given length of fiber. Attenuation is the rate at which power is lost with distance, and is expressed in decibels of optical power per kilometer (dB/km).

   Attenuation: 10 dB/km maximum
   7 dB/km typical

   Measurement Conditions:
   Wavelength: 850 nm
   Spectral Width: 5 nm FWHM
   Launch Numerical Aperture: 0.25
   Cable Constraints: Fiber Optic cable wrapped on final shipping reel.

2. Bandwidth: The bandwidth of an optical fiber denotes the maximum optical signal modulation frequency that can be transmitted through a length of fiber with a resultant signal power drop of 50% (-3dB) of the original power with zero frequency signal modulation. The bandwidth is measured using a known fiber length and a specified radiation wavelength. It is expressed in megahertz-kilometers (MHz-km).

   Bandwidth: 20 MHz-km (nominal)
   Measurement Conditions:
   Wavelength: 850 nm
   Spectral Width: 2.1 nm FWHM
   Fiber Test Length: In excess of 500 meters

2. Properties of the Cabled Fiber (Continued)

3. Numerical Aperture: The numerical aperture is a parameter which indicates the radiation-capturing ability of the optical fiber. It is calculated as the sine of the acceptance angle, within which incident meridional radiation will undergo total internal reflection resulting in transmission. The numerical aperture is dependent upon fiber test length, and the fractional intensity chosen as baseline for the calculation. NA_{100} is the numerical aperture calculated from the angular distribution of virtually 100% exit power. All measurements are under steady-state conditions.

   NA_{100}: 0.28
   Measurement Conditions:
   Test length: in excess of 500 meters
   Source: Xenon arc lamp
   Launch Numerical Aperture: 0.40
   Cable Constraints: Fiber Optic Cable wrapped on final shipping reel.

B. Fiber Construction and Dimensions

1. Materials: The fiber is all glass partially-graded refractive index with an acrylate composite buffer coating, mechanically strippable.
2. Core Diameter: 100 ± 4 um
3. Glass Cladding Outer Diameter: 140 ± 6 um
4. Coated Diameter: 500 um, nominal

3. Cable Descriptions

A. Fiber Buffer Diameter: 500 um, nominal
B. Reinforcement: Kevlar™ 49 Aramid Yarn strength member
C. Cable Jackets: Black Flame Retardant Polyurethane

1. 226101 Dimensions: BitLite 226101 is a single-fiber construction.

   Jacket Inner Diameter: 1.78 mm (nominal)
   Jacket Outer Diameter: $3.00\ \text{mm}\ {}^{+0.05}_{-0.15}\ \text{mm}$

2. 226102 Dimensions: BitLite 226102 is a two-fiber cable. Each fiber is individually reinforced and jacketed together into a parallel duplex construction.

   Inner Diameter: 1.78 mm (nominal) for each conductor
   Outer Diameter: 3.0 ± 0.1 mm by 6.2 ± 0.2 mm

D. Flame Retardency Rating

226101 and 226102 exhibit superior flame retardant properties and are UL VW-1 rated. This cable also passes the IEEE-383-1974 70,000 BTU flame test as revised by the U.S. Nuclear Regulatory Commission in Guide 1.131.

E. Cable Weight

1. Unit weight of 226101: 8.14 kg/km (17.9 lbs/km)
2. Unit weight of 226102: 16.3 kg/km (35.9 lbs/km)

4. Cable Physical Properties and Environmental Performance

These performance characteristics are the result of repeated in-use simulation testing.

A. Tensile Strength

1. Tensile Strength of 226101:

Load to Fiber Breakage: 2150 Newtons (475 lb-force), short gage length

Recommended Maximum Load for Installation: 544 Newtons (120 lb-force)

Recommended Maximum Residual Load for Long Term Operation: 20 Newtons (4.42 lb-force)

2. Tensile Strength of 226102:

Load to Fiber Breakage: 4300 Newtons (950 lb-force), short gage length

Recommended Maximum Load for Installation: 1088 Newtons (240 lb-force)

Recommended Maximum Residual Load for Long Term Operation: 40 Newtons (8.84 lb-force)

B. Temperature Performance

The following performance parameters are characteristic of both 226101 and 226102.

1. Operating Temperature Range - Installed:
-40 to +85°C (−40° to + 180°F)
Typical attenuation change from +20° to−40°C, less than 2 dB/km. Typical change from +20° to +85°C, less than 1 db/km.

During testing the full kilometer length was exposed to the temperature extremes. Exposure of shorter lengths will result in a proportionately reduced attenuation change throughout the temperature range.

2. Storage Temperature Range: -40°C to +85°C (-40°F to +180°F).
A storage temperature as low as -40°C (-40°F) may be used with 100% recovery in the operating temperature range.

C. Bend Radius

1. Long Term Bend Radius: 50 mm (2 in.) minimum, unloaded.

2. Short Term Bend Radius: 7 mm (0.27 in.) minimum, unloaded.

D. Cyclic Flexing

The cable is inserted between a pair of mandrels of a specified radius and under a specified tensile load. The cable is then bent between the mandrels through a 180° arc.

1. Cyclic Flexing Over 50 mm Radius Bend: 1000 cycles
Load for 226101: 10 Newtons (2.2 lb-force)
Load for 226102: 20 Newtons (4.4 lb-force)
Results: 1000 cycles with no change in optical transmission.

2. Cyclic Flexing Over 14 mm Radius Bend: 50,000 cycles
Load for 226101: 10 Newtons (2.2 lb-force)
Load for 226102: 20 Newtons (4.4 lb-force)
Results: Test terminated at 50,000 cycles. No jacket degradation and no fiber breakage.

4. Cable Physical Properties and Environmental Performance (continued)

E. Twist-Bend

The cable is twisted ± 90° while simultaneously being bent 180° over a 50 mm radius pulley under a tensile load of 100 Newtons (22 lb-force).

1. Twist-Bend: 1,000 cycles
   Results: Less than 0.1 dB attenuation increase.

F. Impact Testing

A known mass is dropped from a specified height onto a mandrel having a 1.25 centimeter radius. The mandrel is placed across the cable such that the total force of impact is imparted to the cable.

1. Impact Resistance 1: 10 impacts at 500 Newton-centimeters (43 lb-inches). Impacted cable is again subjected to the Cyclic Flexing test.
   No optical or mechanical degradation occurs.
2. Impact Resistance 2: 1000 impacts at 37 Newton-centimeters. (3.2 lb-inches) No optical or mechanical degradation after testing. No attenuation increase.

G. Crush Resistance

A load is applied to the cable and continually increased until the optical transmission has decreased to virtual zero. The load is then removed and the cables allowed to return to an unstressed state. Attenuation change after testing is recorded.
Crush Load: 2,595 Newtons/centimeter (1,453 lbs/inch).
Attenuation Change: 0.3 dB.

H. Cold Temperature Flexibility

Cable remains flexible to below -40°C (-40°F)

I. Lifetime: In excess of 40 years.

A cable's lifetime is directly related to the mechanical and environmental conditions it experiences. The materials and structure have been tested by accelerated aging conditions similar to that of conventional cable products to indicate a potential lifetime in excess of 40 years for normal indoor and protected outdoor installations.

J. Dielectric Strength: Greater than 1.4 Megavolts/inch.

5. Installation Considerations

A. Solar Radiation Resistance: Excellent.

After 1000 hrs. of exposure to ultra-violet radiation, no change in the elongation or tensile strength of the jacketing compound was induced. 1000 hrs. of exposure in this test is equivalent to 40 years of continuous Arizona sun.

B. Fungal and Bacterial Resistance: Very good.

Jacketing material has been tested in accordance with ASTM G-22-76 and ASTM G-21-70 for fungal and bacterial resistance and has been proven to be highly effective in withstanding fungi and bacteria with no incurred degradation in elongation or tensile strength after testing.

C. Ozone Resistance: Very good.

BitLite 226101 was tested in accordance with MIL-I-3930D for ozone resistance. After 168 hours of exposure, no degradation in elongation or tensile strength was incurred.

D. High Humidity Performance: Very good.

The cable was tested to MIL-I-3930D for hydrolytic stability. After 28 days at 97°C and 97% humidity, no degradation was incurred.

5. Installation Considerations (continued)

E. Water Immersion

Short term immersion or exposure to high humidity environments does not affect the cable. Long term immersion is also possible provided the temperatures do not go below 0 °C. Water may enter the cable without damage or measurable effects on the fiber performance, however, the freezing of this water will cause an increase in attenuation due to microbending of the fiber.

F. Nuclear Radiation Resistance

Nuclear radiation causes increases in optical attenuation of the fiber during the radiation period with a recovery of transmission after irradiation. Specific test details are available from publications and articles. Based on current data, normal terrestrial background radiation levels produce no major effect over the estimated cable lifetime.

G. Flame Propagation and Gases Due to Burning

Based on the UL VW-1 test and IEEE-383-1974 70,000 BTU test, the cable will not support a vertical self–propagating flame. In high temperature fire environments the gases produced by polyurethane are known to be toxic. For applications requiring nontoxic gas production, other jacket materials can be considered.

H. Vehicle Roll Over

Cable samples were subjected to 48,000 tire impacts at an average vehicle speed of 50 miles per hour from a passenger car. No fiber breakage occured nor was any splitting of the jacket induced.

In a second test, the transmission was monitored during vehicle roll-over. A maximum transmission change of 2.50 dB was observed at the moment of impact with 100% recovery after impact.

I. Environmental Considerations

The cable materials are considered safe for human exposure and contact. Natural long term (100 years) degradation results in no known toxic by-products.

J. Safe Handling Procedures

The optical fiber in this cable can transmit infrared (non-visible) radiation levels which may be hazardous to the eye. Never directly view the end of an energized fiber.

The fibers are composed of glass which may present major problems if it enters the body. Care must be taken to properly dispose of fiber pieces. Safety glasses are recommended when fracturing or working with the fibers to prevent eye damage.

6. Labeling, Packaging and Shipping

Fiber Optic cables are shipped in suitable containers to protect them during air or ground transit. The single fiber cables are placed on a reel and in a container such that the total weight for a 1 km length is less than the 50 lbs. limit for UPS. Each cable reel is labeled with the product trade number, type of cable, and a reel control number assigned during manufacture.

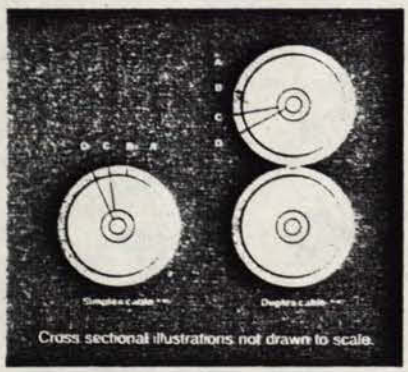
7. Non-Conforming Fiber Optic Cable

If the customer believes that any goods received are defective, they must notify Belden within thirty (30) days of discovery of the alleged defect. No material is to be returned until a written Return Material Authorization has been received by the customer. Upon receipt of a written Return Material Authorization, the merchandise may be returned to the Belden Corporation, Geneva, Illinois, freight collect, and will be credited based on the Belden Inspection Department's report that the material is defective. Adjustment will be granted on the basis of replacing the material to the customer, transportation charges prepaid, or crediting the customer's account.

8. Note that this product description may be subject to change without notice.

BELDEN

BitLite™ PARTIALLY GRADED INDEX FIBER OPTIC CABLES



Cross sectional illustrations not drawn to scale.

A. Black flame retardant polyurethane jacket
B. Kevlar® strength member
C. Coating
D. Optical fiber

100μm core and 50μ core glass-clad fibers

This "ruggedized" tubeless construction fiber optic cable offers outstanding cost efficiency when used in a variety of computer, instrumentation and control applications.

Available in one- and two-fiber configurations, Belden tubeless construction fiber optic cables feature toughness, strength, flexibility, light weight, excellent optical properties and flame retardance. Minimum bandwidth is 20 MHz-Km for the 100μm core cable and 200 MHz-km for the 50μm core construction. All cables pass the UL VW-1 flame test.

Simplex cable passes U.S. Nuclear Regulatory Commission version of the IEEE-383-1974, 70,000 BTU Test.

On special request, Belden can provide other cable types with a wide range of bandwidths up to 1,500 MHz-Km and low attenuations, approaching 1.0 dB/Km. In fact, for most optical budgets and environmental conditions, Belden can deliver a cable to meet your needs.

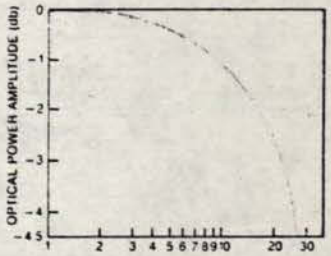
Belden can also supply cables with a variety of other optical fibers, including both single and double window types. **For custom jacket colors, configurations such as terminated assemblies, and other custom capabilities, consult the Belden Fiber Optics Group.**

2261 SERIES CABLES

100 μm core

FIBER SPECIFICATIONS

Fiber core	100 μm
Clad O.D.	140 μm
Coated O.D.	500 μm
Numerical aperture	0.30
Attenuation	7dB/Km at 850 nm (typical). max. 10dB/Km
Bandwidth	20 MHz-Km



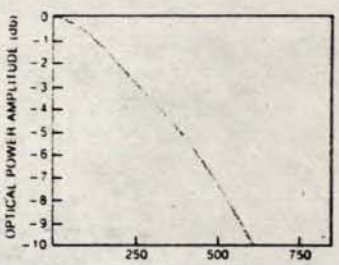
TYPICAL FREQUENCY RESPONSE

2271 SERIES CABLES

50 μm core

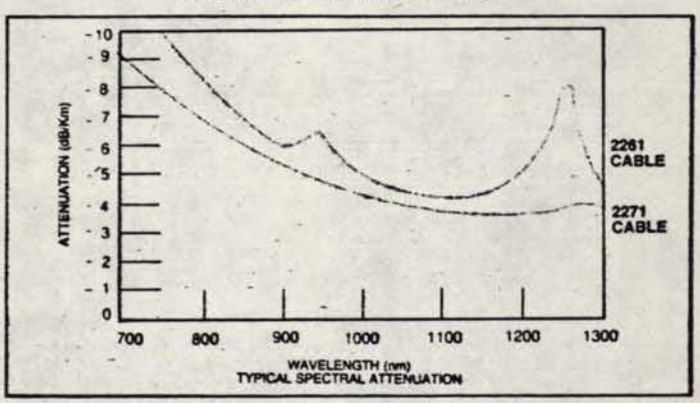
FIBER SPECIFICATIONS

Fiber core	50 μm
Clad O.D.	125 μm
Coated O.D.	500 μm
Numerical aperture	0.21
Attenuation	6dB/Km at 850 nm (typical). max. 8dB/Km
Bandwidth	200 MHz-Km



TYPICAL FREQUENCY RESPONSE

CABLES PASS THE UL VW-1 FLAME TEST



TYPICAL SPECTRAL ATTENUATION

226101	1	3.0	8	120	50
226102	2	3.0x6.0	16	240	50
227101	1	3.0	8	120	50
227102	2	3.0x6.0	16	240	50

All dimensions are nominal. Standard lengths 1 Km.

FOR MORE INFORMATION WRITE OR CALL US:

BELDEN CORPORATION, FIBER OPTICS, 2000 S. BATAVIA AVE., GENEVA, IL 60134. PHONE: 312-232-8900.

Bulletin FOS81-1
Superseding FOS80-1
July 1, 1981

BELDEN

SUGGESTED TRADE NET PRICE SHEET
FIBER OPTIC CABLE

(See Current Fiber Optic Catalog for Description)

DOLLARS PER METER

Trade Number	Less than 0.5 Km	0.5 to 1 Km	1 to 5 Km	5 to 10 Km	Weight Kg/Km
220001	$ 1.91	$ 1.78	$1.65	$1.59	13.5
220002	3.63	3.39	3.14	3.03	27
220006	10.10	9.43	—	—	40
220012	20.48	19.11	—	—	155
220018	30.30	28.28	—	—	260
221001	2.56	2.39	2.22	2.14	13.5
221002	4.91	4.59	4.25	4.10	27
221006	13.78	12.86	—	—	40
221012	28.12	26.24	—	—	155
221018	41.77	38.98	—	—	260
226001	1.94	1.81	1.68	1.62	13.5
226002	3.65	3.40	3.15	3.04	27
226006	10.21	9.53	—	—	40
226012	20.66	19.28	—	—	155
226018	30.60	28.56	—	—	260
226101	2.00	1.86	1.73	1.57	8
* 226102	3.80	3.54	3.29	2.99	16
227101	1.43	1.33	1.24	1.17	8
227102	2.71	2.53	2.35	2.22	16
227001	1.34	1.25	1.16	1.11	13.5
227002	2.47	2.31	2.14	2.06	27
227006	6.22	5.80	—	—	40
227012	12.66	11.81	—	—	155
227018	18.61	17.37	—	—	260
227201	1.50	1.40	1.30	1.25	13.5
227202	2.78	2.59	2.41	2.31	27
227206	7.16	6.68	—	—	40
227212	14.51	13.54	—	—	155
227218	21.39	19.96	—	—	260

225XXX series shown in Catalog FO-78 is obsolete. Substitute 227XXX series.

Prices Subject To Change Without Notice

BELDEN CORPORATION/FIBER OPTICS GROUP/2000 S. BATAVIA AVE., GENEVA, ILLINOIS (312) 232-8900

WHITE RADIO LIMITED

CANADIAN WAREHOUSING REPRESENTATIVES SINCE 1925

Burlington, Ontario.
September 15th, 1981.

Foundation Instruments Ltd.,
1794 Courtwood Crescent,
Ottawa, Ontario,
K2C 2B5.

Attention: Pete Wheeler

Dear Pete:-

Re: Belden Bit-Lite Cable

Thank you for the order Beth placed today for the 3,040 metres of Belden 226102 cable at $4.15/m, F.S.T.N.I.P. The order has been entered and delivery is estimated at four to six weeks or better.

Confirming our recent discussions, Belden have given us a budgeting estimate on 250km of this cable of $2.94/m, F.S.T.N.I.P., F.O.B. Burlington, Ontario. Delivery is estimated at commencing in six to eight weeks, and would obviously need to be scheduled over a period which would be negotiated to both parties' satisfaction.

If we can be of further assistance in the meantime, Pete, please feel free to call John or me.

Thank you for your valued business.

Yours truly,

Dan Hansen

Dan Hansen,
Fiber Optics Product Manager,
WHITE RADIO LIMITED.

DH:ak
cc: Beth Manners
John Pembry

4445 HARVESTER ROAD, BURLINGTON, ONT. L7L 4X1 • TELEX 061-8618 • PHONE 632-6894 • TORONTO 827-8550
MONTREAL OFFICE • 3300 CAVENDISH BLVD. SUITE 245, MONTREAL, P.Q. H4B 2M8 • PHONE 481-0158

BELDEN

March 10, 1982

Mr. Dan Hansen
White Radio, Ltd.
940 Gateway Dr.
Burlington, Ontario, Canada L7L 5K7

Dear Dan:

In response to your inquiry concerning the BitLite duplex cable which is being supplied by Foundation Instruments for the Canadian army, I have investigated both the overhand knot test and the status of a splice kit. Concerning the overhand knot test, we have performed a series of tests and found that one fiber broke on one in six twelve knots when tied. Each of these knots was subjected to a 25 lb. load for a 5 minute period. It is felt that when this cable is tied in the knot the fiber is experiencing tensile load on its outer surface in excess of 250,000 psi. This tensile load is in excess of the fiber proof test and consequently breaks will occasionally appear. Should this be an objectionable feature and have the potential of nullifying any future order, a larger cable jacket might be suggested. This would, in fact, require development of a special fiber optic cable type for the army application; however, due to the potential volumes of fiber optic cable, we would consider such a special construction.

Currently we are planning to generate a splice kit for our 227102 duplex cable product. The components for such a kit are currently being obtained, and we expect to fabricate a number of experimental splices and test them with respect to both temperature and mechanical performance. Consequently, we do not expect to have a finalized product available until at least June, 1982. With the potential problem of the overhand knot requiring cable redesign, it would seem unwise to develop a splice kit for a cable construction which may be modified. Please inform us on the necessity for a splice kit or if our strategy should be to establish initially the correct cable design and then follow later with a splice kit.

Hopefully this response answers all outstanding questions and this information will be transmitted to Peter Wheeler at Foundation Instruments. Should you require any additional information or if questions arise, please feel free to contact Dennis Gudgel, Sales Application Engineer or me.

Sincerely yours,

Ron Ohlhaber
Product Development Manager
Fiber Optic Department

cc: D. Gudgel

dt/DB/JX

APPENDIX 2
ASSEMBLY OF THE 226102 FIBRE CABLE AND U-185-B/G CONNECTOR.

ASSEMBLY OF THE 226102 BELDEN FIBRE-OPTIC CABLE INTO THE U-185 B/G ELCO ELECTRICAL CONNECTOR.

STEP 1. Separate the duplex fibre cable for a length of 18" (see Figure 1.). Note that one side of the cable is labelled and the other side is ribbed.

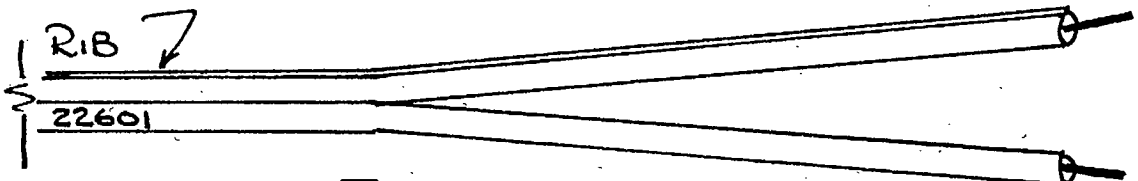


Figure 1.

STEP 2. Obtain two matched halves of 1833 Waterproof bushing (see Figure 2), and two #4 x 7/16 phillister head screws.

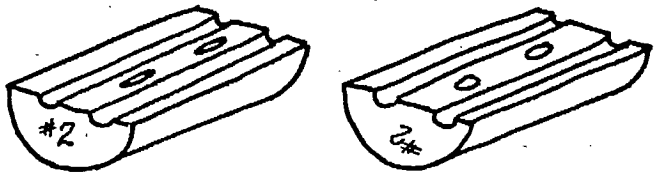


Figure 2

STEP 3. Apply RTV 3141 Dow Corning or similar silicone rubber sealant to the 1833 bushing relief. (See Figure 3.)

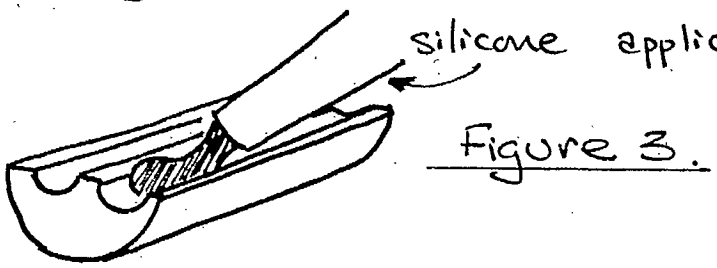


Figure 3.

The silicone will provide a moisture barrier into the connector.

Step 4 Obtain a ring crimp connector and section of heatshrink and assemble the strain relief as per Figure 4.

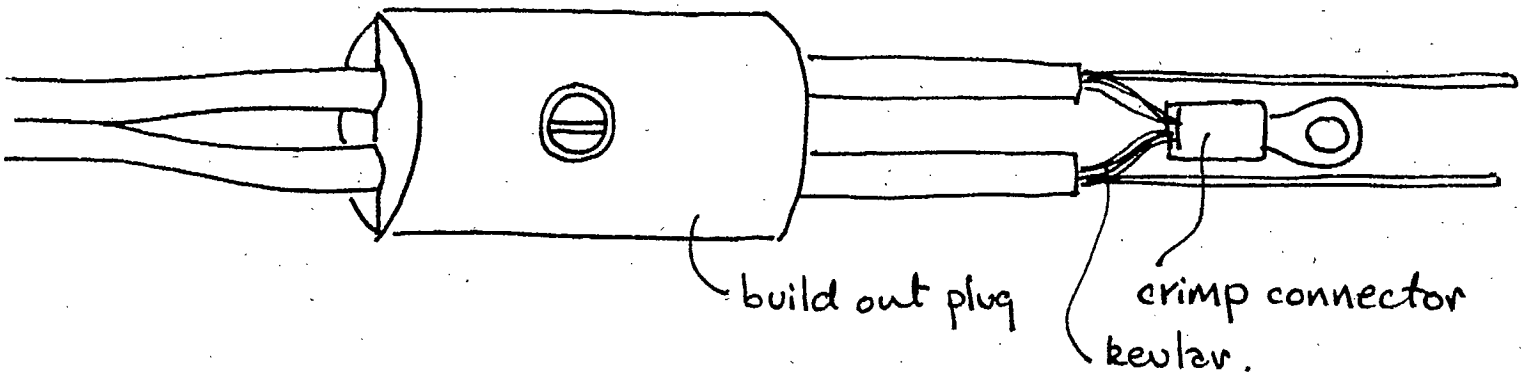
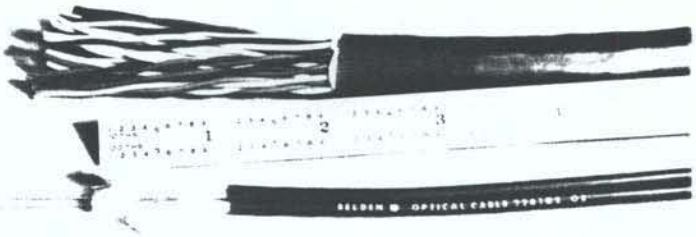
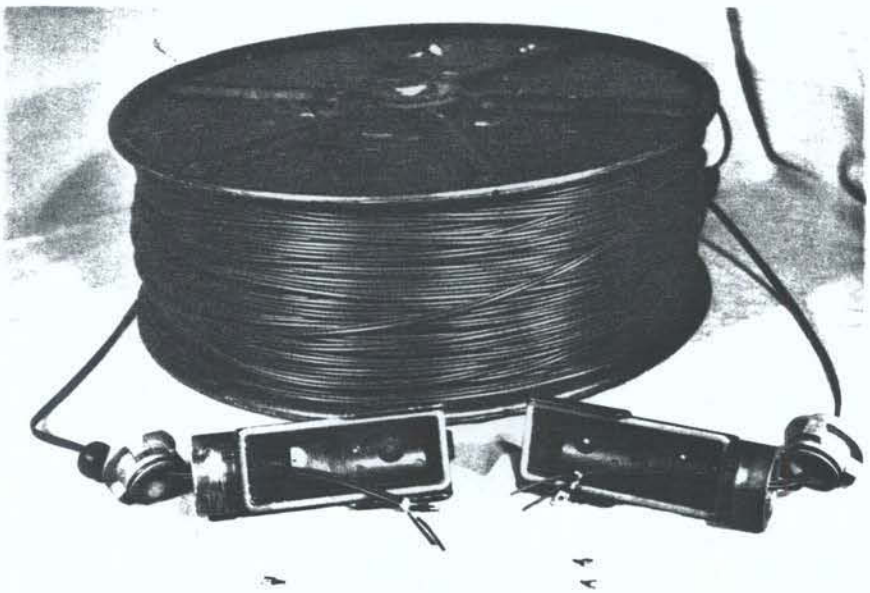


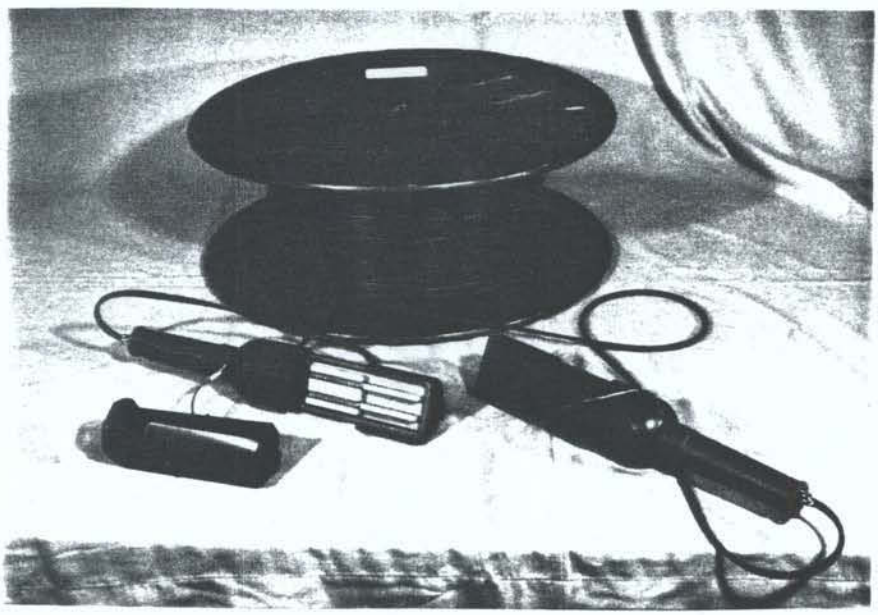
Figure 4.

Step 5

Fasten the crimp ring to the grounding screw inside the U-185 B/G connector and complete as per following illustrations.







APPENDIX 3

L.E.D. AND OPTICAL POWER BUDGET DATA.

Spectronics
A division of Honeywell

GaAlAs LIGHT EMITTING DIODE

SE 3352

PRELIMINARY DATA

FEATURES

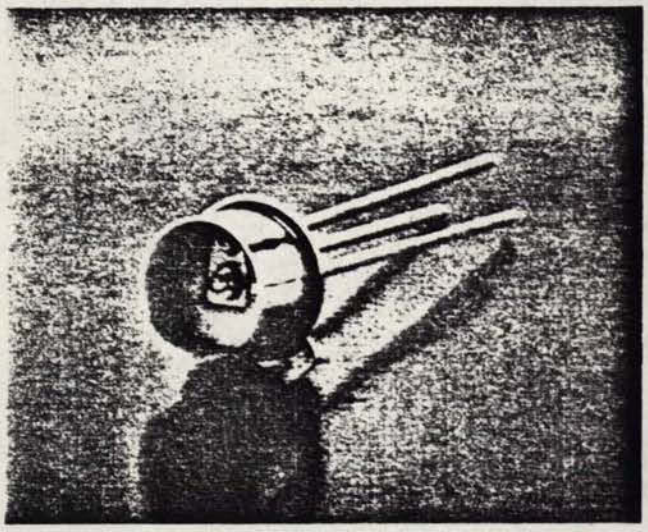
- Efficient pluggable coupling to single fiber cables
- Exceptional linearity
- Fast response
- Wide temperature range
- Matched with SD3322 PIN photodiode

DESCRIPTION

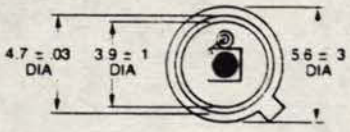
The SE 3352 is a high radiance GaAlAs IR LED optimized for coupling to a variety of optical fibers. Its unique integrated optical element projects a uniform spot 300μm in diameter at the window surface allowing efficient coupling to single fibers without the high precision connectors normally required for pigtail sources. The SE 3352 case is isolated for EMI shielding.

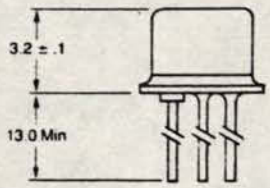
ABSOLUTE MAXIMUM RATINGS

Storage temperature	−25°C to +85°C
Case operating temperature	−20°C to +70°C
Lead solder temperature	240°C, 5 sec.
Continuous forward current	150mA
Reverse voltage	1V @ 10μA
Case-cathode (anode) voltage	180 volts

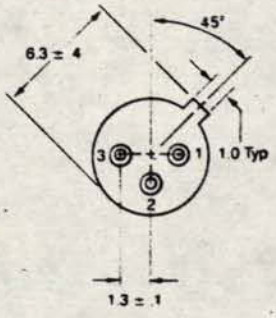


PACKAGE CONFIGURATION





NOTES:
1. Anode & cathode insulated from case
2. PIN 1 — anode (P-type), PIN 2 — cathode (N-type), PIN 3 — case (ground)

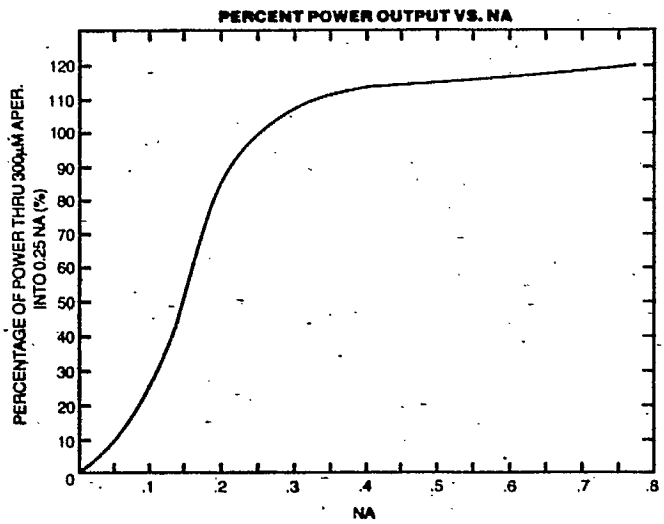


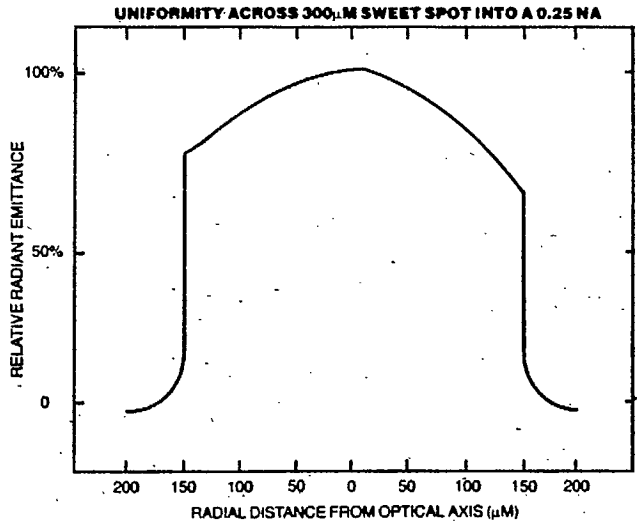
ALL DIMENSIONS IN MILLIMETERS

ELECTRO-OPTICAL CHARACTERISTICS (T_{case} = 25°C)

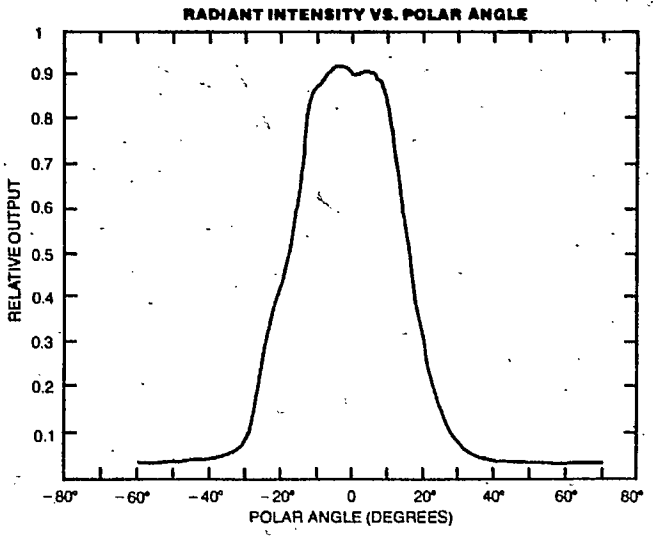
PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Forward Drop	I_f=100mA	V_f		1.6	2.0	volts
Series Resistance		R_S		1.6		Ω
Device Capacitance	V_R=1V	C_T		800		pf
Power Output	I_f=100mA Aperture=300μm NA=.25	P_O				μW
-001			150	250	400	
-002			400	700	1000	
-003			1000	1500	2000	
-004						
-005						
Response Time		t_f		12		ns
Peak Output Wavelength	I_f=100mA	λ_p		820		nm
Spectral Bandwidth	I_f=100mA	$\Delta\lambda$		35		nm
V_f Temperature Coefficient		$\Delta V_f/\Delta T$		-1.70		mV/°C
P_O Temperature Coefficient	I_f=100mA			-.012		dB/°C
λ Temperature Coefficient		$\Delta\lambda/\Delta T$		.35		nm/°C
Thermal Resistance		Θ		100		°C/W

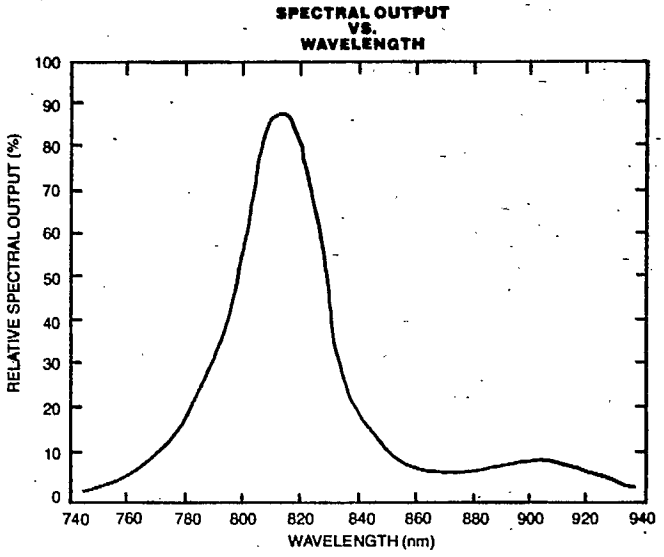
TYPICAL PERFORMANCE CURVES

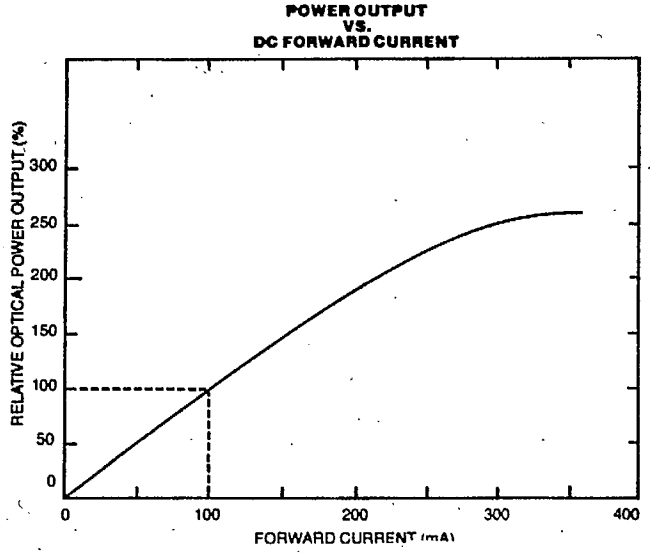


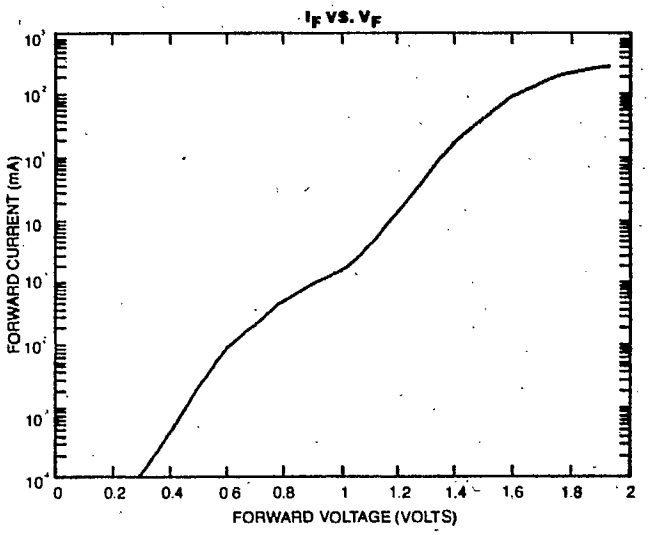


TYPICAL PERFORMANCE CURVES









APPLICATION RECOMMENDATIONS

The SE3352 LED is designed for use with optical receptacles that align the optical axes with respect to the outer surface of the LED can. Several manufacturers supply such receptacles with inner cavities matched to both TO-46 and TO-5 devices. The SE3352 LED is a modified TO-46 package requiring an adapter ring that fits a TO-5 receptacle. This part is supplied by Spectronics and is designated SPX 3694-002; adapter ring. When ordering receptacles, TO-5 cavities must be specified so as to accommodate the LED adapter ring assembly. For more information contact a Spectronics representative.

Power Budget for DND Land Tactical Fibre Optic Communication System using Sweetspot 3352-004 l.e.d. and Belden Bit Lite Cable No. 226102

	Conditions	Best Case	Worst Case
Input Power	I_f = 100 ma Aperture = 300 µm NA = 0.25	3 dBm	0 dBm
Coupling loss into fibre	(see note)	-10.1 dB	-10.1 dB
Cable loss		-7.(typ) dB	-10 dB
Temp. degradation		+0.3 dB	-0.15 dB
Net received power		-14.3 dBm	-22.3 dBm
Required receive power for 40 dB SNR		-33 dBm	
Link Margin		18.7 dB	10.7 dB

Note 1

The coupling loss from the Sweetspot emitter into the Bit Lite fibre can be estimated by the relation:

$$P_L = \frac{dA_f}{dA_s} \left(1 - \frac{dA_f}{dA_s}\right)$$

$$= \frac{100^2}{300^2} \left(1 - \frac{100^2}{300^2}\right)$$

$$= \frac{1}{9} \left(1 - \frac{1}{9}\right)$$

$$P_L \text{ (dB)} = -10.1 \text{ dB}$$

The exact form of the expression in parenthesis is dependent on the actual index of refraction profile of the fibre. The approximation given above has been found to give good agreement with measured results.

APPENDIX 4
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

MOTOROLA

MC3417, MC3517
MC3418, MC3518

Specifications and Applications Information

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

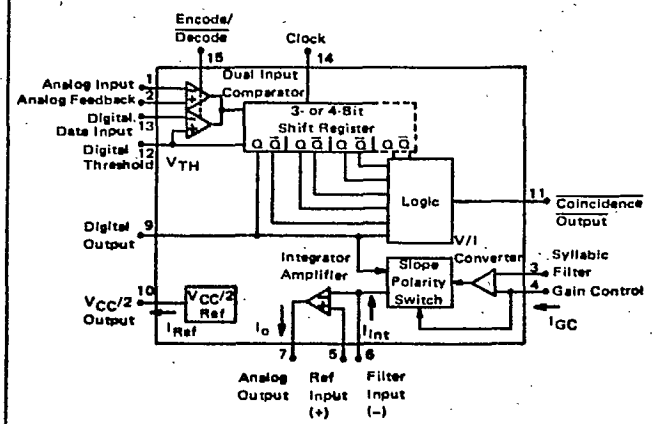
Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

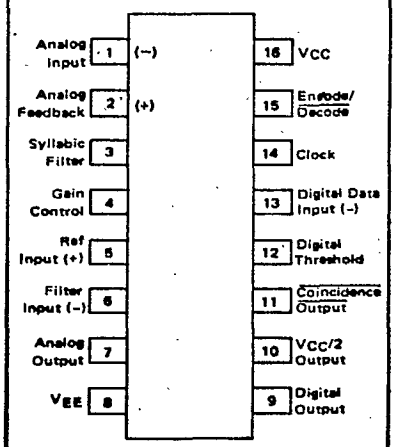
L SUFFIX
CERAMIC PACKAGE
CASE 620

6

CVSD BLOCK DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	V_{CC}/2 − 1.0 to V_{CC}	Vdc
V_{CC}/2 Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to +70°C for MC3417/18, T_A = −55°C to +125°C for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3.7	5.0	–	3.7	5.0	
(V_{CC} = 15 V)		–	6.0	10	–	6.0	10	
Clock Rate	SR	–	16 k	–	–	32 k	–	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.001	–	3.0	0.001	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ± 5.0 mA)	V_O	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							µA
Analog Input (I1)		–	0.5	1.5	–	0.25	1.0	
Analog Feedback (I2)		–	0.5	1.5	–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.5	–	0.06	0.3	
Reference Input (I5)		–	−0.06	−0.5	–	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							µA
Analog Input/Analog Feedback |I1−I2| — Figure 3		–	0.15	0.8	–	0.05	0.4	
Integrator Amplifier |I5−I6| — Figure 4		–	0.02	0.2	–	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	–	2.0	6.0	–	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	0.1	0.3	–	
Integrator Amplifier, 0 to ± 5.0 mA Load		1.0	10	–	1.0	10	–	
Propagation Delay Times (Note 1)								µs
Clock Trigger to Digital Output	t_{PLH}	–	1.0	2.5	–	1.0	2.5	
(C_L = 25 pF to Gnd)	t_{PHL}	–	0.8	2.5	–	0.8	2.5	
Clock Trigger to Coincidence Output	t_{PLH}	–	1.0	3.0	–	1.0	3.0	
(C_L = 25 pF to Gnd) (R_L = 4 kΩ to V_{CC})	t_{PHL}	–	0.8	2.0	–	0.8	2.0	
Coincidence Output Voltage — Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	–	0.12	0.25	–	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State (V_{OH} = 15.0 V, 0°C ≤ T_A ≤ 70°C)	$I_{OH(Con)}$	–	0.01	0.5	–	0.01	0.5	µA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

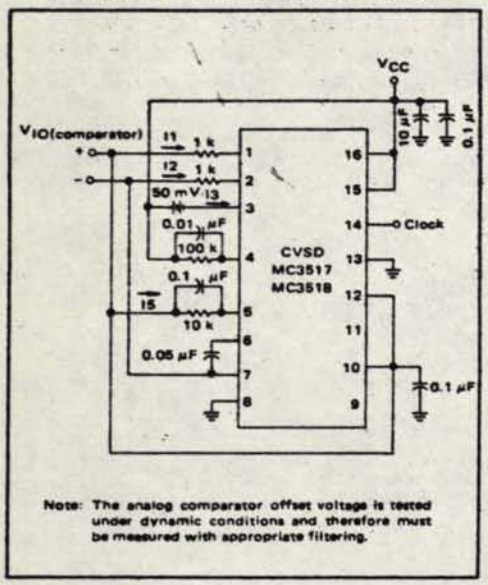
6

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	–	V_{CC} – 2.0	+1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current ($1.2\ V \le V_{th} \le V_{CC} - 2.0\ V$)	$I_{I(th)}$							μA
(V_{IL} applied to Pins 13, 14 and 15)		–	–	5.0	–	–	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		–	– 10	–50	–	–10	–50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	–	–	±5.0	–	–	mA
$V_{CC}/2$ Generator Maximum Output Current (Source only)	I_{Ref}	+10	–	–	+10	–	–	mA
$V_{CC}/2$ Generator Output Impedance (0 to +10 mA)	z_{Ref}	–	3.0	6.0	–	3.0	6.0	Ω
$V_{CC}/2$ Generator Tolerance ($4.75\ V \le V_{CC} \le 16.5\ V$)	e_r	–	–	±3.5	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	–	V_{th} – 0.4	Gnd	–	V_{th} – 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	–	18.0	V_{th} + 0.4	–	18.0	
Dynamic Total Loop Offset Voltage (Note 2) – Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12.0 μA, V_{CC} = 12 V								
T_A = 25°C		–	–	–	–	± 0.5	± 1.5	
0°C ≤ T_A ≤ +70°C MC3417/18		–	–	–	–	± 0.75	± 2.3	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	–	–	–	± 1.5	± 4.0	
I_{GC} = 33.0 μA, V_{CC} = 12 V								
T_A = 25°C		–	± 2.5	± 5.0	–	–	–	
0°C ≤ T_A ≤ +70°C MC3417/18		–	± 3.0	± 7.5	–	–	–	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	±4.5	±10	–	–	–	
I_{GC} = 12.0 μA, V_{CC} = 5.0 V								
T_A = 25°C		–	–	–	–	± 1.0	± 2.0	
0°C ≤ T_A ≤ +70°C MC3417/18		–	–	–	–	± 1.3	± 2.8	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	–	–	–	± 2.5	± 5.0	
I_{GC} = 33.0 μA, V_{CC} = 5.0 V								
T_A = 25°C		–	± 4.0	± 6.0	–	–	–	
0°C ≤ T_A ≤ +70°C MC3417/18		–	± 4.5	± 8.0	–	–	–	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	± 5.5	± 10	–	–	–	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{OH} = –0.35 mA)	V_{OH}	V_{CC} – 1.0	V_{CC} – 0.2	–	V_{CC} – 1.0	V_{CC} – 0.2	–	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	–	V_{CC}	+3.2	–	V_{CC}	Vdc
Integrating Current (Figure 2)	$i_{I(Int)}$							
(I_{GC} = 12.0 μA)		8.0	10	12	8.0	10	12	μA
(I_{GC} = 1.5 mA)		1.45	1.50	1.55	1.45	1.50	1.55	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$	–	± 100	± 250	–	± 100	± 250	mV
Input Current – High Logic State (V_{IH} = 18 V)	I_{IH}							μA
Digital Data Input		–	–	+5.0	–	–	+5.0	
Clock Input		–	–	+5.0	–	–	+5.0	
Encode/Decode Input		–	–	+5.0	–	–	+5.0	
Input Current – Low Logic State (V_{IL} = 0 V)	I_{IL}							μA
Digital Data Input		–	–	–10	–	–	–10	
Clock Input		–	–	–360	–	–	–360	
Encode/Decode Input		–	–	–36	–	–	–36	
Clock Input, V_{IL} = 0.4 V		–	–	–72	–	–	–72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

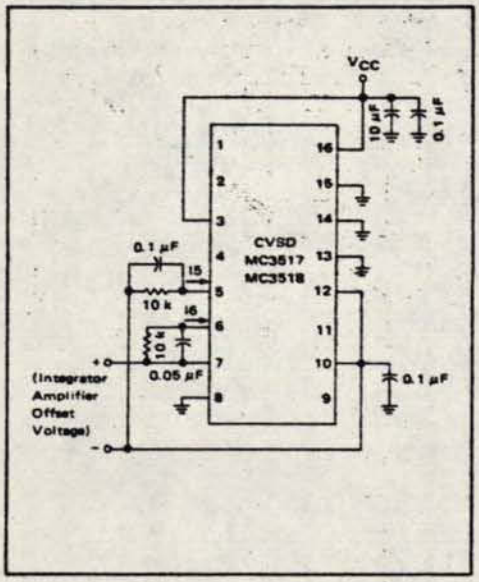
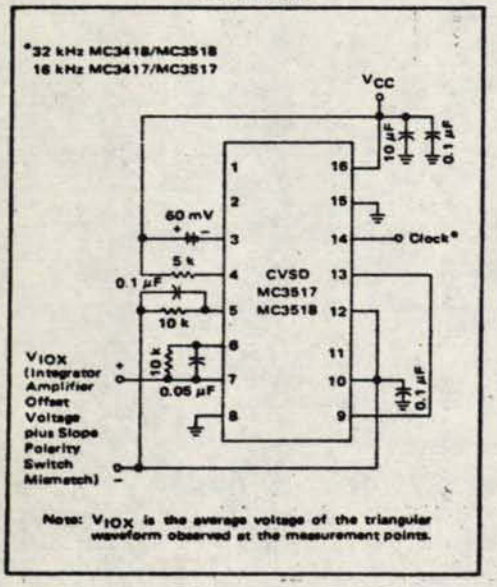
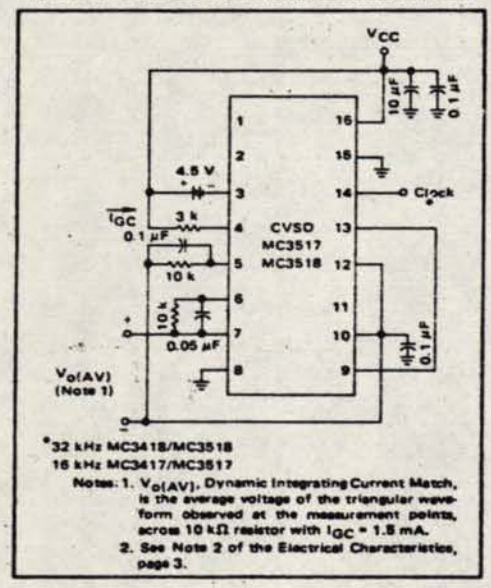


FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH



*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{o(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, page 3.

6

TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

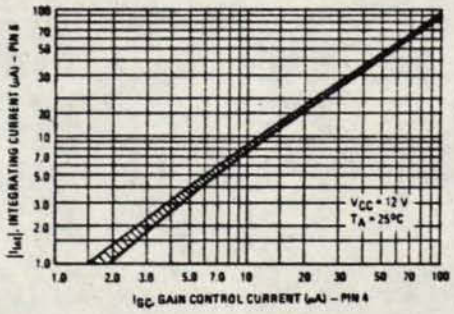


FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

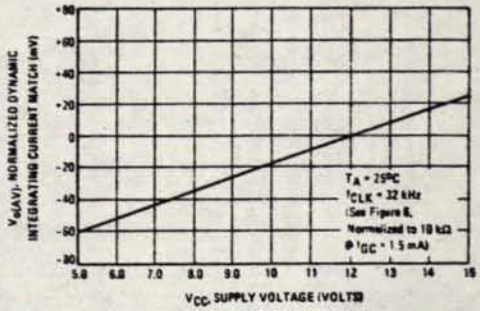


FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

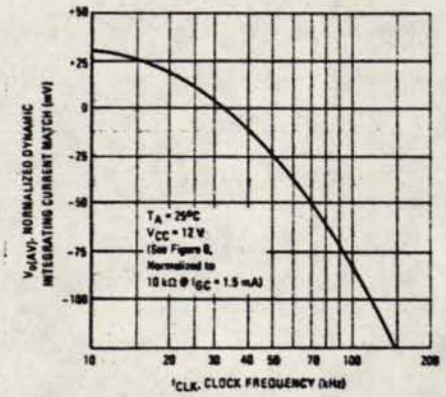


FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

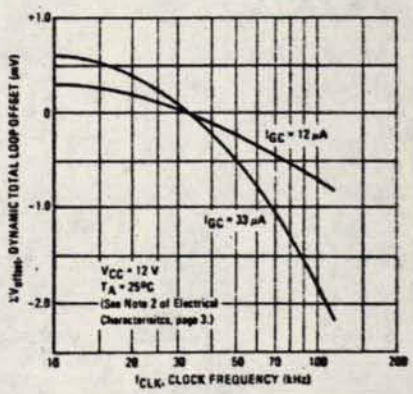


FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER

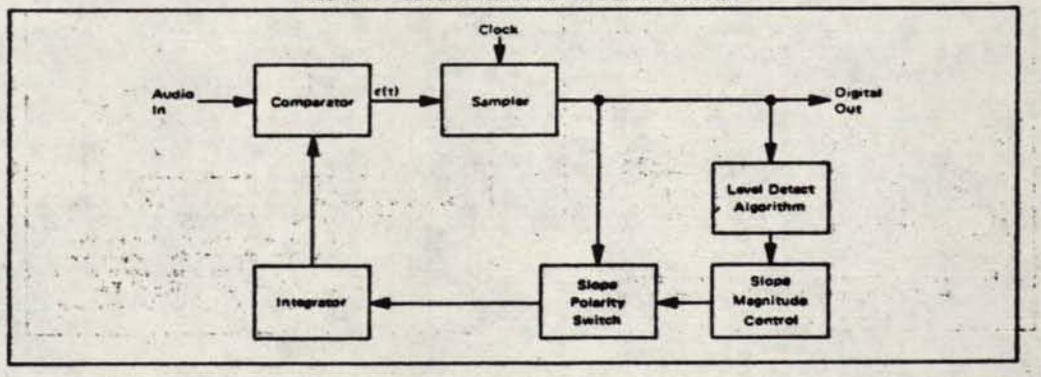


FIGURE 12 – CVSD WAVEFORMS

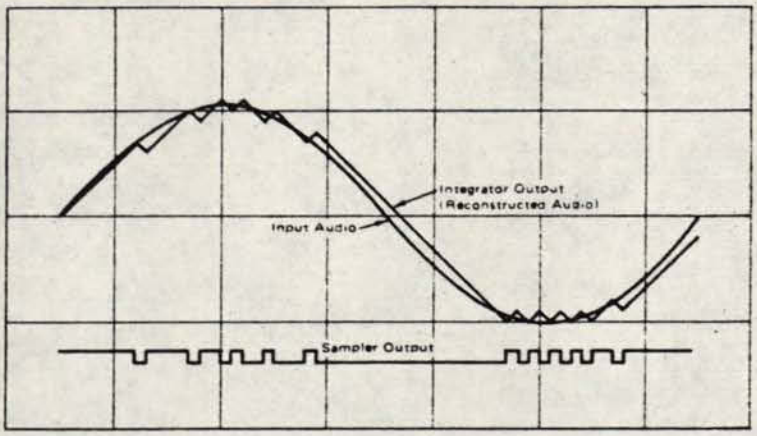
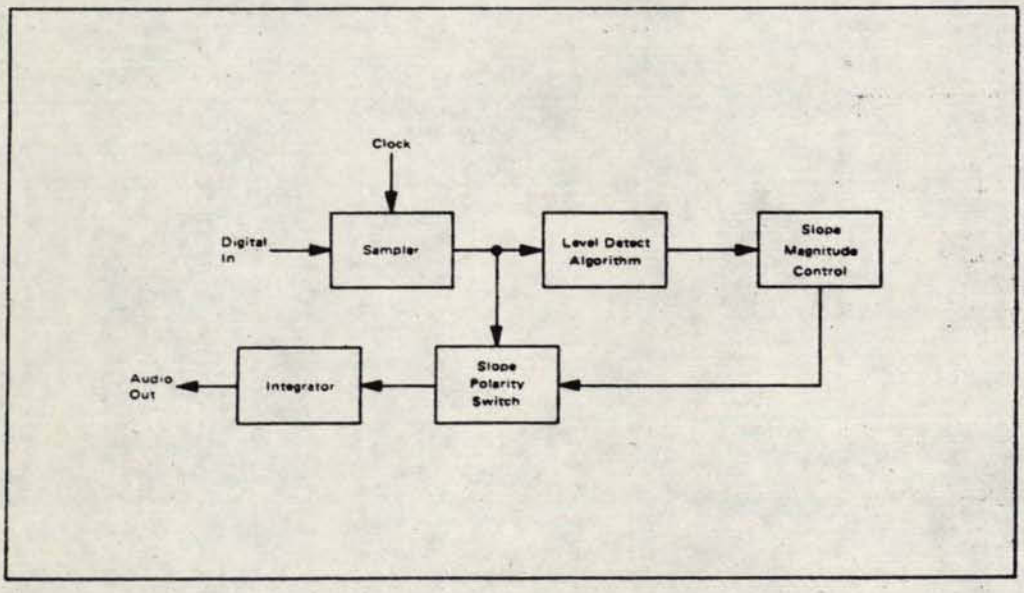


FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER



APPENDIX 5
CONTRACTOR REPORT ON A CROWN CONTRACT DEVELOPMENT

Contractor report of a development made under Crown contract containing supplementary conditions DSS1036.

Information furnished by:

1. Name: P.C. Wheeler

2. Address: 1794 Courtwood Crescent, Ottawa Ontario K2C 2B5

3. Nationality: Canadian citizen

4. Organization: Foundation Electronic Instruments Inc.

5. Telephone Number: (613) 226-4000

6. a) Problem: as per Appendix 'A', Statement of Work DSS File Number 12ST.3200313 and DSS Serial Number 2ST81-00032
   b) How Accomplished: as above
   c) Present Limitations: as above
   d) Proposal: as above
   e) Novel: the application of fibre-optics is edge of the art technology in the Military Land Tactical Environment.

7. Financing: Much was financed by the Crown except for existing optical transmitter/receiver and signal processing circuitry presently designed and proprietary to Foundation Electronic Instruments Inc.

8. References: Since 1981, this subject has been addressed at Fibre-Optic Conferences and in fibre-optic magazines as a result of research work with various telecommunication organizations.

9. Publication: Feature article in the CEE magazine, May issue.

10. Deliverables: Two complete systems exist and are available for testing and demonstration.

11. Photographs and Slides: These are available from the Scientific Authority or Foundation Electronic Instruments Inc.

12. Continued Work: Work will continue if there exists outside research funding.

13. Journal or Society Presentation: Possibly at the IEEE Communications Conference, Toronto Canada, September 1983.

14. Use: Military Land Tactical Systems using the CX4566 A/G cable assembly.

APPENDIX "B"

REQUIREMENTS FOR COMPLETION AND DISPOSITION OF REPORTS OF DEVELOPMENTS MADE UNDER CROWN CONTRACTS CONTAINING SUPPLEMENTARY CONDITIONS DSS 1036 OR DSS 1053

(1) The submission of reports of developments by Crown Contractor personnel shall be in the form of a "Report of a Development Made Under Crown Contract" as set out in the following Parts I, II and III hereunder, or as may be amended from time to time.

(2) Such reports are to be routed to the addressees specified in the contract, only via the person designated by the Contractor to be responsible for reporting developments under the contract.

(3) When requested to do so by the Crown, the Contractor shall

(a) provide, as best it reasonably can in the circumstances prevailing at the time, technical and other assistance for the preparation and prosecution of patent applications and other protection of proprietary interests which may be filed in respect of developments reported under the DSS contract;

(b) obtain, at the expense of the Crown to the extent necessary, the execution of all documents required for patent applications or other protection of proprietary interests; and

(c) obtain, at the expense of the Crown to the extent necessary, the requisite documents for transfer to the Crown of all right, title and interest in and to any such development.

CONTRACTOR REPORT OF A DEVELOPMENT MADE UNDER CROWN CONTRACT CONTAINING SUPPLEMENTARY CONDITIONS DSS 1036 OR DSS 1053

PART I

The information to be furnished by the individual(s) directly involved in the development.

1. Name(s) of Individual(s);

2. Address(es): Residence; Business (if now different from 4 or 5 below);

3. Nationality of such individual(s);

4. Organization, section and department where employed;

5. Position(s), building(s), telephone number(s);

6. Brief description and drawings where necessary, of the proposal under the following headings:

(a) what is the problem?

(b) how may it be accomplished according to present knowledge?

(c) limitation or drawbacks of present apparatus, product or process?

(d) what is the proposal?

(e) what is thought to be novel in the proposal?

.../2

7. Was this made as a result of research or development wholly financed by the Crown? If not, give name(s) of other financial participant(s).

8. Provide references in published literature or patents relating to the problem or subject, to the extent feasible.

9. Has any publication or disclosure to others been made? If so, specify.

10. Has the apparatus, product or process been made or tested? If yes, does a sample or model exist? If so, has it been preserved, and can it be made available for demonstration purposes?

11. Are photographs (prints, slides, stereos, motion pictures) available? If so, specify.

12. Will there be continued work towards improving the apparatus, product or process?

13. Is there within the next six (6) months a possibility of a meeting of a learned society or deadline or publication of a scientific journal at which this development may be disclosed?

14. Where might this apparatus, product or process have use? Please elaborate where possible.

1794 Courtwood Cr.

PLACE Ottawa Ontario DATE April 15/83

SIGNATURE

NOTES:

(1) If the Crown decides to protect rights in the development by filing a patent application, the appropriate assignment form will be forwarded for execution by the individual(s) named herein.

(2) Copies of this form to be made up locally using such spacings between components as desired or, alternatively, recording the answers on a separate sheet of paper and numbering them to correspond to the questions on this form.

PART II

Comments on the answers contained in Part I to be completed by Contractor supervisory personnel, e.g. section, departmental or functional head of individual(s) concerned, or a contract administrator.

DATE (Signature(s))

Name and Appointment

Telephone Number

.../3

DSS FILE NO. 12ST.3200313
DSS SERIAL NO. 2ST81-00032

To be completed with copies of Part I and to be forwarded to the following:

(a) Science Procurement Manager or Engineering Procurement Officers named in the contract;

(b) Scientific Authority or Design Authority/Technical Authority named in the contract; and

(c) Director Patent Administration
National Defence Headquarters
Department of National Defence
101 Colonel By Drive
Ottawa, Ontario.
K1A 0K2

PART III

DSS FILE NO._____

DSS CONTRACT NO._____

To be completed by the person designated by the Contractor to be responsible for reporting developments under the contract, with copies of Part I and to be forwarded to the following:

(a) Science Procurement Manager or Engineering Procurement Officers named in the contract;

(b) Scientific Authority or Design Authority/Technical Authority named in the contract; and

(c) Director Patent Administration
National Defence Headquarters
Department of National Defence
101 Colonel By Drive
Ottawa, Ontario.
K1A 0K2

The development reported on the accompanying Part I of this form by:

Peter C. Wheeler
Name of Individual(s)

Foundation Electronics Instruments Inc.
Name of Organization

and dated April 15 1983 is being forwarded for consideration and assessment with a view to protecting and exploiting the Crown's rights therein.

DATE: April 15 1983 P. Wheeler
(Signature)

P.C. WHEELER
(Name)

VICE-PRESIDENT
(Appointment)
OPERATIONS

To be accompanied by signed copies of Part I and Part II if applicable.

APPENDIX 6
DOCUMENTATION CHECKLIST

DATA LIST	FI	FOUNDATION INSTRUMENTS OTTAWA				DWG NO. 2425	REV.
APPROVAL	CONTRACT NO. 810113	CONTRACT CANADIAN LAND TACTICAL				SHEET 1 OF 3	DATE
CODE IDENT.	DWG. SIZE	DWG NO.	SHEET NO	REV.	TITLE	DESCRIPTION	RELEASE DATE
	C	1828			FOTX MODULE	SCHEMATIC	
		1829		B	" "	ARTWORK	
	C	1830			" "	COMP. LAY	
	C	1831			" "	MASTER	
	C	1833		A	FIBER CABLE WATERPROOF BUSHING	MECH.	
	C	1861		C	TX HEAT SINK	MECH.	
OBSOLETE	C	1873			TACTICAL LINK CV/SDM	SCHEM.	
	C	2020			CONNECTOR MTNG BRKT.	MECH.	
		2021			PROTOTYPE PCB	ARTWORK	
	D	2022			EXTENDER FLANGE	MECH.	
		2023		A	EXTENDER PCB	ARTWORK	
	C	2024			EXTENDER PCB	MASTER	
OBSOLETE	C	2025			PROTOTYPE PCB	MASTER	
	D	2201		E	PSK DATA & VIDEO TX	SCHEMATIC	
		2202		B	PSK DATA & VIDEO TX	ARTWORK	
	D	2203		A	PSK DATA & VIDEO TX	COMP. LAY	
	C	2204			PSK DATA & VIDEO TX	MASTER	
	D	2205		D	DATA MULTIPLEXER	SCHEMATIC	
		2206		A	DATA MULTIPLEXER	ARTWORK	
	D	2207		A	DATA MULTIPLEXER	COMP. LAY.	
	C	2208			DATA MULTIPLEXER	MASTER	
	D	2209		B	PSK DATA & VIDEO SEPARATOR	SCHEMATIC	
		2210		B	PSK DATA & VIDEO SEPARATOR	ARTWORK	
	D	2211			PSK DATA & VIDEO SEPARATOR	COMP. LAY	

DATA LIST	FI	FOUNDATION INSTRUMENTS OTTAWA			DWG NO. 2425	REV.
APPROVAL	CONTRACT NO. 810113	CONTRACT. CANADIAN LAND TACTICAL			SHEET 2 OF 3	DATE
CODE IDENT.	DWG. SIZE / DWG NO.	SHEET NO	REV.	TITLE	DESCRIPTION	RELEASE DATE
	C 2212			PSK DATA & VIDEO SEPARATOR	MASTER	
	D 2213		F	DESCRAMBLER & "F" BIT RECOVERY	SCHEMATIC	
	2214		A	DESCRAMBLER & "F" BIT RECOVERY	ARTWORK	
	D 2215		B	DESCRAMBLER & "F" BIT RECOVERY	COMP. LAY.	
	C 2216			DESCRAMBLER & "F" BIT RECOVERY	MASTER	
	D 2217			PSK DATA RECOVERY	SCHEMATIC	
	2218		B	PSK DATA RECOVERY	ARTWORK	
	D 2219	1		PSK DATA RECOVERY	COMP. LAY.	
	" "	2		" " "	" "	
	C 2220			PSK DATA RECOVERY	MASTER	
	D 2221		E	DATA DEMULTIPLEXER	SCHEMATIC	
	2222		B	DATA DEMULTIPLEXER	ARTWORK	
	D 2223		B	DATA DEMULTIPLEXER	COMP. LAY.	
	C 2224			DATA DEMULTIPLEXER	MASTER	
	C 2334			GROUND PLATES	MECH.	
	D 2385	1		DUPLEX TX VOICE CIRCUIT	SCHEMATIC	
	" "	2		" " " "	"	
	" "	3		" " " "	"	
	" "	4		" " " "	"	
	" "	5		" " " "	"	
	" "	6		" " " "	"	
	2386		A	DUPLEX TX VOICE CIRCUIT	ARTWORK	
	C 2387	1		DUPLEX TX VOICE CIRCUIT	COMP. LAY.	
	" "	2		" " " "	"	

DATA LIST	FI	FOUNDATION INSTRUMENTS OTTAWA			DWG NO. 2425	REV.
APPROVAL	CONTRACT NO.	CONTRACT CANADIAN LAND TACTICAL			SHEET 3 OF 3	DATE

CODE IDENT.	DWG. SIZE	DWG NO.	SHEET NO	REV.	TITLE	DESCRIPTION	RELEASE DATE
	C	2388			DUPLEX TX VOICE CIRCUIT	MASTER	
	D	2389			FO/RX SHIELD	MECH.	
	A	2423			WIRING (PARTIAL)	LIST	
	A	2425			CDN LAND TACTICAL	DATA LIST	
	A	2426			F/O RX MODULE	SCHEMATIC	
		2427		A	F/O RX MODULE	ARTWORK	
	C	2428			F/O RX MODULE	COMP. LAY.	
	C	2429			F/O RX MODULE	MASTER	
		2431			AUDIO INTERFACE - 4 WIRE	ARTWORK	
	C	2432			AUDIO INTERFACE - 4 WIRE	COMP. LAY.	
	C	2433			AUDIO INTERFACE - 4 WIRE	MASTER	
		2435			AUDIO INTERFACE - 2 WIRE	ARTWORK	
	C	2436			AUDIO INTERFACE - 2 WIRE	COMP. LAY.	
	C	2437			AUDIO INTERFACE - 2 WIRE	MASTER	
	D	2447			BACK PLANE WIRING	DIAGRAM	
OBSOLETE	C	2515		B	CDN LAND TACTICAL TX/RX	SCHEMATIC	
OBSOLETE	C	2516			CDN LAND TACTICAL TX/RX	ARTWORK	
OBSOLETE	C	2518			CDN LAND TACTICAL TX/RX	MASTER	
	C	2588			POWER SUPPLY	SCHEMATIC	
	C	2589			POWER SUPPLY	PARTS LIST	
	D	1710		A	SYSTEM BLOCK DIAGRAM	DIAGRAM	