CRC Copy #3

DEVELOPMENT OF FFSK MODEM MICROCIRCUIT MODULES

PRELIMINARY REPORT

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SUMMARY

This report describes the work done by Bell-Northern Research in the development of a manufacturable FFSK modem as contracted by CRC. The design prior to this study is described briefly and then a detailed account of its evolution into the present design is given. It is concluded that the integrated circuit (IC) implementation of this design is expected to meet all the required performance criteria, and commencement of the IC layout is recommended.

1.0 INTRODUCTION

The purpose of this report is to describe the work done by BNR and, in part, by Canadian General Electric (CGE) in developing a manufacturable FFSK modem design.

The work, described in CRC Specification DSRD-MC-06, consisted of specific tasks some of which were assigned to BNR and some to CGE. The end result is a general specification for an LSI implementation.

Section 1.1 of this report describes the modem design that was generated by previous contracts with CRC. Section 1.2 outlines the specifc tasks contracted by BNR and CGE to develop a new modem design. Sections 2.1 and 2.2 describe in detail the evolution of this design, and in section 2.3 the results of the breadboard implementation are given. Section 3 concludes the report and gives recommendations for the microcircuit implementation. The last section lists differences between the CRC specification, cited above, and the final modem design.

The electrical schematics generated by this work have been included in the Appendices.

1.1 SUMMARY OF PREVIOUS CONTRACT WORK

Previous to the current contract, studies were undertaken to determine the feasibility of integrating an FFSK modem in a Large Scale Integrated (LSI) circuit. BNR concluded that while most of the modem functions were easily integrated, and some were integratable conditionally, some functions were not integratable (i.e. would not achieve desired specifications).

A block diagram of the modem circuit designed in the previous studies is shown in Figure 1. The detailed schematic is given in Reference 1.

For reference purposes, a brief description of each block (in Figure 1) will be given, with some of the problems encountered.

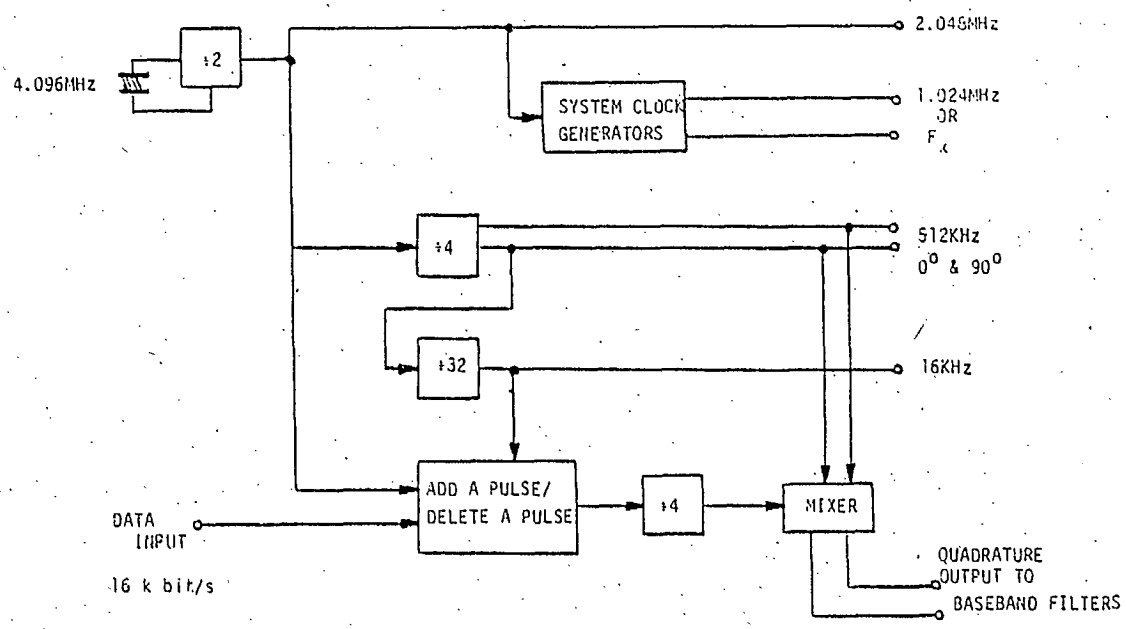
1.1.1 Modulator

System clocks were generated using a 4.096 MHz oscillator and cascaded divide-by-two stages. The phase of the output signal was controlled by an add-a-pulse/delete-a-pulse circuit and a mixer. In-phase and quadrature (I and Q) outputs were provided for off-chip baseband filtering and subsequent mixing with a high frequency IF oscillator output. There were no significant problems with this circuit.

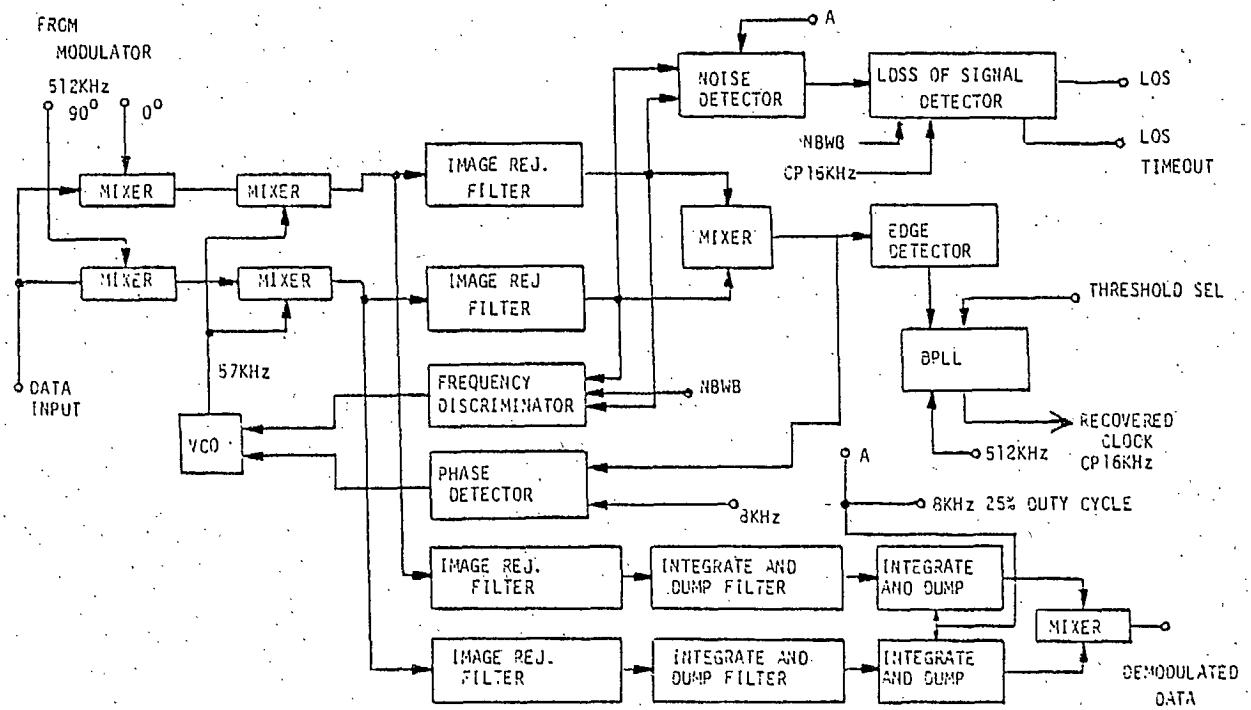
1.1.2 Demodulator

Translation of the received signal from the 455 kHz IF to baseband I and Q channels was accomplished with two pairs of mixers, one pair at 512 kHz (generated on-chip) and the second at 57 kHz (generated by the VCO). The latter drove two pairs of image rejection filters: one pair were used by integrate-and-dump filters to derive the data stream, and the other pair were used by the data edge detector and the noise detector. A digital phase lock loop (DPLL) recovered the 16 kHz clock from the data edge pulses and the 512 kHz reference clock. A loss-of-signal (LOS) detector compared the noise detector output to the recovered 16 kHz to determine presence of the FFSK signal and could be used to control the mode of operation.

The carrier phase lock loop, consisted of a frequency discriminator, a phase detector, and a voltage controlled oscillator (VCO), and required ten



MODULATOR



DEMODULATOR

Figure 1. Block Diagram of Previous LSI Design

connections (pads) between the proposed LSI chip and external passive components. Some problems were encountered in the three-state output devices required, and temperature instability was found to be excessive.

The image rejection filters comprised several cascaded RC sections. Their operation caused problems until the characteristics of the interfacing Exclusive OR gate mixers and inverters were well understood. The performance improved greatly when the inverters were replaced by comparators and the EXOR gates were buffered. Comparators were also used in the integrate-and-dump circuitry. The reference voltage ($V_{DD}/2$) for these four comparators was derived using a resistive divider across the power supply.

The outputs of the two integrate-and-dump circuits were then mixed together with the 8 kHz recovered clock (using EXOR gates) to yield the output data.

The edge detector used could only transmit edge information synchronously with the 512 kHz clock. This caused an average delay of one microsecond for the recovered 16 kHz clock, which was not a serious problem for a 16 kBaud data rate (5.6° phase error).

The DPLL consisted of an up/down binary counter, count decoding logic, a binary ripple counter, more count decoding logic, and various count inhibit, counter reset and analog delay circuits. Problems were encountered (particularly in the breadboard version of the circuit) in using the decoded outputs to reset their respective counters. As well, the analog delays were quite dependent on the power supply voltage, which caused the phase error to be voltage dependent.

The LOS detector was implemented easily, with two parallel binary counters, decoding logic, an LOS flip-flop and a pulse expander utilizing analog delay to ensure a minimum width reset pulse.

Provision was made for selecting various threshold options, and an LOS time-out counter with several delay options was also included. The input to one of the binary counters was the output of the noise detector circuit, and the other counter's input was the recovered 16 kHz clock.

1.2 SUMMARY OF CONTRACT TASKS

Contract work consisted of sub-tasks, which were assigned to CGE, and tasks which were assigned to BNR.

The sub-tasks provided for:

(1) the re-design of sections of the existing modem design

(2) generation of design information required by BNR to evaluate and modify the new design,

(3) evaluation of the new modem breadboard built by BNR.

More specifically, a new, single, down-conversion stage for the FFSK demodulator input, and frequency and phase discriminators for a new VCO (the VCO was designed in a separate contract between CRC and CGE) were to be designed; the DPLL was to be modified to eliminate decoding "glitches"; a new modulator design and detailed chip input/output specifications were to be provided to BNR; and finally, the BNR-built breadboard was to be evaluated.

BNR was required, in task 1, to evaluate and modify if necessary the new modulator design. This included digital simulations to verify timing relationships, and analog simulations to estimate the frequency response of the analog outputs. Task 2 involved evaluation of the demodulator which included simulation and modification of a new DPLL, and re-design to eliminate analog delays. Both tasks required the implementation of the modem in breadboard form, and the development of an automated test procedure which could be used for the microcircuit version.

This report fulfills the requirements of Task 3. A General Specification of the FFSK modem chip will be submitted by BNR at a later date to complete Task 4.

2. THE DESIGN OF A NEW FFSK MODEM

The FFSK modem design prior to this contract has now been described. Under the tasks defined in section 1.2 the circuit was redesigned by CGE and BNR to yield a manufacturable high performance 16 kBaud modem, for which simulations show that a 64 kBaud data rate is feasible. Its design will be described in detail in the following sections. A block diagram of the new circuit is shown in Figure 2 and the detailed schematics are given in Appendices 1 and 2.

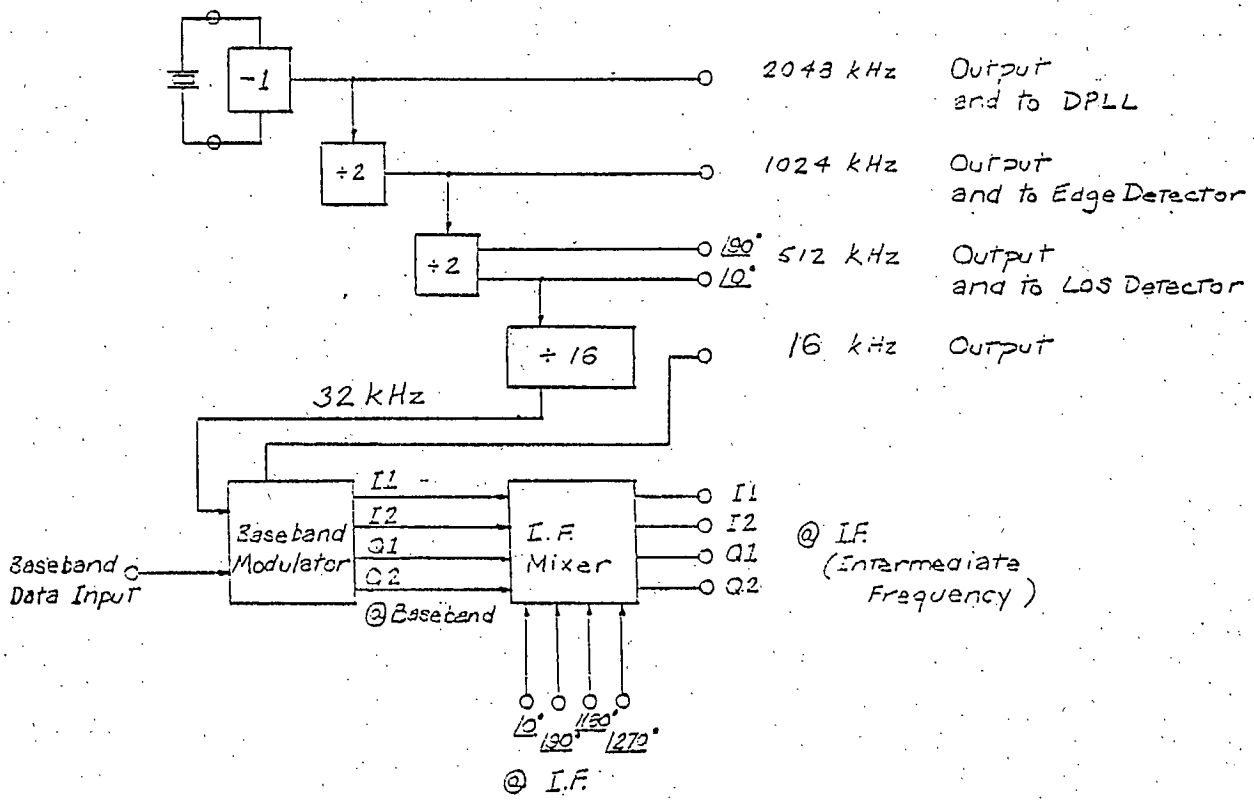
2.1 MODULATOR

The add-a-pulse/delete-a-pulse modulator analyzed in the previous study [1] was found to be entirely satisfactory for a 16 kBaud data rate but performance was degraded for a 64 kBaud rate. To allow the higher baud rate as an option, CGE designed at CRC's request, a new modulator with several versions. The versions differed in the number of summing resistors required (4 or 6) and the use of D-type flip-flops for delay equalization, which allowed for data rates in excess of 64 kBaud. [2]

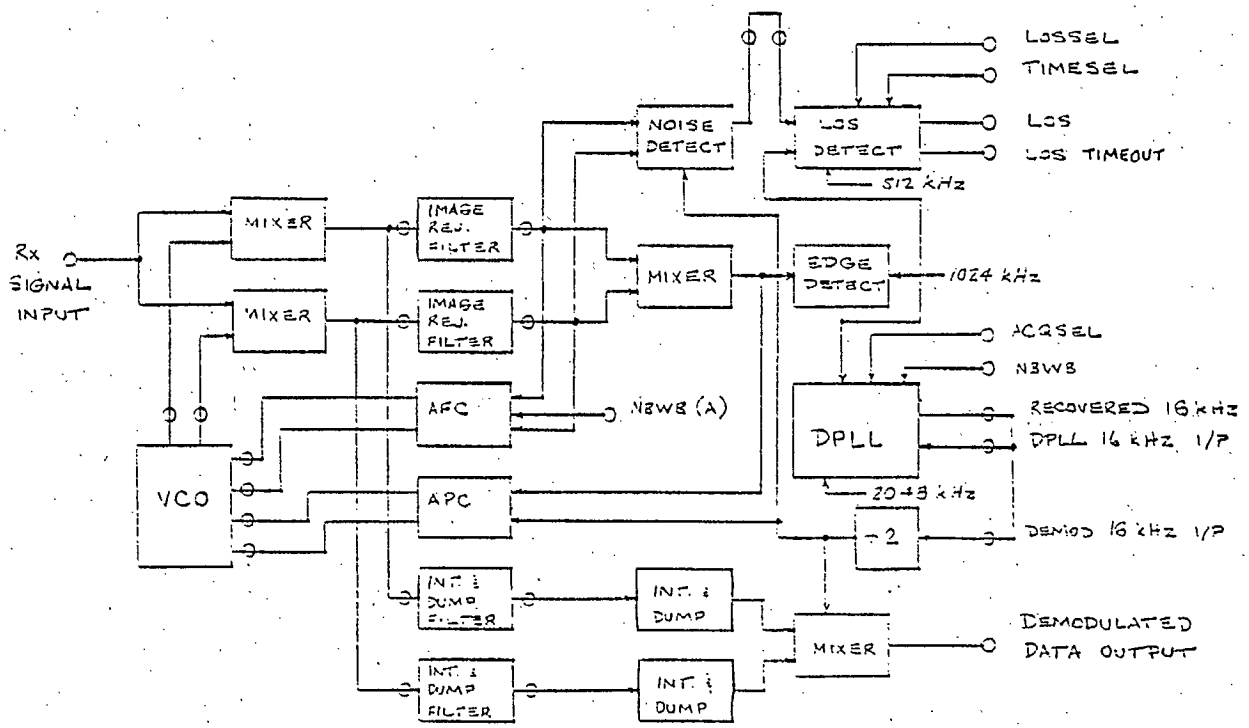
Computer simulation of the circuit operation by BNR revealed the generation of output "glitches" in the six-resistor version but not in the four-resistor version [3]. Also, the four resistor version required significantly less chip area, and thus was chosen as the best option.

Subsequently, CGE suggested the addition of transmission gates at the output, to provide on-chip mixing with an HF carrier. It was noted that no additional risk was incurred by incorporating the gates since DC voltages could be connected at the carrier inputs and mixing could then be accomplished off-chip.

Analog simulations of the standard BNR CMOS II transmission gates revealed that although the gates give a frequency range equal to that of a 4016 gate, the channel ON resistance was very dependent on the DC level of the signal. Simulation of a modified BNR transmission gate design, similar to that of a Fairchild 4066 gate, showed that a much lower channel resistance over the entire voltage range was possible. The frequency response of the unloaded



MODULATOR



DEMODULATOR

Figure 2. Block Diagram of the New LSI Design

gate is shown in Figure 3.

The use of off-chip summing resistors was chosen over integrated resistors for two reasons: resistance accuracy (i.e. laser trimming of hybrid resistors gives < 1% error vs integrated resistors have up to 5% error); lower risk (i.e. high frequency mixing on-chip may affect other chip circuitry).

Automatic testing of the modulator can be accomplished easily because of the small number of states and the large number of outputs.

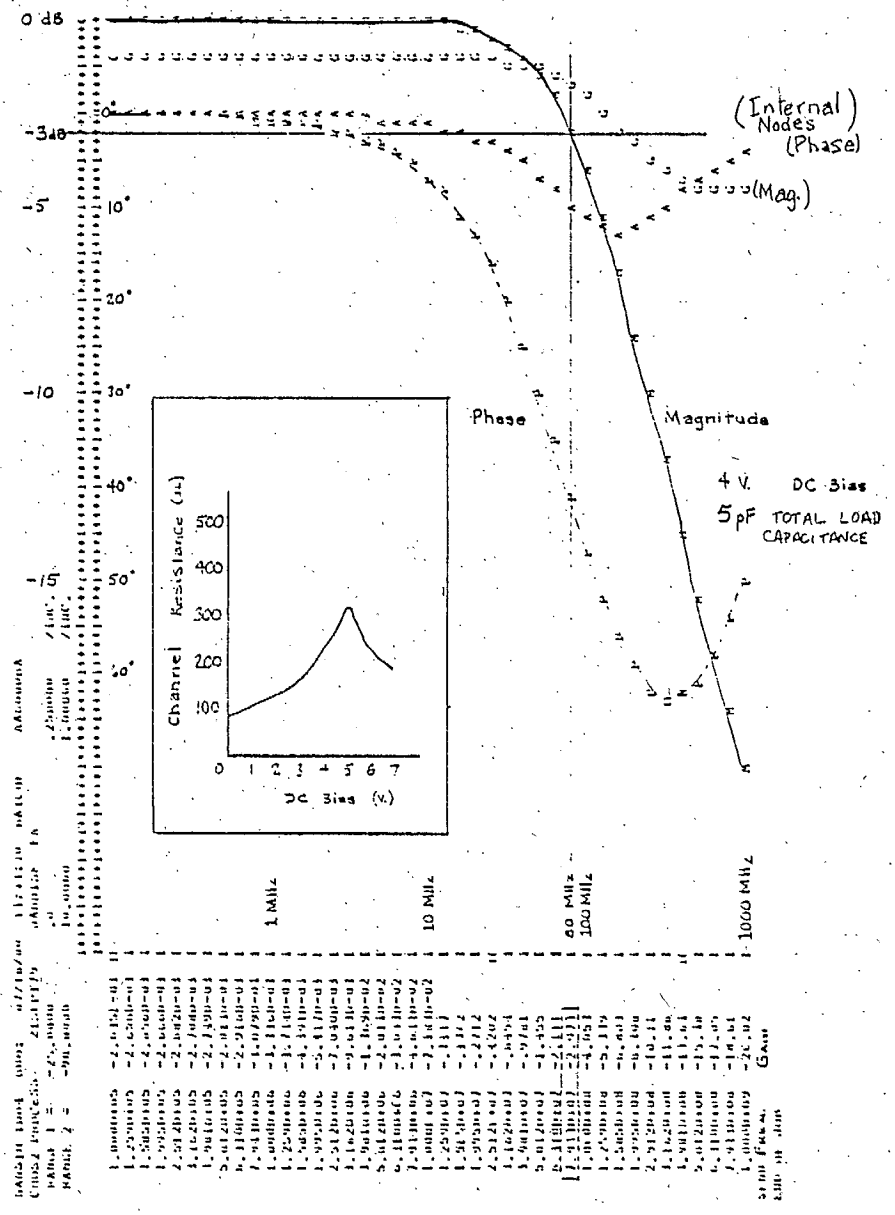


Figure 3. Computer Simulation of Frequency Response of BNR Transmission Gates

2.2 DEMODULATOR

2.2.1 Input Signal Buffers

Buffering of the low level VCO output signals and the received IF signal, to provide square waves to the mixers, can be accomplished by capacitively coupling the signal to an inverter input which is resistively coupled either to its output, or to a common reference voltage.

The first method has a very low input impedance, ($< 10\,\Omega$) at its switching point, due to negative feedback, but has a very high gain. This impedance increases greatly as soon as the inverter output goes to the high or low logic state. An advantage of this approach is the insensitivity of the switching point to process variations.

The second approach has a constant high input impedance but the reference voltage required must be equal to the switching threshold voltage of the inverter. It could be obtained using a "phantom ground": an inverter whose input is connected to its output. If the signal inverter and the reference inverter are located physically close to one another and have the same orientation their switching thresholds should be equal to within 20 mV. This inaccuracy causes phase error of less than 3° (opposite errors for rising and falling edges). CGE has stated that both circuits were found to work equally well. The BNR breadboard was constructed using the "phantom ground" approach but recommends the former approach for LSI implementation for lower power consumption (fewer inverters) and less error.

2.2.2 The Mixers and the VCO

Conversion of the received signal to baseband is accomplished in the present design by one pair of EXOR gates, instead of two as in the previous design. The VCO centre frequency has been changed to 455 kHz (from 57 kHz) to allow the use of a ceramic resonator. CGE claims that this design greatly improves temperature stability and sensitivity to power supply changes.
The higher mixing frequency also relaxes the bandwidth requirement of the image rejection filters since the separation, in frequency, between the baseband signal and its image is greatly increased. When implemented in hybrid technology the resistors of the image rejection filters could be trimmed to obtain the necessary -3 dB frequency. This method would take

into account the output impedance of the mixer output buffers.

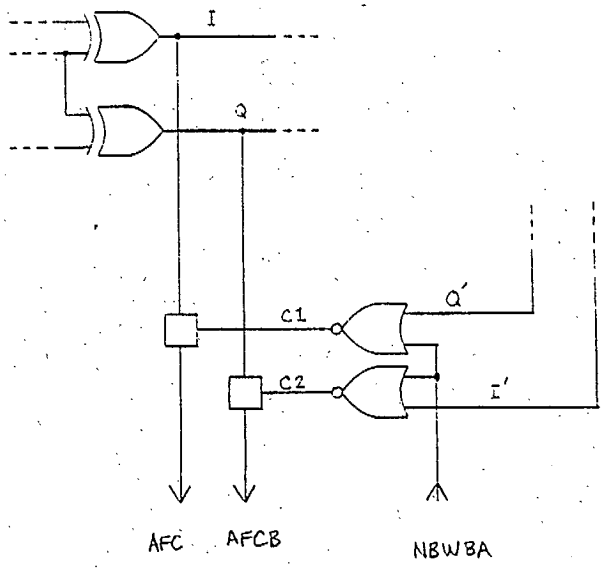
The automatic frequency control (AFC) signal and the phase control (APC) signal, for VCO control, are derived from the outputs of the comparators.

The AFC differential voltage is obtained by effectively multiplying each data stream, I and Q, by a delayed version of the other. The circuit submitted by CGE to accomplish this is shown in Figure 4 with its logic table. As stated previously the BNR transmission gates have an impedance which is very dependent on signal voltage. To provide a low impedance output, a different AFC circuit was designed by BNR. As shown in Figure 5 the logic table for this circuit is the same as for the CGE designed circuit. The maximum output impedance has been reduced approximately from 8 KΩ to 200 Ω. Although CGE was at first reluctant to accept this circuit, no specific reasons were given. Breadboard tests have since confirmed functional equivalence of the two circuits. CGE has not given a description of the circuit's operation, which would aid further BNR analysis.

The APC voltage is generated by an EXOR phase comparator, the inputs of which are the output of the I/Q channel mixer EXOR gate and the recovered 8 kHz clock. In the original CGE design the differential APC voltage was generated by two EXOR gates: one connected as above and the other used the inverted 8 kHz clock. This arrangement ensured that the outputs of the two EXOR gates were exactly complementary. The design was later simplified by omitting the latter EXOR gate and using an inverter to obtain the complement. The delay through an LSI inverter is less than 5 nS.

2.2.3 Image Rejection Filters and Integrate-and-Dump

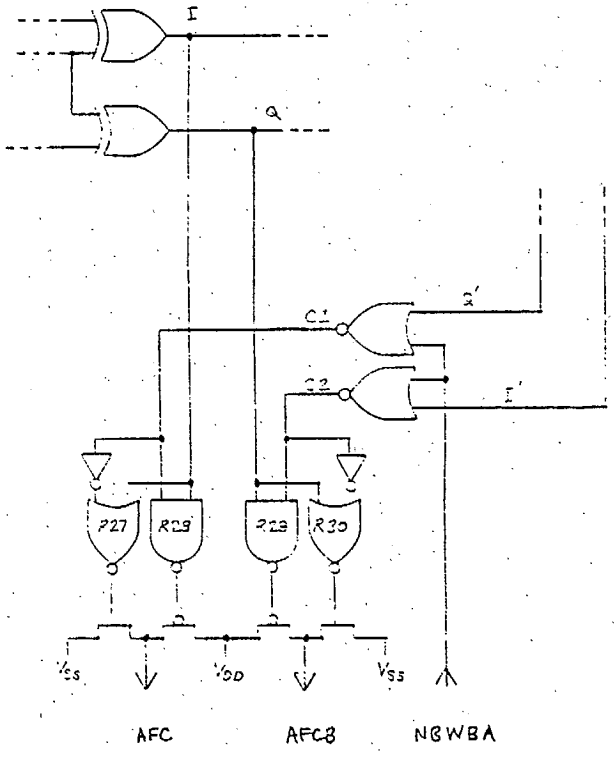
The image rejection filters have a -3 dB frequency of 30 kHz and provide data centered about $V_{DD}/2$ to the detection circuitry. To ensure a low bit error rate (BER) the detection threshold must be very close to this midpoint. The BNR comparators to be used have an offset voltage of less than 50 mV, which meets the requirements specified by CGE to cause less than 0.1 dB BER degradation [4].



	INPUTS				OUTPUTS	
NBWBA	I'	Q'	C1	C2	AFC	AFCB
0	0	0	1	1	I	Q
0	0	1	0	1	Z	Q
0	1	0	1	0	I	Z
0	1	1	0	0	Z	Z
1	X	X	0	0	Z	Z

X = don't care
Z = high impedance

Figure 4. CGE AFC circuit and logic table



	INPUTS								OUTPUTS	
NBWBA	I'	Q'	C1	C2	R27	R28	R29	R30	AFC	AFCB
0	0	0	1	1	1	1	0	0	I	Q
0	0	1	0	1	0	1	0	0	Z	Q
0	1	0	1	0	1	1	1	0	I	Z
0	1	1	0	0	0	1	1	0	Z	Z
1	X	X	0	0	0	1	1	0	Z	Z

X = don't care
Z = high impedance

Figure 5. BNR AFC circuit and logic table

Transmission gates, used to reset the integrate-and-dump capacitors, are controlled by a 25% duty-cycle clock. For a 16 kBaud data rate the reset time is 31.3 μS. The transmission gates have an impedance which is maximum at $V_{DD}/2$, The time constant at this voltage is approximately 8 kΩ x 620 pF = 5 μS. Thus, six time constants have been allowed for discharging the capacitors.

All four capacitors in the image rejection and I/D filters have been connected to V_{SS}. Measurements by CGE have shown that connecting the capacitors to the $V_{DD}/2$ reference voltage does not affect performance for the breadboard circuit. Both connections will be tested with the LSI version to verify this characteristic.

The demodulator circuitry used to generate the output data from the buffered I and Q data channels is the same as that designed in the previous contract, with the exception that data at the demodulator output is now non-inverted with respect to data at the modulator input (previously it was inverted).

2.2.4 Edge Detection

An edge detector with essentially 0° phase delay at 16 and 64 kBaud was designed by CGE to replace the previously used version. Analysis, by CGE previous to this contract, had shown that non-zero phase delay degraded the BER of the demodulator. One potential problem with this new edge detector is its ability to transfer noise spikes at its input through to its output, into the DPLL and LOS detector. It is expected, though, that all high frequency noise will have been greatly attenuated by the image rejection filters, prior to edge detection.

The edge detector in previous studies was clocked using 512 kHz. The new (CGE) design also used this clock frequency, but the new DPLL was changed to use 2048 kHz. Computer simulations revealed a new incompatibility between these two circuits arising from this difference. It was found that when the rising edge of an edge pulse was received by the DPLL (let us assume number two pulse for N = 2) it caused a reset pulse to be generated which was shorter than the edge pulse. This meant that after the up/down counter had reset, the falling edge of the same edge pulse clocked the counter again - incorrectly

registering a count of "one".

The problem was solved by using 1024 kHz to clock the edge detector.

2.2.5 The DPLL

The final LSI design previously submitted to CRC by BNR was free of any "glitch" or race problems according to computer simulations, however, the initial breadboard implementation did not corroborate this conclusion. Detailed experimentation with the breadboard revealed that all problems were dependent on which manufacturer's CMOS chips were used and therefore on delay. But the delay characteristics of MSI gates are quite different to those of LSI gates, whose propagation delays can be two orders of magnitude shorter. It was finally concluded that although the BNR DPLL design would perform well in an LSI implementation, a new, simpler, CGE designed DPLL would be studied and simulated by BNR for LSI implementation.

Several changes in the DPLL design were made by BNR to enable substitution of the BNR CMOS II synchronous up/down binary counter for the 40193 counter used by CGE. The 40193 inputs are a COUNT UP clock input and a COUNT DOWN clock input, whereas the BNR counter requires a COUNT clock input and an UP/DOWN input with the additional restriction that the up/down line can only change state when the count input is low. Also, the 40193 is a positive edge triggered counter, whereas the BNR circuit is a negative edge triggered counter.

When a data edge pulse is presented to the DPLL counter, first the up/down line must be set (while clock input is low) and then, a short time later, the pulse clocks the count input. These pulses are asynchronous with respect to the master clock and therefore, the short time delay required for the up/down signal to set the counter must be provided by an analog delay. Simulations of a 300 nS delay revealed that no phase delay was introduced but problems occurred at a 64 kBaud data rate because edge pulses of shorter duration than 300 nS were generated [1/(2 x 2048 kHz) = 244 nS]. Consequently, several "slow" logic gates were cascaded to realize a delay of 30 nS, which solved the problems.

The delay was not required in the breadboard however, because the UP/DOWN input is permitted to change any time (200 nS set-up time) for the CMOS 4029 counter used.

Additional logic was then included in the DPLL to provide the counter decoding options, N = +/- 1 or N = +/- 2. These thresholds correspond to, N = +/- 2 or N = +/- 4 respectively, in the previous DPLL. In the "track" mode, the counter threshold is +/- 81 which corresponds to +/- 162 in the previous DPLL.

The counter thresholds have been halved for the new DPLL and as a result the phase adjustments, that occur each time have also been halved. Phase adjustments are made using an add-a-pulse/delete-a-pulse circuit at the input to a 6 stage (÷64), binary, ripple counter. No decoding of this counter's output is required.

Chip outputs for the DPLL have changed. Two phase adjustment monitor points will be provided, "positive adjust required" and "negative adjust required", and the phase lock loop will be interrupted between the phase controlled oscillator output and the phase detector. These outputs will facilitate rapid, automatic testing of the entire DPLL.

2.2.6 Loss-of-Signal Detection

The loss-of-signal (LOS) detection circuitry designed in previous contract work proved satisfactory except for two minor problems: (1) an analog delay was used to obtain a minimum reset pulse width; and (2) the time base input was derived from the recovered 16 kHz clock which did not ensure that only FFSK signals would enable the track mode.

The first problem was solved using a D-type flip flop, as shown in Figure 6. To ensure that gate L4 or L9 did not change state after the first decoded output is detected, a lockout action occurs using NOR gates L3 and L8: normally the Q outputs of L4 and L9 are low; when a count is detected by L4, say, its Q goes high which maintains the D input to L9 at a low until L14 has captured the output. The reset pulse, generated by L14, is always one

512 kHz clock period long. The twelve-stage binary counter will reliably reset in 400 nS, thus a 2048 kHz clock (which corresponds to a 64 kBaud data rate) will also provide sufficient reset time.

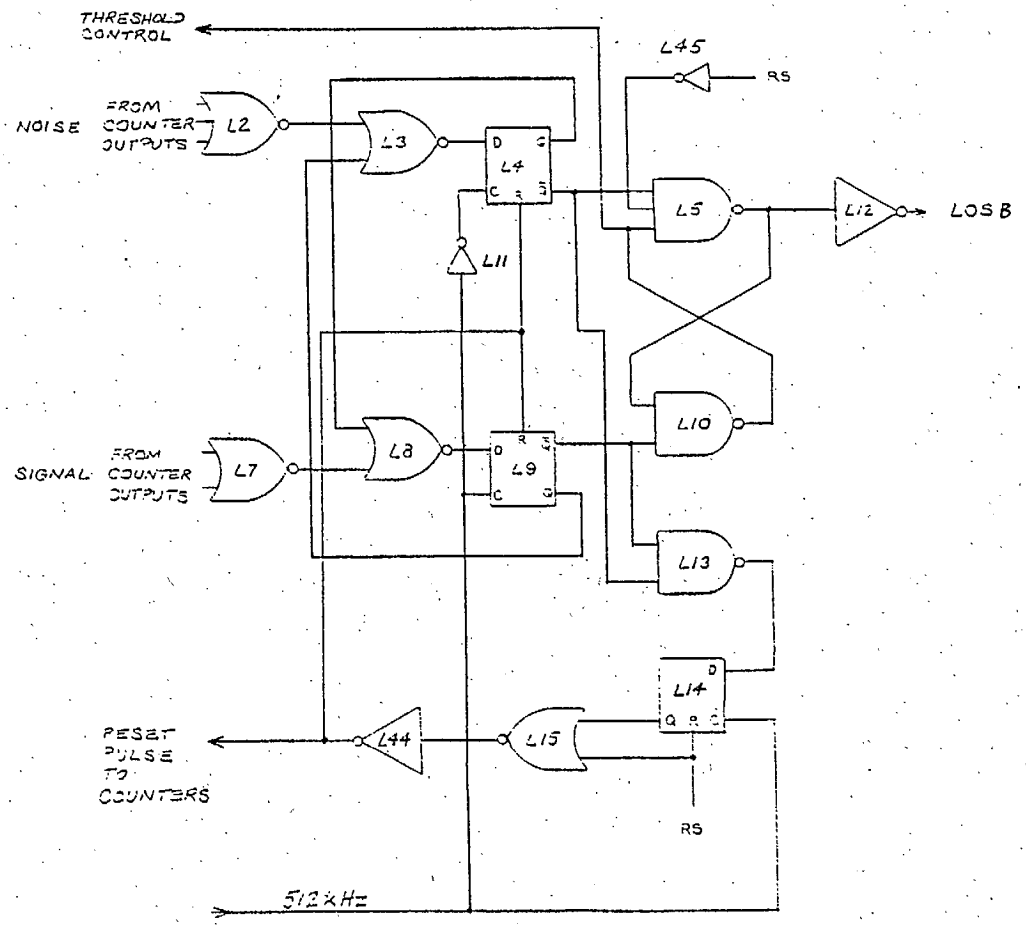


Figure 6. LOS Clocked Delay Circuit

The second problem was solved by using the edge detector output, as specified by CRC, as the time base input.

Logic gates have been included to provide off-chip control of the noise threshold, as specified in the contract. It is understood that this control pin will be connected permanently high or low when the hybrid is assembled.

The noise detection circuitry, which provides noise pulses to one of the counters in the LOS circuit, is the same as that designed in the previous contract.

An LOS timeout circuit has been included in the modem design, as asked for by CRC, but was not mentioned in this contract. Its purpose is to provide a delayed version of the LOS signal for use by external circuitry. The delay can be set to two or four seconds, and is controlled by an external pin. The LOS timeout output is low when "power on" (initialization) occurs, or when $\overline{\text{LOS}}$ is high, or when the NBWB(D) input is low.

2.2.7 Initialization and Global Reset

Initialization of all counters and flip-flops is controlled by an on-chip cell called "INI2". The input to this cell is V_{DD}. During power-up, the output of this cell is "low" when V_{DD} is between 1.2 and 3 volts (approx.), and follows V_{DD} above 3 volts. If we assume that on-chip V_{DD} rises no faster than 1 V/μS then the INI2 cell will generate an inverted reset pulse of at least 1.8 μS duration, which is sufficient to reset all on-chip circuitry.

To provide off-chip control of this reset function, a "Global Reset" pin has been provided. This pin will reset only the timing chain, the modulator ring counter, and the phase controlled oscillator. Thus, all clocks are reset for synchronism with other system clocks. The function does not introduce risk for the LSI device.

2.3 BREADBOARD IMPLEMENTATION

After the new modem circuit design was completed, and all digital portions had been simulated using the BNR F/LOGIC program, a breadboard circuit was designed. There were three reasons for building a breadboard version of the LSI circuit: (1) it provided a vehicle for verifying the design intent, ensuring that the design would interface with other chips in the Special Communications Equipment; (2) it ensured that the breadboard version built by CGE, during design development, was a repeatable design - a check that all resistances, capacitances, etc. had been included in the approved circuit schematic; (3) it ensured that the tests performed by BNR were sufficient to detect all possible faults, including those of an analog nature. The board was not built to verify the computer simulations since MSI gates have delay parameters quite different to those of LSI gates.

The board was designed using 4000 series CMOS chips, and discrete passive components. All parts were mounted on wire-wrap modules provided by CRC.

Several test circuits were included on the boards, as suggested by CGE, to simplify the test procedure. The final breadboard schematic is given in Appendix 3.

2.3.1 BNR Breadboard Tests

The prime purpose for testing the breadboard at BNR was to ensure that a fully debugged modem was sent to CGE for performance evaluation. The testing also served to check the BNR test procedure which will be used to test the LSI modem.

The BNR test procedure incorporated most of the "Recommendations for BNR Testing of Breadboard and LSI Chips at BNR Facilities," which was submitted by CGE in June, 1980. The tests are not identical (but similar) to those which will be used for the LSI version because insufficient time was available for writing Automatic Test software or building the equivalent hardware.

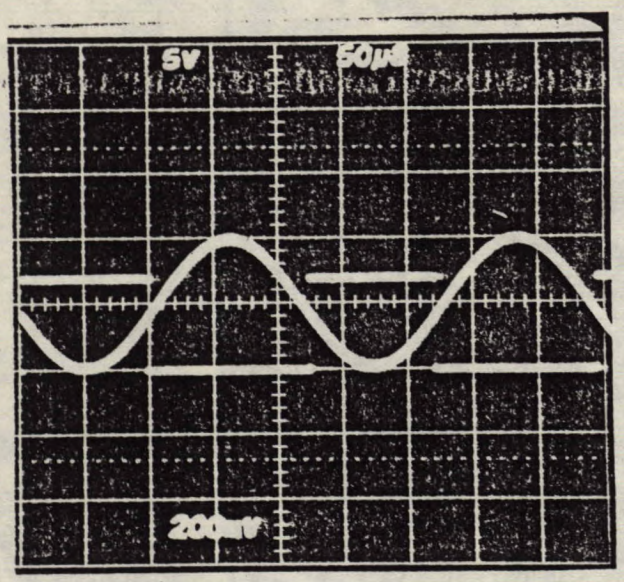
The breadboard tests performed by BNR are listed in Table 1. The power supply for all tests was set at 7 volts. Only a 2.048 MHz crystal was used for the master clock and only 455 kHz was used as the carrier centre frequency.

2.3.2 BNR Breadboard Test Results

All the tests were successful (results listed in Table 1) except for the AFC test. It was assumed that the instability of this output was caused by the highly regular test data sequence (00010001). Since CGE already had a pseudo-random code generator, BNR asked them to do the test. The CGE test proved successful when a 63 bit pseudo-random bit sequence was used.

The output of the IF amplifier is shown in Figure 7. The input signal is 140 mV rms (200 mV amplitude) at 455 kHz. It can be seen that the switching point is approximately 40 mV off-centre. For a 300 mV rms signal the resulting phase error is less than six degrees.

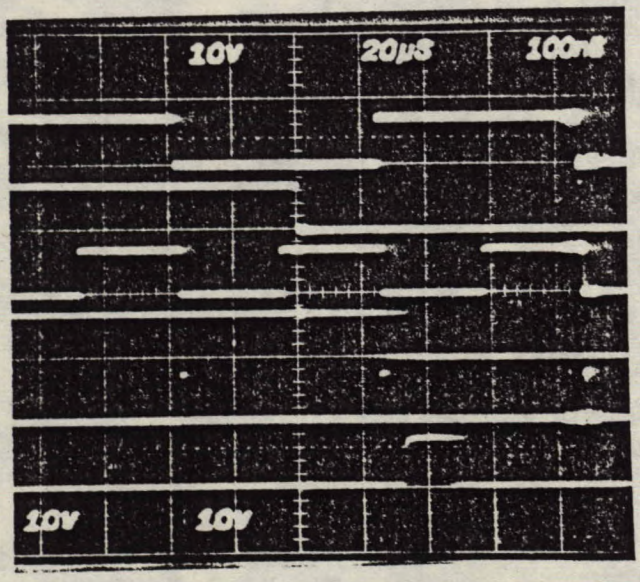
Several DPLL waveforms are shown in Figure 8. The delay between the falling edge of the 8 kHz input signal and the falling edge of the 16 kHz recovered clock is about 140 nS (0.8°). It can be seen that this is entirely due to the delay through the edge detector (note the position of the edge pulse in Fig. 7). The LSI implementation of this circuit will have a delay of about 10 nS.



Output signal (7 V. sq. wave)

Input signal (400 mV p-p)

Figure 7. IF Amplifier Waveforms



X1
X200
} 8 kHz Input

X1
X200
} 16 kHz Recovered Clock

X1
X200
} Edge Detector Output

Expanded Section

Figure 8. DPLL Waveforms

TABLE 1 BNR BREADBOARD TEST PROCEDURE

tion to Tested	Inputs (cumulative unless stated otherwise)	Outputs
ulator	- Tx data: 4 kHz @ 25% duty cycle (equivalent to 00010001)	- I & Q outputs (before mixing) compared to computer simulation - reference 16 kHz checked
Amp	- Rx signal: ≥ 300 mV RMS VCO 0° : V_{SS} VCO 90° : V_{DD} - Rx signal: VSS VCO 0° & 90°: 455 kHz	- I: 455 kHz square wave Q: 455 kHz square wave (inverted) - I & Q: 455 kHz square wave
ector DPLL	IR & I/D filters removed DPLL in closed loop - I : 8 kHz square wave Q : V_{SS} 8 kHz varied ± 150 Hz - N=1 - N=2 - N=81	- recovered 16 kHz checked for synchronization - phase error measured as 0.8° - bandwidth = ± 250 Hz @ 16 kHz - bandwidth = ± 125 Hz - bandwidth = ± 2 Hz
ector	I & Q : as in previous step Noise : square wave varied from 400 to 2100 Hz LOSSEL : V_{SS} - Noise : < 1 kHz - : 900 → 1100 Hz - > 500 Hz - : 600 → 400 Hz LOSSEL : V_{DD} Noise frequencies doubled	- check 'noise' frequency required to change $\overline{LOS}$ $\overline{LOS}$ = 1 = 1 → 0 @ 1 kHz = 0 = 0 → 1 @ 500 Hz $\overline{LOS}$ = 1 → 0 @ 2 kHz 0 → 1 @ 1 kHz
	NBWB(A) : V_{SS} IF & I/D filters inserted modulator summed output connected to demodulator input - vary 455 kHz of mod. with respect to 455 kHz of demod.	- observed differential voltage output to be unstable (phase dependent?)
ction	- 455 kHz of mod. same as 455 kHz of demod.	- Rx Data output observed to to be same as Tx Data input

2.3.3 The CGE Breadboard Evaluation

A report entitled, "Performance Test of Bell Northern Research FFSK Modem by Canadian General Electric", was received by BNR, September 27, 1980.

The report concluded that,

"The FFSK modem has passed all performance testing with good results except for the following items: ... current consumption ... is unacceptable ... LOS programming is unacceptable for one of the filters (16 KHz) intended for ... the chip. This report contains many cautions and qualifications ... CGE cannot approve the present LSI design until the two items are resolved." [5]

Each of the CGE points concerning the LSI design will now be addressed.

The current consumed by the BNR breadboard was in excess of 25 mA, whereas the microcircuit is required to operate at less than 5 mA. CMOS circuitry consumes power only during transitions and primarily it is used to charge the load capacitances. The capacitive loads in an LSI chip are approximately fifty times smaller than those in the boardboard. There are several circuits however, that consume more power than their capacitive loads warrant: the IF amplifier inverters, and the $V_{DD} \div 2$ resistive divider. Power, for the former, will be reduced by using fewer and smaller inverters; for the latter, power may be reduced by increasing the resistances, with a larger capacitance to maintain a low AC impedance.

Detailed analog simulations show that each input inverter uses a peak current (during transitions) of less than 500 μA whereas the corresponding breadboard invert rs required 3 mA average current.

A 2048 kHz divide-by-two gate in the breadboard DPLL has been eliminated in the LSI schematic since it was essentially redundant and required a significant current (measured by CGE).

It is expected that the current required by the LSI chip will be less than 5 mA, but this cannot be determined exactly since power is partially dependent on the particular layout of the circuit.

The LOS circuit was programmed for IF filter bandwidths of 12 kHz and 24 kHz. After the breadboard was built (breadboard construction was completed July 29, 1980) the IF bandwidth was changed, by CRC, to 16 kHz. CGE found that the LOS circuit did not operate correctly for the new bandwidth. CRC then commissioned CGE to determine new programming for the LOS circuit to accommodate the 16 kHz bandwidth. The new thresholds recommended by CGE for the noise counter are: 25 and 353 (formerly 32 and 512). Both of these new counts require decoding of the LSB output of the noise counter. The LOS threshold detectors were designed by BNR with the assumption that the decoded count would be present for at least two microseconds. The new CGE modification does not guarantee this, and therefore cannot be accepted by BNR. CGE has stated that, "firing points are not distinct," [6] for the LOS detector. This suggests that changing the programmmed thresholds to 24 and 352 would have minimal effect on modem performance and yet, would ensure the presence of a decoded count for the required time (2 μS). The LSI schematic in Appendix 1 shows the LOS circuit recommended by CGE but not by BNR.

Two circuit faults were found by CGE in the BNR-built breadboard, after the board had passed the BNR tests: (1) the switching voltage of the integrate-and-dump comparator (inverter) was found to be too low; (2) a connection to the noise discriminator flip-flop was found to be incorrect. The BNR test procedure will be modified to detect the first type of fault. The second type of fault is detectable with the automatic test pattern (which was not used for the breadboard).

CGE found it necessary to add hysteresis to the four comparators used, to obtain glitch free outputs. CGE has recommended 438 mV hysteresis, yet "no degradation or improvement in the demod performance with or without 0.4 volt hysteresis," [7]

was found. BNR will provide this hysteresis using on-chip resistors, since its necessity could then be determined experimentally (if desired).

Operation of the entire modem was found to be satisfactory for supply voltages from 4.5 to 13.5 volts, except of course, for the current consumption.

3.0 CONCLUSIONS AND RECOMMENDATIONS

The circuit illustrated in Appendix 2 is suitable for LSI implementation and can be expected to meet all the requirements of CRC Specification DSRD-MC-06 subject to the minor changes stated in section 4 of this report. Computer simulations show that the digital logic in the schematic is capable of handling a data rate of 16 kBaud and that 64 kBaud operation is feasible Analog simulations of the modulator output mixers show that transmission of a 20 MHz carrier frequency through the chip (with less than 3 dB attenuation, depending on the load) is also feasible.

It is recommended that layout of the FFSK modem IC begin as soon as possible, with the slight change in the LOS circuit specified on page 21 of this report. Also, some experimentation should be done with the finished IC to ensure that the off-chip component values give optimum performance.

4. SPECIFICATION COMPLIANCE

All specifications listed in Appendix A of CRC Specification DSRD-MC-06 will be achieved exactly as stated except for the changes listed below:

A.2.1 Basic Functions

pg. 2 1) "It shall be possible to operate the modem from an external 512 kHz clock".

It will not be possible. The new DPLL design requires 2048 kHz.

2) "The three configurations are shown in Figure 1."

Only two configurations are possible due to change in (1).

3) "(b) provide a 2048 kHz master reference signal to the delta codec and the PFSR."

A bonding option will provide a choice between 2048 or 1024 kHz.

4) "(d) provide internally a 512 kHz reference to ... the DPLL ..."

Changed to 2048 kHz as stated in (1).

pg. 3 5) see Figure 9

pg. 4 6) "(a) be capable of using 512 kHz references at 0° and 90° ... for down-conversion demodulation".

This is possible if IF signal is centered at 512 kHz.

7) "(b) use a 512 kHz reference ... for clock recovery"

Changed to 2048 kHz as stated in (1).

8) "The actual DPLL control signal is the complement of the carrier loop control signal. Logic level inversion shall be performed on chip."

The DPLL control signal is the same as the carrier loop control signal. Both inputs are connected to separate pads which may be connected together externally.

9) "The PFSR will use $\overline{\text{LOS}}$ and the 16 kHz reference provided to it by the modulator to derive an LOS TIMEOUT signal."

The LOS TIMEOUT signal will be generated by the FFSK modem chip.

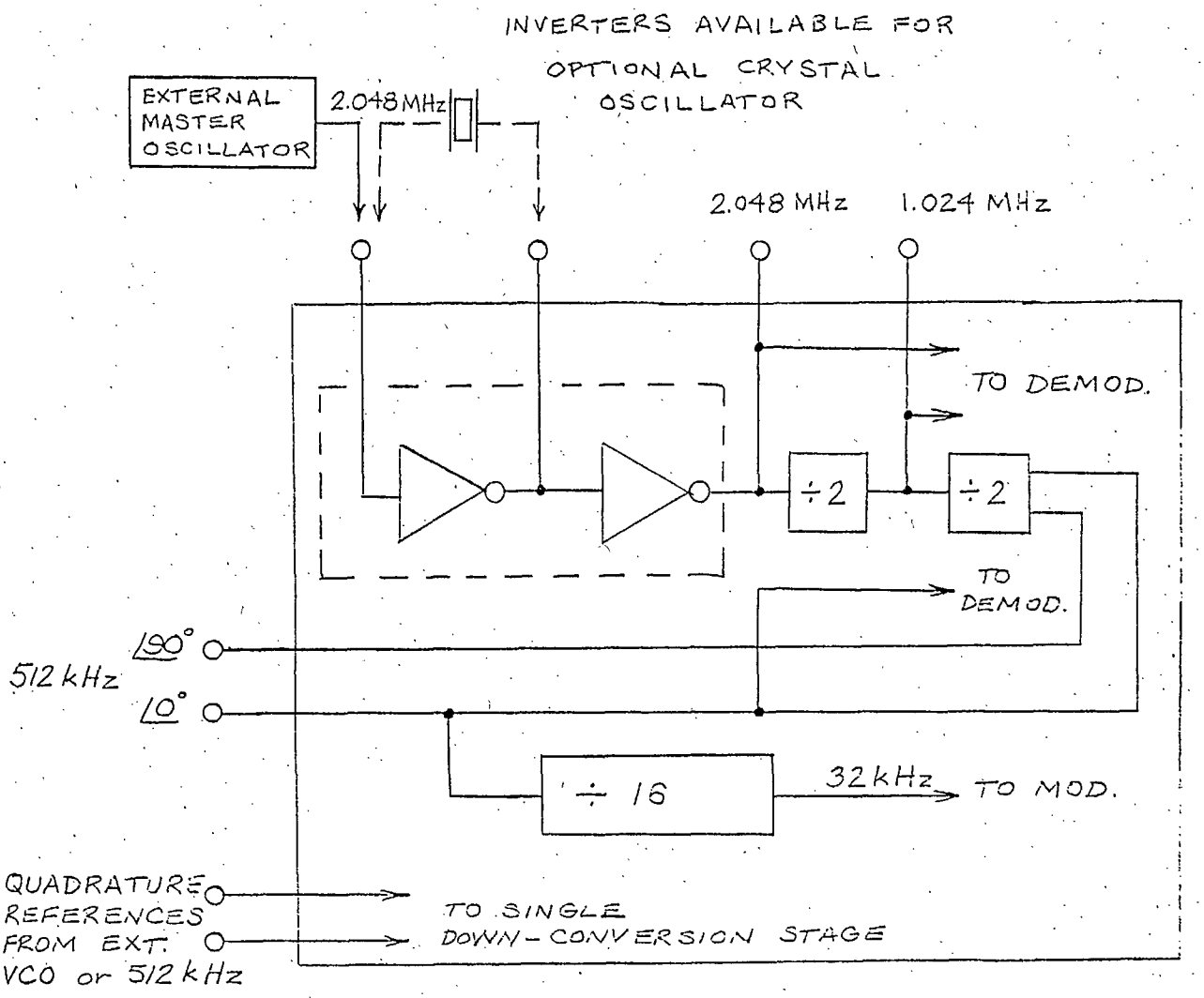


Figure 9. The Revised Oscillator Connection Diagram

10) "(i) provide a monitor of the inputs to the buffers preceding the quadrature integrate-and-dump circuits."

Change to, "provide separate inputs to the quadrature integrate-and-dump circuits."

A.2.2 LOS Detection

pg. 5 "To allow operation with twice as large an SCE IF bandwidth the input to the noise counter shall be divided by 2".

Change to, "To allow operation with a wider SCE IF bandwidth, noise count thresholds of 25 and 353, respectively, will also be provided."

A.2.3 DPLL

pg. 6 11) "The track threshold shall be fixed at $N_{TRACK} = 161$"

The new DPLL design halves N, and halves the phase correction. Therefore, $N_{TRACK} = 81$.

A.3.1 Inputs

pg. 7 12) "DPLL WB/NB control signal from the PFSR. LOW when in the NB mode. The DPLL signal is the complement of the frequency discriminator control signal and shall be derived from same on chip."

Change to, "DPLL WB/NB control signal from the PFSR. HIGH when in the NB mode (the same as $\overline{LOS}$). The DPLL signal is the same as the frequency discriminator control signal and the respective input pins may be connected together off chip." This allows these pins to be connected, off chip, directly to $\overline{LOS}$.

A.3.2 Outputs

pg. 8 13) "The output to the RF Modulation circuitry shall be two conditioned CMOS data streams. The modulator shall be capable of driving up to 8 inch shielded lines on each of the two output lines."

Change to, "The output to the RF Modulation circuitry shall be four IF-carrier-modulated data streams."

14) "A lock indicator signal $\overline{LOS}$ (low when the demodulator is in lock)."

Change, "low" to "high".

A.3.3 Crystal Oscillator Specifications

pg. 9 15) Delete, "It shall also be possible to operate the modem using a 512 kHz external reference," for the same reason as (1).

5.0 REFERENCES

1. "FFSK Modem Microcircuit Feasibility Studies", Dept. 5D23, BNR, January 1979, pg. 2-1.

2. "CGE Consultation on FFSK Modem Implementation in LSI January-April 1980", P. Jeans and C. Jagger, CGE, pg. 3-5.

3. "Report on the Choice of Modulator for the FFSK Modem", J. Bennett and A. Ho, BNR, March 14, 1980.

4. "CGE Consultation...", P. Jeans and C. Jagger, pg. 73.

5. "Performance Test of Bell-Northern Research FFSK Modem by Canadian General Electric", P. Jeans, CGE, August, 1980, pg. 36.

6. "FFSK Chip, Second LOS Option", letter by P. Jeans, CGE, October 7, 1980 pg. 2.

7. "Performance Test ... ", P. Jeans, pg. 35.