Analog-to-Digital Converter Technology for Digital Radio

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CONTRACTOR: queens university

CRC SC. AUTH: V. Szwarc

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D. G. Nairn and W. M. Snelgrove

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Table of Contents

CRC Report: Data converters for Digital Radio

1: Introduction: Data converters in digital radio

Digital implementation of radios, as proposed in the CRC report "Proposal to Develop a Proof-of-Concept Digitally-Implemented Narrowband Radio" [1], offers advantages in flexibility and cost over purely analogue architectures. This report focuses on the data conversion issues for radios in which the IF and baseband signal processing are digital. Data converters would have to handle IF signals with centre frequencies in the 10-70MHz range, with bandwidths varying from a few kilohertz to more than a megahertz, and with SNR of about 70dB.

These are stringent requirements for the data converters, particularly for the A/D. When the radio is to be portable, power requirements are also tough. D/A converters exist that have the required speed and resolution at reasonable power, but A/Ds do not. This report shows why they don't, yet, but suggests that the problem is not fundamental.

We see two general approaches to data conversion at IF: broadband and bandpass conversion, where the latter is a very new technology. The original system design [1] assumes a broadband 8-bit converter running at 280MHz, giving roughly 9-bit accuracy in a 40MHz band (or 12 bits in 1MHz) through oversampling. Equivalent performance from a bandpass converter would be acceptable.

Data converters limit short-term development, because they make credible radio prototypes difficult to put together, and may — if fundamental — affect long-term radio architecture. Here we review the state of the art in converter performance, and estimate the likely progress of the technology by identifying theoretical and practical limitations on performance.

2: Video, voice and audio applications

Data converters currently available are aimed at applications other than digital radio. Comparing these applications with radio, in terms of conversion requirements, helps in seeing what issues will be important and what problems early prototypes can expect to have.

Table 1 summarizes major present applications and compares them to the radio needs outlined in [1]. Where a parameter is not critical, the entry is "—".

Table 1: Data Converter Applications

Application	Sample rate	bits	Max power	Linearity	Market	Nearest radio application
Analogue to Digital						
70MHz IF	280MHz	8	100mW	high	digital radio	All
10MHz IF	40MHz	8	100mW	high	digital radio: less general	BW<1Mhz
Sampling oscilloscope	50MHz-2GHz -∞	5-7	—	—	scientific	All except portables
Radar			—		military	All except portables
HDTV (1125/60)	75MHz or muxed 150MHz	8	—	—	consumer TV	20MHz IF
TV (CCIR spec)	13.5MHz	8	—	—	multimedia, eventually consumer	5-10MHz IF, FM, TV
N-ISDN	200kHz	14	—	high	business, then consumer telephone	FM
DAT	50kHz	16-18	some portables	very high	consumer audio	
Voice codec	8kHz	13	—	—	1 per 'phone at central office; consumer gadgets	AM
Meters	10Hz	20+	some handheld	high	scientific and industrial	
Digital to Analogue						
Computer graphics and HDTV [2,23]	130MHz	8	150mW	—	professional/ scientific and high-end consumer	20MHz IF
TV-NTSC	14.25MHz	8	—	—	consumer	

Table 1: Data Converter Applications

Application	Sample rate	bits	Max power	Linearity	Market	Nearest radio application
TV-MAC[24]	27MHz	8	—	—	consumer	10MHz IF
N-ISDN	200kHz	14	—	high	business, then consumer telephone	FM
CD/DAT [26]	50kHz	16-18	15mW	high	consumer	FM/cellular
Codec	8kHz	13	—	—	telephony etc.	AM

For speed, digital radio requirements are comparable with those for video and 'scope applications; but linearity and power (for portables) specifications are more stringent. In terms of circuits and performance limits, broadband converters for digital radio will therefore probably resemble video converters.

In terms of bandwidth and linearity, ISDN converters might be a better analogy. A bandpass converter would be likely to resemble these.

Converters are also produced as results of curiosity-driven research, with specifications not particularly adapted to any of the above applications.

This report therefore focuses on the types of converters used for video and ISDN, extrapolating their techniques and performance to the levels required for digital radios.

3: Converter speed, power and resolution: present art

There are several trade-offs in converter design; the plots presented here illustrate them and show where the needs for digital radio fit in. Advancing technology improves performance, so plots present figures of merit against time to get an estimate of "how close" current technology is to being able to produce the devices required.

In these graphs there are generally large clusters of points, each corresponding to a choice of technology and to an application. Technology choices are distinguished by symbols, keyed in the graphs to descriptions which we elaborate in later sections.

Accuracy and speed are competing objectives in converter circuit design. Figure 1 plots resolution (in bits) against sampling rate for about two hundred converters from the academic and industrial literature. There is a general downward trend indicating a trade-off of about 1 bit per octave in the best converters.

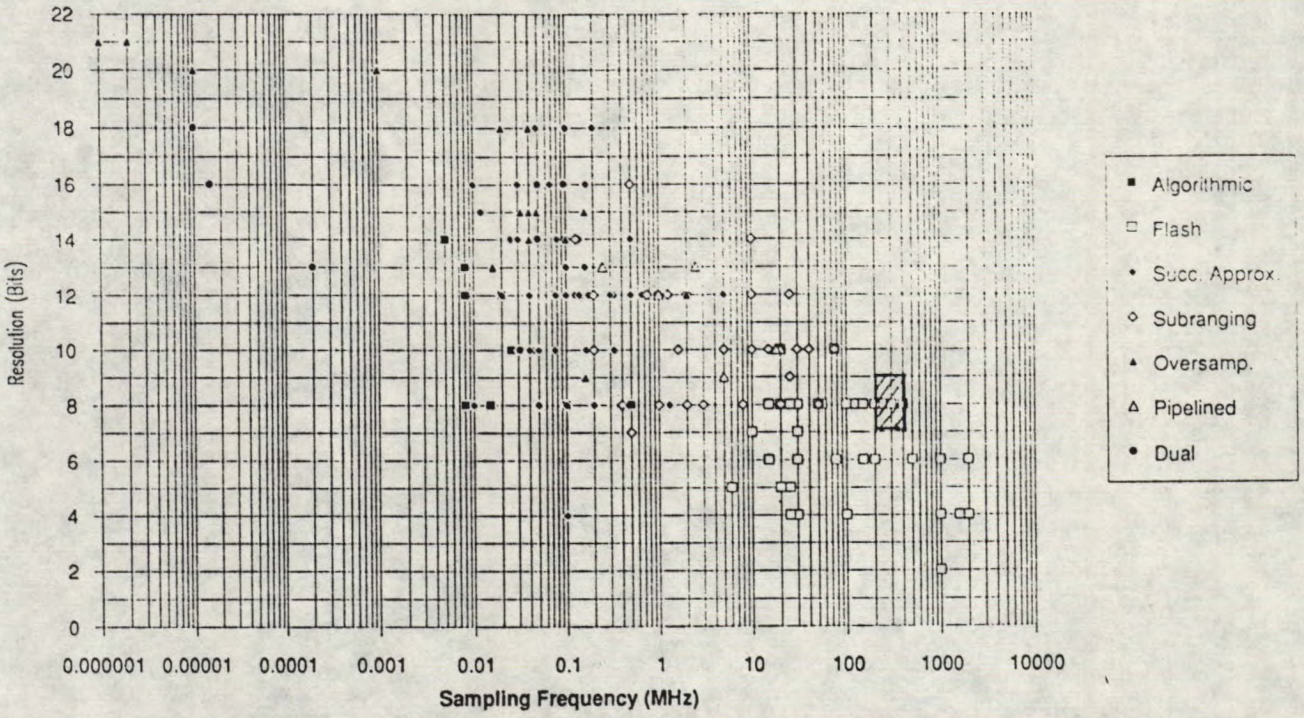

Figure 1: Resolution versus sampling rate

High-speed operation costs power: the power consumption of most converters has a large dynamic component, so that for a given converter $P_d \propto f_s$. There is also a fundamental limit requiring converters to draw a certain amount of power to get samples above thermal noise. This gives a lower bound on power that is proportional to frequency for a given resolution. Figure 2 plots power consumption against sampling rate for 8-bit converters. At present even the best converters require too much power for portable radios, but the 80MHz specification is close enough to the curve that a custom-designed part could probably be made with present technology. The 280MHz specification will require about an order of magnitude improvement.

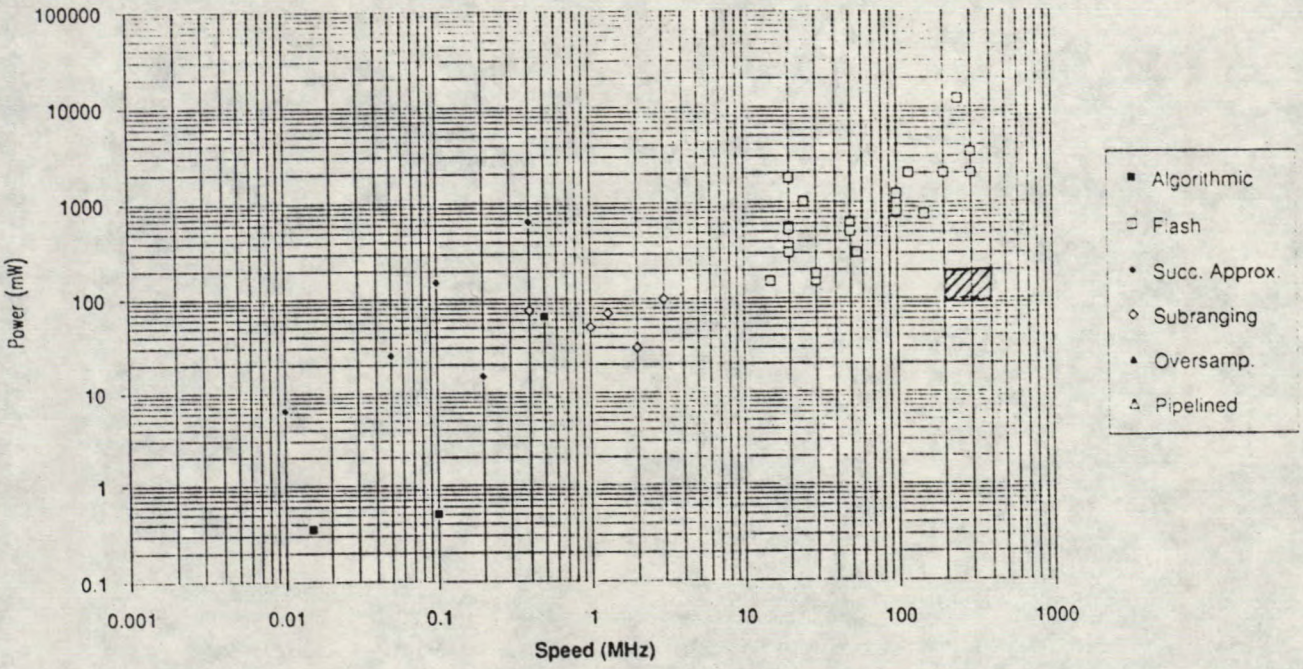

Figure 2: Power versus sample rate for eight-bit ADCs

Advancing process and circuit technology can be used to improve power-efficiency or increase speed. Figure 3 plots a figure of merit — energy per sample — against the year of publication for eight-bit converters running in the MHz range. Commercial products are not directly shown, since their dates of introduction do not appear in manufacturer's data, but many commercial converters have been described in the technical literature, and these do appear. At 1nJ/sample (or 1mW/MHz, the bottom of the graph), a 280MHz converter would consume 280mW, and be a plausible component of a digital radio. The best 8-bit parts are running at about 2.5mW/MHz, and most run at about 10 — far too much for a portable radio. At the eight-bit level, designers are typically pushing speed rather than power.

High resolution also costs power, so figure 4 plots energy/sample against resolution. The plot indicates an increase of a factor between 2 and 4 in power per bit of resolution, with a few high-resolution converters doing significantly better than the overall pattern.

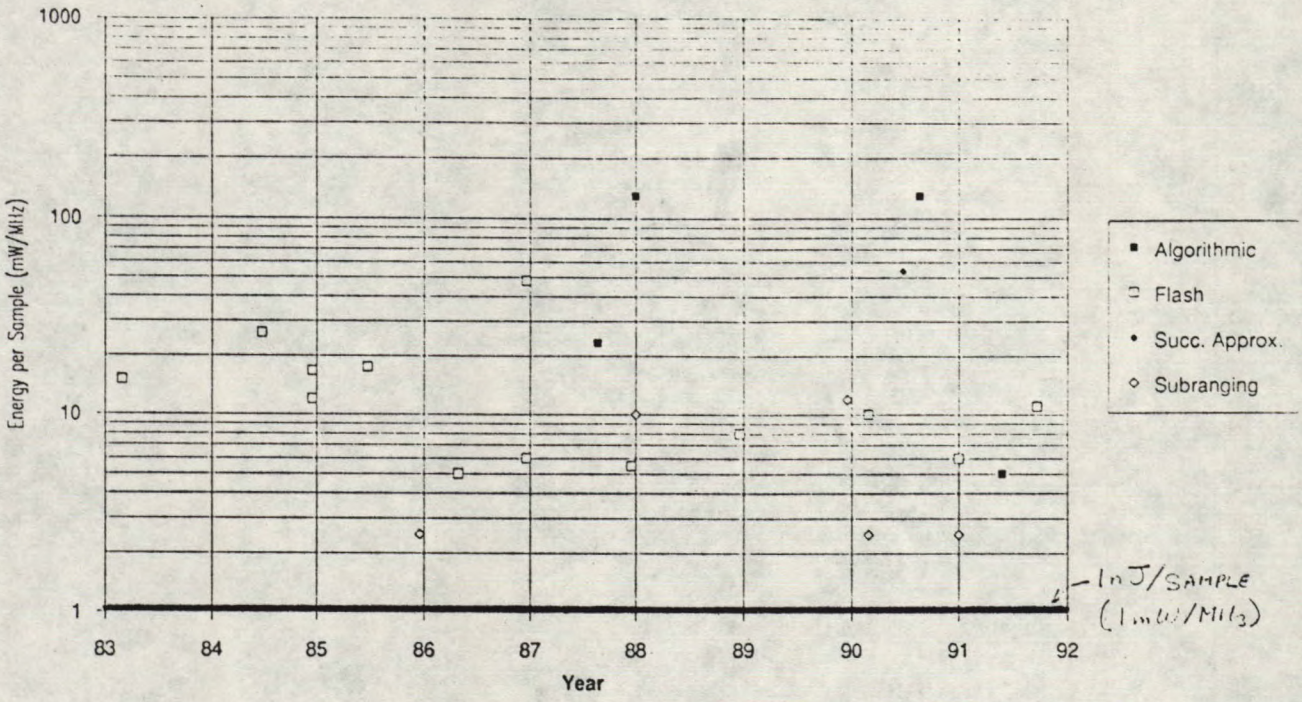

Figure 3: Energy per sample versus time for eight-bit ADCs

The cost of resolution can be factored into a more sophisticated figure of merit with a (distant!) physical bound, SNR/ (energy/sample) [51,60]:

$$\frac{2^{2 \times \text{resolution}}}{\text{energy / sample}} \qquad \text{Eq. 1}$$

The simplest bound on this quantity comes from the need for the energy on a sampling capacitor to exceed the thermal noise energy by a margin large enough to give the required dynamic range, and from assuming that this signal energy is dissipated when a new sample is read in. Equipartition of energy among thermodynamic states guarantees that thermal sources (such as thermal motion in channel charges of a switch) will leave an average noise energy $(kT)/2$ on the sampling capacitor. For a useful converter, the LSB can't afford to be smaller than this noise, so that the maximum signal voltage must by about 2^N times larger — i.e. the maximum signal energy must be at least 2^{2N} times larger, at

$$2^{2N-1}kT = 2^{2N}2.08\times10^{-21}\,\text{Joules} \qquad \text{Eq. 2}$$

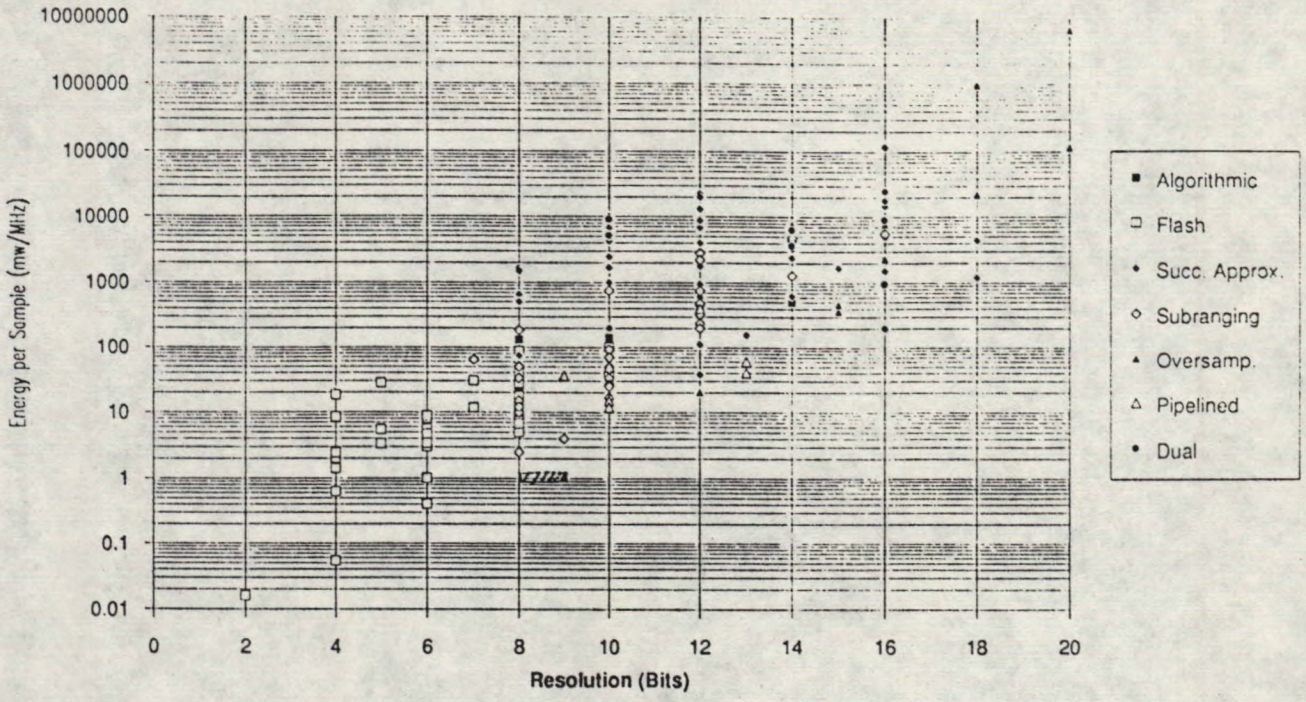

Figure 4: Energy/sample versus resolution

So the SNR/ (energy/sample) figure is bounded below

$$\frac{\text{SNR}}{\text{energy/sample}} < \frac{2}{kT} \approx 4.8076923\ldots \times 10^{20}\,\text{Joules}^{-1} \qquad \text{Eq. 3}$$

For 16-bit conversion, this bounds energy/sample above $8.933532\ldots \times 10^{-12}$ Joules — about 9μW/ MHz. A 280MHz/eight-bit converter running at the limit would dissipate only

$$2^{2(8)}\, 2.08\times 10^{-21}\, 280\times 10^{6} \approx 38.168166\ldots \text{nW}. \qquad \text{Eq. 4}$$

and conversely a "tolerable" 100mW dissipation level in the same converter would correspond to

$$\frac{\text{SNR}}{\text{energy/sample}} = \frac{280\times 10^{6} 2^{16}}{0.1} \approx 1.835008\times 10^{14}\,\text{Joules}^{-1} \qquad \text{Eq. 5}$$

No present converters are near the ideal performance level, but quite a few are better than tolerable. Plotting the figure against year of publication gives figure 5. It is clear that there has been steady progress towards the bound, and that the best converters are within striking distance.

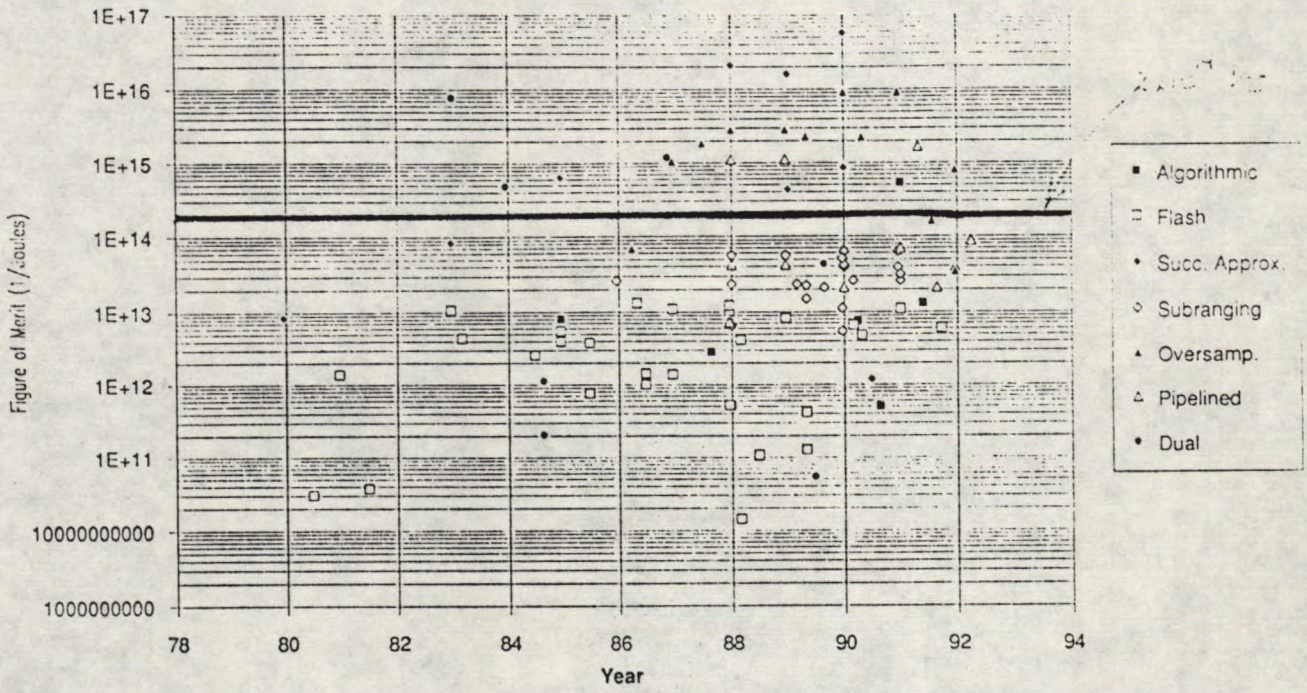

Figure 5: Energy/(sample.SNR) versus time, with a thermal bound

Practical video converters are orders of magnitude below the limit, and their performance is dominated by a range of practical problems. Technological changes are attacking these problems in a reasonably predictable way, which we will look at in more detail in sections 9. A way to summarize the effect of technology on performance is to look at converter speed as a fraction of f_t, the unity-gain frequency of the transistors provided by the process. Over time the maximum attainable f_t (for MOSFETs, at any rate) has been steadily improving, pulling converter speeds in its wake. BJT f_t has been at a plateau for several years, but heterojunction bipolars will give an order of magnitude improvement in a few years.

Figure 6 plots energy efficiency (SNR/(energy/sample)) against sample rate relative to technology limits, showing the power penalty for running near the limits of a given process. The f_t figure used for BJTs is the maximum attainable, but that for MOSFETs is f_t when the devices are operated at the edge of the subthreshold region. This is because MOSFETs are often operated well below their best f_t because they have poor power efficiency at high bias levels. Some CMOS converters appear to operate very close to f_t because these are circuits that run their devices at an inefficient (but fast) high bias level.

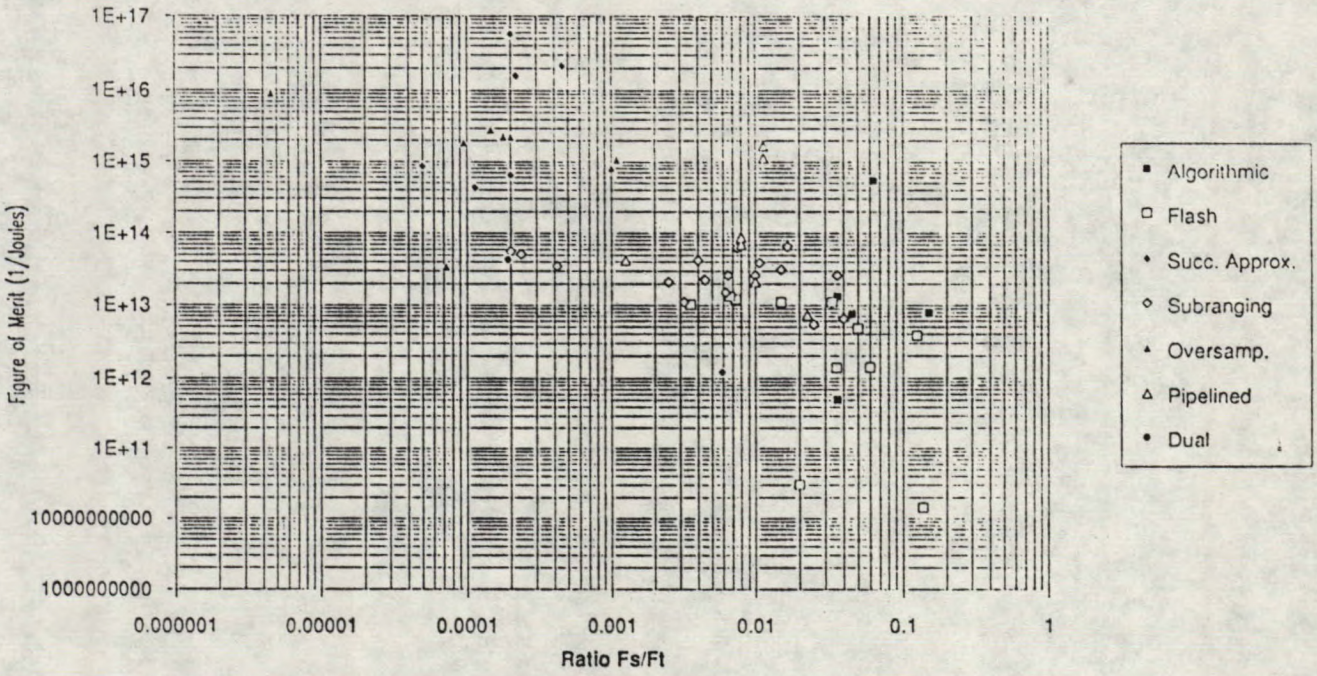

Figure 6: SNR/(energy/sample) versus sample rate relative to unity-gain

A major part of the power penalty for "pushing" performance in a given technology comes from the need to use inefficient architectures at high relative speeds, as suggested by the keying of plot symbols to architectures — architectures change as speed goes up. These architectures are discussed in section 9.

summary

A survey of some two hundred converters shows trade-offs among speed, power and resolution. Steady progress is being made in pushing back the envelopes defined by these trade-offs. The requirements for data converters for a 70MHz IF in a handheld radio (as in [1]) are beyond present technology but not implausible within a few years; a 20MHz IF at 200mW may be possible in a custom design with present technology. The input sample/hold is a problem all by itself, particularly for fast-slewing signals.

4: Sample/hold Performance: Limitations and Current Art

The input sample/hold circuit of an A/D is a problem for high-frequency inputs, and in fact aggressive tests of converter performance often drive inputs with large signals at frequencies comparable to the sampling rate in order to detect sample/hold errors. These are exactly the kinds of signals that can be expected in digital radios. Silicon sample/hold circuits have SNR below 40dB when input signals are in the 100MHz range, while GaAs gets similar accuracy out to 500MHz[36].

Figure 7 shows a basic sampling circuit: when ϕ is **high** the output and input are supposed to track; when it goes **low** the value of the input at the falling edge of ϕ should be held on C.

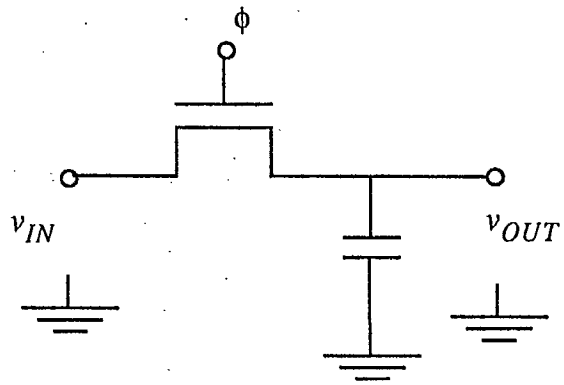

Figure 7: A simple sample/hold circuit

Firstly, when "on" the MOS switch has finite resistance. This means that the signal being tracked is a low-pass filtered version of the input. Converters are sometimes tested with high-frequency inputs to discover the 3dB frequency of the input sampler. Typically, if the switch has $10k\Omega$ on-resistance and C is 1pF, then the 3dB frequency is about 15MHz.

Secondly, the transistor doesn't turn "off" cleanly, but injects charge from the transistor channel into the sampling capacitor. There is a relationship between bandwidth for the "on" state and the error voltage from charge injection [17] that puts the resulting error in signal voltage at the 100mV level for fast samplers. This relationship is:

$$\Delta V = \frac{1}{\tau}\frac{L^2}{2\mu} \qquad \text{Eq. 6}$$

where τ is the lowpass time-constant when tracking, L is channel length, μ is mobility and ΔV is the minimum attainable error voltage.

For a 280MHz sampler to have 6τ to settle, and for 1μm n-channel devices,

$$\Delta V = \frac{6\,(280)\times 10^{6}}{1}\,\frac{10^{-12}}{2\,(0.066)} = 12.727273\ldots\text{mV} \qquad \text{Eq. 7}$$

The offset voltage that this produces is not critical for digital radio, but there are important second-order effects because the amount of charge injected depends on the signal. In particular, there is a nonlinear component to the dependency that will contribute intermodulation distortion to the signal. Techniques used to reduce this problem are

- the use of balanced signals to cancel offset and even-order distortion products. This is more difficult if the original signal is single-ended, as the circuits for converting single-ended to balanced signals have their own problems, and does not reduce odd-order products such as the $2f_1 - f_2$ terms important in radio

- "bottom plate sampling", in which an additional switch disconnects the capacitor from ground in order to effect sampling. This reduces the signal voltage on the critical switch, so that charge dependencies are minimized. For high-frequency input signals, though, large $C\frac{dv}{dt}$ signal currents force significant signal-related voltages across even a grounded switch and there is still a significant problem

- the use of short channel-length or high-mobility devices available in advanced process technologies

Figure 8a shows a typical modern balanced sample/hold [136]. It uses the clocks shown in figure 8b, includes a balanced buffer, and is also insensitive to capacitor nonlinearities.

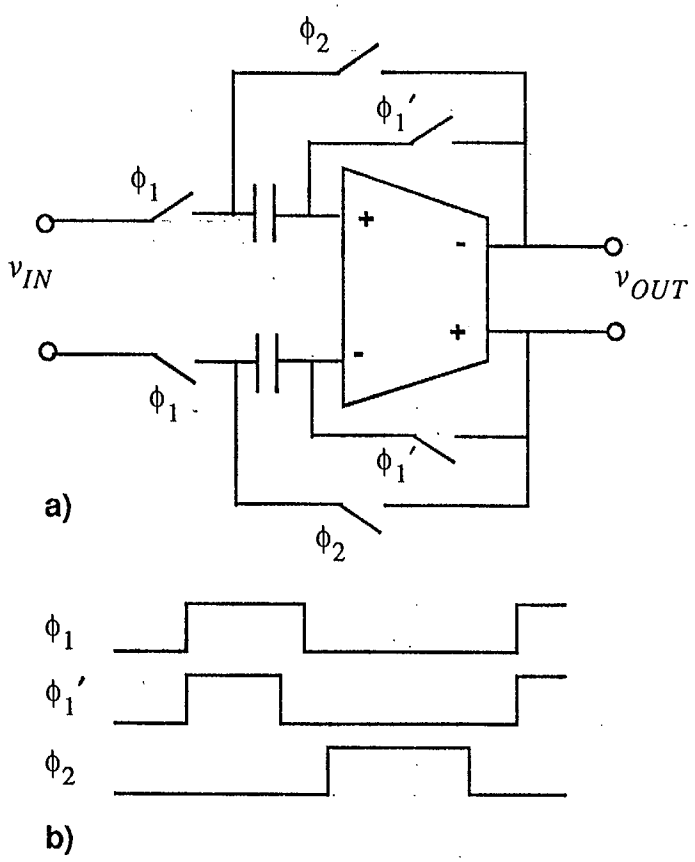

Figure 8: Balanced sample/hold and its clocks

aperture time and jitter

Small timing errors in sampling can contribute significant errors: a peak error of 0.5Δ will result, when a full-scale sine at the Nyquist frequency is applied, if the sampling time is wrong by one part in $\pi 2^N$ — about 0.1% accuracy for compatibility with an 8-bit converter. These timing errors can come from clock jitter or from second-order circuit effects. For example, the simple sampler of figure 7 effectively samples when the transistor turns off, and that in turn is a function of the input voltage and the slope of the clock signal. Dependence of sampling time on signal voltage creates a kind of FM distortion, and practical clock slopes are slow compared to 0.1% of the sampling rates required for digital radio. Even the more sophisticated sampler of figure 8 has some sensitivity of sampling time to the slew rate of the input signal.

There is little uniformity in the literature as to reporting the linearity of input sample/hold circuits for high-frequency inputs, so the kind of summary data that is available for speed, resolution and power cannot be obtained. For example, though, the SNR of the AD9028 drops from 47dB at DC through 43dB for a 40MHz input to 36dB (equivalent to less than 6 bits) with a 92MHz input.

5: Linearity: Current Art

An ideal A/D converter is usually defined to have the "staircase" transfer characteristic shown in figure 9. Real converters are generally characterized by two different kinds of nonlinearity [5]: **differential nonlinearity** (DNL) models small perturbations of individual stepsizes from their ideal widths and **integral nonlinearity** (INL) describes maximum overall deviation from a best-fit straight line characteristic. Figure 10 shows a characteristic with high DNL, while figure 11 shows one with low DNL but high INL. High DNL implies high INL, but not vice-versa.

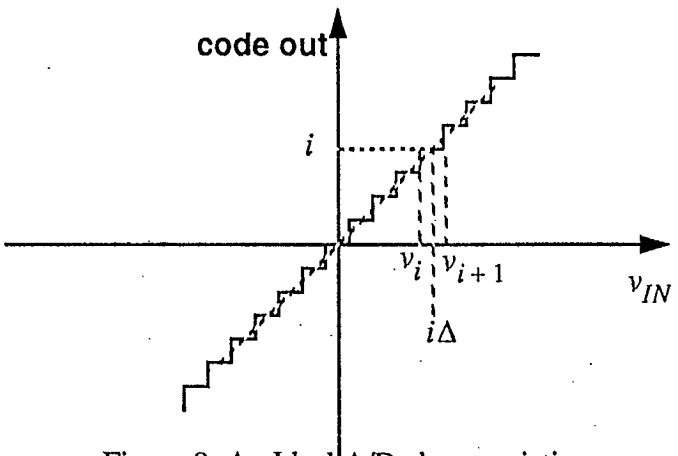

Figure 9: An Ideal A/D characteristic

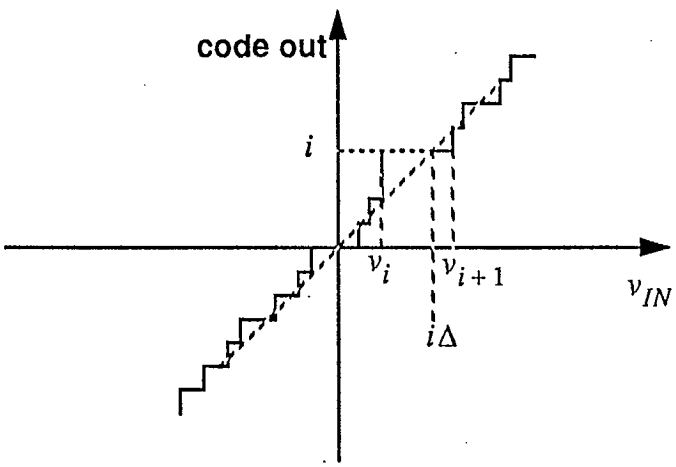

Figure 10: Non-ideal A/D characteristics with high DNL

Mathematically, differential and integral nonlinearity are functions of code output i:

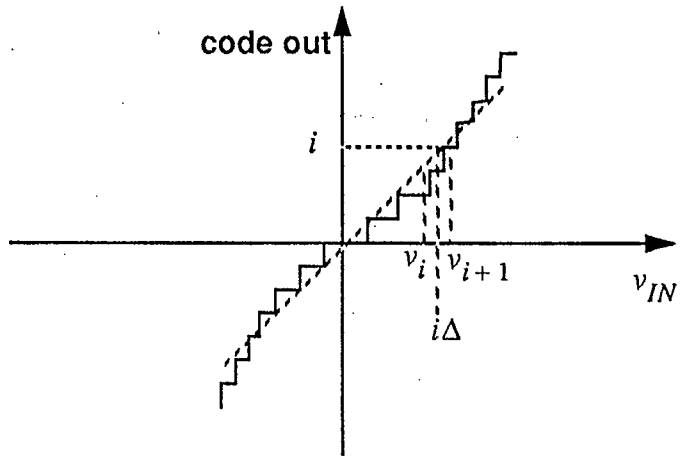

Figure 11: Non-ideal A/D characteristics with high INL

$$DNL_i = (v_{i+1} - v_i) - \Delta \qquad \text{Eq. 8}$$

$$INL_i = i\Delta - (\frac{v_i + v_{i+1}}{2}) \qquad \text{Eq. 9}$$

where Δ is the step size (usually defined after the fact to minimize peak INL, so that gain errors are factored out) and the v_i are input voltages at which code transitions occur as shown in the figures. When a single figure is given for INL or DNL, it is the maximum of the function over i.

Differential nonlinearity usually limits practical resolution in video-type converters, so that typically converters are designed to have DNL levels on the order of one-half of the size of the least significant bit. The importance of DNL is often reduced by oversampling because large input signals convert the resulting error into a nearly-random component. For small inputs, though, it produces large relative amounts of intermodulation distortion products. Adding dither, a random noise component at the input, can randomize this error and convert distortion to (less noxious) noise[6].

Many practical converter architectures have their worst performance at the point where the MSB changes; since that is usually at zero input, where random signals spend most of their time, these converters are used at their worst-case operating point for DNL.

Noise-shaped converters (for details see section below) naturally dither their inputs, so that they usually have lower IM (especially for small inputs) than even an ideal converter. That could be very useful for digital radio. Circuit difficulties, specifically finite amplifier gain, and mathematical peculiarities degrade the effectiveness of this mechanism.

Integral nonlinearity can be input-referred to an equivalent polynomial distortion on the input, a type of nonlinearity familiar to radio engineers. It is not reduced by oversampling, and in many converters (especially video-rate converters) is larger than the LSB in peak magnitude. The nonlinearity of the sample/hold contributes to INL, but component nonlinearities and mismatches contribute too. These internal problems can add distortion terms of high degree, so that while third-order IM can be assumed to dominate conventional RF circuits the same cannot necessarily be said of an A/D. These high-degree terms may be a problem for digital radio, generating exotic mixing products.

The AD9028 converter, for example, specifies 1-bit INL and DNL, while the (slower, more accurate) AD9020 specifies 1 bit of DNL and 1.25 of INL.

Peak DNL and INL are good accuracy measures for instrumentation purposes, but not necessarily for radio. Video converters are often specified in terms of their signal/(noise+distortion) ratio for maximum-amplitude sines.

There are many other measures of nonlinearity: for example, when DNL is large enough output codes can disappear as the range of inputs able to produce them shrinks; converters without this problem are said to have "no missing codes", and any converter with worst-case DNL less than 0.5LSB is guaranteed to have no missing codes. Probably the most interesting such measure for digital radio is **noise power ratio**, which measures the extent to which IM distortion "fills in" a notch in an otherwise white input signal; this would be a good measure of receiver image rejection, but is rarely quoted.

Self-calibration

Some converters [97,98,99,101] obtain high resolution (14 bits or more) by including calibration circuitry. They usually require that the converter be taken off-line during calibration, and are significantly more complex than uncalibrated converters.

The most common technique [101] forces the analog step-size Δ at each bit transition to be correct by measuring it during the calibration phase, then adding compensation components at run-time. In terms of the transfer characteristic, it moves thresholds left or right to their proper positions. These converters have been aimed at the audio market, and so are too slow for digital radio. The general idea could be applied at higher speeds, but video converters haven't usually demanded high resolution. The particular architectures to which self-calibration has been applied have been slow ones, so the details of the technique would have to be changed.

Another technique, not currently in a commercial converter, corrects on the digital side: the output of a nonlinear converter addresses a RAM containing accurate digital estimates of the corresponding analog transitions. In terms of the converter transfer characteristic, it leaves the thresholds where it finds them, but moves steps up and down. The output of the RAM is usually one or two bits wider than the converter data. The RAM is loaded by applying a test signal of known statistics during a calibration cycle. There are two problems with this for digital radio: it doesn't improve resolution, since many of the possible output values become missing codes; and the DSP requirements are increased because the words that must be handled are wider than the useful resolution.

A more recent technique currently under development [21] by Gu and Snelgrove does self-calibration of video converters on-line, moving analog thresholds so as to minimize DNL. It does not attempt to correct INL, but may improve the speed and resolution available in moderately power-efficient converters. If commercially practical, it may be a good candidate for oversampled digital radio in five to ten years. It will still need to be augmented by some technique to correct INL.

Process scaling and device matching

As MOS process technology advances, the minimum channel-length gets smaller. This steadily improves area, speed and power consumption for digital circuits, but analogue circuits do not scale quite as well. Power limits from the need for signal energy to dominate thermal noise are unaffected by scaling, and the amount of energy that can be stored in a given silicon area actually decreases in newer technologies: thinner oxides increase capacitance per unit area but decrease allowable voltages, and because capacitor energy is $(1/2)\,CV^2$ the net result is a loss. The components in newer technologies also suffer from non-ideal effects (like channel-length modulation, velocity saturation, threshold drifts and nonlinearities in passive components) at higher levels relative to the nominal behaviour, and circuit design is increasingly tightly constrained by the low power-supply voltages needed for the new small devices. Further: good matching of, for example, threshold voltages requires large areas even in a small-geometry process [18-].

These effects tend to push the natural division of functions between analogue and digital technologies towards the digital side. This is, of course, a major reason for the interest in digital radio, but it also pushes data converter design towards techniques that rely on digital processing rather than analog precision. This is a long-term force favouring oversampled techniques.

summary

Data converters have very complex nonlinearities, not generally well characterized for digital radio because the converters are designed and tested for other applications. Integral nonlinearity can be expected to be a problem, especially for a 70MHz input signal. Self-calibration techniques have been proposed that may mitigate linearity errors, but they remain to be proven for radio.

6: Oversampling and noise shaping

There are two related techniques, oversampling and noise shaping [63-86], that are important for digital radio. They are often conflated, but should be treated separately. "Oversampling" refers to sampling above the Nyquist rate, while "noise shaping" is a technique that uses feedback to control the spectrum of quantization noise. Noise shaping is most useful in combination with oversampling, and the combination is often loosely called "oversampling".

Sampling above the theoretical minimum rate has two general advantages: it eases specifications on analogue anti-aliasing (for A/D) and smoothing filters (for D/A) and it allows error averaging so that a lower-resolution converter can be used — an advantage of 1/2 bit per octave of oversampling. The disadvantages are that a faster converter is needed and that more computation is needed on the digital side.

From the point of view of converter requirements, oversampling trades speed for resolution. This has strong practical implications, because it gives the system designer a degree of freedom in choosing a converter and because any given technology has practical constraints on the frequency and resolution of which it is capable. The trade-off is in principle neutral as far as power dissipation is concerned, because for a given SNR in a given bandwidth the thermal-noise bound on power (see section 3 above) sees cancelling effects from increased frequency and decreased resolution.In practice it means that the freedom to exchange speed and resolution can be used to choose a converter that is well adapted to its technology.

The effect of oversampling on linearity is more complicated than its effect on noise. When signals are large and spectrally rich, differential nonlinearity may be randomized and so not be a problem; integral nonlinearity, however, can cause intermodulation products that are not affected by oversampling. Getting 12-bit conversion by oversampling an 8-bit A/D would call for an 8-bit converter with INL at the 12-bit level, and these converters do not exist — in fact it is more common that 8-bit converters have INL at the 6 or 7 bit level.

Noise shaping

Noise shaping is a variation of oversampling in which quantizer outputs are fed back, through a filter, to the quantizer input in such a way that feedback controls the spectrum of quantization noise [8]. The resulting circuits are also called delta-sigma, sigma-delta, or bit-stream converters. Figure 12 is a block diagram of the well-known first-order noise-shaped A/D that illustrates the idea.

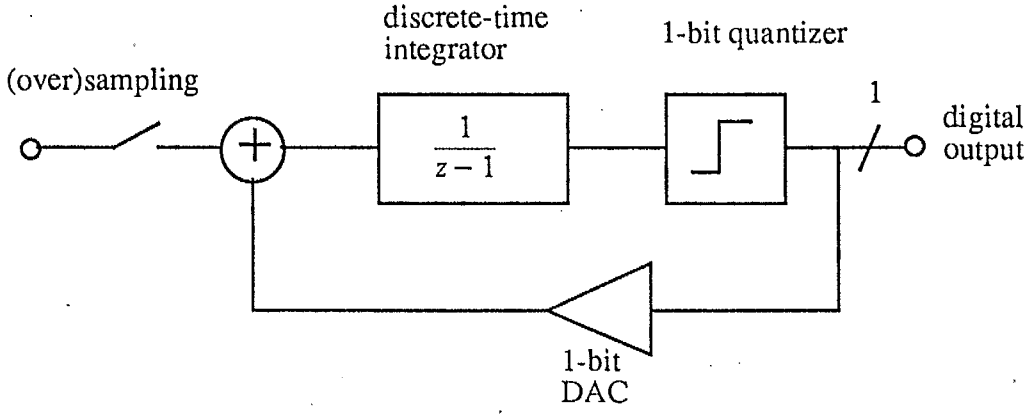

Figure 12: A first-order sigma-delta converter

First, a basic summary of A/D operation: if the signal at the output of the (discrete-time) integrator stays finite (because of the overall negative feedback), then the DC component at its input must be zero; but this means that the DC (average) value of the binary output stream is equal to the DC component of the analogue input. So averaging the binary output with a digital filter gives an A/D converter. The result is an extremely simple circuit (although only exactly described by very sophisticated mathematics) that produces highly linear converters tolerant of a wide range of circuit errors. Finite integrator gain and internal distortions seem to be the dominant problems.

For a first-order converter, linearity is dominated by the linearity of the feedback D/A converter. For this reason, one-bit converters are very popular: a converter that only has to produce two different values is inherently "linear". DNL is in fact very good, though there are second-order effects that can compromise INL. There is still an input sample/hold, so its contribution to INL remains.

A more sophisticated analysis of the first-order circuit [10] shows that the negative feedback does work, and that the feedback attenuates quantization noise in a band around DC. As sampling rate increases the noise shaping is proportionately more effective, so that it yields 1 bit less noise for each octave of oversampling; adding this to the 1/2b per octave gain from ordinary oversampling gives an overall noise-shaped oversampling gain of 1.5 bits per octave. Thus a 280MHz sampler

used in a first-order loop would have approximately 11-bit performance for a 40MHz signal bandwidth around DC (it has almost two octaves of oversampling beyond the 80MHz Nyquist rate, hence almost 3 bits of gain), where simple oversampling gives only about 9 bits.

Higher-order filters can be used, and give better performance; a second-order loop, for example, has a 2.5b/octave oversampling gain. Higher-order loops are also harder to design, as the mathematical theory needed to demonstrate their internal stability does not yet exist. This is a very active research area, and there is no clear consensus yet on attainable performance or best architectures. High-order filters tend, for example, to be stable with high-resolution quantizers in the loop and to dither DAC errors more thoroughly, but low-resolution D/A converters give better linearity. Despite their novelty and the difficulty of design, these converters are already dominant in high-linearity applications at moderate speed and should be taken seriously for digital radio.

Decimation

The high-rate digital signals from sigma-delta modulators are generally filtered and decimated down to baseband, and the DSP to do this has to be counted in the power budget. On the other hand, this filtering partly replaces analog anti-alias filtering, giving something back for this power. The decimators can be simple, because the input streams are narrow — usually only one bit wide. The two techniques used in commercial codes are

1 - sinc^n filters made up of counters and accumulators [9] which give simple implementations of mathematically simple impulse responses like triangles, and do a first-cut decimation which is followed by a conventional recursive digital filter.

2 - general FIR filters implemented with ROMs and adder/subtracters [76,68].

bandpass

Conventional sigma-delta converters shape noise away from DC, making them good candidates for baseband codecs in radios or for the conversion required in a zero-IF receiver. A very new technique [3,12,13,14,63,67] adjusts the filtering to move noise away from a passband, typically centred around $f_s/4$. A second-order bandpass sigma-delta converter behaves much like a first-order lowpass converter, so that 11 bit performance in a 40MHz band could be expected from noise-shaping a 280MHz 8-bit converter.

The first monolithic bandpass converter has just been fabricated [63]; it is a switched-capacitor device which provides fourth-order noise shaping of the noise from a 1-bit quantizer and can clock at up to about 3Mhz. It is intended to do 13-bit conversion of AM bandwidth signals centred around

455kHz. It is a two-channel part, for historical and research reasons. A simple approach to decimation, by modifying an existing decimator [76], would bring total power consumption to 450mW/channel. Both power figures can be improved radically: power was not considered a major issue for the experimental device, and a factor 10 improvement would probably be easy enough to get.

The power, speed and resolution characteristics of bandpass converters are likely to be very similar to those of lowpass converters with similar bandwidths, so the lowpass literature can be monitored for an idea of the performance to expect. The ISDN converters in figure 1, with bandwidths ranging from 80 to 120kHz bandwidths, 10-15MHz sample rate, and 11-14-bit performance at 15-75mW, are good benchmarks. Though not commercially available, the experimental converter by Brandt and Wooley [65] is a particularly close fit: it clocks at 50Mhz, has 75dB SNR over a 1MHz bandwidth, and the analogue portion dissipates only 41mW (they only fabricated that part, so that there is no figure available for the power required for the decimator; this is likely to be in the 100mW range). This converter can be taken as a demonstration that the 1.25MHz bandwidth converters required by CRC are now feasible with 12 bits of resolution and perhaps 100-200mW of power.

The major differences between lowpass and bandpass noise-shaped converters will likely come from bandpass designs having a more difficult sample/hold problem (because of the high-frequency content of the input signal) but less trouble from 1/f noise in the input stage. The 1/f problem forces lowpass designs to use large input amplifiers at high resolutions, which wastes power and reduces speed.

There are also preliminary reports of high-speed bandpass modulators (clocking in the hundreds of megahertz) using continuous-time filters — discrete LC resonators. Descriptions in the open literature are still sketchy. Mathematical studies [15] suggest that these may have resolution limited by the Q available in the resonators, unless positive-feedback techniques are used.

While bandpass noise-shaping is a specialized research area, there is a good deal of industrial and academic interest and rapid development can be expected.

summary

Oversampling is a valuable technique that allows the system designer to trade speed for resolution and move some anti-alias filtering to the digital side of a system. It can be combined with noise-shaping, and a very recent version of this combination looks very promising for obtaining high resolution at low power for a moderate IF with present technology. Application to a 70MHz IF will be difficult in switched-capacitor technology, but the use of LC or other resonators might allow a breakthrough.

7: DAC Circuits

Digital-to-analogue converters are of interest for use in digital radio both in their own right and because A/D architectures often contain D/A subconverters. D/A converters are already available that are fast enough for digital radio and dissipate little power [22].

Oversampling techniques work for D/A as well as A/D, and have the same effects of moving complexity from the analogue to the digital side. Noise shaping is also used, particularly for digital audio, although it adds large amounts of out-of-band noise that must be filtered on the analogue side. At high speeds, non-feedback circuits are used, and three general types are in widespread use: resistor-string, charge redistribution and current-mirror. These can be used in combination.

Resistor Strings

Conceptually, the simplest type of DAC consists of a string of resistors between two voltage references, with switches connecting the output to an appropriate point as shown in figure 13. Digital circuits are responsible for converting a binary input to a "one-hot" code to select the right tap.

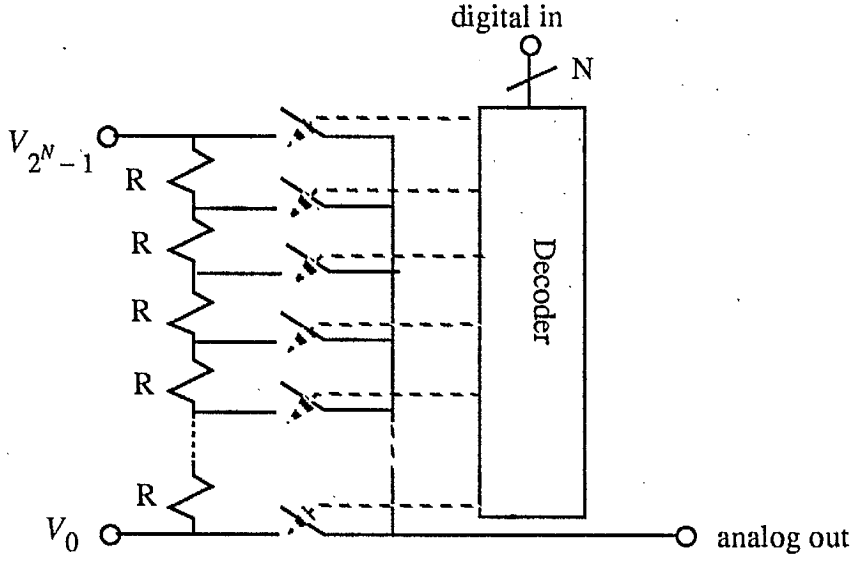

Figure 13: A resistor-string D/A

Differential nonlinearity is very low in these D/A converters [7], because adjacent resistors are likely to be well-matched so that voltage steps are nearly equal [7]. Integral nonlinearity comes from

- resistor nonlinearity: the value of a resistor implemented in a monolithic process often depends slightly on its bias voltage above the substrate, as bias depletes the

resistor material of carriers. This produces a nonlinearity that is dominantly second-order.

• output current: the output impedance of the string is low for codes near the top and bottom of the array and high for codes in the middle. This nonlinear output impedance, multiplied by output current, gives a (dominantly) third-order characteristic. Reducing the values of all the resistors reduces this effect, and 1Ω resistors are common [62]. This costs power.

• nonlinearity in the sample/hold used to de-glitch the output.

These converters dominate for producing the reference voltages for high-speed A/D converters, partly because they can produce many outputs simultaneously. Their INL performance therefore contributes to the INL of high-speed A/D, and their power consumption accounts for 10-100mW of an A/D power budget.

Weighted capacitor array DACs

A switched-capacitor technique for D/A conversion uses a binary-weighted array of capacitors as shown in figure 14. After being charged to a reference voltage, a subset of capacitors is switched to the op-amp virtual ground transferring charge to the output. These are sometimes known as charge-redistribution ("QR", occasionally) converters.

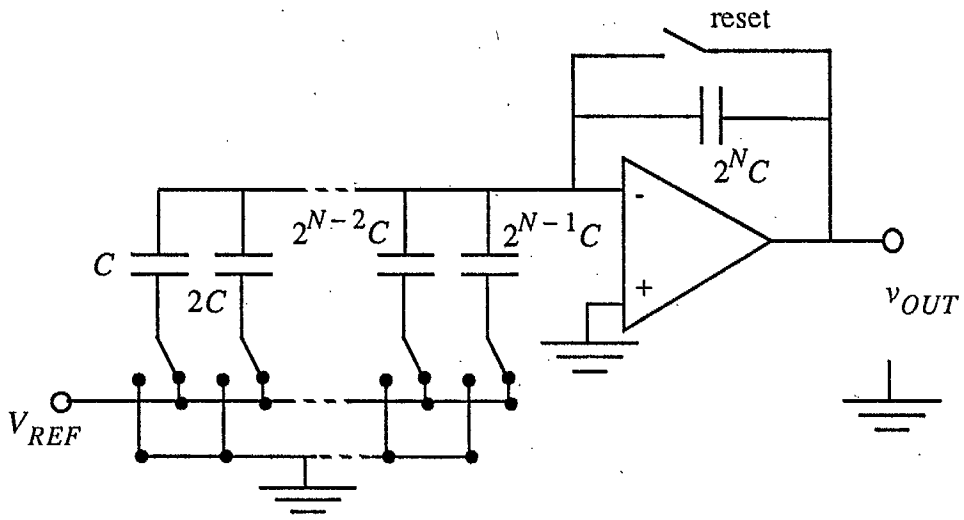

Figure 14: A switched-C D/A with binary-weighted capacitors

The large capacitors in these converters are actually constructed as arrays of unit capacitors, so that although the number of capacitors in the schematic is linear in the number of bits in the converter, the number and area of capacitors fabricated is exponential in resolution, just as for the resistor string. These converters have differential nonlinearity dominated by capacitor mismatch at the most-significant bit transition: for example, in an eight-bit converter, the code 0x7f switches in 127 capacitors while 0x80 switches in 128 *different* capacitors, which may not be quite the right size. The alternative is to use a thermometer-code switching arrangement [28] as for resistor strings, which requires an exponential number of switches. The integral nonlinearity in these converters comes primarily from the same mechanism as the DNL, as long as the amplifier has a large enough output swing.

Current process technology, with careful layout, allows 10-12 bit accuracy in these converters [16]. There is no reason to think that this will improve very much with newer technologies. Charge-redistribution converters have been the standard at audio rates for telephone-quality resolution, and are also widely used internally in CMOS A/D converters.

Binary-weighted current sources

Two bipolar transistors with equal base-emitter voltages and equal areas produce approximately equal collector current. By connecting transistors in parallel, binary-weighted current sources can be obtained, and these currents can be switched into an output or to a supply to obtain a D/A as shown in figure 15.[1] The notation "4x" just means that four unit devices are in parallel. The reference voltage needed for all the base-emitter junctions is usually obtained by driving a reference current into a transistor connected as a diode, as is Q1 in the figure. This arrangement is called a current mirror, since Q2 etc. "mirror" the reference current in Q1, scaled by the ratio of device sizes.The accuracy of matching between input and output currents is limited by base currents, output impedance and area mismatch between Q1 and Q2. More sophisticated mirrors exist which reduce the importance of base current and output impedance.

Just as for capacitor arrays, a thermometer-code switching arrangement can be used to control DNL.

[1] In principle it is good enough to scale the junction areas of the devices, but the most accurate way to scale areas in the presence of lithographic errors and edge effects is to connect identical units in parallel, just as is done for capacitors.

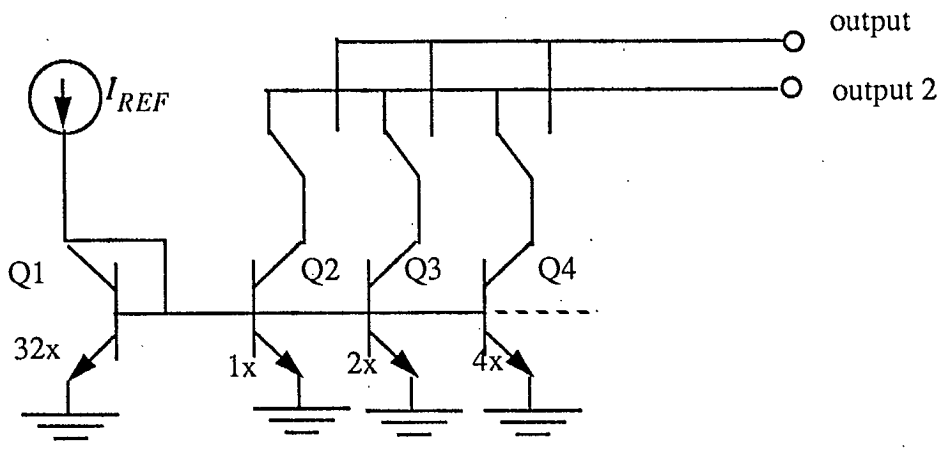

Figure 15: A D/A with binary-weighted current sources

Current mirrors can be made with silicon MOSFETs and GaAs MESFETs as well as bipolars, but the matching between devices is poorer in FETs because threshold voltages contain a large random component from fixed charges at the gate. MESFETs are also worse than MOSFETs by about 2 bits [36]. This mismatch forces the use of large FETs, where random variations are averaged over a large gate, to get high accuracy. Short-channel FETs also have low output impedance, which makes matching worse. MOSFETs, of course, have no base currents to cause gain errors, while MESFETs have extremely low gate current while properly biased.

The need for an exponential number of transistors can be avoided by cascading current mirrors with binary-weighted gains [26], but the number of bits that can usefully be obtained is not in any case very large.

These converters can be extremely fast, when the output desired is a current, because there are no high-impedance nodes in the circuit. Conversion from current to voltage costs speed or linearity.

This is the dominant technology for video-rate D/A conversion.

Sampled-current

A new technique [27,137,140] uses a single switched transistor as a **current copier** (a type of current mirror) as in figure 16. The device is initially diode-connected on ϕ_1 and driven by a reference current; this establishes a voltage on the gate capacitance which is held during ϕ_2 and keeps the transistor running at the right current when its output is switched to the load.

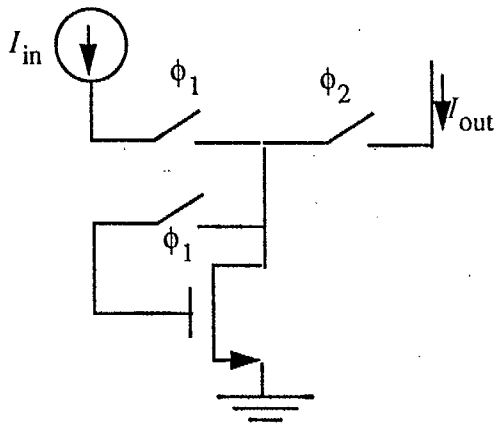

Figure 16: A simple current copier and its clocks

Currents may be added at a node, so that an accurate gain of two can be obtained by repeatedly copying a single reference and adding the resulting currents. Present art gives accuracies up to 16 bits at speeds from 50kHz to 1MHz with power dissipation in the tens of milliwatts, but the technology is too new for these values to be interpreted as representative of the best that could be obtained. Speeds probably are better than for switched-capacitor, but this has yet to be clearly demonstrated.

The technique does not require linear capacitors or well-matched devices, and so is well-suited to processes optimized for digital circuits. This may become a strategic advantage.

segmented D/A

High-resolution D/A converters often use a combination of techniques, with the more significant bits being converted one way and the less significant ones another [25,26,29]. For example, the upper bits can be produced with a resistor string that provides reference voltages for a charge-redistribution converter.This approach is called segmented conversion, because the overall conversion range is divided into segments by the coarse conversion. This technology can be used to ensure D/A monotonicity but does not guarantee good INL.

While segmentation techniques are important for D/A, they are not commonly used as components of high-speed A/D and are therefore not covered further here.

8: Broadband ADC Architectures

There are several common architectures for A/D conversion, ranging from "flash" architectures that trade everything for speed to highly precise low-speed structures that make heavy use of averaging. In any given technology, converters operating below a certain frequency can be quite power-efficient, but beyond that point architecture and bias decisions have to be made that burn far more power than required to overcome thermal noise.

As well as differing in power efficiency, the different architectures have different problems with linearity.

Flash

Flash (or parallel) converters [30-61]have $2^N - 1$ clocked comparators, each comparing the input signal to a distinct threshold level, as shown in figure 17. Digital logic is used to convert the resulting thermometer code to a one-hot code and thence to binary. This "brute-force" approach is very fast, and so flash converters dominate the high-speed end of the speed/resolution plot of figure 1.

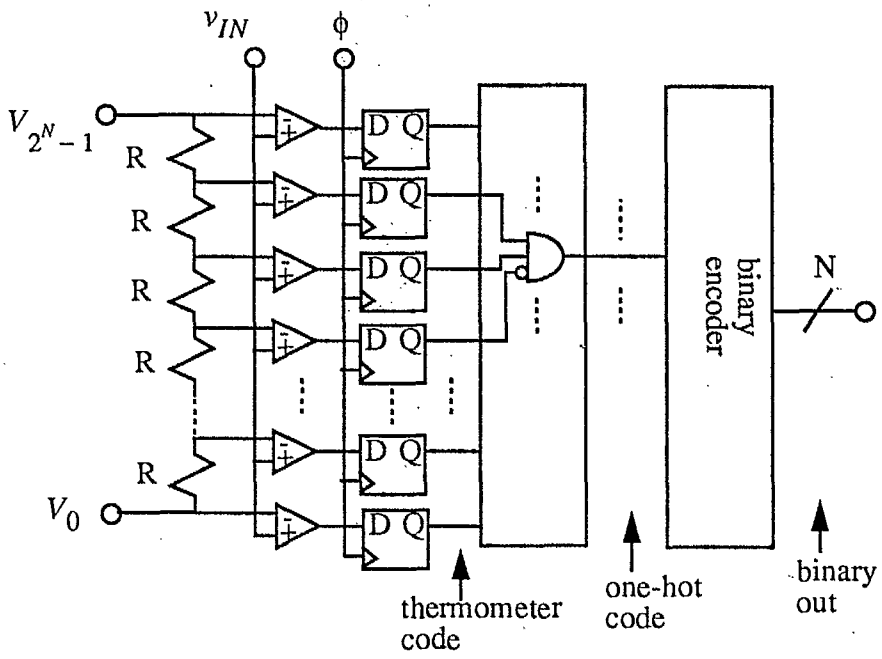

Figure 17: A simple flash A/D

Since the number of comparators in these converters is exponential in resolution, they quickly dominate the power budget, and are rarely used above 8-bit resolution (again, cf. figure 1).

The fastest flash converters have no explicit sample/hold circuit, but in these devices the comparators contain implicit samplers. This approach just multiplies the difficulties of sampling, since individual sample/holds are not perfectly matched and the clocks that they receive are skewed. For fast-slewing input signals in particular, because effective sampling instants are different at each comparator and because of the high sensitivity of A/D conversion to timing errors, large distortions can result. The SNR of these converters therefore deteriorates for high-frequency signals, and signals above 100MHz show distortion significantly worse than 8-bit performance in state-of-the-art converters.

When the sample/hold is distributed, the input signal has to drive a very large number of comparators, and so the input capacitance is usually large and an input buffer is needed. This alone costs a good deal of power. Each comparator has to have a large enough sampling capacitor so that $(kT)/C < \Delta$, which means that flash converters necessarily consume a factor of 2^N more power than the "one-sample" bound of equation 3.

The comparators in a flash converter all draw dynamic current from the resistor string used to generate the reference voltages, and linearity requirements force the resistors to be on the order of 1Ω each [62].

Multistep

Multistep (or "subranging") converters [102-126] do a rough conversion with a reduced-accuracy ADC ("subconverter"), then use a DAC to subtract the rough estimate from the original analog signal and use another A/D subconverter to estimate the residue. The most common types are two-step (or "half-flash") converters in which two 4-bit subconverters are used to make an 8-bit ADC. A generic block diagram appears in figure 18. These are slower (very roughly by a factor of two) than pure flash converters because there are two steps involved, but use only 2.2^{N+2} comparators — saving a factor of 8 for 8-bit conversion and 16 for 10-bit conversion. Subranging converters can be seen (figure 1) to form the next group slower than flash converters, and are common at about 10 bits of resolution. They tend to be implemented in CMOS, while the pure flash converters tend to be bipolar parts because they are aimed at the highest-speed market. This difference helps explain why two-steps are typically a decade slower than flash devices.

The DAC can be a charge-redistribution device or a resistor ladder. One of the commercial parts closest to fitting the needs of digital radio [108] uses a single resistor ladder both to provide reference voltages for the ADC's and as a DAC, as shown in figure 19. This device wins back some of

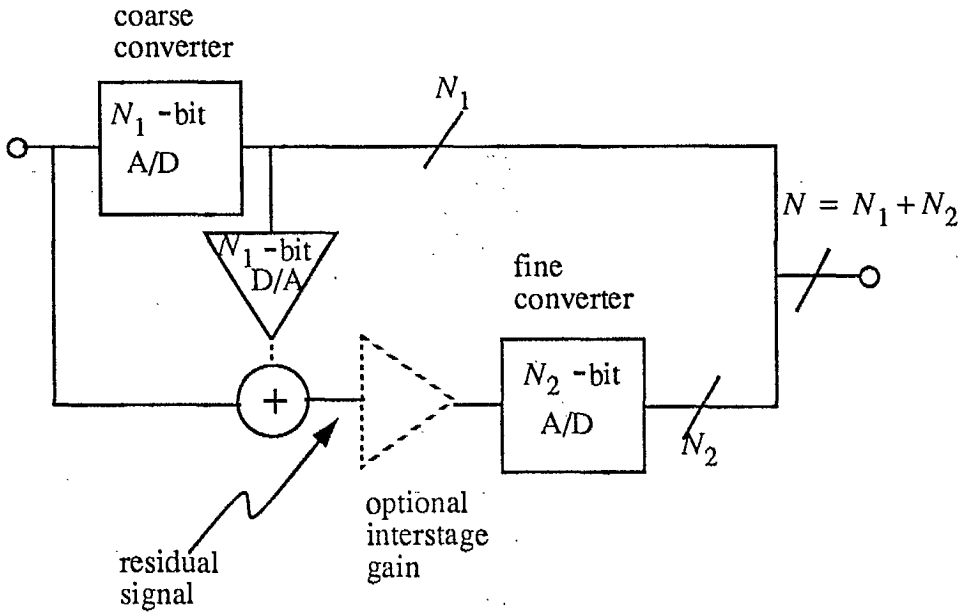

Figure 18: A two-step converter (block diagram level)

the speed lost by two-step operation, at a cost of a factor 2 in power, by alternating between two banks of comparators to make each A/D subconverter — a kind of subsampling that is prone to pattern noise at $f_s/2$.

Interstage gain

When a charge-redistribution DAC is used in a two-step converter, there is generally an op-amp gain stage to do the subtraction. This can have gain, and then there is a trade-off between accuracy and speed: at high gains the amplifier is slow (gain-bandwidth product is roughly constant in op-amp circuits), but at low gains the output signal is small and offset voltages in the fine converter have a worse effect on linearity. The fastest two-step converters have no interstage gain and are no better than flash converters in accuracy.

digital error correction

Nonlinearity in the "coarse" subconverter of a two-step A/D need not matter, as long as the "fine" converter can compensate for it. Figure 20 shows how the residue signal at the input of the fine converter is related to the overall input, without and with errors in the thresholds of the first subconverter. No information about the input has been lost, even with threshold errors, and so by converting the residue accurately it is still possible to calculate the original input. The fine converter needs to be able to handle a larger input range (and so will use a few core comparators) and a binary

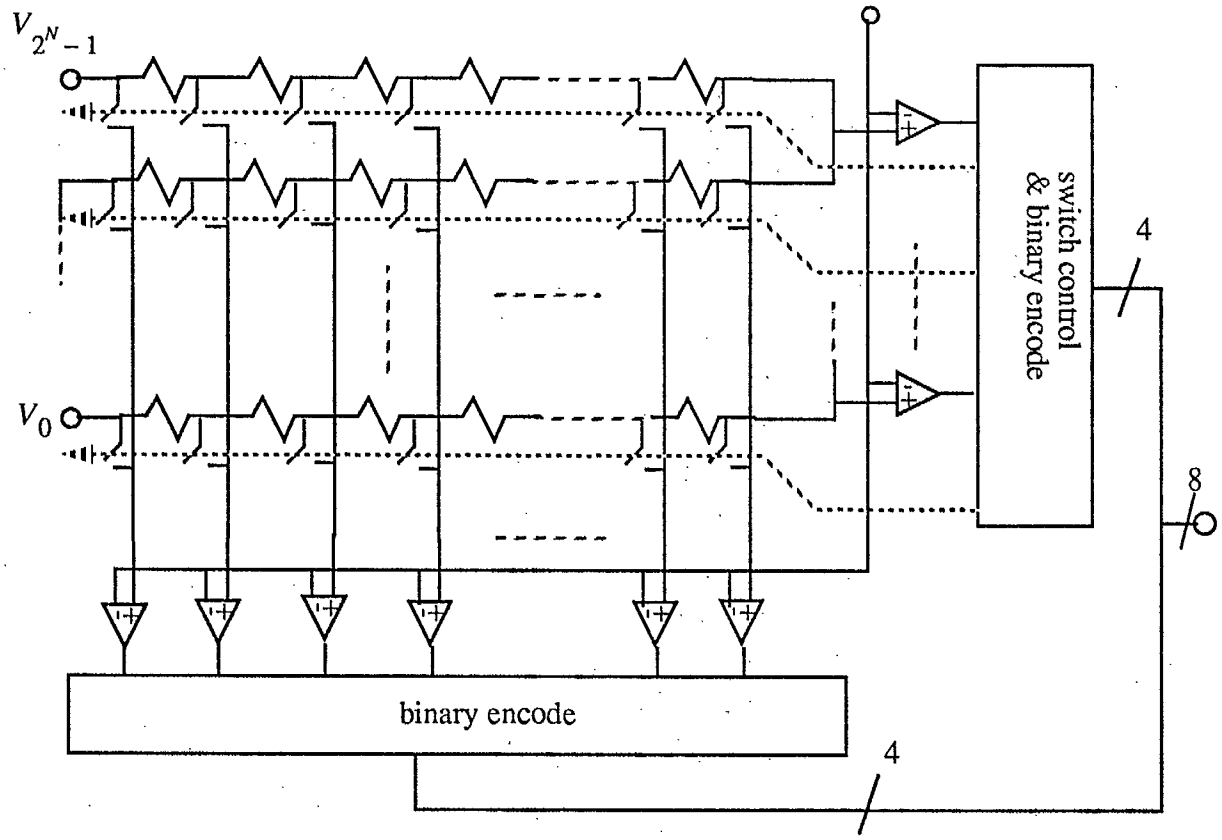

Figure 19: A two-step converter using a resistor-string DAC

addition $D = 2^4 D_1 + D_2$ has to be done. This technique is called digital error correction and is commonly used in modern converters. In principle it means that a two-step A/D with $2N$-bit accuracy can be built in a technology that only provides N-bit subconverters.

In practice, improvements in resolution are much smaller: digital error correction still assumes that the DAC is ideal, and doubling the accuracy of the subconverters would require interstage gain so that the second converter could see large signals. Inaccuracies and offsets in the interstage gain are not compensated either. These converters have been reported running at 75MHz with 10-bit resolution [111,112], good specifications for digital radio with a moderate IF, but at power over 2W. The 1988 design from Hitachi [108] ran at 8 bits, 20MHz and 200mW; in a more modern process it could be expected to improve both resolution and speed at roughly the same power, and would be a good candidate.

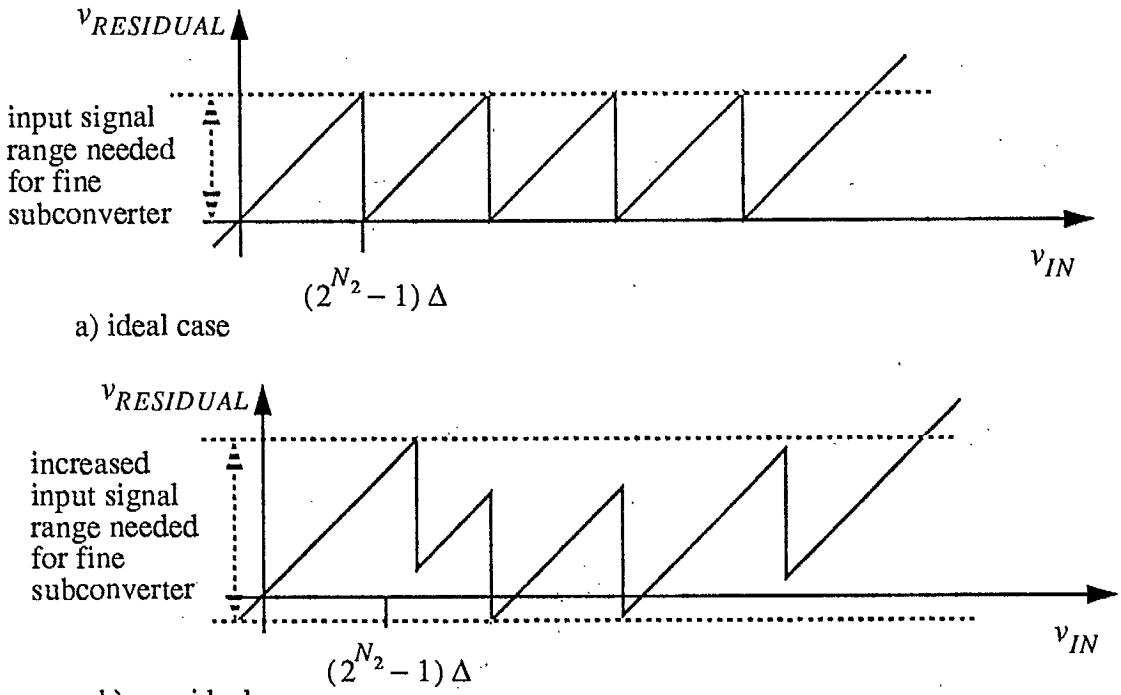

Figure 20: The transfer characteristic from input to residual: ideal and non-ideal coarse A/D

Folding

"Folding" converters [38,39] use nonlinear shaping circuits based on cascades of BJT differential pairs to generate residual signals directly, without passing through coarse A/D and D/A. The technology is not widespread, so it is difficult to know how mature the designs are as compared to flash and two-step designs, but converters have been fabricated and appear to be generally competitive with two-step converters in terms of speed, complexity and power.

Pipelined

Adding sample/holds between the stages of a multistep A/D gives a pipelined architecture [127-136], in which the second stage is doing a fine conversion on sample $k-1$ while the first stage does a coarse conversion on sample k. In the extreme case, an N-stage pipeline uses only N comparators, and the $N-1$ interstage amplifiers consume most of the power. Because of the samplers, increasing the number of steps does not slow down the converter.

The cost of adding pipeline samplers to a multistep converter is low, but they do cost settling time. Two-step converters therefore may or may not benefit from pipelining, but multistep converters with more than two steps are usually faster when pipelined. So the availability of pipelining means that in practice "multistep" means "two-step".

Digital error correction can be used with pipelined converters [127,128], and interstage gain can be used to exchange power for speed. The accuracy of these converters is dominated by the accuracies of the amplifier and DAC of the first stage. A state-of-the-art pipelined converter in 0.9μ CMOS [127,128] has 10-bit accuracy at 20-30MHz and consumes about 200mW. Its INL has an interesting structure, because the way in which error correction is done puts the largest errors at $\pm 1/3$ of full-scale rather than at the zero crossing: this may give it better performance than other converters with similar linearity specifications when the input has, for example, Gaussian statistics. A faster revision of this device, perhaps at lower resolution in order to save power, would probably satisfy the digital radio requirement for an IF sampled at 80MHz.

In feedback applications, pipelined converters may be difficult to use because they delay their outputs by several samples (the number of stages). For example, they do not naturally fit as the Nyquist subconverters of a noise-shaped feedback converter.

A study by Lee [11] derived bounds for the power efficiency of pipelined converters, accounting for the fact that they have multiple samplers and amplifiers with class AB outputs. The bound for converters with N identical stages is

$$\frac{2^{2N}}{\text{energy/sample}} < \frac{V_{DD}/(2kT)/q}{1152NkT\,(N\ln 2 - \ln 1/8)} \qquad \text{Eq. 10}$$

which, for an 8-bit converter with a 5V power supply, gives a bound on figure-of-merit of

$$\frac{5/0.052}{1152\,(8)\,1.6\times10^{-19}\,(0.026)\,(8\log 2 - \log 0.125)} = 3.2893699\ldots\times10^{17}\,\text{Joules}^{-1}$$

This in turn would correspond to

$$\frac{65536}{3.2893699\ldots\times10^{17}}280\times10^{6} = 55.786003\ldots\mu\text{W} \qquad \text{Eq. 11}$$

in a 280MHz 8-bit converter — still very much better than necessary for digital radio.

The best pipeline converters (see figure 5) are still about 2 orders of magnitude below this limit, partly because it can only be reached by operating at bias levels that would limit conversion rate to a few MHz with present MOS technologies. They could be efficient at higher speeds in bipolar technologies, but they have been implemented in CMOS because pipelining is much easier there. The new BiCMOS processes may allow radical improvements in power efficiency for these converters at high speeds, making them appropriate for digital radio, by mixing bipolar amplifiers with CMOS sampling.

Algorithmic and Successive Approximation

Successive-approximation converters [87-101] use a single comparator and an N-bit DAC in the feedback loop of figure 21 to do a kind of multistep conversion. They take N settling times to do a conversion, just like multistep converters, but are cheap on hardware, as only one comparator and DAC are needed. Reference to figure 5 shows that these are the most power-efficient A/D converters available. Resolution is limited by the DAC, but the architecture is popular at roughly the 12-bit level. These converters are widespread in commercial practice, most running below 1MHz.

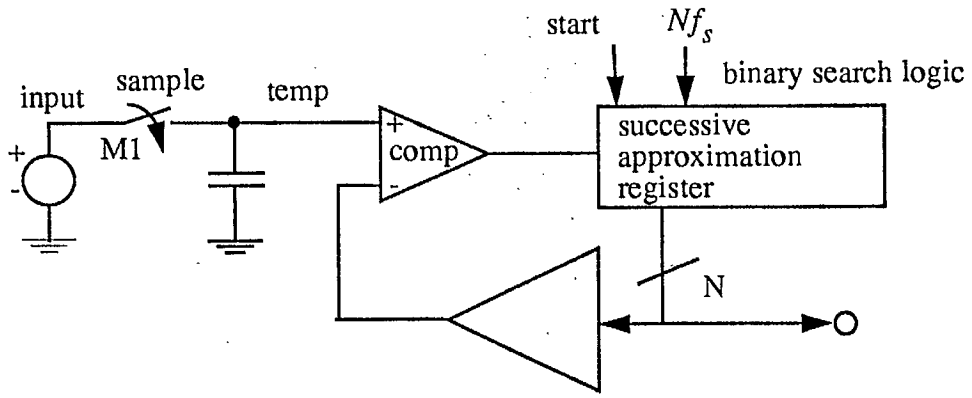

Figure 21: A successive-approximation converter

Algorithmic converters [4,137-147] calculate the residual signal (as in a multistep converter) and recycle it through a simple loop as shown in figure 22. They can be very power-efficient, but take N settling times to do a conversion and so are also too slow for digital radio. Accuracy is limited by the amplifier gain and offset, and is typically in the range from 10 to 13 bits. "Unrolling" them to give N stages gives a pipelined converter.

Algorithmic and successive-approximation converters are obviously very similar, since both cycle analog signals past a single comparator. Successive-approximation converters experiment with different comparator references against a fixed input, while algorithmic ones circulate both the reference and an input signal. The algorithmic type contains only a 1-bit DAC, but has a more

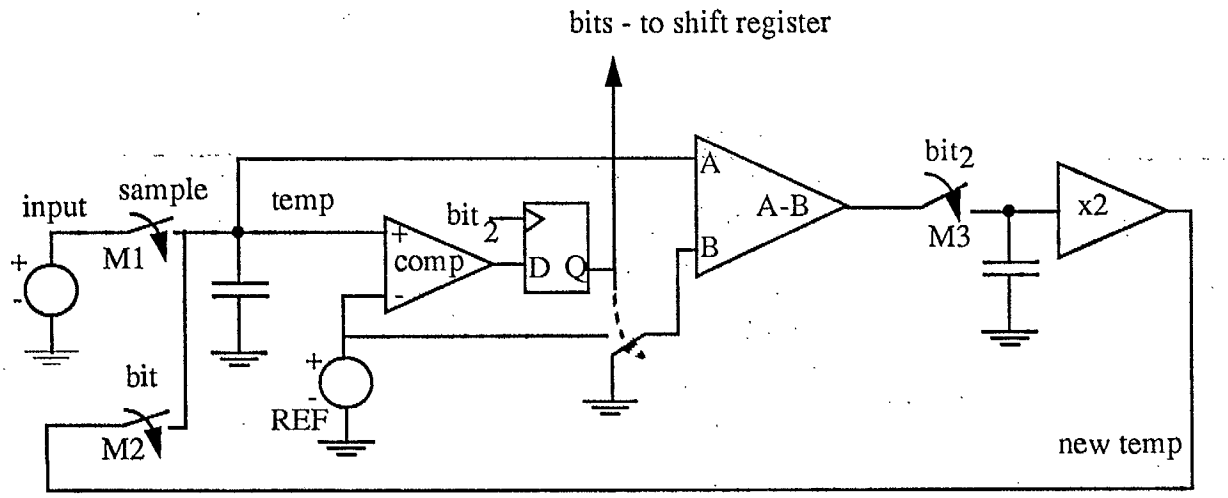

Figure 22: An algorithmic converter

complicated signal path and is not as widespread in commodity converters. They do not seem to be likely candidates for digital radio until very much faster technologies are available, although heterojunction bipolar technology might make an 80MHz successive-approximation converter possible.

Counter-based

Older instrumentation converters known as "slope-type" or integrating converters [148-151] compare the input to a sawtooth signal of known slope while counting at a high speed: the digital output is the count when the reference crosses the input. Sophisticated versions use multiple slopes. The fastest converters of this type are early digital-audio parts [150], with 16-bit resolution at 44kHz. These seem to have no prospect of becoming fast enough for digital radio. Though slow, they can have accuracies beyond 20 bits.

linearity

Different converter architectures have different characteristic nonlinearities. Flash converters have essentially random DNL, as each comparator has a different threshold; multistep converters (and their close relatives, pipelined and algorithmic converters) have large DNL at the voltages corresponding to transitions of the first subconverter, then geometrically smaller DNL contributions at the transition voltages of later stages. These steps are often consistent in direction, because an important contribution to them is made by the finiteness of op-amp gain; this means that residual sig-

nals tend to be systematically too small and that thresholds are systematically too close near these particular voltages. When signals are particularly sensitive to zero-crossing distortions, multistep converters can systematically operate near their worst-case behaviour.

Integral nonlinearity is contributed by the input sample/holds of all converters. The resistor strings used to produce reference voltages also produce INL in several types of converter. Because there is a systematic structure to the DNL in multistep converters, there is corresponding systematic INL.

summary

Flash converters, although already fast enough for digital radio, consume power that increases exponentially with increasing resolution. Consequently they are not likely to be practical in handheld digital radio unless very low resolution is acceptable, but are practical in base stations and vehicular radios. They have severe INL problems, especially when the input signal has a high slew rate, which may limit radio performance.

Pipelined and two-step converters are much more power-efficient and a small constant factor slower than flash parts. Power efficiency for the best converters is good enough for handheld radio. They are likely to be the winning architectures if broadband A/D conversion is required. Op-amp performance and component matching limit linearity for these converters to the 13-bit level. Folding converters are relatively experimental but may also be competitive.

9: ADC Subcircuits and their Performance

Practical A/D converters spend power on reference voltages, amplifiers, comparators, internal logic and output drivers. Consumption levels quoted in technical papers and specifications often ignore some of these components, making comparison and design difficult. Many of the circuit issues are common to all A/D architectures.

logic and pad drivers

Regardless of the structure of A/D converter used, driving the lines on a circuit board takes substantial power. A converter that drives N output lines, each with capacitance C, with random data at a frequency f between V_{DD} and ground discharges energy $(1/2)\,CV_{DD}^2$ on $(Nf)/2$ lines each second, for a total pad-driving power of:

$$P_{\text{pad}} = \frac{N}{4} CV_{DD}^2 f \qquad \text{Eq. 12}$$

For an 8-bit 280MHz converter running from 5V supplies, this comes to 140mW. Large power savings are to be had by reducing the supply voltage (a 3V supply reduces this by 64%) and by reducing the load capacitance with, for example, multichip modules or by doing later processing on-chip.

Internal logic is usually quite cheap on power, partly because very small capacitances are involved and partly because converters have generally had quite simple logic. Minimum-size transistors in a 1μm process have about 2fF of gate capacitance; driving a 10fF logic gate in a 5V technology costs 125fJ (125nW/MHz). A 1mW/MHz power budget allows for one to ten thousand gates.

Transistor speed and power consumption

The basic limit on converter speed comes from device f_t, the frequency at which the power gain of the transistors provided by a process has dropped to unity. The sampling rates attainable with an A/D are typically about an order of magnitude below this frequency, for a variety of reasons outlined below. For both bipolar and MOS transistors unity-gain frequency is a function of bias current, with the general shapes shown in figure 23. Since f_t increases with current, fast converters are operated at high current levels and therefore consume more power.

For data conversion, we expect speed to cost power (recall figure 2 and the energy/sample bound of equation 3). To see the effect of the speed-bias relationship on speed/power *efficiency*, we should plot f_t/I_{bias} against I_{bias}. These plots are also sketched in figure 23.

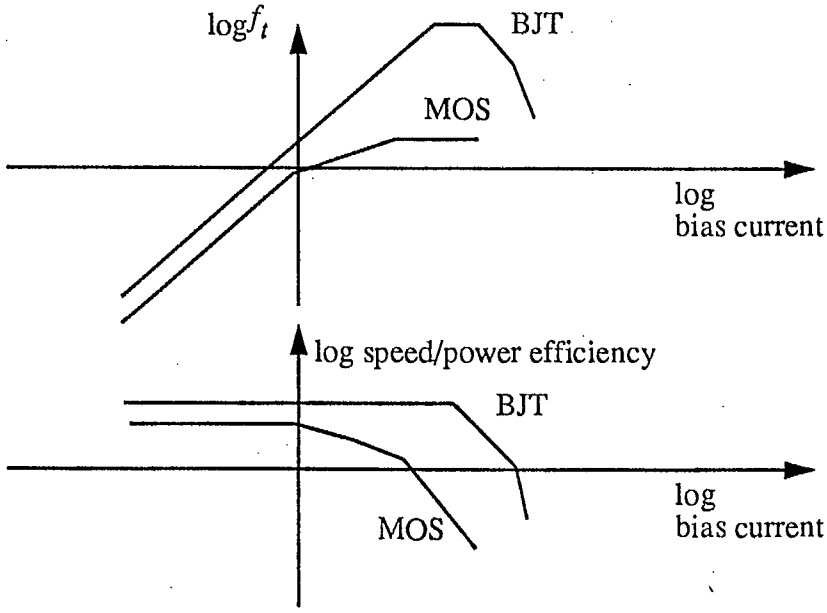

Figure 23: Unity-gain frequency and speed/power against bias current for BJT and MOS

For bipolar devices speed/power efficiency is approximately flat up to a critical bias level, where Kirk effect causes it to fall off catastrophically as f_t starts to drop. A/D converters implemented with bipolar devices therefore operate up to the maximum device f_t without a power penalty. Unity-gain frequencies around 10GHz are typical of a good modern process. Experimental heterojunction bipolar transistors are almost ten times as fast, but that technology is still exotic and should not be expected to be practical for large production circuits for several more years.

In bipolar technologies, the value of speed (and the lack of an efficiency penalty) drives designs to run at the highest practical bias levels. For typical production bipolar and BiCMOS processes a minimum-size BJT needs about 100μA to reach its best f_t of about 10GHz. With 5V power supplies, it takes only 200 transistors running at this level to consume 100mW.

For MOS devices at low bias levels, in which the devices are operating in subthreshold or weak inversion mode, speed/power efficiency is approximately constant; above that, when the devices are operating in strong inversion, the power efficiency drops off steadily with increasing bias level. In weak inversion MOS devices are very similar to bipolar transistors and have a unity-gain frequency proportional to bias current and hence constant power efficiency. In strong inversion, on the other hand, the unity-gain frequency is only proportional to $\sqrt{I_{\text{bias}}}$ and higher frequencies are obtained only by paying a penalty in speed/power efficiency. At even higher bias levels, a short-channel MOSFET enters velocity saturation and f_t becomes constant, so that the efficiency drops off even faster. The bias level at which the critical "corner" from weak to strong inversion occurs is roughly that corresponding to an "on-voltage" $V_{GS} - V_t \approx 2kT/q \approx 52\text{mV}$.

The maximum *efficient* f_t can therefore be related directly to process parameters as follows:

$$2\pi f_t = \omega_t \approx \frac{g_m}{C_{gs}} \approx \frac{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)}{(C_{ox} WL)/2} \approx \frac{4\mu}{L^2} \frac{kT}{q} \qquad \text{Eq. 13}$$

This means that a rapid improvement of the speed of efficient MOS converters can be expected with improving technology, as L steadily decreases. For a reasonably current process with $L = 1\mu\text{m}$, the efficient f_t for the n-type MOSFET is about

$$\frac{4}{2\pi} 26\times10^{-3} \frac{0.066}{10^{-12}} \approx 1\,\text{GHz} \qquad \text{Eq. 14}$$

while in a 0.5μm process, probably typical of the mid '90s, the figure would be around 4 GHz. P-type devices are about a factor of three slower, and in many circuits limit speed.

Running at high bias levels, MOSFET f_t is limited by velocity saturation. 1μm MOSFETs typically have a maximum f_t of about 2-3GHz.

comparators

Figure 24 shows the circuit at the heart of a simple CMOS latched comparator — basically a RAM sense amplifier. A loop consisting of two cross-coupled inverters is turned on by switch M1, after which positive feedback amplifies any difference voltage between nodes X and Y until a result big enough to handle digitally is obtained; then M1 turns off and shorting switch M2 is used to reset the circuit so that it "forgets" what it did on the last sample.

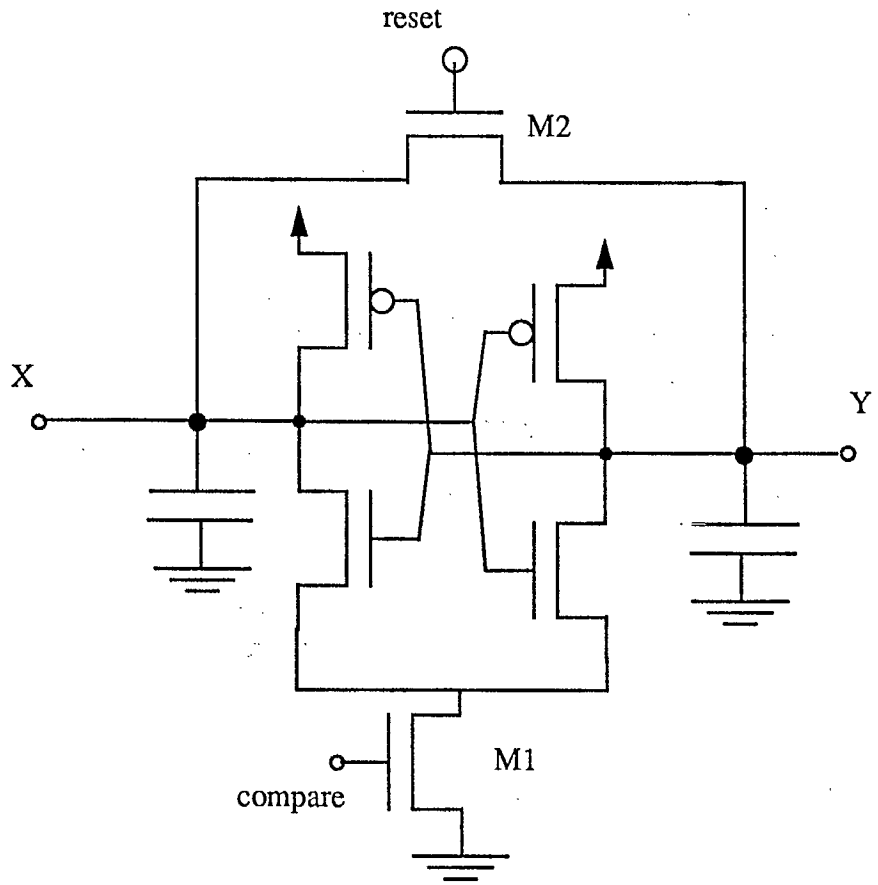

Figure 24: A simple CMOS sense amplifier

Both the positive-feedback latching and the reset phase have exponential voltage with time, and the time constant is somewhat longer than $\tau = 1/\omega_t = 1/(2\pi f_t)$ because of the number of transistors involved, the presence of (slow) p-channel devices in the signal path and layout parasitics. Allowing six time constants for both amplification and settling and a factor of five penalty below f_t for the overall circuit gives a maximum speed of about 100MHz for a 1μm technology.

The power dissipation of this MOS comparator is dominated by its dynamic component. Estimating that it would dissipate the power of a pair of CMOS logic gates gives a figure of about 250fJ.

A full comparator consists of a sense amplifier driven by two or three simple differential-pair gain stages, because better switching speeds are obtained with a cascade of low-gain high-bandwidth stages. The gain stages also dissipate power, and are biased according to the considerations in the "Transistor speed" subsection above.

A simple comparator has an input offset voltage set by the input offsets of its differential pairs, which are random errors on the order of a few millivolts, and not likely to improve. To reduce these offsets, and to control the bias voltages at which comparators operate, the input amplifiers are generally used in simple switched-capacitor offset-cancelling circuits. In these circuits a sampling capacitor is switched between the reference and the input on every cycle, so that the power demands are like those of a sample/hold.

BJT comparators also consist of gain stages followed by a regenerative loop, and are faster roughly in proportion to their f_t.

amplifiers

Interstage gain is usually obtained using single-stage operational amplifiers [136], and they typically have gain-bandwidth products that are about 10%-30% of the f_t of their devices. With a 1μm CMOS process, unity-gain settling times on the order of 20-30ns are practical, and this limits the performance of pipelined converters.

These amplifiers are dissipating 1-10mW in current designs, and are an important part of the power budget in pipelined converters where $N-1$ of them are required. The power required for a single-stage amplifier is defined by its required transconductance, which is in turn set by the load capacitance it must drive and the required speed. Load capacitance is in turn defined by resolution requirements. The only one of these factors that is technology-sensitive is the power-efficiency with which a given transconductance can be obtained in MOS, which gets better as channel-length decreases. This factor may be expected, in a 0.5μm process, to allow 50MHz pipeline converters with roughly 100mW power dissipation.

Bipolar amplifiers operate efficiently at much higher frequencies, but have not been used in pipeline converters to date because the pipelines require good samplers, which have been better in CMOS. Since BiCMOS processes now offer both device types, it is possible that much faster-settling amplifiers are now practical. If this really helps, new converters with this mix of device types will start appearing in the next two or three years.

summary

CMOS speed and power-efficiency will continue to improve in the next few years as linewidths drop to 0.5μm and below, and pipeline and two-step converters will benefit. 280MHz conversion is still a long way from proven speeds for these architectures, but 80MHz is quite reasonable.

BiCMOS technology is becoming available, and may make it possible to combine the better features of bipolar and CMOS converters shortly. This would help with the 80MHz objective, but 280MHz should still be seen as aggressive.

Heterojunction bipolar technology provides a very fast BJT, which will improve the speed of bipolar flash and two-step converters and may even make a successive-approximation part capable of running at 50MHz.

This report has not covered radically new device technologies, such as Josephson and resonant-tunnelling, which may offer radical improvements in performance and in which some interesting converters have already been fabricated in laboratories. We assume that these technologies are still five to ten years from commercial exploitation at the scale and prices needed for consumer radio, and that a good deal of engineering has yet to be done before their performance can be evaluated.

10: Summary

A survey of the state of the art in data conversion shows that, while D/A converters fast and efficient enough for digital radio implemented as in [1] are available, A/D converters still consume too much power for handheld applications. The requirements for a 20MHz IF are not far from the overall trend, and a custom design in a leading-edge production technology could probably produce an 8-10 bit converter consuming 100-200mW. The design would probably be based on a known approach for video converters, which have similar specifications.

The high input frequency is difficult for present converters to handle, and even the initial sample/hold circuit will add significant distortion to a 70MHz IF. Improvement in this area will come gradually as MOS linewidths shrink.

Linearity errors from mismatches, offsets and finite amplifier gains limit the SNR of present video A/D converters to 8 or 10 bits, and an important component of this nonlinearity is large-scale integral nonlinearity that is difficult to remove by oversampling. There are several self-calibration schemes in the literature, and some in practice for lower-speed converters, that may help. These may have to be implemented specifically for digital radio, since INL has not been as important for video.

Adding noise shaping by feeding back quantizer outputs to the analog anti-alias filter gives a radically different approach: narrowband conversion. This is a very new technology, but already dominates audio-rate high-resolution conversion and has recently been extended to bandpass signals. The only monolithic part now available runs at 455kHz, but it is reasonable to expect that something suitable for a 20MHz IF can be made with present technology and could consume under 100mW. Radical approaches involving the use of passive resonators may make a 70MHz IF practical at milliwatt power levels, but it is too early to know.

An overview of the circuits used in video-rate conversion suggests that pipeline and half-flash converters are good candidate architectures for the near term, gives an idea of the improvements to be expected in the next generation of CMOS technology, and suggests that BiCMOS may allow mixed circuit approaches to offer better performance than is available now.

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Appendix A

Published Analog-to-Digital Converters

1980 to 1992

Type	Author	Date	Journal	Bits	Speed	Area		Power	Technology		Comments
					(MHz)	Die	Active		Size	Type	
Flash	Decourant T.	86.06	JSSC	2	1000		0.18	16	1	GaAs	
Flash	Walden R.H.	90.04	JSSC	4	1600		0.91	86	0.25	CMOS SOI	Implant Adjusted Threshold
Flash	Garuts V.E.	89.04	JSSC	4	2000		1	1250	0.6	Bipolar	
Flash	Thomas F.	89.04	JSSC	4	1000	4		2000		GaAs	System
Flash	Daniel D.	88.06	JSSC	4	1000	9		2400	2	Bipolar	System
Flash	Kumamoto	88.02	JSSC	4	30		3.75	540	3	CMOS SOI	(Power Est.)
Flash	Saul P.H.	80.06	JSSC	4	100	7.5		850		Bipolar 5GHz	
Flash	Fiedler H.L.	81.06	JSSC	5	20	7.1		550	7	NMOS	
Flash	Wakimoto T	88.02	ISSCC	6	2000	12		2000	0.35	Bipolar	
Flash	Hotta M.	87.12	JSSC	6	30		0.91	12	2	Bipolar 8.4 GHz	
Flash	Poulton K.	87.12	JSSC	6	1000	12		8000	1	Bipol&GaAs	System for DSO
Flash	Zojer B.	85.06	JSSC	6	200	8.8		1100	2.5	Bipolar	Comparator Metastable Analysis
Flash	Emmert G.	80.12	JSSC	6	150	10.7		450		Bipolar	Figure of Merit Proposed
Flash	Joy A.K.	86.06	JSSC	7	30	12.6		350	2	CMOS	
Flash	Nejime Y.	91.09	JSSC	8	300	33		3300	2.5	Bipolar	
Flash	Manglesdorf C.W	90.02	JSSC	8	200	15		2000	2	Bipolar	
Flash	Goodenough F.	89.12	Elec Des	8	75					Bipolar	Interpolating Flash
Flash	VanDeGrift R.E.J	87.12	JSSC	8	55	6		300	2.5	Bipolar 7.5GHz	Folding
Flash	Peetz B.	86.12	JSSC	8	250	31		12000		Bipolar 7GHz	shows need for S/H
Flash	Kumamoto T.	86.12	JSSC	8	30	7.1		180	1.5	CMOS	Compute Delay vs Tech.
Flash	Michel J.P.	86.08	Cons. Elec.	8			8	1000	3	CMOS	Double Folding
Flash	Hotta M.	86.04	JSSC	8	30	30		150	3	Bipolar 4.5GHz	
Flash	Yukawa A.	85.06	JSSC	8	20	30		350	3.5	CMOS	R=10 Ohms
Flash	VanDeGrift R.E.J	84.06	JSSC	8	20	12.6		520		Bipolar	Double folding
Flash	Inoue M.	84.12	JSSC	8	120	32		2000	4	Bipolar	
Flash	Yoshii Y.	84.12	JSSC	8	100	22		1200	2.5	Bipolar	
Flash	Van DePlassche	88.12	ISSCC	8	100	12		800		Bipolar	Folding Type
Flash	Shiwaku N.	91	CICC	8	30		11.5	180	1	CMOS	
Flash	Blauschild R.	83.02	ISSCC	8	20	27		300	6.5	Bipolar	Folding Type
Flash	Takemoto T.	82.12	JSSC	10	20	90		2000	3	Bipolar	Laser Trimmed

Type	Author	Company	Date	Journal	Bits	Speed	Area		Power	Technology		Comments
						(MHz)	Die	Active		Size	Type	
Algorithmic	Deval Ph.		91	CICC	14	0.005		1	2.5	3	CMOS	Current Mode
Algorithmic	Kim S.W		91.05	Elec. Lett.	8	0.1			0.5	3	CMOS	Current Mode
Algorithmic	Nairn D.G.		90.08	JSSC	8	0.5		0.75	65	3	CMOS	Current Mode
Algorithmic	Nairn D.G		90.03	CAS	10	0.025		0.18	3.5	3	CMOS	Current Mode
Algorithmic	Nairn D.G		88 .	ISCAS	8	0.5		0.75	65	3	CMOS	Current Mode
Algorithmic	Onodera H.		88.02	JSSC	8	0.008		0.8		2	CMOS	SC
Algorithmic	Valencic V.		87.08	Elec. Lett.	8	0.015		0.5	0.35		CMOS	SC
Algorithmic	Shih C. C.		86.08	JSSC	13	0.008		2.5		5	CMOS	SC
Algorithmic	Li P.W.		84.12	JSSC	12	0.008		1.5	17	5	CMOS	SC
Algorithmic	Woods J.V.		80.04	IEE Proc.	8	30						Discrete System
Algorithmic	Hornak T.	H.P.	75.12	JSSC	12	0.02						Discrete System

Type	Author	Date	Journal	Bits	Speed	Area		Power	Technology		Comments
					(MHz)	Die	Active		Size	Type	
		Integrating Dual Slope ADC									
Dual Slope	Rodgers B.J.	89.06	JSSC	14	1.00E-05	21.2		50	4	BiCMOS	
Dual Slope	Nakamuta M.	89.08	Cons. Elec	14	0.096	16.3		600	2	Bipolar	
Multi Slope	Iso Y.	86.11	Cons. Elec	16	0.05	10		180		CMOS/Bipolar	DAT Coarse/Med/Fine (Hitachi)
Multi Slope	Abe M.	84.08	Cons. Elec	10	0.0315	7.4		30		CMOS	Audio PCM, Coarse/Fine (Sony)
Multi Slope	Sugimoto Y.	84.08	Cons. Elec	10	0.0315	19		160		Bipolar	Audio PCM, Coarse.Fine (Toshiba)
Multi Slope	Sugawara T.	83.12	JSSC	16	0.05	11.7		450	2	Bipolar	Coarse/Fine
Multi Slope	Sugawara T.	83	ISSCC	18	0.05	11.7		450	2	Bipolar	Coarse/Fine

			Oversampling A/D Converters															
Type	Author	Date	Journal	Res	Fs(eq)	Range	Bits	Fs	Fo	BW	Order	Area		Power	Technology		Comments
					(MHz)	(dB)		(MHz)	(MHz)	(KHz)		Die	Active		Size	Type	
Fabricated	Del Signore B.P	90.12	JSSC	20	0.001	126	1-b	0.256		0.5	4	29		120	3	CMOS	Current Mode
Fabricated	Del Signore B.P.	90	ISSCC	20	0.001	126	1-b	0.256		0.5	4	29		120	3	CMOS	Current Mode
Fabricated	Dressler H.J.	90.09	Elec.Lett	9	0.16	58	1-b	10	2.5	80	2						Digital Radio/Discrete Comp.
Fabricated	Chao, K.C.H.	90.03	CAS	15	0.04	90	1-b	2.1	0	20	4						Discrete Components
Fabricated	Boser B.H.	88.12	JSSC	15	0.032	89	1-b	4	0	16	2		0.77	12	3	CMOS	Theory and SC Tech.
Fabricated	Matsumoto K.	88	ISSCC	18	0.04	105	4-b	6.144	0	20	4				2.4	BiCMOS 4GHz	Multi Chip Set
Fabricated	Boser B.H.	88	ISSCC.	15	0.032	89	1-b	4	0	16	2		0.77	12	3	CMOS	Theory and SC Tech.
Fabricated	Matsuya Y.	87.06	JSSC	16	0.048	91	1-b	3	0	24	3	48.6	7.3	110	2	CMOS	MASH defined (Analog Pwr: 35mW)
Fabricated	Carley L.R.	87.01	CAS	14	0.1	82	5-b	0.8	0	50	3						Discrete Components
Fabricated	Roettcher	86.06	JSSC	14	0.04	84	1-b	12	0	20	2		3.3		3.5	CMOS	
Fabricated	Adams R.W.	86.03	J.Aud.Soc.	18	0.04	105	4-b	6.144	0	20				40000		Bipolar	Discrete Components
Fabricated	Brandt B.P.	91.12	JSSC	12	2	74	1+3	50		1000	2+1		0.65	41	1	CMOS	Cascaded Multibit - SC Type
Fabricated	Lerch R.G.	91.12	JSSC	14	0.016	80	1-b	2.048		8	2		31	125	3	CMOS	CCITT G722 Codec-Cont.Time
Fabricated	Naus P.J.A.	91.07	JSSC	12	0.016	72	4-b	8.5	0	8	1		63		1.6	CMOS	
Fabricated	Leopold H.A.	91.07	JSSC	20	1E-06	120		1		0		14		6.7	2	CMOS	Continuous Time
			ISDN														
Fabricated	Norsworthy S.R.	89 April	JSSC	15	0.16	88.5	1-b	10.24		80	2		2	75	1.75	CMOS	ISDN AT&T Inc.Limitations SC Type
Fabricated	Rebeschini M.	90.04	JSSC	15	0.16	91	1-b	10.24	0	80	3		3	76	1.5	CMOS	ISDN Motorola SC Type
Fabricated	Koch R	86.12	JSSC	13	0.24	77	1-b	15.36	0	120	2	3		15	3	CMOS	ISDN Siemens Current Mode
			Simulation														
Simulation	Jantzi S.	91.11	CAS	16				3	0.46	20							Bandpass Simulation
Simulation	Zhang Z.X.	91.10..	Elec.Lett	15													Bandpass Simulation

Type	Author	Date	Journal	Bits	Speed	Area		Power	Technology		Comments
					(MHz)	Die	Active		Size	Type	
Pipeline	Wantanabe K.	90.02	CAS								
Pipelined	Lewis S.H.	91	CICC	10	20	9.3		300	0.9	CMOS	Digital Error Correction AT&T
Pipelined	Real P	91.08	JSSC	10	20	48		1000	2	BiCMOS 2GHz	Current Mode - Analog Devices
Pipelined	Real P.	90	ISSCC	10	20	48		1000	2	BiCMOS 2GHz	Current Mode - Analog Devices
Pipelined	Lin Y.	91.04	JSSC	13	2.5	26		100	3	CMOS	Self Calibrating
Pipelined	Sutarja S.	88.12	JSSC	13	0.25		4.2	15	3	CMOS	Reference Correction
Pipelined	Sutarja S.	88	ISSC	13	0.25		4.2	15	3	CMOS	Reference Correction
Pipelined	Song B.	88.12	JSSC	12	1	14		400	1.75	CMOS	
Pipelined	Song B.	88	ISSCC	12	1	14		400	1.75	CMOS	Error Averaged
Pipelined	Lewis S.H.	87.12	JSSC	9	5	5.5		180	3	CMOS	Digital Error Correction
Pipelined	Temes G.C.	85.08	Elec. Des.								
Pipelined	Lewis S.H.	92.03	JSSC	10	20	8.7		240	0.9	CMOS	Digital Error Correction

Type	Author	Company	Date	Journal	Bits	Speed	Area		Power	Technology		Ft	Comments
						(MHz)	Die	Active	(mW)	Size	Type	(GHz)	
Subranging	Grant P.S.		87.04	JSCC	6						CMOS		
Subranging	Tsuji K.	Toshiba	91	CICC	8	20		2.9	50	0.8	CMOS		
Subranging	Dingwall A.G.F.	RCA	85.12	JSSC	8	8	7		20	3	CMOS		
Subranging	Matsuura T.	Hitachi	88	ISSCC	8	20	14.6	7.6	200	2	CMOS		Digital T.V.
Subranging	Hosotani S.	Mitsubishi	90.02	JSSC	8	20		4.5	50	1	CMOS		
Subranging	Ishikawa M.	NTT	89.12	JSSC	8	50	14		600	1	CMOS		
Subranging	Kasahara M.	Hitachi	91	CICC	9	25	12	4	100	1.3	CMOS		
Subranging	Marsh J.	Tektronix	91	CICC	10	75	28		2500		Bipolar	5	
Subranging	Petschacher R.	Siemens	90.12	JSSC	10	75	20		2000	1.5	Bipolar	7	Digital Error Correction
Subranging	Zojer B.	Siemens	90	ISSCC	10	75	20		2000	1.5	Bipolar		HDTV
Subranging	Song B.	AT&T	90.12	JSSC	10	15	1.75		250	1	CMOS		Digital Video
Subranging	Song B.		90	ISSCC	10	15	1.75		250	1	CMOS		
Subranging	Matsuzawa A.	Matsushita Elec.	90	ISSCC	10	30	25		750	1.2	BiCMOS	7.5	
Subranging	Mayes M.K.	National Semicond	89.12	JSSC	10	1.6	10		150	2	CMOS		Error Correction
Subranging	Sugimoto Y.	Toshiba	89.08	JSSC	10	10	26		500	3	BiCMOS	4	Digital Video
Subranging	Doernberg J.		89.04	JSSC	10	5	47	35	350	1.6	CMOS		Digital Video
Subranging	Shimizu T.	Hitachi	89.02	JSSC	10	20	25		900	3	Bipolar	4.5	Digital Video
Subranging	Shimizu T.	Hitachi	88	ISSCC	10	20	25		900	3	Bipolar	4.5	Digital Video
Subranging	Mercer D.A.	Analog Devices	91.12	JSSC	12	1.25	24		600	2	BiCMOS	3	
Subranging	Kolluri M.P.V.	Signetics	89.12	JSSC	12	2	25		650	2	Bipolar	8.5	Self Correct & Trimming
Subranging	Kerth. D.	Crystal Semi-Corp	89.04	JSSC	12	1	80		750	3	CMOS		Self-Calib.
Subranging	Fernandes J.	Analog Devices	88.12	JSSC	14	0.1	44		480	4	BiCMOS		Analog&Dlg.Error Corr.
Subranging	Fernandes J.	Analog Devices	88	ISSCC	14	0.1	44		480	4	BiCMOS		Analog&Dlg.Error Corr.

Type	Author	Company	Date	Journal	Bits	Speed	Area		Power	Technology		Comments
						(MHz)	Die	Active		Size	Type	
Succ. Approx.	Hadidi K.H.		90.06	JSSC	8	1.3	2.4		70	3	CMOS	Resistor/Capacitor Array
Succ. Approx.	Goodenough F.	Burr Brown	89.05	Elec. Des	12							
Succ. Approx.	Naylor J.R		89	AES Conf	18	0.048			210	3	CMOS	Laser Trimmed
Succ. Approx.	Ramet S.	SGS Thom.	89	ISSCC	13	0.16		1.9	25	1.2	CMOS	Resistor/Capacitor Array
Succ. Approx.	VanDePlassche	Phillips	82.12	JSSC	14	0.14	15.4		450		Bipolar	Dynamic element matching
Succ. Approx.	C.M. Kyung		81.12	JSSC	4	0.1	2.7				CCD	
Succ. Approx.	Timko M.P.	Analog Dev.	80.12	JSSC	12	0.04					Bipolar	IIL Chip set
Succ. Approx.	Fotouhi B.		79.12	JSSC	12	0.02		7.7	40	12.5	NMOS	First Resistor Cap. Array
Succ. Approx.	McCreary J.L.		75.12	JSSC	10	0.044		5.2		12.5	NMOS	Charge Redistribution
Succ. Approx.	Suarez R.E.		75.12	JSCC	8	0.01		3.2		12.5	NMOS	Charge Redistribution
SA(self calibr)	Hester R.K.	Texas Inst.	90.02	JSSC	13	0.1	20.6			3	CMOS	
SA(self calibr)	Tan K.	Texas Inst.	90	ISSCC	16	0.1	110		500	1	CMOS	
SA(self calibr)	Miller G.	Analog Dev.	90	ISSCC	18	0.1	29		120	2	BiCMOS/CMOS	2 chip set
SA(self calibr)	Draxelmayr D.	Siemens.	88	ISSCC	16	0.1			20	3	CMOS	
SA(self calibr)	Barcrania K.	Harris.	86.12	JSSC	12	0.14				5	CMOS	
SA(self calibr)	Lee H.S.		84.12	JSSC	15	0.012	28	7.5	20	6	CMOS	Chip set

Appendix B

Commercial Analog-to-Digital Converters

ADC	Data	Fs	Pwr.	Type	Company	Code	Comments
	N	(MHz)	(mW)				
Dual Slope	16	15 Hz		BiCMOS	Harris	HI7159	
Dual Slope	13	200 Hz	10	CMOS	Harris	HI7135	
Flash	8	20	1750	Hybrid	SIPEX	HS1068	
Flash	8	25	1000	Hybrid	SIPEX	HS1070	
Flash	8	50	600	Hybrid	SIPEX	HS1078	
Flash	4	25	35	CMOS	Harris	CA3304	
Flash	6	15	70	CMOS	Harris	CA3306	
Flash	8	15	150	CMOS	Harris	CA3318	
Flash	8	20	550	CMOS	Harris	HI5700	
Flash	5	25	135	BiCMOS	Micro Power Systems	MP7686	
Flash	5	6	20	CMOS	Micro Power Systems	MP76L86	
Flash	7	10	300	CMOS	Micro Power Systems	MP7684	
Flash	8	200	2000	BiPolar	Analog Devices	AD770	
Flash	6	77	675	Bipolar	Analog Devices	AD9000	
Flash	8	150	750	Bipolar	Analog Devices	AD9002	
Flash	6	500	1700	Bipolar	Analog Devices	AD9006	
Flash	8	100	1000	Bipolar	Analog Devices	AD9012	
Flash	8	300	2000	Bipolar	Analog Devices	AD9028	
Flash	8	50	500	Bipolar	Analog Devices	AD9058	
Flash	10	75	2800	Bipolar	Analog Devices	AD9060	Uses Folding
Integrating	22	250 Hz	910	Hybrid	Analog Devices	AD1170	
Oversamp.	16	0.05	400	BiCMOS	Analog Devices	AD776	
Oversamp.	18	0.02	450	Hybrid BiCMOS	Analog Devices	AD1879	
Oversamp.	20	10 Hz	40	CMOS Hybrid	Analog Devices	AD7703	Fs=16kHz BW=10 Hz
Oversamp.	21	2 Hz	25	CMOS Hybrid	Analog Devices	AD7710	Fs=20 kHz BW=2Hz
Oversamp.	21	1 Hz	3.5	BiCMOS	Analog Devices	AD7713	Fs=4kHz BW=1 Hz
Pipelined	10	18	1.2	BiCMOS 2u	Analog Devices	AD773	Error Corr. Laser Trimmed
S.A	8	0.4	650	Hybrid	SIPEX	HSADC82	
S.A	12	0.1	1320	Hybrid	SIPEX	HSADC85	
S.A	12	0.5	56	Hybrid	SIPEX	HS5251	
S.A	12	0.67	150	CMOS	SIPEX	SP674A	
S.A	12	5	1700	Hybrid	SIPEX	SP9550	
S.A	14	0.5	2100	Hybrid	SIPEX	SP9588	

S.A	16	0.01	1200	Hybrid	SIPEX	HS9516	
S.A	16	0.067	1000	Hybrid	SIPEX	HS9576	
S.A	12	0.077	500		Linear	LTC1290	
S.A	8	0.01	6.5	CMOS	Harris	ADC0802	
S.A	10	0.075	15	CMOS	Harris	CA3310	
S.A	12	0.1	400	Bipolar/CMOS	Harris	HI774 (2 Die)	Biploar -Analog/CMOS-Digital
S.A	14	0.025	60	CMOS	Harris	ICL7115	Self-Calibrating
S.A.	10	0.05	500		Linear	LTC1090	
S.A.	12	0.04	275	CMOS/Bipolar	Micro Power Systems	MP574A (2 Die)	
S.A.	8	0.05	25	CMOS	Micro Power Systems	MP7574	
S.A.	12	0.15	275	CMOS	Micro Power Systems	MP774	
S.A.	10	0.04	170	Hybrid	Analog Devices	AD571	
S.A.	12	0.04	900	Hybrid	Analog Devices	AD572	
S.A.	10	0.05	250	Hybrid	Analog Devices	AD573	
S.A.	12	0.125	220	BiCMOS II	Analog Devices	AD774	
S.A.	10	0.03	200	Hybrid	Analog Devices	AD575	
S.A.	10	0.33	550	Hybrid	Analog Devices	AD578	
S.A.	12	0.33	775	Hybrid	Analog Devices	AD579	
S.A.	8	0.1	150	Hybrid	Analog Devices	AD670	
S.A.	16	0.1	235	BiCMOS Hybrid	Analog Devices	AD676	Auto calibration
S.A.	16	0.1	600	Hybrid	Analog Devices	AD1377	
S.A.	16	0.05	900	Hybrid	Analog Devices	AD1380	
S.A.	16	0.1	235	BiCMOS Hybrid	Analog Devices	AD1876	Auto calibration
S.A.	12	0.33	100	BiCMOS	Analog Devices	AD7572A	
S.A.	8	0.2	15	BiCMOS	Analog Devices	AD7575	
S.A.	12	0.1	75	CMOS	Analog Devices	AD7578	
S.A.	10	0.05	50	BiCMOS	Analog Devices	AD7580	
S.A.	12	0.1	75	CMOS	Analog Devices	AD7582	
S.A.	12	0.3	110	BiCMOS	Analog Devices	AD7672	
S.A.	12	0.1	60	BiCMOS	Analog Devices	AD7870	
S.A.	14	0.08	50	BiCMOS	Analog Devices	AD7871	
S.A.	12	0.66	25	BiCMOS	Analog Devices	AD7880	
S.A.	16	0.166	250	BiCMOS Hybrid	Analog Devices	AD7884	
S.A.	12	0.14	30	BiCMOS Hybrid	Analog Devices	AD7892	
S.A.	14	0.03.	645	Hybrid	Analog Devices	ADC71	
S.A.	12	0.04	800	Hybrid	Analog Devices	ADC80	

S.A.	12	0.1	880	Hybrid	Analog Devices	AD5240	
S.A.	12	0.175	135	BiCMOS	Analog Devices	ADC170	
S.A.	10	0.165	400	BiCMOS	Analog Devices	ADC910	Area = 19 mm sq.
S.A.	12	0.1	95	BiCMOS	Analog Devices	ADC912A	
S.A.	16	0.03	750	Hybrid	Analog Devices	ADC1140	
Subrange	8	0.4	75		Linear	LTC1099	
Subrange	10	0.2	150	CMOS	Harris	HI7152	
Subrange	8	2	30	CMOS 2.0u	Micro Power Systems	MP7696	
Subrange	7	0.5	32	CMOS	Micro Power Systems	MP0820	
Subrange	8	3	100	CMOS	Micro Power Systems	MP7683	
Subrange	12	2	475	BiCMOS	Analog Devices	AD671	
Subrange	12	0.2	560	BiCMOS Hybrid	Analog Devices	AD678	Laser Trimmed
Subrange	14	0.128	560	BiCMOS Hybrid	Analog Devices	AD679	Laser Trimmed
Subrange	14	0.128	560	BiCMOS	Analog Devices	AD779	Laser Trimmed
Subrange	16	0.5	2800	Hybrid	Analog Devices	AD1382	Error correct.
Subrange	12	1.25	570	BiCMOS	Analog Devices	AD1671	Error correct.
Subrange	12	1	200	BiCMOS	Analog Devices	AD7586	
Subrange	8	1	50	BiCMOS	Analog Devices	AD7821	
Subrange	12	0.75	250	BiCMOS	Analog Devices	AD7886	
Subrange	12	10	3200	Hybrid	Analog Devices	AD9005	
Subrange	14	10	12800	Hybrid	Analog Devices	AD9014	Error Correct
Subrange	12	25	5000	Hybrid	Analog Devices	AD9032	
Subrange	10	40	1000	Hybrid	Analog Devices	AD9040	
Subrange /S.A.	12	1	2200	Hybrid	Analog Devices	AD9003	Subranging / Succ. Approx.