Communications
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Hopping Synthesizer Controller Interface Board Design for Skynet Uplink Trials

by

Dr. Lloyd Mason

CRC REPORT NO. 98-005

June 1998
Ottawa

Industry Canada Industrie Canada

The work described in this document was sponsored by the Defence R&D Branch of the Department of National Defence under work unit 5CA11.

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Abstract

In this report the design of an integrated circuit board for use in the payload of an extremely high frequency satellite communications experiment is described. This board, called the hopping synthesizer controller interface (HSCI) board, provides all necessary clock signals for the payload as well as the means to control the hopping synthesizer controller used in dehopping the received signal at the payload. Most of the integrated circuits on this board are standard off-the-shelf 7400 series transistor-transistor logic devices. The complexity of the printed circuit board (PCB) is greatly reduced by using two erasable programmable logic devices (EPLDs). One of these EPLDs derives all of the necessary clock signals from a single crystal oscillator. The other EPLD provides a board addressing capability as well as a strobe signal to control the hopping synthesizer controller. Two different versions of the HSCI board were built, one was a speed-wrap prototype version while the other was the finalized PCB version. Both boards were found to operate reliably and to meet expected performance.

Résumé

Dans ce rapport, on décrit la conception d'une carte à circuit intégré, qui est utilisée dans une charge utile d'un satellite expérimental à ondes millimétriques. Cette carte appelée *hopping synthesizer controller interface (HSCI) board* contient tous les signaux d'horloges nécessaires à la charge utile. En plus, elle permet de contrôler le synthétiseur de saut de fréquence utilisé pour le processus d'enlèvement des sauts de fréquences du signal de réception à bord de la charge utile. La plupart des circuits intégrés sur la carte sont des composantes standards de la série *7400 transistor-transistor* de logic devices. La complexité de la carte à circuits imprimés est réduite considérablement grâce à l'utilisation de deux circuits intégrés programmables *erasable programmable logic devices (EPLDs)*. Un de ces circuits est utilisé pour dériver, à partir d'un oscillateur à cristal, les signaux d'horloges qui sont nécessaires. L'autre circuit intégré fournit les capacités d'adressage de la carte en plus de contenir le signal à pulsion qui permet le contrôle du contrôleur de saut de fréquence du synthétiseur. Deux différentes versions de la carte HSCI ont été conçues. La première version est une carte prototype *speed-wrap*. La deuxième, qui est la version finale, est une carte à circuits imprimés.s d'opérer avec fiabilité, les deux cartes répondent aux performances recherchées.

Executive Summary

The Communications Research Centre and the Defence Research Establishment Ottawa have for several years jointly carried out research into secure satellite communications in the EHF band for the military. Recently, under this program, preparations were made to carry out tests on the uplink portion of a frequency-hopped spread spectrum system using frequency division multiple access (FDMA) as the format for a small multiuser scenario. These tests were to be conducted by using a ground terminal simulator which was to transmit up to the British Skynet 4A transponder then back to the ground where the signal was to be received by a payload simulator. The object of this experiment was to test some algorithms for synchronization and data processing which were developed in-house in order to determine their effectiveness and practicality.

The design, construction, and operation of a hopping synthesizer controller interface (HSCI) board used in the payload (PL) simulator is described in this report. The HSCI board has four principal functions. They are: (1) provision of all needed clock signals for the PL simulator; (2) provision for operation of the hopping synthesizer controller (HSC); (3) provision of analog-to-digital converter signals for controlling the number and start-time of samples taken in each hop period ; and (4) generation of an interrupt signal used to control a TMS320C40 signal processor.

The board was designed to use mostly 7400-series transistor-transistor logic devices. A crystal oscillator and two erasable programmable devices (EPLDs) are the only specially designed components on this board. One EPLD was designed to provide all of the clock signals by performing frequency divisions using D flip-flop circuits. As a result, all clock signals could be derived digitally from one source with no need for analogue phase-locked loops. The other EPLD performs a variety of functions including a board address decoding capability, the generation of a strobe for the HSC, and an interrupt signal for controlling the TMS320C40 signal processor used in the PL simulator.

Two versions of this board were made, the first being a speed wrap prototype and the second a final PCB version. Both versions were found to perform up to their specifications when tested and used in the payload simulator.

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List of Abbreviations

ADC	Analogue Digital Converter
CRC	Communications Research Centre
CRI	Catalina Research Inc.
DFT	Discrete Fourier Transform
DIB	Data Interface Board
DPST	Double Pole Single Throw
DREO	Defence Research Establishment Ottawa
DSPLINK	Digital Bus Connecting C40 Processor with other Devices
EHF	Extremely High Frequency
EPLD	Erasable Programmable Logic Device
FDMA	Frequency Division Multiple Access
FFT	Fast Fourier Transform
FHSS	Frequency-Hopped Spread Spectrum
FIFO	First In First Out
FSK	Frequency Shift Keying
GT	Ground Terminal
HSC	Hopping Synthesizer Controller
HSCI	Hopping Synthesizer Controller Interface
I	In-phase
MILSATCOM	Military Satellite Communications
MOU	Memorandum Of Understanding
PL	Payload
Q	Quadrature
RL	Return Link
SHF	Super High Frequency

1 Introduction

The Military Satellite Communications (MILSATCOM) group at the Communications Research Centre (CRC) and the Defence Research Establishment Ottawa (DREO) have carried out a program over several years to study and determine the performance of systems which use the Extremely High Frequency (EHF) band. Systems for military applications use frequency hopped spread spectrum (FHSS) methods of transmission to lessen the effect of hostile jamming signals. It is because these methods require a large bandwidth that necessitates operation at EHF where spectral congestion is less severe. Several algorithms for the signal processing required for synchronization and data detection have been developed in-house. It was deemed necessary to investigate and test these algorithms in an environment as close as was practical to the actual operational situation. To allow testing in a real environment a Memorandum Of Understanding (MOU) was signed between the United Kingdom and DREO to allow use of the Skynet 4A EHF transponder. This transponder receives an EHF signal and translates it to a SHF signal before retransmission to the ground. Testing the downlink processing methods has already been completed [1]. The work in this report deals with aspects of the uplink data processing and synchronization methods.

The system signal format to be used in the experiment to be conducted is laid down in [2]. The basic interval of signaling is 62.5 microseconds, denoted a "hop interval" or more simply in what follows a "hop". The corresponding frequency, called the "hop frequency", is 16 kHz. This system uses frequency division multiple access (FDMA) to allow several users to transmit and receive data over the system at one time. Upon logging onto the system, each user is assigned a channel in a sub-frame, called a cell, in which to transmit information. This channel consists of eight prescribed frequencies. In this cell , the user on the system transmits one of the eight tones. Thus, three bits of information are transmitted by the user in the hop. This uplink modulation technique is known as 8-ary frequency shift keying (FSK) [2].

In an actual system the payload (PL) is located aboard the satellite and information is transmitted via the uplink to the satellite, processed onboard, and then transmitted over the downlink to the ground terminal (GT). In the simulation of this PL, access must be provided in order to carry out the experiment. Hence, the following experimental setup was used. A GT simulator is used to frequency spread and then transmit a signal bearing synchronization and/or data information up to the Skynet satellite according to the format in [2]. The satellite translates and retransmits this signal to the payload (PL) simulator on the ground. The received signal is unspread and converted to an intermediate frequency band using a dehopping synthesizer. Then the signal from this synthesizer is converted down to baseband. The in-phase (I) and quadrature (Q) signals are sampled, demodulated, and processed to determine their binary equivalents. These binary data are then sent to a data interface board (DIB) where the data are reformatted and then sent to the data sink.

An important function of the PL simulator is to carry out processing of the received signal to determine the time domain alignment error of the signals when they arrive at the PL simulator. Time alignment with the system clock (on the PL simulator) is necessary to prevent reduction of signal energy of each user and to control inter-channel interference among the various users on the system. Time alignment information is then sent to the GT simulator so that adjustments can be made to ensure that all signals arriving at the PL simulator are in alignment with the system clock. This information is sent over a return link (RL) established between the PL simulator and the GT simulator to enable the GT simulator to respond to synchronization estimates sent by the PL simulator.

In this report the design, construction, and operation of a hopping synthesizer controller interface (HSCI) printed circuit board (PCB) used in the PL simulator is described. This PCB provides: (a) all needed clock signals on the PL simulator, (b) a means to control the hopping synthesizer, and (c) analogue-to-digital converter signals used to control the number and start-time of sampling of the received signal taken in each hop interval.

2 Payload Simulator Description

A detailed block diagram of the PL simulator is given in Fig. 1. The analogue I and Q signals derived from the PL simulator down-converter are inputs to the Catalina Research Inc. (CRI) Nimble board. This board is one of the components of the CRI equipment which is shown surrounded by the dashed box in Fig. 1. The CRI equipment is described in [3]. This equipment consists of four units. The CRI Nimble board is an analogue-to-digital converter (ADC). It samples the I and Q analogue signals at the converter clock rate. This converter clock is provided by the hopping synthesizer controller interface (HSCI) board. The point at which the ADC starts sampling after the rising edge of the 16 kHz hop clock, also provided by the HSCI board, is controlled by the rising edge of a frame-start signal. The CRI Critir board reads the sampled data into first-in-first-out (FIFO) devices located on the Nimble board.

One important function of this part of the PL simulator is to perform a Discrete Fourier Transform (DFT) on the received signal after it has been dehopped and converted to baseband. Because the modulation format for data communication is 8-ary FSK [2], the symbol sent by each user on the system can be easily determined by looking at the DFT output bins. The DFT is performed by the CRI 1M40 board. This board is a very fast processor capable of performing a fast Fourier transform (FFT) with 512 points in about 50 microseconds. This number of points corresponds to 32 channels of 8-ary FSK modulation. Once the FFT has been completed the resulting data is sent back to the Critir board and held in FIFOs, readily available to be read out. The CRI equipment is under the control of a Radisys personal computer which has its own hard disk from which the various software routines are loaded to run the CRI equipment. The complete CRI equipment module resides in a VME chassis.

For this experiment only the four channels corresponding to the lowest frequencies

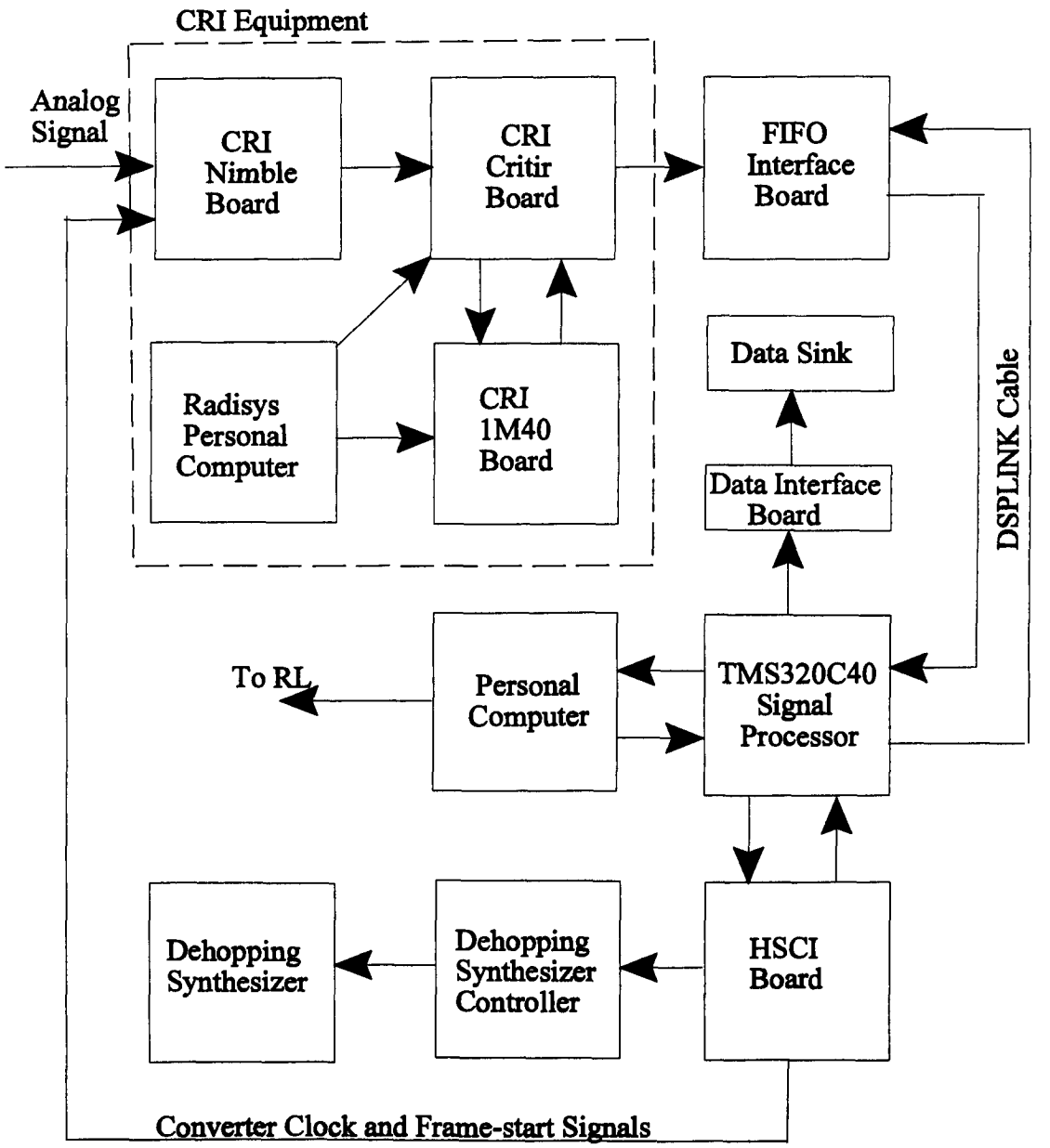

Figure 1. Block Diagram of PL Simulator.

are to be used as specified in [2]. Processing of these channels requires that only 64 data points be made available. However, in each hop period, the CRI equipment provides 512 points of data at a speed of 20 Mbits/sec. The DSPLINK bus can carry data at a maximum rate of 10 Mbits/sec. To accommodate this speed difference, a FIFO interface board is needed to act as a buffer between the CRI equipment and the DSPLINK bus. The FIFO interface board is under the control of the TMS320C40 processor, referred to simply as the "C40 processor" in what follows.

The C40 processor also controls the hopping synthesizer controller interface (HSCI) board. This board , the subject of this report, provides clock signals to various parts of the PL simulator, controls the dehopping synthesizer through the dehopping synthesizer controller (HSC), and sends frame-start and converter clock signals to the ADC. Refer to Section 3 for a more detailed description.

Also shown in Fig. 1 is a data interface board (DIB). This board, described in [4], receives data words which are 12 bits in length from the C40 processor. These words are converted to a single bit stream by the DIB before they are sent to the data sink.

A personal computer is used for loading software to the C40 processor and to control the information sent to the RL

3 HSCI Board General Description

The block diagram of the HSCI board is shown in Fig. 2. This board is required to provide the following clock signals: (A) a hop clock signal at a frequency of 16 kHz with 50 percent duty cycle; (B) ADC sample clock frequencies at 9.216 MHz, 4.608 MHz, 2.304 MHz, and 1.152 MHz; (C) an ADC frame-start signal; (D) data clock signals at 9.6 kHz, 4.8 kHz, and 2.4 kHz; (E) a strobe pulse to the HSC. All signals are to be transistor-transistor logic (TTL) level signals.

Two Erasable Programmable Logic Devices (EPLDs) comprise the essential part of this board. These are named the clock EPLD and the HSCI EPLD in Fig. 2. These devices are described in more detail in Sections 6 and 7 below.

The clock EPLD, generates all needed clock signals from the single crystal oscillator which operates at a frequency of 36.864 MHz. The clock EPLD generates and passes the hop clock signal at 16 kHz and another required clock signal at 18.432 MHz to the HSCI EPLD. A data clock signal is needed on the DSPLINK bus. It is generated by the clock EPLD also. This data clock signal can be any one of 9.6 kHz, 4.8 kHz, or 2.4 kHz and is switch selectable. For the experiments conducted a data rate of 2.4 kHz is used.

The Catalina Research Inc (CRI) Nimble Board requires a converter clock signal with a 50 percent duty cycle, the frequency of which can be switch selected from 9.216 MHz,

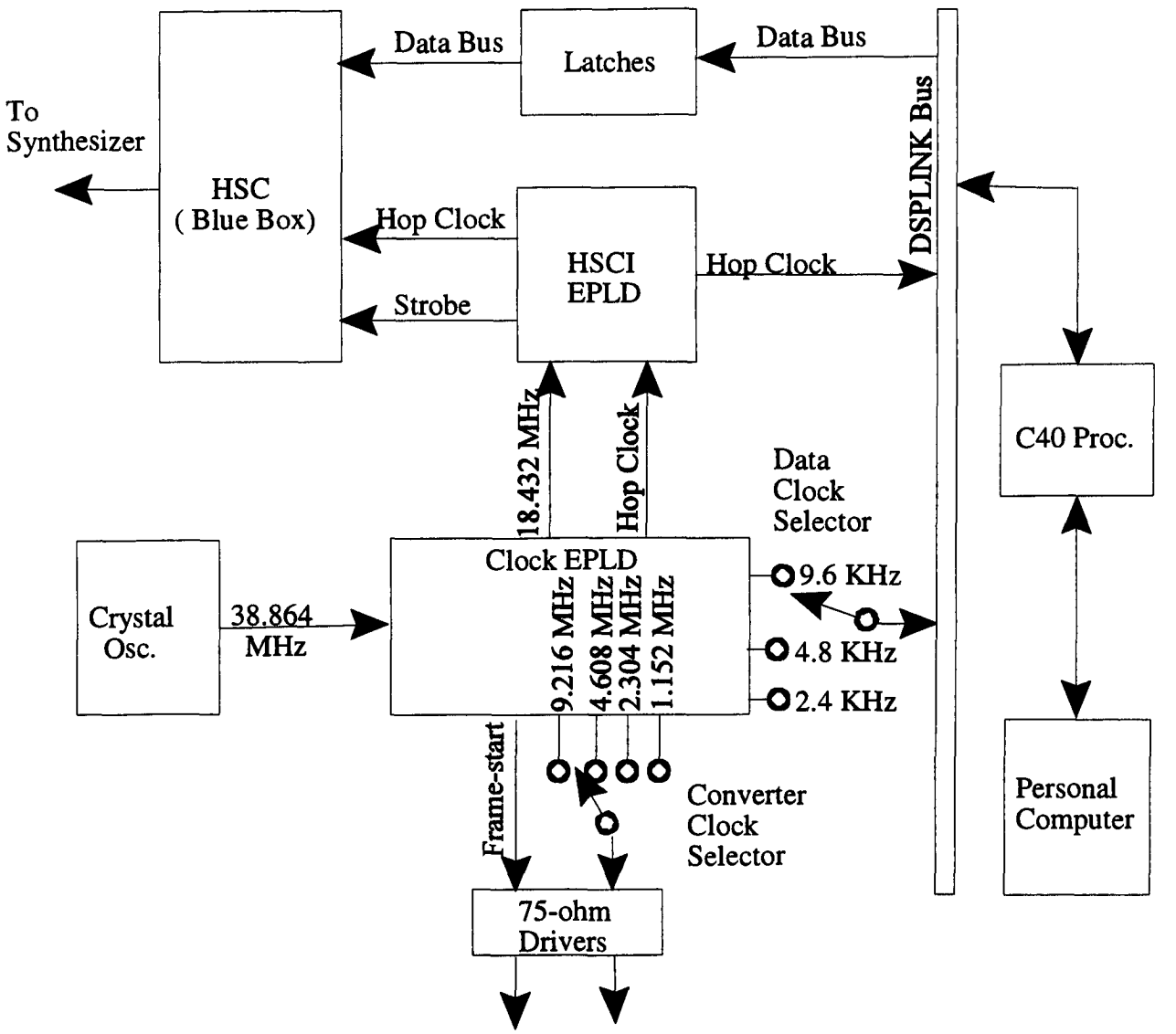

Figure 2. HSCI Board Block Diagram.

4.608 MHz, 2.304 MHz, or 1.152 MHz. The frequency of 9.216 MHz is used in the experiments. The other converter clock frequencies were provided so that lower sampling rates could be investigated if need be. The Nimble board also requires a frame-start pulse which starts the analogue to digital conversion in each hop. This pulse is delayed by 5 microseconds with respect to the rising edge of the hop clock as required by [2] and has a duration of 4 converter clock cycles or 0.434 microseconds at a frequency of 9.216 MHz. This pulse duration exceeds the minimum of one converter clock cycle as specified by the CRI specification [5]. All signals to the CRI equipment are at TTL levels and are driven with 75-ohm line drivers (ALS 804).

The HSCI EPLD receives the 16 kHz hop clock signal from the clock EPLD as well as a 18.432 MHz clock signal. The latter signal is used to drive a counter to generate a strobe for the HSC. The strobe pulse signals to the HSC that the next command may be read from the data latches U4 and U5 in Fig. 3 below. This strobe pulse has a duration of three cycles of the 18.432 MHz clock or 162.75 nanoseconds. The minimum required is 50 nanoseconds [6].

The HSCI EPLD passes the hop clock to the Hopping Synthesizer Controller (HSC) (known as the "blue box") and to the DSPLINK bus. This EPLD also provides the means for addressing the HSCI board. The DSPLINK address lines are A3, A2, A1, A0

The DSPLINK bus carries the data to and from the C40 signal processor board. This board is controlled by a Personal Computer (PC) and resides in a PC chassis.

4 HSCI Board Circuit Description

The schematic for the HSCI board is shown in Fig. 3 below.

All signals from the DSPLINK bus are buffered with 74ALS244 devices U1-U3. Data from the C40 processor can be latched into the two 74ALS374 latches U4 and U5. These data, consisting of commands and initial values for the HSC, then can be read by the HSC at the appropriate time.

Device U9 is used to read the status and perform monitoring of the HSC. One buffer line in U9 is used to transmit the hop clock to the front panel. This signal is used by the FIFO interface board to control reading and writing of data from the CRI equipment.

Device U8 is another buffer which sends the hop clock and the strobe to the HSC. This strobe is generated by the HSCI EPLD U6. All clock signals are generated by the clock EPLD U8 as described below.

Device U10 is a 36.864 MHz crystal oscillator which drives the clock EPLD.

Device U11 consists of 75-ohm drivers used to transmit the converter clock and the

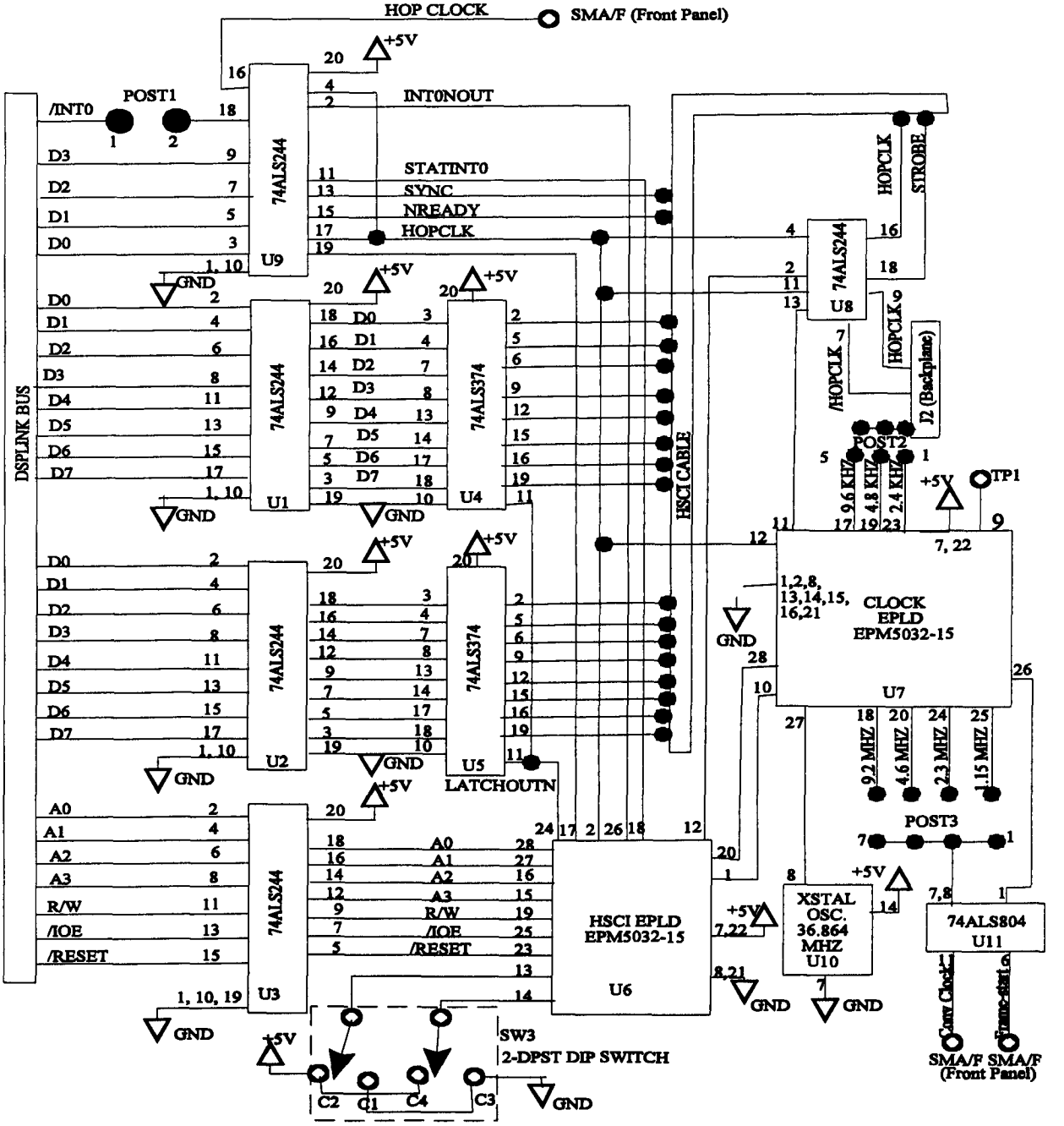

Figure 3. HSCI Board Schematic Diagram.

frame-start pulse to the CRI equipment. These signals are available on the front panel of the HSCI board.

Board addressing is required as there is more than one board to be addressed on the DSPLINK. The dual double pole single throw (DPST) dip switch SW3 is used for setting the board address. By means of this switch the lines to pins 13 and 14 on the HSCI EPLD may be set independently to either ground potential, corresponding to a logic level of 0, or to 5 volts, corresponding to a logic level of 1. As explained in Section 6 below, the voltages on these two lines are compared with those on the DSPLINK address lines A2 and A3. If these voltages are equal the HSCI board is enabled. The base addresses corresponding to the switch settings of SW3 are given in Table 7 of Section 8.

The component POST1 is a one-pin header which makes a signal available to the C40 for interrupt services. For this experiment the jumper was inserted, making the interrupt capability available on the C40. The component POST2 is a 6-pin header to select the desired data clock frequency. For this experiment the jumper was set to the 2.4 kHz position. The component POST3 is a 8-pin header used to select the converter clock frequency and for this experiment was set to the 9.216 MHz position.

5 HSCI Printed Circuit Board

A plan view of the HSCI printed circuit board is shown in Fig. 4 on the next page. A list of the major components mounted on this board is given in Table 1.

Table 1
Major Components List

Component Label	Component Type	Component Value	Component Function
U1, U2, U3, U8, U9	74ALS244		Octal Buffer/Line Driver
U4, U5	74ALS374		Octal Latch
U6	EPM5032DC-15		Address decoder, HSC strobe
U7	EPM5032DC-15		Provides PL clock signals
U10	Crystal Oscillator	36.864 MHz	Source for all clock signals
U11	74ALS804		Quad 75-ohm line driver
DC1 to DC11	Capacitor	0.1uF	Bypasses ac signals
C2, C4, C6, C8, C10	Capacitor	1.0uF	Bypasses ac signals
C1, C3, C5, C7, C9	Capacitor	0.1uF	Bypasses ac signals

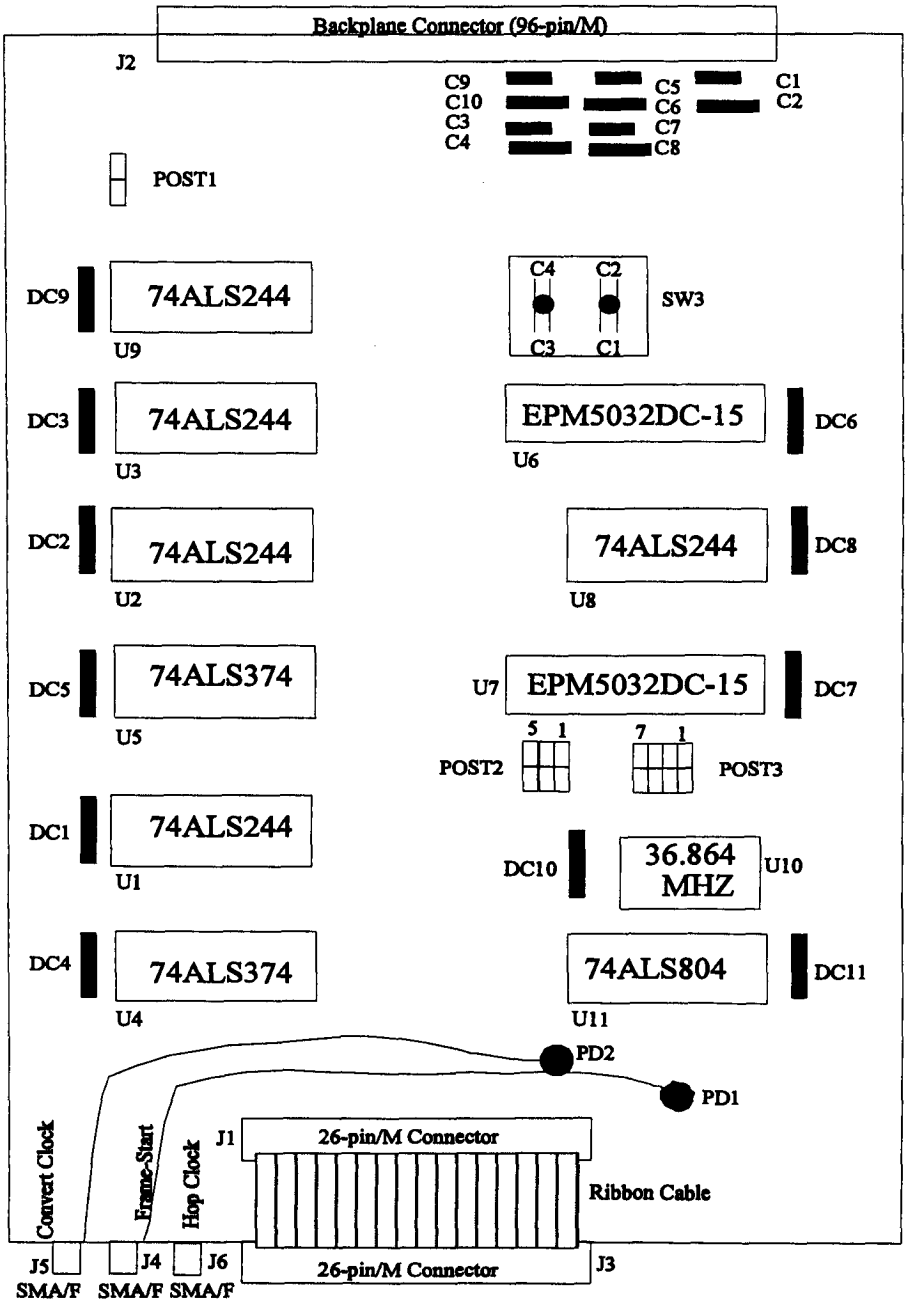

Figure 4. HSCI Printed Circuit Board Layout.

6 HSCI EPLD Description

The schematic for this EPLD is shown in Fig. 5 below. This circuit consists of an address decoder, a 3-bit comparator, a shift register, and some D flip-flops.

Board addressing is required as there is more than one board to be addressed on the DSPLINK bus. The base address is set by the switch SW3 on the HSCI board. The lines AIN2 and AIN3 on the EPLD are set using this switch to the required base addresses as given in Table 7 below. The 7485 comparator is used to compare the voltages on the AIN2 and AIN3 pins with those on the two address lines A2 and A3 of the DSPLINK bus respectively. The output AEB0 of this comparator is in the high state only if the following three conditions apply: (1) the input IOEN is low, (2) the inputs AIN2 and BIN2 are equal, (3) the inputs AIN3 and BIN3 are equal. When AEB0 is high the74138 decoder is enabled.

The address decoder inputs to the A, B, and C nodes are labeled AIN0, AIN1, and R/W respectively. These three inputs are the three DSPLINK bus signals A0, A1, and /W respectively.

The 74138 decoder outputs are Y0 to Y7. These outputs are active LOW according to Table 2 below.

Table 2
74138 Decoder Functions

Mode	R/W = C	A1 = B	A0 = A	Output (active low)	Function
Write	0	0	0	Y0	Send data to HSC
Write	0	0	1	Y1	Software Reset
Write	0	1	0	Y2	Reset Interrupt
Write	0	1	1	Y3	Not Used
Read	1	0	0	Y4	Read Status
Read	1	0	1	Y5	Not Used
Read	1	1	0	Y6	Not Used
Read	1	1	1	Y7	Not Used

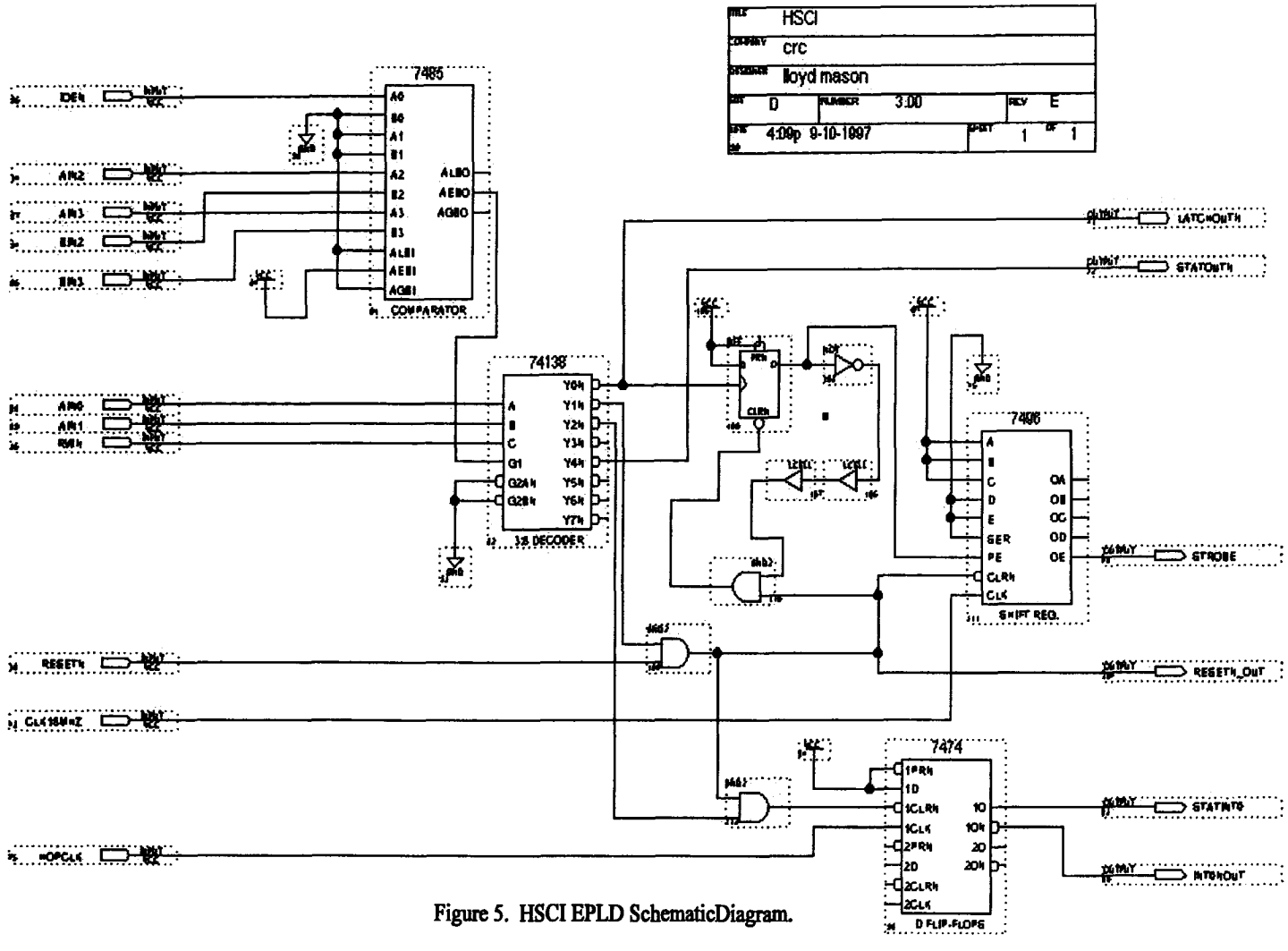

Figure 5. HSCI EPLD SchematicDiagram.

The 74138 output Y0 is used to latch data into the 74ALS374 latches U4 and U5 on the HSCI board. The falling edge of Y0 also triggers a single D flip-flop which in turn enables the preset-enable terminal of the 7496 5-bit shift register. The single D flip-flop is cleared by routing its output through an inverter and two LCELLs to the clear node CLRN. These LCELLs, which do not invert the signal, provide sufficient loop delay to allow automatic resetting of this D flip-flop.

The 7496 shift register is used to generate a strobe pulse at the output pin marked "STROBE".This strobe is required by the HSC to allow HSC commands to be transferred from the C40 processor. The 7496 shift register is clocked by the 18.432 MHz clock from the clock EPLD. The strobe pulse must be delayed with respect to the falling edge of Y0 to give the data at the outputs of the latches U4 and U5 time to become stable. In this design the delay is approximately two cycles of the 18.432 MHz clock, or 108.5 nsec. The strobe width is required to be at least 50 nsec. In this design the pulse length is approximately three clock cycles, or 162.75 nanoseconds. The strobe is returned to zero after three rising clock edges. The 7496 register is reset when the board is reset and is loaded with its initial values each time the Y0 output from the 74138 decoder goes low, which occurs each time data are sent to the HSC.

The 7474 D flip-flop is used to set up an interrupt signal to the C40 by connecting the hop clock signal to the clock input terminal. Thus, the output 1Q of the D flip-flop is normally low and its complement 1QN is normally high. When the hop clock signal rises to a high level, this sets the output 1Q high and 1QN low. The 1Q output, which is connected to the output pin labeled STATINT0 can be read by the C40 as it is one of the components of the status register for the HSCI board. The output 1QN, which connects to the output pin labeled INT0NOUT is connected to pin 2 of U9 on the HSCI board. The output of U9 is connected to the interrupt line /INT0 of the DSPLINK, provided the jumper for POST1 is in place. This is elaborated upon in Section 7 below.

The HSCI EPLD also provides the means for reset of the HSCI board either from the DSPLINK line /RESET or by means of a command from the HSCI board command register.

A list of the pins on the HSCI EPLD, their labels, and their functions is given in Table 3 below.

Table 3
Pin Descriptions for HSCI EPLD
Type: Alterra EPM 5032DC-15

Pin Number	Input/Output	Name	Function
1	IN	CLK18MHZ	HSC Strobe Clock
2	IN	HOPCLK	16 kHz Hop Clock
3			Not Used
4			Not Used
5			Not Used
6			Not Used
7	IN	Vcc	5-volt Supply
8		GND	Ground Reference
9			Not used
10			Not Used
11			Not Used
12	OUT	STROBE	Strobe for HSC
13	IN	BIN3	Selectable Board Address Digit
14	IN	BIN2	Selectable Board Address Digit
15	IN	AIN3	Address Line A3 of DSPLINK
16	IN	AIN2	Address Line A2 of DSPLINK
17	OUT	STATOUTN	Status Reg. Read Control
18	OUT	STATINT0	Interrupt Status
19	IN	RWN	DSPLINK /W
20	OUT	RESETN_OUT	Clock EPLD Reset
21		GND	Ground Reference
22	IN	VCC	5-volt supply pin
23	IN	RESETN	DSPLINK Reset line
24	OUT	LATCHOUTN	Latches data on 374 chips
25	IN	IOEN	Input-Output Signal from DSPLINK
26	OUT	INT0NOUT	Interrupt signal to C40 on DSPLINK
27	IN	AIN1	Address Line A1 of DSPLINK
28	IN	AIN0	Address Line A0 of DSPLINK

7 HSCI Clock EPLD

The block diagram of this circuit is shown in Fig. 6. The attractive feature of this circuit is that all required clock signals are derived from the single crystal oscillator frequency by division by whole numbers. This type of division is easily realized by D flip-flops and simple counters. Thus, no analogue phase locked loop circuits are needed. The diagram of Fig. 6 also shows the four possible converter clock frequencies marked as "To Conv. Sel." and the three possible data clock frequencies marked as "To Data Sel.". The converter clock signals are used by the CRI equipment and the data clock frequencies are used by the Data Interface Board.

The schematic diagram of the clock EPLD is shown in Fig. 7.The first stage divides the 36.864 MHz input clock frequency by two. The output from this stage at a frequency of 18.432 MHz is then sent off chip to the HSCI EPLD where it is used to clock a counter for the HSC strobe pulse. This output is also sent to the second stage which consists of two cascaded D flip-flops. The first D flip-flop in this stage divides the frequency of the input by two to give the required converter clock frequency of 9.216 MHz. The second D flip-flop performs another divide by two to give the next converter clock frequency of 4.608 MHz. The third stage again consists of two cascaded D flip-flops like the second and consequently generates the last two converter frequencies of 2.304 MHz and 1.152 MHz. The fourth stage performs a divide by 12 by means of a 7492 counter. The frequency is now 96 kHz at this stage. The fifth stage consists of another 7492 counter but connected so that division by 6 is performed. The output is now at the required hop clock frequency of 16 kHz and this signal and its complement are brought to output pins. The sixth stage is a 74196 counter which divides the signal by 10 to give the required data clock frequency of 9.6 kHz. The seventh stage consists of two D flip-flops in cascade and generates the data clock frequencies of 4.8 kHz and 2.4 kHz.

The 9.216 MHz clock signal is also used to operate an up-down 8-bit counter. This counter is enabled on the rising edge of the hop clock. It is hardwired to start at a count of 49 and to count down to 3. At this point the outputs QC to QH are low which causes the output of the NOR-6 gate to go high causing the ouput pin labeled "D-HOPCLK" to go high. This output is labeled "Frame-start" on the HSCI board and provides the needed input to the CRI Nimble board. This pulse is required to be delayed by 5 microseconds relative to the rising edge of the hop clock. Since the counter will take 46 /9.216 = 5.0 microseconds, this meets the required guard time at the beginning of the hop period as specified in [2]. The counter is also reset automatically by feeding the counter outputs QC to QH into an AND gate. The inverted output from this AND gate output is fed back to reset the counter so that is ready for the next rising edge of the hop clock.

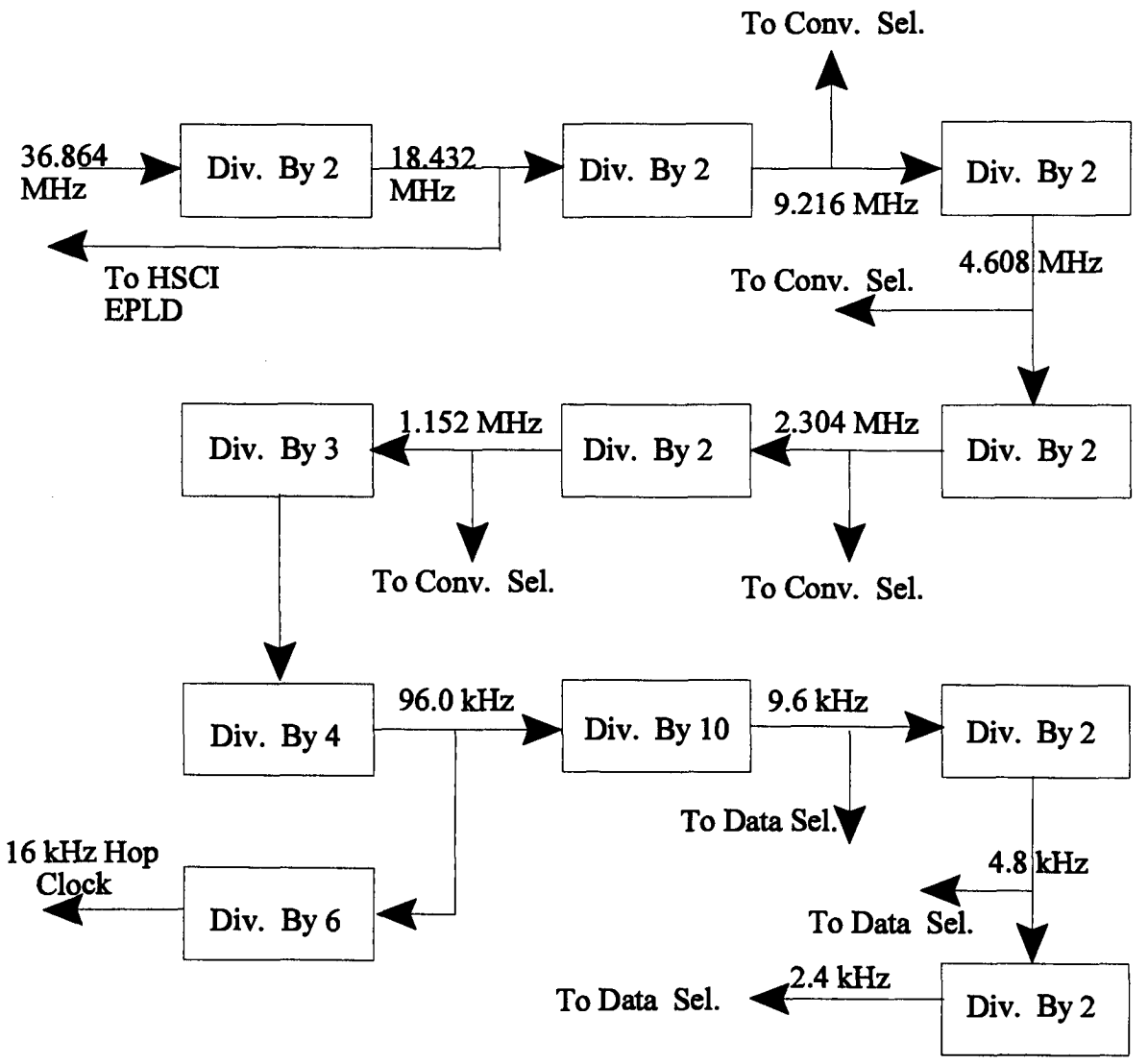

Figure 6. PL Clock Circuit Block Diagram.

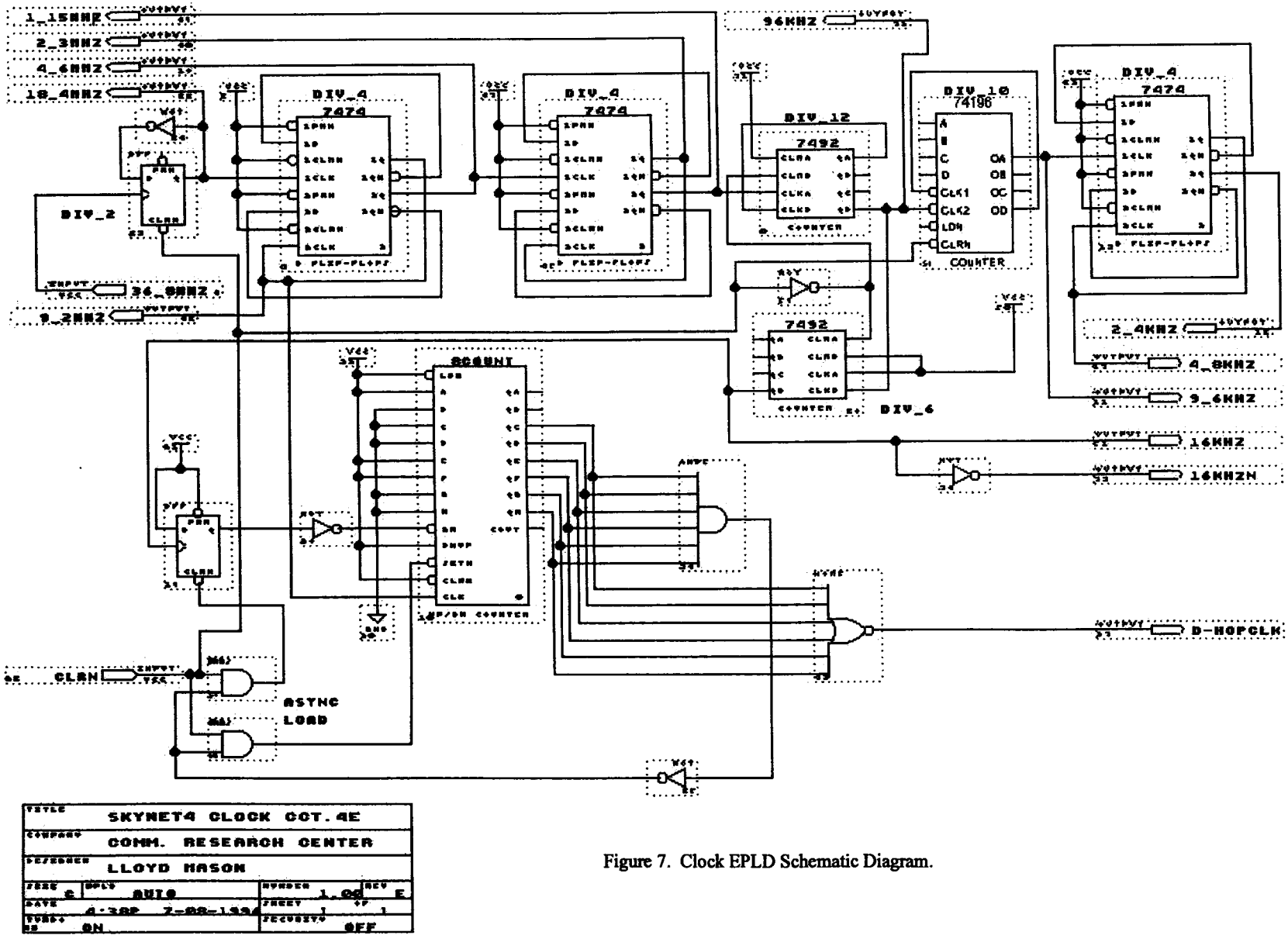

Figure 7. Clock EPLD Schematic Diagram.

Table 4 gives the pin descriptions for the clock EPLD.

Table 4
Pin Descriptions for Clock EPLD
Type: Alterra EPM 5032DC-15

Pin Number	Input/Output	Name	Function
1		GND	Ground Reference
2		GND	Ground Reference
3			Not Used
4			Not Used
5			Not Used
6			Not Used
7	IN	VCC	5-volt supply
8		GND	Ground Reference
9	OUT	96KHZ	Test Point
10	OUT	18_4MHZ	18.4 MHz Clock
11	OUT	16KHZN	Hop Clock Inverted
12	OUT	16KHZ	Hop Clock
13		GND	Ground Reference
14		GND	Ground Reference
15		GND	Ground Reference
16		GND	Ground Reference
17	OUT	9_6KHZ	9.6 kHz Clock
18	OUT	9_2MHZ	9.216 MHz Clock
19	OUT	4_8KHZ	4.8 kHz Clock
20	OUT	4_6MHZ	4.608 MHz Clock
21		GND	Ground Reference
22	IN	VCC	5-volt Supply
23	OUT	2_4KHZ	2.4 kHz Clock
24	OUT	2_3MHZ	2.304 MHz Clock
25	OUT	1_15MHZ	1.152 MHz Clock
26	OUT	D_HOPCLK	Frame-Start Pulse
27	IN	36_8MHZ	36.864 MHz Clock
28	IN	CLRN	Chip Reset

8 Board Settings, Board Addressing, And Status Registers

The jumper settings for the various board features are listed in Table 5.

Table 5
Jumper Settings For HSCI Board

Header Label	Jumper Position	Function
POST1	1-2	Enables C40 Interrupt by INT0 line DSPLINK
POST2	1-2 (2.4 kHz) 3-4 (4.8 kHz) 5-6 (9.6 kHz)	Selects Desired Data Clock Frequency
POST3	1-2 (1.15 MHz) 3-4 (2.30MHz) 5-6 (4.60 MHz) 7-8 (9.22 MHz)	Selects Desired Converter Clock Frequency

The status register bits are defined in Table 6.

Table 6
Status Register Data Bits

Bit	Name	Function
0	HOPCLK	Provides State of Hop Clock
1	NREADY	Indicates if HSC is Ready to Accept Data. Refer to [6].
2	SYNC	Indicates if HSC is Ready to Respond to Go Commands Refer to [6].
3	STATINT0	Status of C40 Interrupt line INT0 on DSPLINK
4-15		Not Used

The HSCI EPLD provides the means for addressing the HSCI board. The DSPLINK address lines are A3, A2, A1, A0. The lines A2 and A3 are used by the HSCI to determine its base address according to Table 7.

Table 7
Board Addresses for SW3 Settings
(Top View)

A3 A2	Base Address	C1/C2 Pole	C3/C4 Pole
0 0	0	C2	C4
0 1	4	C2	C3
10	8	C1	C4
11	C	C1	C3

9 Conclusion

A board to provide the interface between the hopping synthesizer controller and the C40 processor of a PL simulator has been designed, built, and tested. This board also provides all clock signals needed for an ADC board and a data interface board on the PL simulator. It also provides a means to control the HSC used in dehopping the signal at the PL simulator receiver. Further this board provides a facility for implementing interrupts to the C40 signal processor. These interrupts derive from the rising edge of the hop clock. The HSCI board also provides required control signals for the CRI equipment which is an important part of the PL. The board is controlled by the C40 processor with which it communicates by means of the DSPLINK bus. The HSCI board plugs into a VME back plane.

The design mainly uses off-the-shelf components except for a crystal oscillator and two EPLDs. The latter components simplify the PCB layout since much of the control logic and clock generation design is included. The wire-wrap prototype and the final PCB versions of this design performed reliably in all tests.

10 References

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IN THIS REPORT THE DESIGN OF AN INTEGRATED CIRCUIT BOARD FOR USE IN THE PAYLOAD OF AN EXTREMELY HIGH FREQUENCY SATELLITE COMMUNICATIONS EXPERIMENT IS DESCRIBED. THIS BOARD, CALLED THE HOPPING SYNTHESIZER CONTROLLER INTERFACE (HSCI) BOARD, PROVIDES ALL NECESSARY CLOCK SIGNALS FOR THE PAYLOAD AS WELL AS THE MEANS TO CONTROL THE HOPPING SYNTHESIZER CONTROLLER USED IN DEHOPPING THE RECEIVED SIGNAL AT THE PAYLOAD. MOST OF THE INTEGRATED CIRCUITS ON THIS BOARD ARE STANDARD OFF-THE-SHELF 7400 SERIES TRANSISTOR-TRANSISTOR LOGIC DEVICES. THE COMPLEXITY OF THE PRINTED CIRCUIT BOARD (PCB) IS GREATLY REDUCED BY USING TWO ERASABLE PROGRAMMABLE LOGIC DEVICES (EPLDS). ONE OF THESE EPLDS DERIVES ALL OF THE NECESSARY CLOCK SIGNALS FROM A SINGLE CRYSTAL OSCILLATOR. THE OTHER EPLD PROVIDES A BOARD ADDRESSING CAPABILITY AS WELL AS A STROBE SIGNAL TO CONTROL THE HOPPING SYNTHESIZER CONTROLLER. TWO DIFFERENT VERSIONS OF THE HSCI BOARD WERE BUILT, ONE WAS A SPEED-WRAP PROTOTYPE VERSION WHILE THE OTHER WAS THE FINALIZED PCB VERSION. BOTH BOARDS WERE FOUND TO OPERATE RELIABLY AND TO MEET EXPECTED PERFORMANCE.

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