Image Cover Sheet

CLASSIFICATION	SYSTEM NUMBER
UNCLASSIFIED	148874

TITLE

SOSDOR:SOLID-STATE DEVICE SIMULATOR CODE

System Number:

Patron Number:

Requester:

Notes:

DSIS Use only:

Deliver to: BA

National Defence / Défense nationale

SOSDOR: SOLID STATE DEVICE SIMULATOR (U)

by

L. Varga

DEFENCE RESEARCH ESTABLISHMENT OTTAWA
REPORT N0. 1235

Canada

October 1994
Ottawa

National Défense
Defence nationale

SOSDOR: SOLID STATE DEVICE SIMULATOR (U)

by

L. Varga
Space Systems and Technology Section
Radar and Space Division

DEFENCE RESEARCH ESTABLISHMENT OTTAWA
REPORT N0. 1235

PCN
041LS

October 1994
Ottawa

ABSTRACT

A 3-D solid state device simulator code "SOSDOR", developed at DREO, is presented. The code uses a seven-point finite difference scheme to discretize Poisson and the continuity equations. The equations are then solved using the Newton-Raphson iteration method. Additional information pertaining to griding, carrier mobility and recombination models as well as boundary conditions incorporated into the code are also presented. The source files of the code and the graphical I/O interfaces are also described. The code was tested by simulating a PIN diode under 0 V bias and under a 20V reverse bias condition. The simulation results are in excellent agreement with the results of simulation of the same device by the industry-standard PADRE code.

RESUME

Un code de simulation de composants semiconducteurs à trois dimensions "SOSDOR", développé à DREO, est présenté. Le code utilise une méthode de différence finie de sept points pour convertir en numérique les équations de Poisson et de continuité. Les équations sont alors résolues avec la méthode d'itération Newton-Raphson. De l'information additionnelle au sujet du grillage, de la mobilité des porteurs et des modèles de recombinaisons aussi bien que des types de frontières incorporés dans le code est aussi présentée. Les fichiers de code source et l'interface graphique entrée/sortie sont aussi décrits. Le code a été testé en simulant une diode PIN sans aucune polarisation, puis soumis à une polarisation inverse de 20 V. Les résultats de la simulation sont en excellent accord avec les résultats de simulation du même dispositif par le code de norme industrielle PADRE.

EXECUTIVE SUMMARY

In the evolving technology of electronic devices, device modelling provides an investigative tool for understanding the physics of semiconductor devices. This is important during the design stage, where device engineers can visualize the effect of parameter change on the electrical characteristics of the device much faster then via prototyping. Modelling is also a powerful method of analyzing existing devices whose function is perturbed by an external stimulus such as ionizing radiation, heat or some other physical phenomena. In this case, the model helps in understanding the changes in the electrical behaviour of the device as a function of the change in internal parameters. Cause and effect between the phenomena can be established and the potential problems circumvented.

A 3-D computer code, named "SOSDOR" (Solid State Device Simulator), has been developed at DREO to serve as an aid to study the effects of ionizing radiation on the solid-state semiconductor devices. Given a specific geometry and doping, the code determines parameters such as potentials or currents inside a solid-state device. It can also determine effects of applied voltage bias, change of design or effect of ionizing radiation on these parameters. The code has been benchmarked against a well known industry-standard code called PADRE using a PIN diode as the common device. An excellent agreement between the outputs of the two codes is observed. The user can display the results in colour in 3-D or 2-D. At the present, the code is implemented on a IBM RISC 6000 Unix workstation.

TABLE OF CONTENTS

1.0 Introduction

Computer simulation of solid state semiconductor devices is a cost-effective tool for evaluating the operation of these devices in adverse conditions such as are encountered in the space environment. In these environments, the device can be exposed to anomalous radiation fields or unusual temperature gradients that may lead to malfunction. Simulation codes can realistically predict the behaviour of devices under such conditions. They can demonstrate the effectiveness of design changes used to circumvent anomalous behaviour. Simulators have become an indispensable tool for quantifying the effect of process and physical variations on the electrical behaviour of semiconductor devices during the design process. Implementation and design of new devices relies heavily on utilization of numerical simulators as they can considerably reduce the time necessary to optimize the functional design and parameters. It is, therefore, of no surprise that considerable effort is being focused on the development of realistic 3-D electronic device simulators.

In this paper, a 3-D computer code "SOSDOR" (Solid State Device Simulator) capable of simulating solid-state electronic devices, is presented. The code was developed at DREO for the purpose of studying the effects of ionizing radiation on electronic devices. An earlier 2-D solid state device simulator[1], developed at DREO, was used to study the effect of ionizing radiation on the function of semiconductor devices. Inherent physical phenomena such as electrostatic fields and carriers transport, was simulated by using an analog resistance network, also known as the TLM (Transmission Line Matrix) method. The code utilized an electronic circuit solver (SPICE) to calculate the node parameters. The main drawback of the approach was that the speed of simulation was hindered by the speed by which the SPICE program solved the resistance network. Spice also had extremely large memory requirements due to the method employed to solve the node matrix equations. As a consequence, the TLM method was unsuitable for 3-D applications, as these require about n^3/n^2 times as many nodes for similar resolution. Typically, for a medium resolution problem, the value of n (number of nodes in one direction) is about 50. This motivated the development of SOSDOR, a 3-D numerical code, which was implemented on an IBM RISC 6000 machine.

2. Basic Equations in SOSDOR

2.1 The Carrier Equations

The electrical characteristics of many solid state devices can be specified by the Poisson (eqn (1)) and the continuity equations (eqn (2) and eqn (3)).

$$\nabla^2\Psi = -q/\epsilon(p - n + N_D^+ - N_A^-) \quad (1)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla J_n - R_n + G_n \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla J_p - R_p + G_p \quad (3)$$

R and G in the continuity equations are the recombination and generation rates for the minority current carriers. J_n and J_p are the electron and hole current densities, respectively, and are given by

$$J_n = -q\mu_n n\nabla\Psi + k_B T\mu_n\nabla n \quad (4)$$

$$J_p = -q\mu_p p\nabla\Psi - k_b T\mu_p\nabla p \quad (5)$$

In equations (4) and (5), μ_p and μ_n are the hole and electron mobilities, T is the absolute temperature and k_B is Boltzmann's constant. The carriers densities in Poisson's equation can be expressed as functions of "quasi-fermi"(φ_n, φ_p) potentials, i.e.

$$n = n_i\exp[(\Psi-\varphi_n)/k_BT] \quad (6)$$

$$p = n_i\exp[(\varphi_p-\Psi)/k_BT] \quad (7)$$

Under the equilibrium condition ($np=n_i^2$), the quasi-fermi potentials are equal to zero, but become nonzero if an excess of carriers is introduced or if a bias voltage has been applied to the device.

2.2 The Mobility Models.

In SOSDOR, the electron and hole mobilities have doping, temperature and field dependent components that have been combined into a relationship shown in equation (8).

$$\mu_0 = \left(\frac{1}{\mu_T} + \frac{1}{\mu_N} + \frac{1}{\mu_E}\right)^{-1} \quad (8)$$

The doping-dependent empirical mobility model shown in equation (9) below was adopted from Caughey[2].

$$\mu_N = \frac{\mu_{Nmin} - \mu_{Nmin}}{1 + (N/N_{ref})^{\alpha}} + \mu_{Nmin} \quad (9)$$

The mobility parameters N_{ref}, μ_{max}, μ_{min} and α were extracted[2] from experimental data obtained over a doping range from 1.0e14 cm^{-3} to 1.0e21 ^{-3}cm. In this model, the values for the α parameter used were 0.76 for holes and 0.72 for electrons. The reference doping densities (N_{ref}) were 6.3e16 cm^{-3} for holes and 8.5e16 cm^{-3} for electrons. The other two parameters, namely μ_{max} and μ_{min}, are intercepts of a curve fitted into the data. For holes μ_{max} = 495 cm^2 V^{-1} s^{-1} and μ_{min} = 47.7 cm^2 V^{-1} s^{-1} and, as expected, larger values were given for electrons, namely μ_{max} = 1330 cm^2 V^{-1} s^{-1} and μ_{min} = 65 cm^2 V^{-1} s^{-1}. The reduction of mobility with higher doping density is due to increased scattering of current carriers at the impurity centres. Similarly, increased lattice vibration at higher temperature have the same qualitative effect as increasing doping density. For holes and electrons, μ_T is given by

$$\mu_T = 2.3e^9 T^{-2.7} \qquad (holes) \quad (10)$$

and

$$\mu_T = 2.1e^9 T^{-2.5} \qquad (electrons) \quad (11)$$

The expressions in equations (10) and (11) are applicable[3] in the temperature range between 150 to 450 degrees Kelvin.

At the surface of the device, the effect of the electric field on mobility was implemented into SOSDOR using[4] the relation

$$\mu_E = \mu_0 (1 + \chi E_{\perp})^{-0.5} \quad (12)$$

where E is the electric field perpendicular to the surface of the device and χ is the field parameter. For electrons and holes, the values of χ used were 1.54e^{-5} cm V^{-1} and 5.35e^{-5} cm V^{-1}, respectively. Inside the semiconductor bulk the field dependence takes on the form[2]

$$\mu_E = \left[\frac{1}{\left[1+\frac{\mu_0 E}{V_{sat}}\right]^{\beta}}\right]^{\frac{1}{\beta}} \qquad (13)$$

with β having integer values, 1 for holes and 2 for electrons. The carrier saturation velocities v_{sat} have been set[2] to 9.5e6 cm s^{-1} for holes and to 1.1e7 cm s^{-1} for the electrons. In SOSDOR, Boltzmann statistics is implied, and hence the relationship between mobility and the diffusion coefficient is given by Einstein's relationship $D = (k_B T/q)\mu$.

2.3 Recombination Models

Two recombination processes have been implemented into SOSDOR, namely, the Shockley-Reed-Hall and Auger processes. The Shockley-Reed-Hall process is caused by the presence of trapping energy level in the band gap and the Auger process is attributed to band-to-band recombination. The total recombination rate is the sum of the two processes which individually are given by

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left[n+n_i\exp\frac{(E_t-E_i)}{k_B T}\right] + \tau_n\left[p+n_i\exp\frac{(E_i-E_t)}{k_B T}\right]} \qquad (14)$$

and

$$R_{AUGER} = (c_n n + c_p p)\,(np - n_i^2)\,. \qquad (15)$$

where E_i = intrinsic Fermi level
E_t = trap energy levels
c_n = Auger coefficient for electrons
c_p = Auger coefficient for holes
n_i = intrinsic concentration with the band-gap narrowing effect included
τ_n = doping-dependent electron lifetime
τ_p = doping-dependent hole lifetime

The c_n and c_p coefficients show a slight temperature dependence[5] in the temperature range between 77K and 400K, which is, at the present, not included in the code. For the 300K temperature c_n = 2.8×10^{-31} cm^6 s^{-1} and c_p = 9.9×10^{-32} cm^6 s^{-1}.

In addition to bulk recombination, surface recombination has also been implemented into SOSDOR via[6]

$$R_{surf} = \frac{pn - n_i^2}{(n + n_i \exp\frac{(E_t - E_i)}{k_b T}) / s_n + (p + n_i \exp\frac{(E_i - E_t)}{k_b T}) / s_p} \quad (16)$$

The parameters s_p and s_n are the surface recombination velocities for holes and electrons respectively. These values depend on the treatment of the device surface during the manufacturing process (eg. etching, oxidizing). Commonly accepted values for surface recombination velocities are approx $1.0e^2$ cm s^{-1} for oxidized surfaces and $1.0e^3$ cm s^{-1} for other surface conditions[7].

2.4 Boundary Conditions

At the boundaries of the device, other than under the gate area or at the contacts, a homogeneous reflective, also known as Neumann's[8] boundary is implemented. This implies that the electric field at the boundary has no normal component (equation (17)) and the net current flow across the boundary are zero.

$$E \cdot \overline{n} = 0 \quad (17)$$

At an ohmic contact the surface potential is fixed at a value equivalent to the sum of the applied potential V_{app} and the space-charge potential (Dirichlet boundary).

3. Finite Difference Implementation in SOSDOR

SOSDOR uses the finite difference method to solve the basic semiconductor equations (1-3). The discrete form of the first and the second partial derivatives of a function U are derived from the Taylor series[9]

$$U(x+h2,y,z) \approx U(x,y,z) + h2\frac{\partial U(x,y,z)}{\partial x} + \frac{h2^2}{2!}\frac{\partial^2 U(x,y,z)}{\partial x^2} + \frac{h2^3}{3!}\frac{\partial^3 U(x,y,z)}{\partial x^3} + \ldots \quad (18)$$

$$U(x-h1,y,z) \approx U(x,y,z) - h1\frac{\partial U(x,y,z)}{\partial x} + \frac{h1^2}{2!}\frac{\partial^2 U(x,y,z)}{\partial x^2} - \frac{h1^3}{3!}\frac{\partial^3 U(x,y,z)}{\partial x^3} + \ldots \quad (19)$$

The solution for $\partial U(x,y,z)/\partial x$ can be obtained if equation (18) is divided by $h2^2$ and equation (19) by $h1^2$ followed by subtraction of the two. This will eliminate the second derivative terms in the series yielding the finite difference approximation for the first derivative in x-direction, i.e.

$$\frac{\partial U(x,y,z)}{\partial x} \approx \frac{h1\,U(x+h2,y,z)}{h2(h1+h2)} - \frac{h2\,U(x-h1,y,z)}{h1(h1+h2)} \qquad (20)$$

The error in the above expression results from the truncation of the series at the third derivative term, hence the error $\approx (h1h2/3)\partial^3 U(x,y,z)/\partial x^3$. The first derivatives in the y and z directions are obtained analogously.

The second derivative with respect to x, shown in equation (21) is derived in a similar fashion, again using elimination of unwanted differential terms. The results are then added to yield

$$\frac{\partial^2 U(x,y,z)}{\partial x^2} \approx \frac{2U(x+h2,y,z)}{h2(h1+h2)} + \frac{2U(x-h1,y,z)}{h1(h1+h2)} \qquad (21)$$

The total divergence operator, given in equation (22), is the standard seven-point formula which is graphically depicted

$$\nabla^2 U = \sum_1^6 \frac{2}{\rho_i} U_i - \frac{1}{\xi} U \qquad (22)$$

in Figure 1. In Figure 1, h_i is simply a distance between the central node and a branch node. In the more general case, where the grid is nonuniform, the expressions for ρ_i explicitly take on forms

$$\rho_1 = h_1(h_1+h_2),\ \rho_2 = h_2(h_1+h_2),\ \rho_3 = h_3(h_3+h_4),\ \ldots\ \rho_6 = h_6(h_5+h_6) \qquad (23)$$

The scaling factor ζ is equal to $6/h^2$ if the grid is uniform and, for the case of a non-uniform;

$$\zeta = \frac{2}{h_1 h_2} + \frac{2}{h_3 h_4} + \frac{2}{h_5 h_6} \qquad (24)$$

4. The Solution Method

The solution to Poisson equation requires finding the solution to the matrix equation $\mathbf{A\Psi = g}$ where **A** is the divergence operator matrix of size $(M_x-1)(M_y-1)(M_z-1)$ x $(M_x-1)(M_y-1)(M_z-1)$, Ψ is the 1 x $(M_x-1)(M_y-1)(M_z-1)$ column vector representing the node potentials and **g**, also a column vector, is the R.H.S. of equation (1). For 3-D systems, due to the large matrix sizes involved, instead of solving the matrix equation by a direct method (eg. Gaussian elimination), an iterative method of solution is used. SOSDOR solves the device equations iteratively. The iterative technique has an advantage over the direct method in large systems, because of its simplicity and ease of implementation. The main disadvantage of this technique, however, is the possibility of a relatively slower rate of convergence. The device equations are

solved by the Newton-Raphson iteration scheme for which the recursion formula is given by

$$\Psi_{s+1} = \Psi_s - \frac{F(\Psi_s, n, p)}{F'(\Psi_s, n, p)} \qquad (25)$$

Here, s is the iteration loop number, $F(\Psi,n,p)$ is the equation (1), (2) or (3) in the implicit form and $F'(\Psi,n,p)$ is $dF(\Psi,n,p)/d\Psi$. The criteria for the sequence to converge has been discussed by Vilenkin[10] and is not discussed here in detail. Some salient points, however, should be mentioned. First, difficulties can arise if F' approaches zero. In the case of the present application, application of equation (25) does not pose any danger since F' is an exponential function. Second, the number of iterations required for convergence vary from node to node and from case to case. A very rapid convergence with as few as five iterations has been observed at locations within the device, remote from active areas (junctions) and as many as 300 in the active areas of the device. Provided that the first approximation is close to the solution, the method converges quadratically according to $|\Psi_{s+1}-\Psi|<|\Psi_s-\Psi|^2$. This became evident in the neutral regions of the device, where the initial potential and carrier density estimates (obtained from doping densities) were close to final values.

The time-dependent continuity equations were first converted to Crank-Nicolson implicit form and then solved by Newton-Raphson iteration. Crank-Nicolson implicit discretization is more stable than a simple explicit discretization methods[9]. Attempts to solve the continuity equations via explicit Richardson method have resulted in instability and failure after several iterations. The undesirable relative complexity of the implicit form, lies in the fact that the present unknown variable (time=t+1) is expressed by other present unknown variables, as well as variables from the previous time step (time=t). The continuity equation for holes, for example in the implicit discrete form is

$$(1-\lambda)\Sigma_{i=1}^{6}\frac{2}{\rho_i}p_i^{t+1}-\xi p^{t+1}+\lambda\Sigma_{i=1}^{6}\frac{2}{\rho_i}p_i^{t}-\xi p^{t})=(1-\lambda)\,g^{t+1} \qquad (26)$$

where λ is a weighing factor, p_i/p is the concentration of holes at the particular node, t is the time and g is the R.H.S. of equation (2). For example, λ is equivalent to 0.5 in case of Crank-Nicolson method, and is equivalent zero for the explicit form.

5. The Computer Code

Sosdor is a 3-D computer code written in C language for the IBM RS-6000 Unix-based workstation and runs in an X-windows environment. The code is composed of three main modules, namely

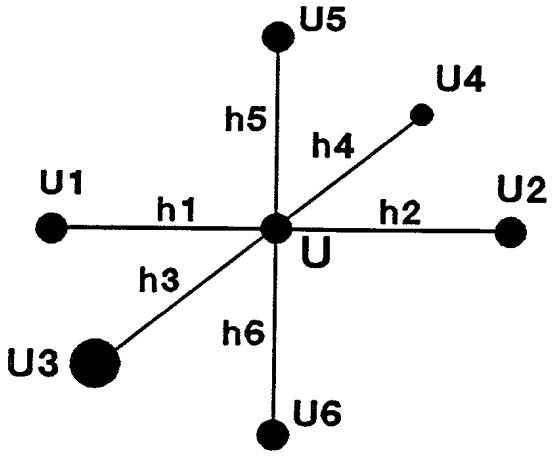


Figure 1 Seven-point 3-D finite difference computational scheme

i) Input module
ii) Processing module
iii) Output module

In the Input module, the user enters information ralated to device layout, doping profiles, electrical connections and the device computational grid. The module consists of a graphical drawing package and a set of standardized device parameter input files that must be generated by the user prior running the code. The menu-driven, graphical drawing package allows the user to graphically design the computing grid inside a graphical window. For a 3-D grid, the user is required to draw a minimum of two 2-D grids in x-y and x-z or y-z planes to overlay the device. Node distances are then automatically placed inside the grid description file and subsequently read by the Processing module. As alternative to a graphical mesh design, the user also has an option to manually enter the node distances in the x, y and the z direction into the grid description file called ***meshdata***. This method of grid generation was found to be satisfactory in a lot of applications (dynamic re-griding at this point is not available). The file named ***design*** contains the information about the number of diffusion wells and the extent of these wells in terms of node numbers. The file ***electrical*** holds information about the voltage bias of the device. Detailed information about the files and subroutines in the graphical part of the Input module is given in greater detail elsewhere[11].

The Processing module processes the device input parameters, solves the transport equations and puts the results into a set of files called ***potentials, holes*** and ***electrons***. The Processing

module is composed of sub-modules *start, device, functions, grid* and variable-related header files. At the beginning, the user is prompted to reply whether the device to be simulated is new. The replay directs the code into either the *start* submodule or *device* submodule. If device simulated is not new, the input module need not be used. The Processing module will simply read the existing output data files obtained earlier, and will examine the effect of changing voltage bias or the effect of ionizing radiation on the potential and the distribution of current carriers. This feature is useful for the cases where unbiased devices are stored and then retrieved for further simulation study. The updated output files receive the prefix "device". The *functions* submodule contains all the functions definitions that are called by other submodules of the Processing module.

The Output module reads the potential or current carriers distribution file and the grid description file to generate a coloured graphical output. The densities or magnitudes are indicated with 21 colour chart available with displays. There are several modes of display are available,

i) 3-D whole device
ii) 3-D surface
iii) 2-D map
iv) 2-D exploded view.

After entering the data file names, the main (default) display shows the device of interest in 3-D. The 3-D surface displays one layer of the device at the time. The 3rd dimension relates to the magnitude of the variable. The 2-D map displays one layer of the device at the time. The 2-D exploded view shows the whole device by showing all planes, separated by small space, simultaneously. To activate the other 3 displays, the user makes a selection from the menu bar located at the top of the main display.

6. Computational Results and Discussion

The device geometry considered for the simulation is shown in Fig. 2a. The device is a MRD500 PIN type diode[12], a planar silicon structure with both, the p++ and n regions heavily doped in relation to the I (intrinsic) region of the device. All the diode regions were considered to be uniformly doped, the junctions were assumed to be abrupt and Shockley-Read_Hall type recombination process was assumed throughout the structure. Device parameters used in the simulation are given in Table 1.

The grid used in this simulation is three dimensional, nonuniform and orthogonal. The grid has 45 nodes uniformly separated by 11.5 microns in the x and y directions and has 35 nodes in the z direction (vertical) with node distances varying

Table I Physical parameters characterizing the PIN diode structure

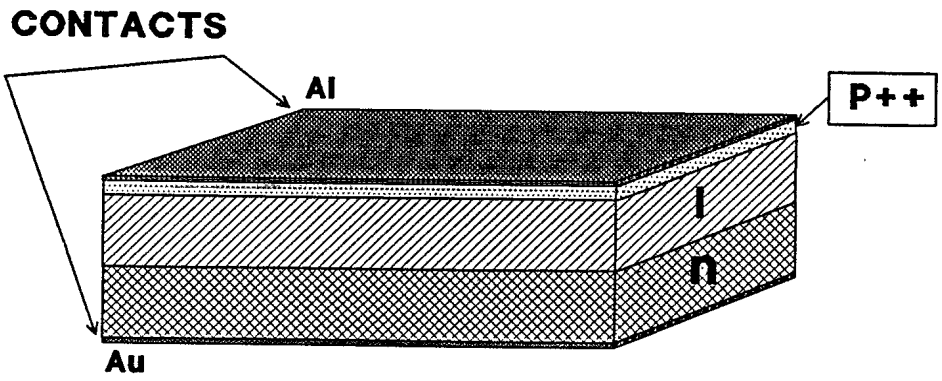
	p++	I	n
Doping cm^{-3}	N_a=7.88e18	N_d =4.18e13	N_d=4.18e15
Thickness	4 μm	23 μm	25 μm
Bias	p++contact=0V		n contact=+20V
Contacts	Al 506 μm x 506 μm		Au 506 μm x 506 μm
Die	506 μm x 506 μm x 52 μm		
Grid	3-D nonuniform, orthogonal 45 x 45 x 35		
Temperature	300 K		

from 0.075 microns to 10 microns, the finer mesh being utilized in the junctions areas (Figure 2b). A constant time step of 0.01 ps was used in all calculations. The temperature was assumed to be 300° K.

Figures 4a, 4b and 4c show the potential and carrier distributions under a zero-bias condition as a function of device depth. The built-in potential varies from -0.4855 V at the p++ side of the diode, to 0.334 V at the n side of the device. One observes that the potential change occurs almost exclusively in the intrinsic region (I) of the device. This is to be expected, due to the low doping (high resistivity) of the I region in relation to P++ and n (Table 1). The corresponding hole and electron density profiles also change in the I region of the device. Holes have two equilibrium minority carrier concentrations, one in the I region and one in the n region. Both satisfy $pn = n_i^2$, the n_i being the intrinsic density of carriers. The doping density of the n region is about two orders of magnitude higher the doping level of the I, however, the value of n_i is essentially the same across these regions of the device. As the doping level approaches approx $1e^{16}$ cm^{-3} there is a prominent decrease in the energy band-gap. This results in an increase in the value of n_i concentration. This band-gap narrowing effect is important in the p++ area of the device (N_a=7.88e18 cm^{-3}), where the value of n_i is about 5 times higher then in both the I and n regions. Figure 3 shows how band-gap narrowing affects the value of intrinsic concentrations of carriers in regions of the device.

The results of the PIN diode simulation by SOSDOR were compared with the simulation results of the same device, carried out at Renssealer Poly. Inst. (Troy, N.Y.) using the well known solid state device simulation code PADRE.

(a)



(b)

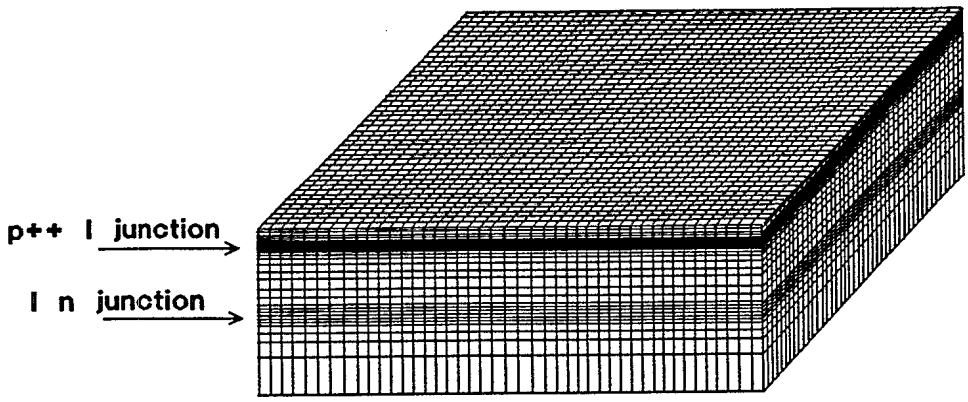


Figure 2 (a) Structural view of the PIN device
(b) Perspective view of the 3-D discretization grid

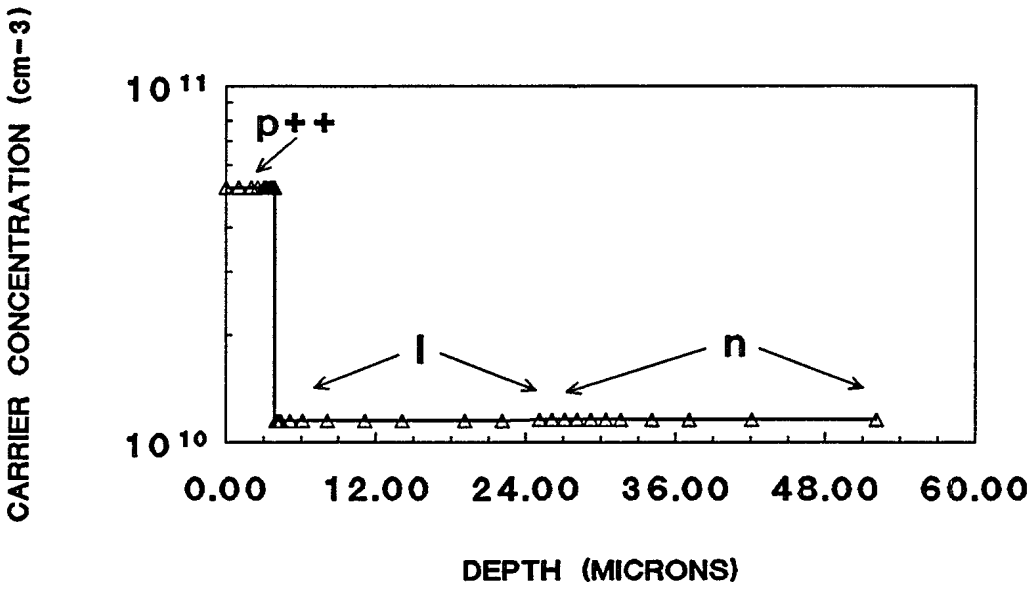


Figure 3 Doping-related band gap narrowing effect in the intrinsic concentration of carriers

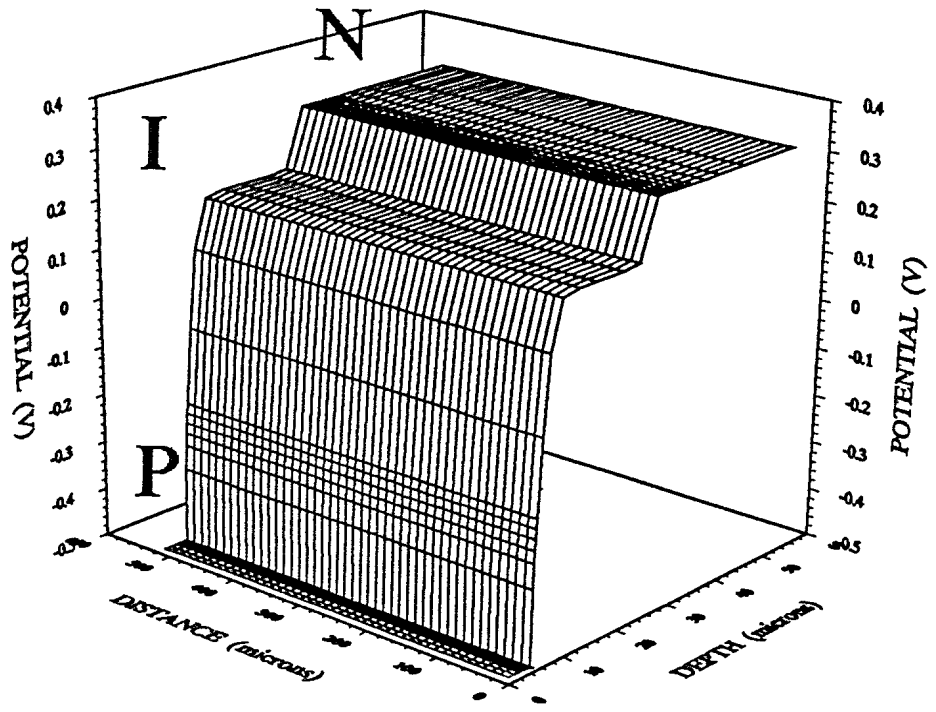


Figure 4a Built-in potential of the PIN diode

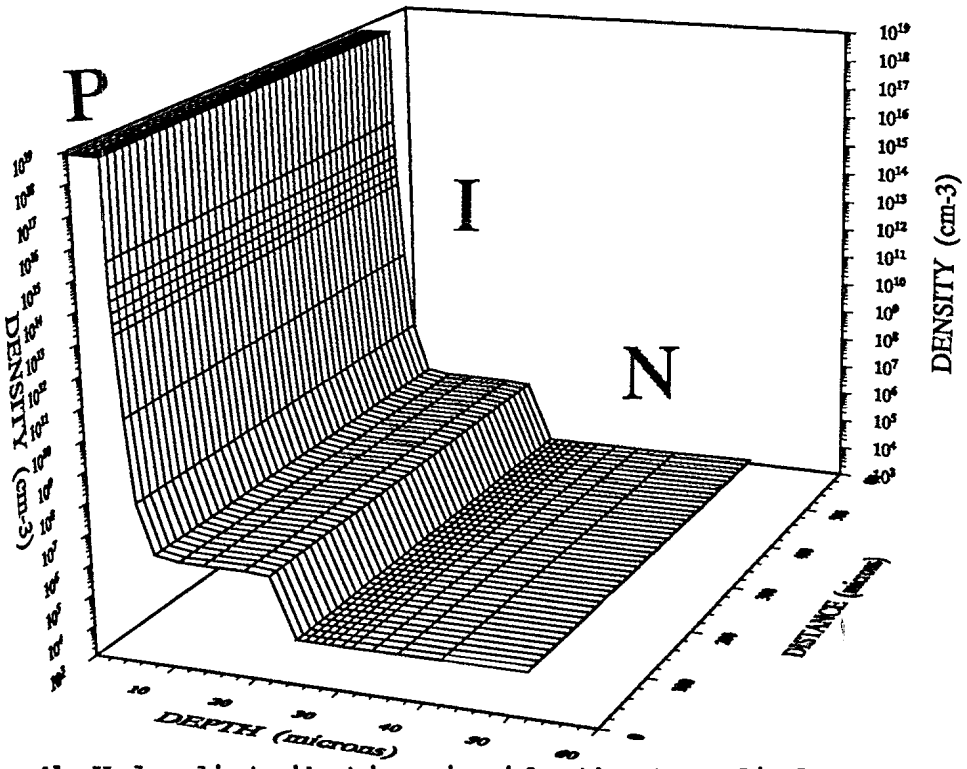


Figure 4b Hole distribution inside the PIN diode

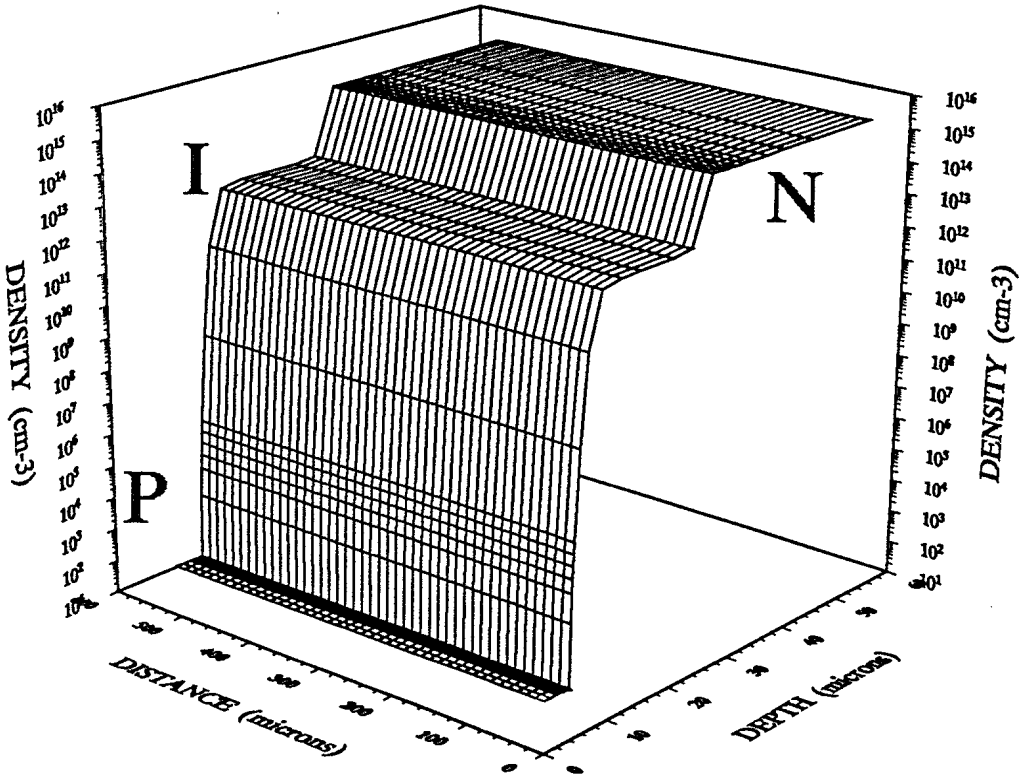


Figure 4c Electron distribution inside the PIN diode

The purpose of this comparison was to validate the correctness of the mathematical approach selected and its implementation into the algorithm of the code. From Figure 5, one easily can conclude that there is an excellent agreement between the results from the two codes.

Figures 6a, 6b and 6c are 3-D plots showing simulation results when the diode is reverse-biased at 20 V. The regional contacts are connected to the diode via metallization (Figure 2a) located at the top and the bottom surface of the device. The contacts have the same area as the die dimension, namely 506 μm x 506 μm. The contacts were considered to be ohmic, so the surface nodes at these areas were set-up as Dirichlet boundaries. For the highly-doped regions of the device such as the p++ region, metallization is applied directly on top of the semiconductor material. For the n region, however, the ohmic contact would be accomplished, for example, via metal-n+ method (not shown in Figure 2a). Oscillations in the intermediate results occurred when the bias voltage was applied suddenly, which in some cases caused the simulation results to diverge. The reason for such an instability was attributed to the sudden dominance of the drift current over the diffusion current inside the I region of the device. The problem was remedied by ramping the bias voltage in small increments. Specifically, in this situation, 0.2 V increments were found satisfactory.

Figure 6a refers to the potential profile while Figures 6b and 6c relate to hole and electron densities respectively. Due to the x-y symmetry of the device, the potential profile and the carrier densities are constant across the horizontal planes, so only vertical profiles are given. All the potential change occurring within the device is, again, confined within the I region of diode, thus resulting in an area of strong electric field. The I region also becomes virtually depleted of mobile carriers. In this mode of operation, the PIN diode can be utilized as an ionizing radiation detector. Note, that although the p++ region is only 4 microns thick, the proximity of the contact potential and the very high doping profile of this region prevents any significant modulation of device parameters in this region of the device.

7. Conclusion

The SOSDOR code, developed at DREO for simulation of semiconductor devices, has been described. The simulation of an MRD-500 PIN diode has been compared with the simulation results obtained with an industry standard code PADRE. The code can be utilized for design of radiation detectors, solid state device characteristics studies and studies of radiation effects on device function. In the future, the code will be extended to include a GUI (graphical user interface) and a re-griding algorithm.

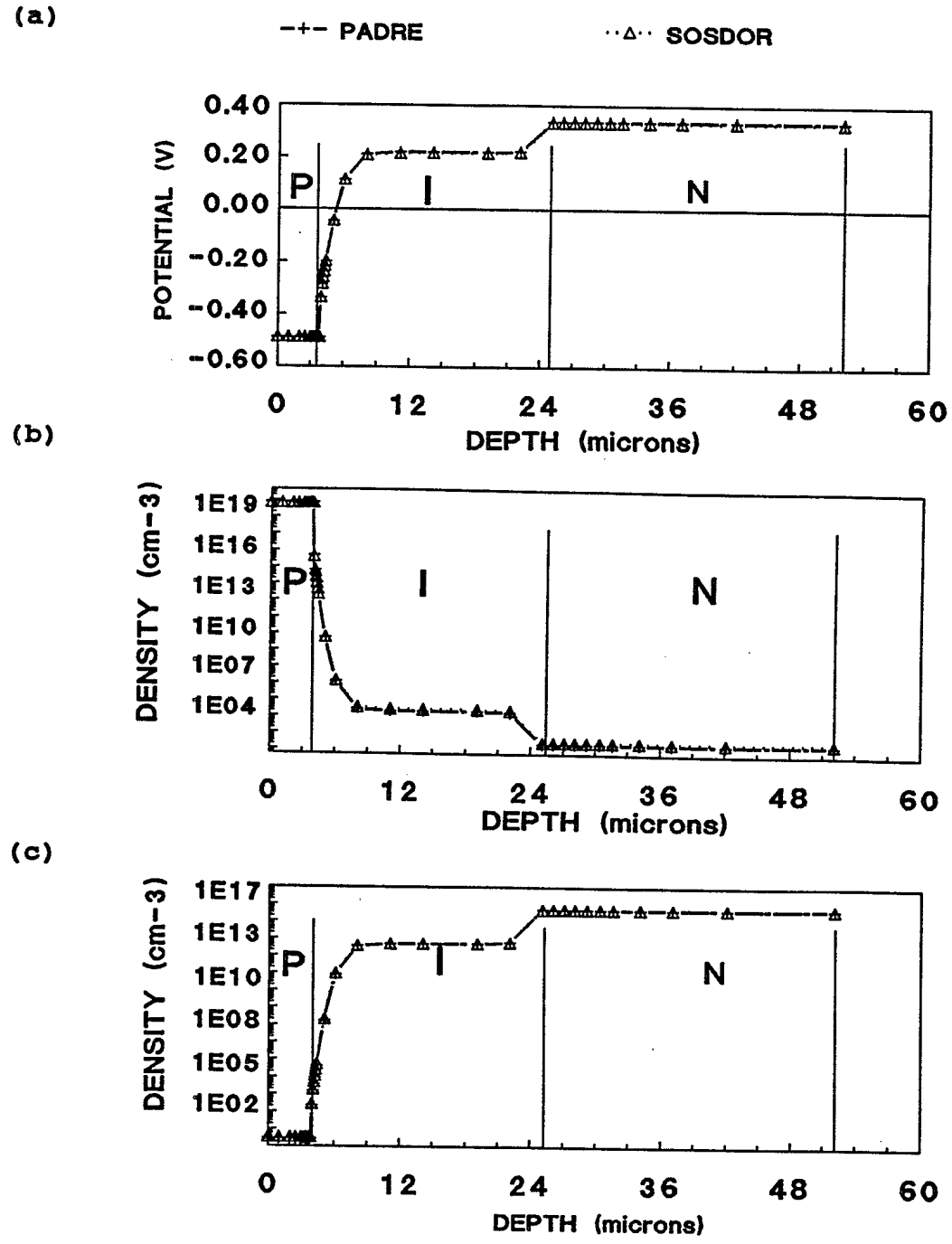


Figure 5 Comparison of the simulation results between SOSDOR and PADRE.
a) Built-in potentials, b) Hole density, c) Electron density

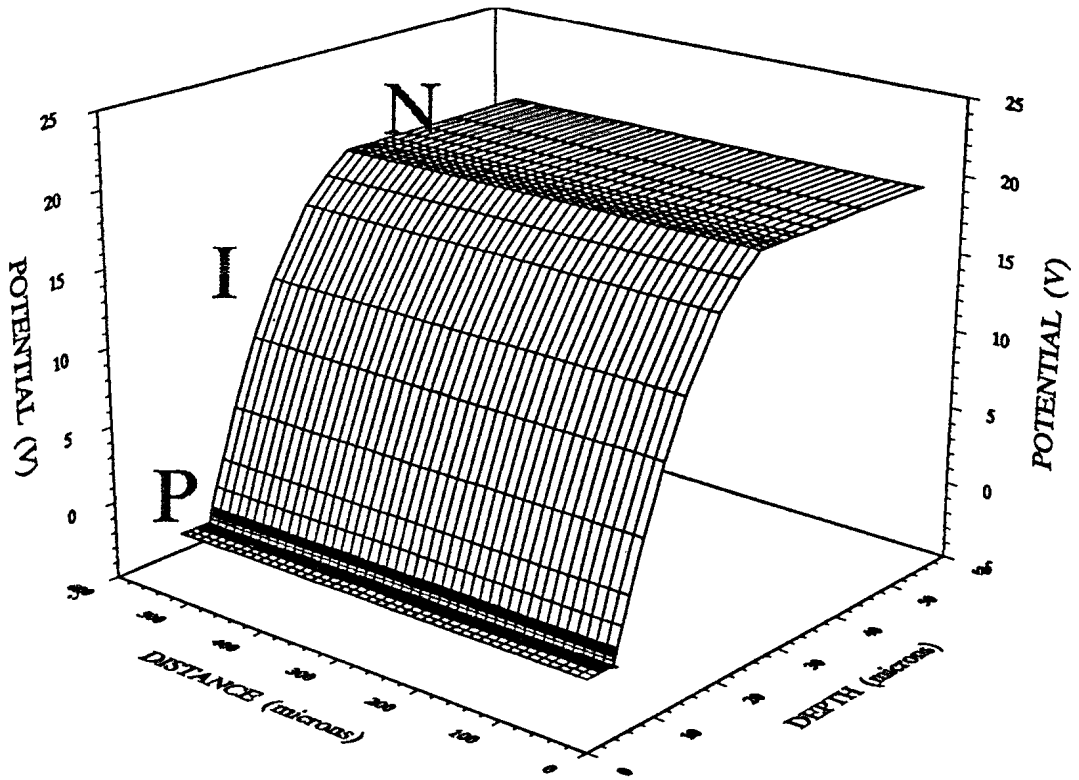


Figure 6a Vertical profile of total potential of the PIN diode under a 20V reverse bias.

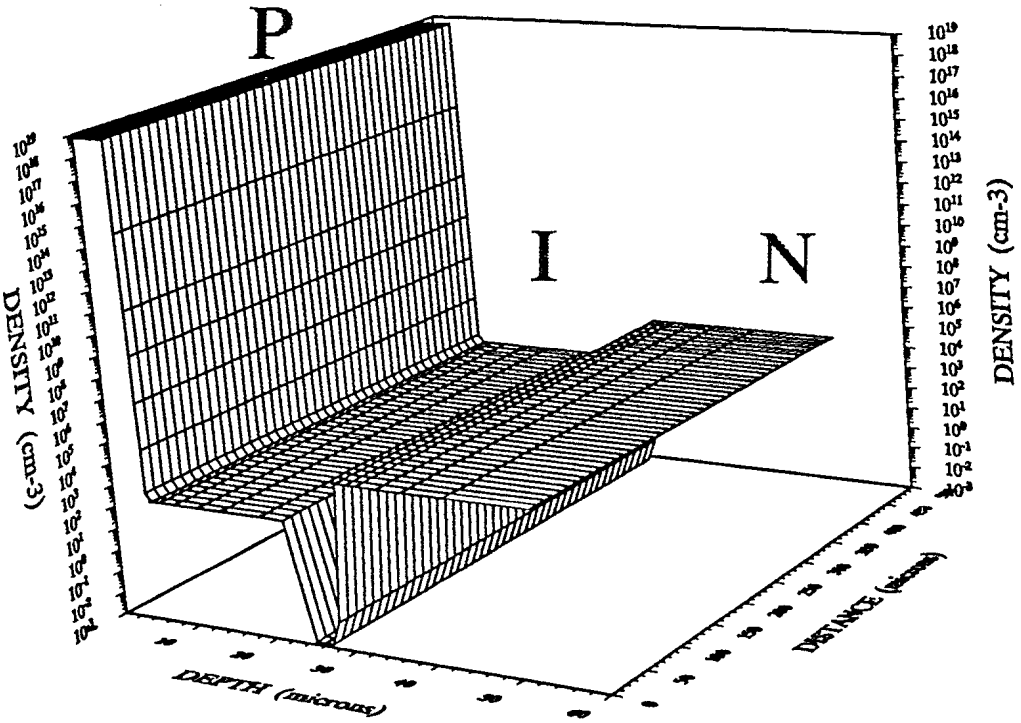


Figure 6b Hole density distribution inside the PIN diode for 20 V reverse bias.

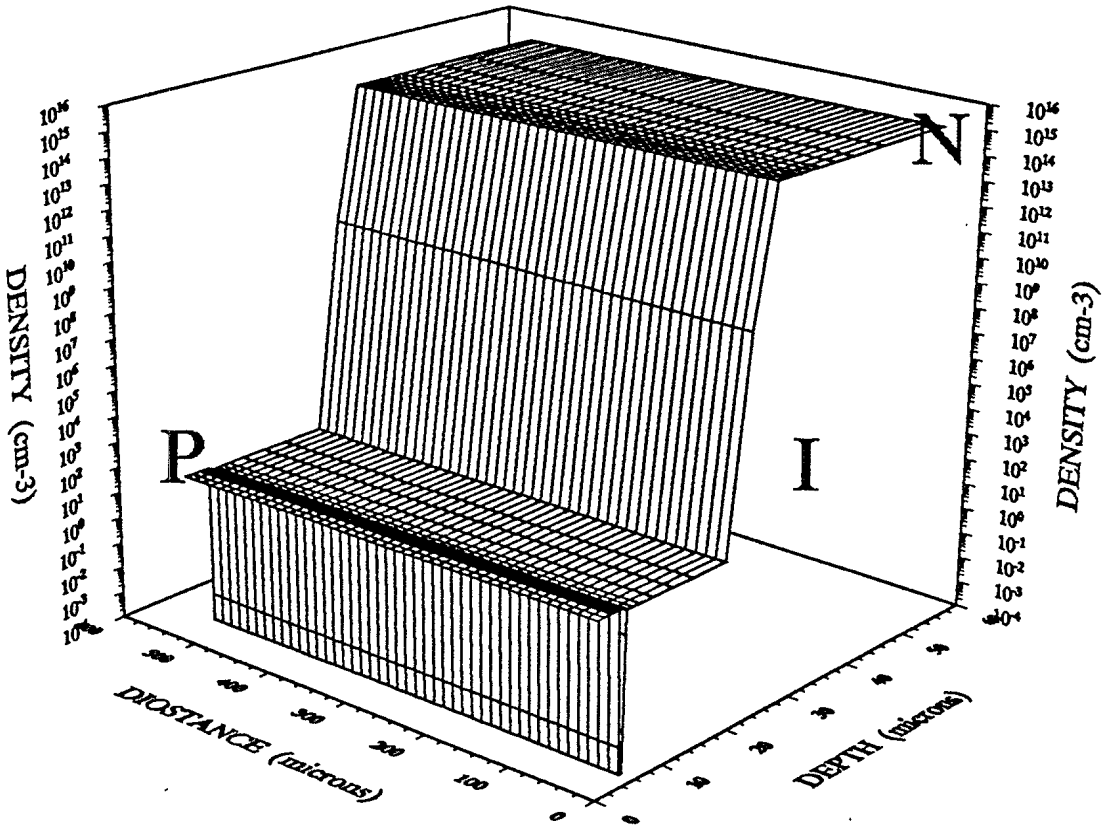


Figure 6c Distribution of electrons inside the PIN diode for 20V reverse bias.

8. Acknowledgement

The author would like to thank Mr. Edd Waller of Renssealer Poly. Inst. (Troy, N.Y.) for the PADRE code simulation results.

9. References

1. Varga L., "Utilization of an Elecronic Circuit Simulator in CMOS Latch-up Studies", Defence Research Establishment Ottawa, Report No. 1144, 1992.

2. Caughey, D.M. and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field", Proc. IEEE, vol. 55, 1967.

3. Levine, N.S., "Principles of Solid-State Microelectronics", Holt, Reinhart and Winston, 1963.

4. Yamaguchi, K., "A Mobility Model for Carriers in the MOS Inversion Layer", IEEE Trans. Electron Dev., vol. ED-30, No. 6, June 1983.

5. Langer, E., Selberherr, S. and H. Mader,"A Numerical Analysis of Bulk-Barrier Diodes", Solid-State Electronics, No. 4, 1982.

6. Heimeier, H.H., "A Two-Dimensional Numerical Analysis of a Silicon N-P-N Transistor", IEEE Trans. Electron Dev., vol. ED-20, No. 8, August 1973. 7. Jonscher, A.K., "Principles of Semiconductor Device Operation", G. Bell and Sons, LTD., 1960.

7. Jonscher, A.K., "Principles of Semiconductor Device Operation", G. Bell and Sons LTD., 1960.

8. Pinto, R.M., Rafferty, S.C. and W.R. Dutton, " PISCES II: Poisson and Continuity Equation Solver", Stanford Electronics Laboratories, Stanford, CA, Rep., 1984.

9. Lapidus, L. and G. F. Pinder, " Numerical Solution of Partial Differential Equations in Science and Engineering", J. Willey & Sons, 1982.

10. Vilenkin, N.Y., "Successive Approximation", Pergamon, 1964.

11. Tétreault, R.H., "Development of a Simulator Shell Program", DREO, (W7714-2-9629), 1993.

12. Pepper, G., DREO, private communications.

DOCUMENT CONTROL DATA

(Security classification of title, body of abstract and indexing annotation must be entered when the overall document is classified)

1. ORIGINATOR (the name and address of the organization preparing the document. Organizations for whom the document was prepared, e.g. Establishment sponsoring a contractor's report, or tasking agency, are entered in section 8.)

Defence Research Establishment Ottawa
Ottawa, Ontario
K1A 0Z4

2. SECURITY CLASSIFICATION (overall security classification of the document including special warning terms if applicable)

UNCLASSIFIED

3. TITLE (the complete document title as indicated on the title page. Its classification should be indicated by the appropriate abbreviation (S,C or U) in parentheses after the title.)

SOSDOR:SOLID-STATE DEVICE SIMULATOR CODE (U)

4. AUTHORS (Last name, first name, middle initial)

L. VARGA

5. DATE OF PUBLICATION (month and year of publication of document)

October 1994

6a. NO. OF PAGES (total containing information. Include Annexes, Appendices, etc.)

21

6b. NO. OF REFS (total cited in document)

12

7. DESCRIPTIVE NOTES (the category of the document, e.g. technical report, technical note or memorandum. If appropriate, enter the type of report, e.g. interim, progress, summary, annual or final. Give the inclusive dates when a specific reporting period is covered.)

DREO Report

8. SPONSORING ACTIVITY (the name of the department project office or laboratory sponsoring the research and development. Include the address.)

Defence Research Establishment Ottawa
3701 Carling Avenue, Ottawa, Ontario
K1A 0Z4

9a. PROJECT OR GRANT NO. (if appropriate, the applicable research and development project or grant number under which the document was written. Please specify whether project or grant)

Project 041LS

9b. CONTRACT NO. (if appropriate, the applicable number under which the document was written)

10a. ORIGINATOR'S DOCUMENT NUMBER (the official document number by which the document is identified by the originating activity. This number must be unique to this document.)

DREO REPORT 1235

10b. OTHER DOCUMENT NOS. (Any other numbers which may be assigned this document either by the originator or by the sponsor)

11. DOCUMENT AVAILABILITY (any limitations on further dissemination of the document, other than those imposed by security classification)

(X) Unlimited distribution
( ) Distribution limited to defence departments and defence contractors; further distribution only as approved
( ) Distribution limited to defence departments and Canadian defence contractors; further distribution only as approved
( ) Distribution limited to government departments and agencies; further distribution only as approved
( ) Distribution limited to defence departments; further distribution only as approved
( ) Other (please specify):

12. DOCUMENT ANNOUNCEMENT (any limitation to the bibliographic announcement of this document. This will normally correspond to the Document Availability (11). however, where further distribution (beyond the audience specified in 11) is possible, a wider announcement audience may be selected.)

Unlimited Announcement

UNCLASSIFIED

SECURITY CLASSIFICATION OF FORM

13. **ABSTRACT** (a brief and factual summary of the document. It may also appear elsewhere in the body of the document itself. It is highly desirable that the abstract of classified documents be unclassified. Each paragraph of the abstract shall begin with an indication of the security classification of the information in the paragraph (unless the document itself is unclassified) represented as (S), (C), or (U). It is not necessary to include here abstracts in both official languages unless the text is bilingual).

A 3-D solid state device simulator code, developed at DREO, is presented. The code uses a seven-point finite difference scheme to discretize Poisson's and the continuity equations. The equations are then solved using the Newton-Raphson iteration method. Additional information pertaining to griding, carrier mobility and recombination models as well as boundary condition types incorporated into the code is also presented. The source files of the code and the graphical I/O interfaces are also described. The code was tested by simulating a PIN diode under no bias and under a 20V reverse bias condition. The simulation results are in excellent agreement with the results of simulation of the same device by the industry-standard PADRE code.

14. **KEYWORDS, DESCRIPTORS or IDENTIFIERS** (technically meaningful terms or short phrases that characterize a document and could be helpful in cataloguing the document. They should be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location may also be included. If possible keywords should be selected from a published thesaurus. e.g. Thesaurus of Engineering and Scientific Terms (TEST) and that thesaurus-identified. If it is not possible to select indexing terms which are Unclassified, the classification of each should be indicated as with the title.)

Poisson equation
Continuity equations
Finite difference scheme
Crank-Nicolson implicit discretization
Newton-Raphson iteration